TPS7B70-Q1 Automotive, 300-mA, 40-V, Low-I_Q LDO With Power Good

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results:
  - Device Temperature Grade 1: –40°C to 125°C Ambient Operating Temperature Range
  - Device HBM ESD Classification Level 2
  - Device CDM ESD Classification Level C4B
- Device Junction Temperature Range: –40°C to +150°C
- Maximum Output Current: 300 mA
- 4-V to 40-V Wide V_{IN} Input-Voltage Range With up to 45-V Transients
- Fixed 3.3-V and 5-V Outputs
- Maximum Dropout Voltage: 400 mV at 300 mA
- Stable With Output Capacitor in Wide Range of Capacitance (4.7 µF to 500 µF) and ESR (0.001 Ω to 20 Ω)
- Low Quiescent Current ($I_{(Q)}$)
  - < 4 µA When EN is Low (Shutdown Mode)
  - 19 µA Typical at Light Loads With VINT High
- Fully Adjustable Power-Good Threshold and Power-Good Delay Timing
- Low Input-Voltage Tracking to UVLO
- Integrated Fault Protection
  - Overload Current-Limit Protection
  - Thermal Shutdown
- 16-Pin HTSSOP PowerPAD™ Package
  - Thermal Resistance ($R_{\theta JA}$): 39.7°C/W

2 Applications

- Body Control Modules (BCM)
- EV and HEV Battery Management Systems
- Transmission Control Units (TCU)
- Head Units
- Electrical Power Steering (EPS)

3 Description

The TPS7B70-Q1 is a 300-mA, low-dropout linear regulator (LDO) that operates from an automotive battery. The device has only 19 µA of quiescent current at light loads. Thus, the TPS7B70-Q1 is an excellent selection to supply power to always-on components, such as microcontrollers (MCUs) and controller area network (CAN) transceivers.

The input voltage range of the TPS7B70-Q1 extends thru 40 V. This voltage helps the device withstand transient conditions, such as load-dump. The device also has a power good (PG) pin to tell the system when the output voltage is in regulation. To achieve the necessary operation, you can adjust the PG threshold voltage and delay. The threshold voltage of the PG signal is adjusted through external resistors. Adjust the delay with an external capacitor.

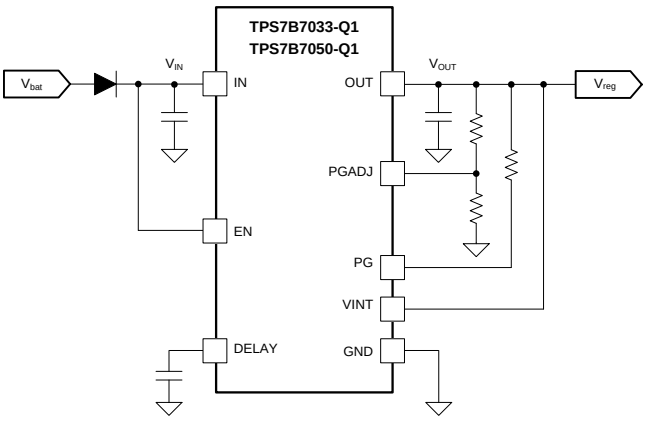
This device operates in ambient temperatures from –40°C to +125°C, and with junction temperatures from –40°C to +150°C. This device also has a thermally conductive package that enables sustained operation despite significant dissipation across the device, a typical property of off-battery operation. These features, along with included current limit and thermal shutdown protection, make the TPS7B70-Q1 an excellent selection to supply power to automotive system components.

Device Information(1)

PART NUMBER	OUTPUT VOLTAGE	PACKAGE
TPS7B70-Q1	3.3 V or 5 V	HTSSOP (16)

(1) For all available packages, see the package option addendum at the end of the data sheet.

Typical Application



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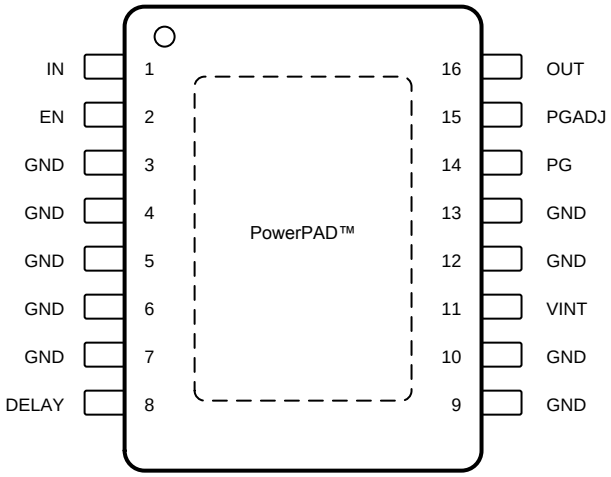
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (August 2018) to Revision A	Page
• Changed device status from *Advance Information* to *Production Data*	1

5 Pin Configuration and Functions

PWP Package
16-Pin HTSSOP With PowerPAD
Top View



Not to scale

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
DELAY	8	O	Power-good delay adjustment pin. Connect this pin through a capacitor to ground to adjust the power-good delay time.
EN	2	I	Device enable pin. Pull this pin down to low-level voltage to disable the device. Pull this pin up to high-level voltage to enable the device.
GND	3, 4, 5, 6, 7, 9, 10, 12, 13	—	Ground reference
IN	1	I	Device input power supply pin
OUT	16	O	Device 3.3-V or 5-V regulated output-voltage pin
PG	14	O	Power-good pin. Open-drain output pin. Pull this pin up to V_{OUT} or to a reference through a resistor. When the output voltage is not ready, this pin is pulled down to ground.
PGADJ	15	O	Power-good threshold-adjustment pin. Connect a resistor divider between the PGADJ and OUT pins to set the power-good threshold. Connect this pin to ground to set the threshold to 91.6% of output voltage V_{OUT}.
VINT	11	I	Internal voltage rail. Tie this pin above 2 V for lowest I_{GND}.
PowerPAD	—	—	Solder thermal pad to board to improve the thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)(2)

			MIN	MAX	UNIT
	Unregulated input	IN, EN	–0.3	45	V
	Power-good delay-timer output	DELAY	–0.3	7	V
	Regulated output	OUT	–0.3	7	V
	Power-good output voltage	PG	–0.3	7	V
	V-internal	VINT	–0.3	7	V
	Power-good threshold-adjustment voltage	PGADJ	–0.3	7	V
T_J	Operating junction temperature		–40	150	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged-device model (CDM), per AEC Q100-011	All pins	±500	
			Corner pins (1, 14, 15, and 28)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Unregulated input	IN	4		40	V
	40-V pins	EN	0		V_{IN}	V
	Regulated output	OUT	0		5.5	V
	Power good	PG	0		5.5	V
	Low voltage pins	PGADJ, DELAY	0		5.5	V
I_{OUT}	Output current		0		300	mA
T_A	Ambient temperature		–40		125	°C
T_J	Junction temperature		–40		150	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS7B70-Q1 PWP (HTSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	23.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	23.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, V_{IN} = 14 V, C_{OUT} ≥ 4.7 µF, and 1 mΩ < ESR < 20 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND CURRENT (IN)						
$I_{(SLEEP)}$	Input sleep current	EN = off			4.5	µA
$I_{(GND)}$	Input quiescent current	V_{IN} = V_{OUT} + 1 V to 40 V, EN = on, VINT > 2 V, I_{OUT} < 1 mA, –40°C ≤ T_J ≤ 85°C		19	29.6	µA
$V_{(UVLO)}$	Undervoltage lockout, falling	Ramp V_{IN} down until output is turned off			2.6	V
$V_{(UVLO\_HYST)}$	UVLO hysteresis			0.5		V
ENABLE INPUT (EN)						
V_{IL}	Low-level input voltage				0.7	V
V_{IH}	High-level input voltage		2			V
V_{hys}	Hysteresis			150		mV
REGULATED OUTPUT (OUT)						
V_{OUT}	Regulated output	V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 0 mA to 300 mA, –40°C ≤ T_J ≤ 125°C	–2%		2%	
		V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 0 mA to 300 mA	–2.5%		2.5%	
$\Delta V_{OUT(\Delta VIN)}$	Line regulation	V_{IN} = V_{OUT} + 1 V to 40 V, I_{OUT} = 1 mA			10	mV
$\Delta V_{OUT(\Delta IOUT)}$	Load regulation	I_{OUT} = 1 mA to 300 mA			20	mV
$V_{(dropout)}$	Dropout voltage (V_{IN} – V_{OUT})(1)(2)	I_{OUT} = 300 mA		300	400	mV
		I_{OUT} = 200 mA		170	325	
$I_{(LIM)}$	Output current limit	V_{OUT} shorted to ground, V_{IN} = 5.6 V	301	680	1000	mA
PSRR	Power-supply ripple rejection(3)	I_{OUT} = 100 mA, C_{OUT} = 10 µF, frequency (f) = 100 Hz		60		dB
		I_{OUT} = 100 mA, C_{OUT} = 10 µF, frequency (f) = 100 kHz		40		
POWER GOOD (PG, PGADJ)						
$V_{OL(PG)}$	PG output, low voltage	I_{OL} = 5 mA, PG pulled low			0.4	V
$I_{lkg(PG)}$	PG pin leakage current	PG pulled to V_{OUT} through a 10-kΩ resistor			1	µA
$V_{(PG\_TH)}$	Default power-good threshold	V_{OUT} powered above the internally set tolerance, PGADJ pin shorted to ground	88.6	91.6	93.6	% of V_{OUT}
$V_{(PG\_HYST)}$	Power-good hysteresis	V_{OUT} falling below the internally set tolerance hysteresis		2		% of V_{OUT}

(1) This test is done with V_{OUT} in regulation, measuring the V_{IN} – V_{OUT} when V_{OUT} drops by 100 mV from the rated output voltage at the specified load.
(2) Dropout is not measured for V_{OUT} = 3.3 V in this test because V_{IN} must be 4 V or greater for proper operation.
(3) Design information—not tested, determined by characterization.

Electrical Characteristics (continued)

T_J = –40°C to 150°C, V_{IN} = 14 V, C_{OUT} ≥ 4.7 µF, and 1 mΩ < ESR < 20 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PGADJ						
$V_{(PGADJ\_TH)}$	Switching voltage for the power-good adjust pin	V_{OUT} is falling	1.067	1.1	1.133	V
POWER-GOOD DELAY						
$I_{(DLY\_CHG)}$	DELAY capacitor charging current		3	5	10	µA
$V_{(DLY\_TH)}$	DELAY pin threshold to release PG high	Voltage at DELAY pin is ramped up	0.95	1	1.05	V
$I_{(DLY\_DIS)}$	DELAY capacitor discharging current	V_{DELAY} = 1 V	0.5			mA
TEMPERATURE						
$T_{(SD)}$	Junction shutdown temperature			175		°C
$T_{(HYST)}$	Hysteresis of thermal shutdown			25		°C

6.6 Switching Characteristics

T_J = –40°C to 150°C, V_I = 14 V, C_O ≥ 4.7 µF, and 1 mΩ < ESR < 20 Ω (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER-GOOD DELAY (DELAY)						
$t_{(DEGLITCH)}$	Power-good deglitch time			180	250	µs
$t_{(DLY\_FIX)}$	Fixed power-good delay	No capacitor connect at DELAY pin		248	900	µs
$t_{(DLY)}$	Power-good delay	Delay capacitor value: $C_{(DELAY)}$ = 100 nF		20		ms

6.7 Typical Characteristics

T_J = –40ºC to 150ºC, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)

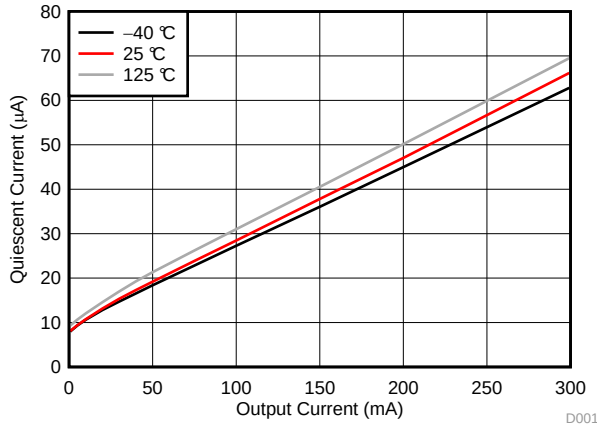


Figure 1. Ground Current vs Output Current

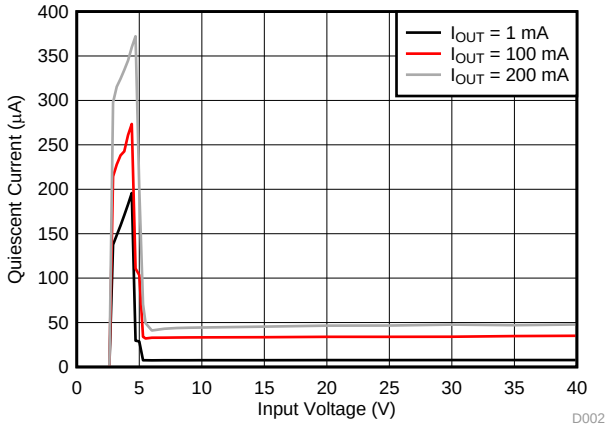


Figure 2. Ground Current vs Input Voltage

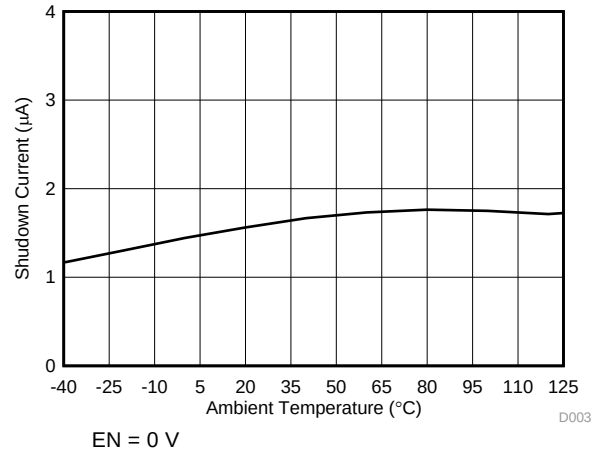


Figure 3. Shutdown Current vs Ambient Temperature

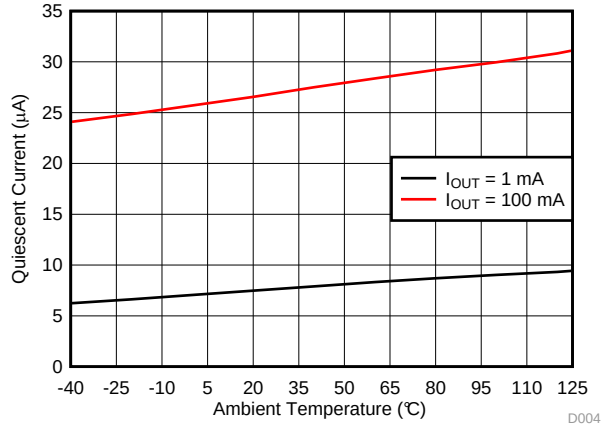


Figure 4. Ground Current vs Ambient Temperature

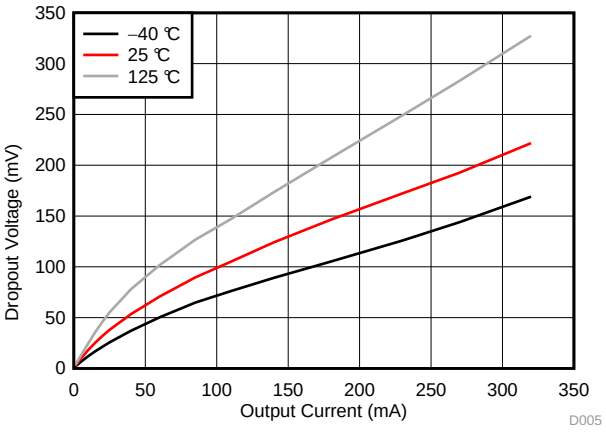


Figure 5. Dropout Voltage vs Output Current

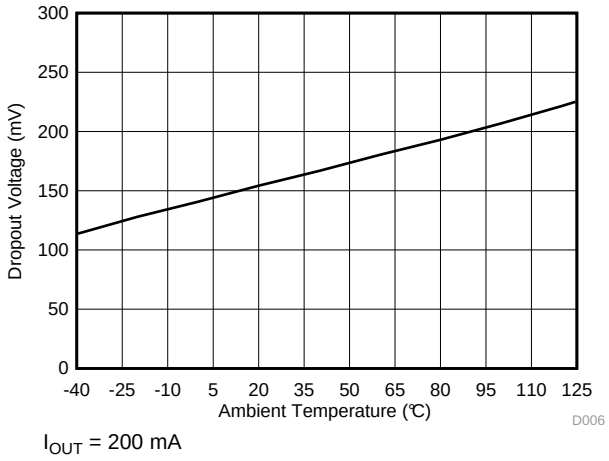
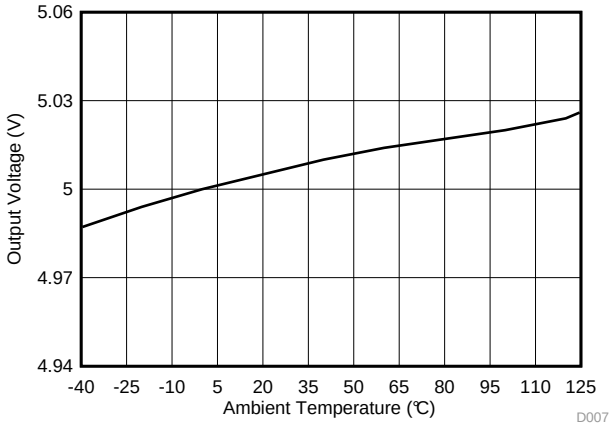


Figure 6. Dropout Voltage vs Ambient Temperature

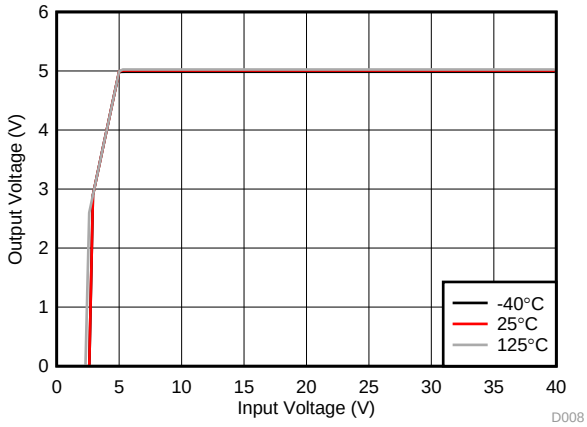
Typical Characteristics (continued)

T_J = –40ºC to 150ºC, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



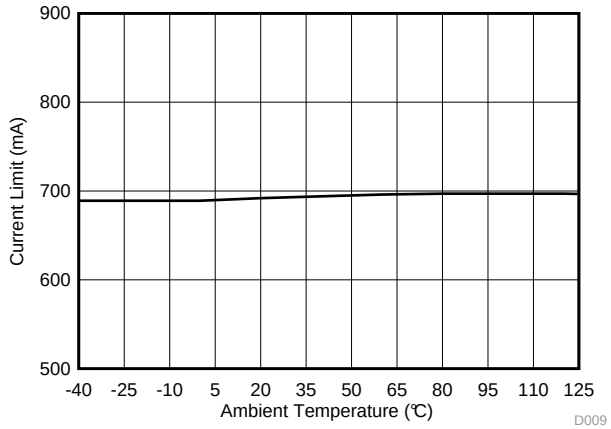
V_{OUT} = 5 V

Figure 7. Output Voltage vs Ambient Temperature



V_{OUT} = 5 V

Figure 8. Output Voltage vs Input Voltage



V_{IN} = 5.6 V

Figure 9. Output Current Limit (I_{LIM}) vs Ambient Temperature

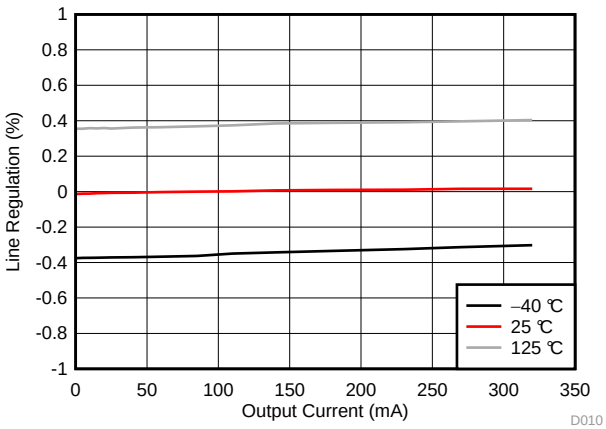


Figure 10. Load Regulation

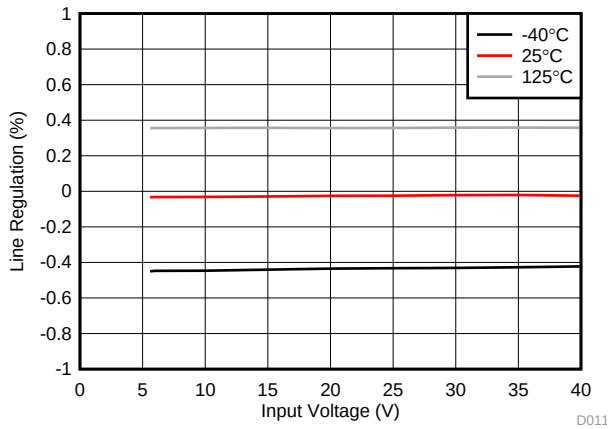
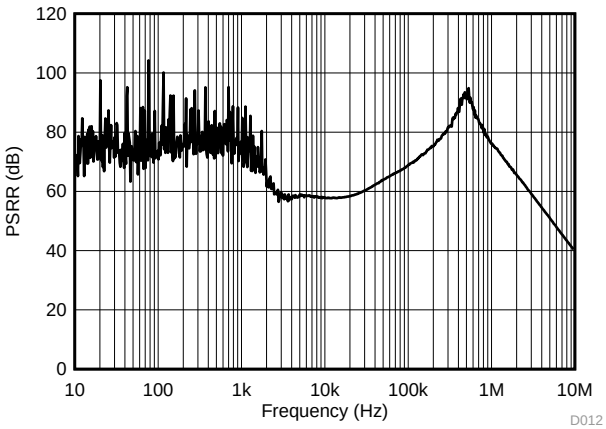


Figure 11. Line Regulation

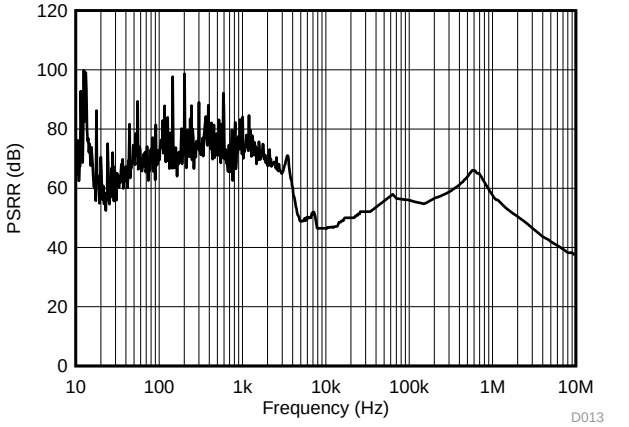


C_{OUT} = 10 µF I_{OUT} = 1 mA T_A = 25°C

Figure 12. PSRR vs Frequency

Typical Characteristics (continued)

T_J = –40ºC to 150ºC, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



C_{OUT} = 10 µF I_{OUT} = 100 mA T_A = 25°C

Figure 13. PSRR vs Frequency

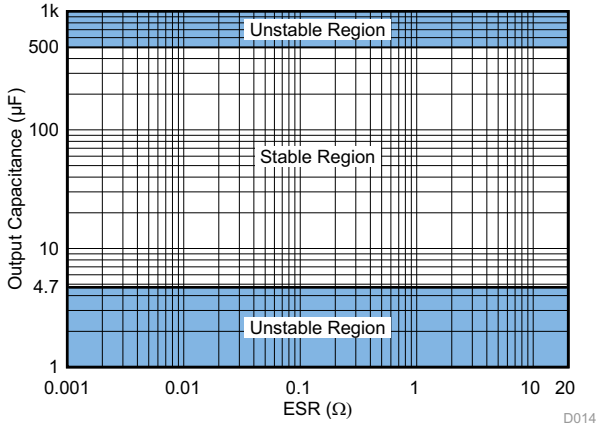
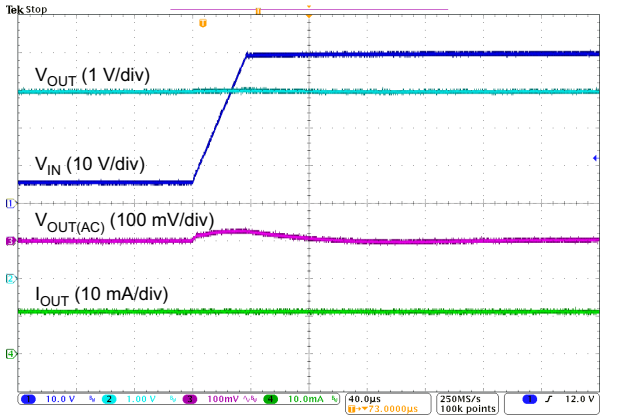
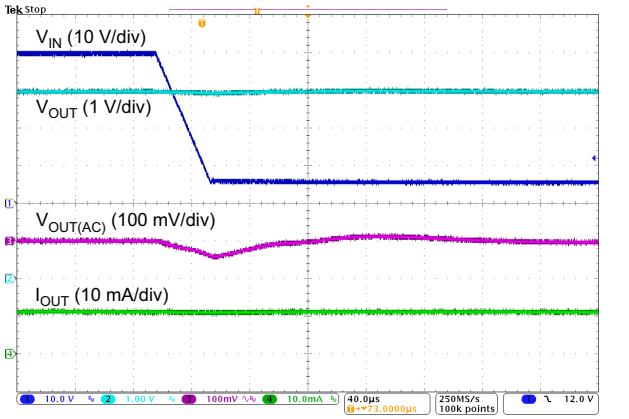


Figure 14. ESR Stability vs Output Capacitance



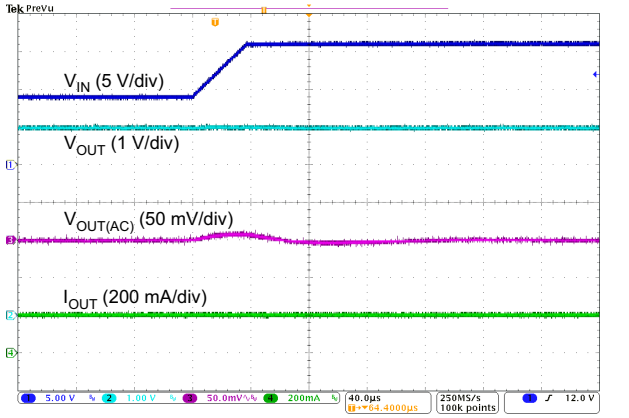
V_{IN} = 6 V to 40 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 1 mA

Figure 15. Line Transient



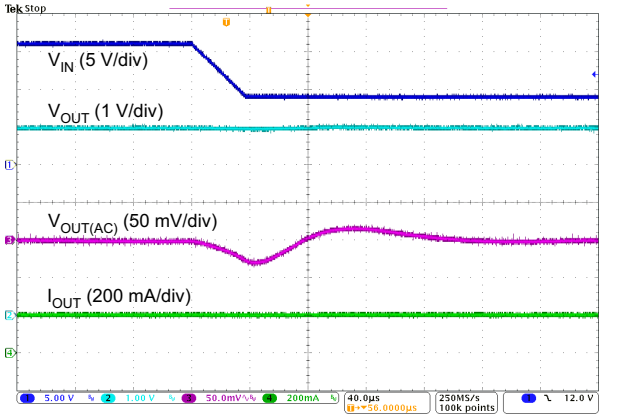
V_{IN} = 40 V to 6 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 1 mA

Figure 16. Line Transient



V_{IN} = 6 V to 40 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 200 mA

Figure 17. Line Transient

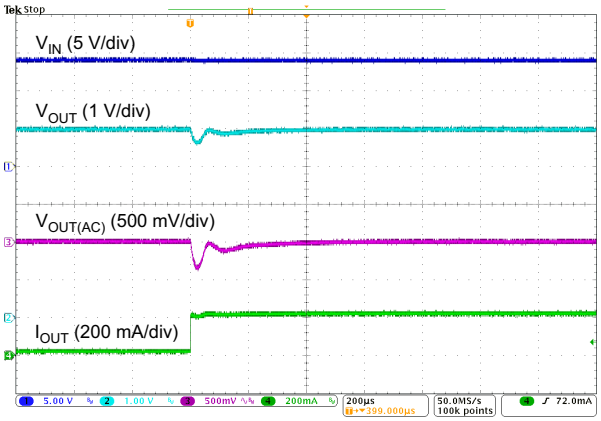


V_{IN} = 40 V to 6 V V_{OUT} = 5 V C_{OUT} = 10 µF
I_{OUT} = 200 mA

Figure 18. Line Transient

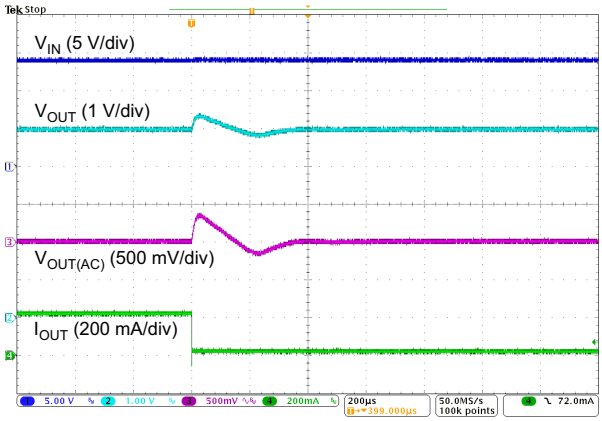
Typical Characteristics (continued)

T_J = –40ºC to 150ºC, V_{IN} = 14 V, and V_{EN} ≥ 2 V (unless otherwise noted)



V_{OUT} = 5 V C_{OUT} = 10 µF I_{OUT} = 1 mA to 200 mA

Figure 19. Load Transient



V_{OUT} = 5 V C_{OUT} = 10 µF I_{OUT} = 200 mA to 1 mA

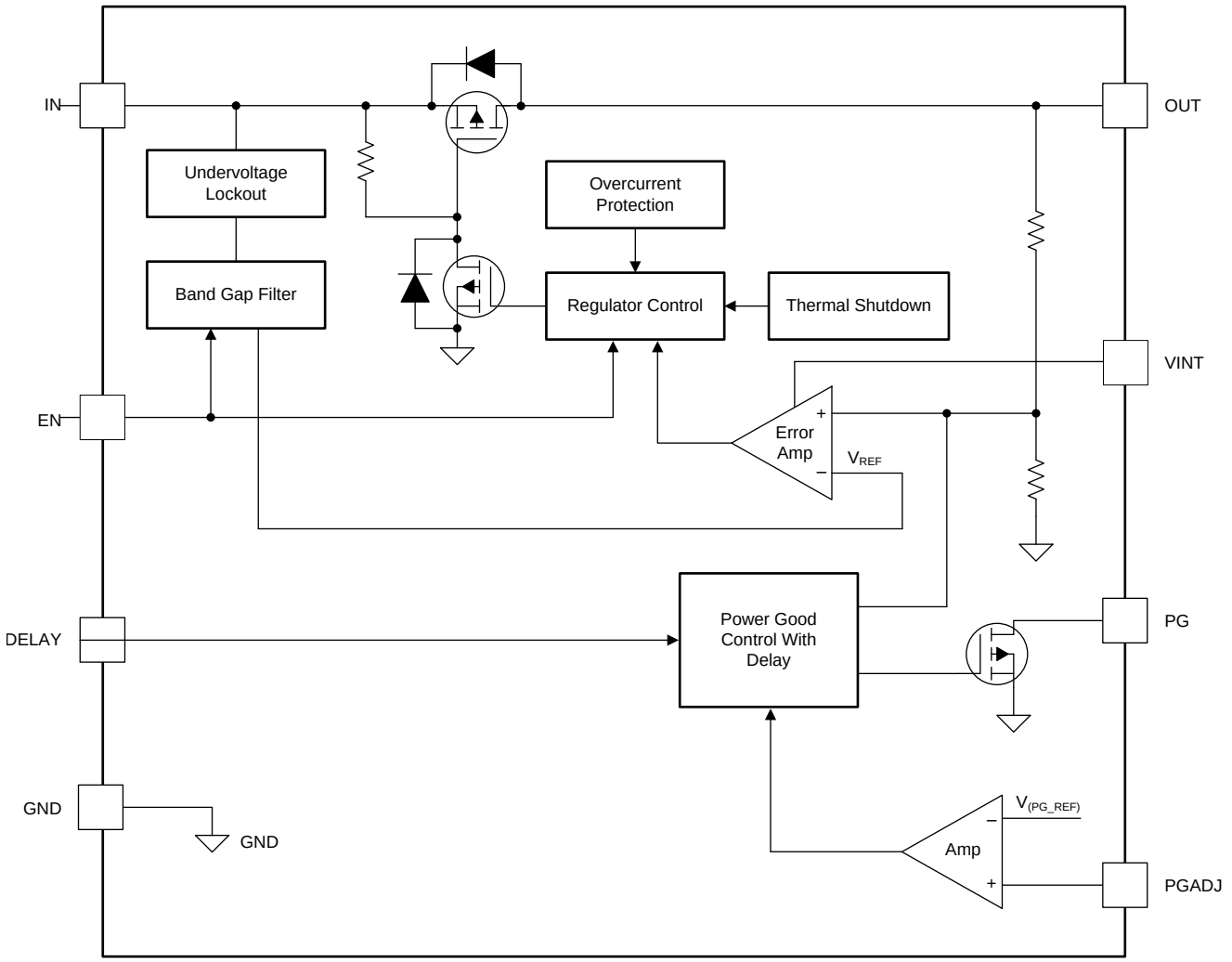
Figure 20. Load Transient

7 Detailed Description

7.1 Overview

The TPS7B70-Q1 is a 300-mA, 40-V monolithic low-dropout linear voltage regulator with adjustable power-good threshold functionality. This voltage regulator consumes only 19-µA quiescent current in light-load applications. Because of the adjustable power-good delay (also called power-on-reset delay) and the adjustable power-good threshold, this device is an excellent choice as a power supply for microprocessors and microcontrollers in automotive applications.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Device Enable (EN)

The EN pin is a high-voltage-tolerant pin. A high input activates the device and turns the regulator on. Connect this input pin to an external microcontroller or a digital control circuit to enable and disable the device, or connect to the IN pin for self-bias applications.

Feature Description (continued)

7.3.2 Adjustable Power-Good Threshold (PG, PGADJ)

The PG pin is an open-drain output with an external pullup resistor to the regulated supply, and the PGADJ pin is a power-good threshold adjustment pin. Connecting the PGADJ pin to GND sets the power-good threshold value to the default, $V_{(PG\_TH)}$. When V_{OUT} exceeds the default power-good threshold, the PG output turns high after the power-good delay has expired. When V_{OUT} falls below $V_{(PG\_TH)} - V_{(PG\_HYST)}$, the PG output turns low after a short deglitch time.

The power-good threshold is also adjustable from 1.1 V to 5 V by using an external resistor divider between PGADJ and OUT. Equation 1 calculates the threshold:

$$V_{(PG\_ADJ)\,falling} = V_{(PGADJ\_TH)\,falling} \times \frac{R1 + R2}{R2}$$

$$V_{(PG\_ADJ)\,risng} = \left[V_{(PGADJ\_TH)\,falling} + 26\ mV\ (typ) \right] \times \frac{R1 + R2}{R2} \quad (1)$$

where:

- $V_{(PG\_ADJ)}$ is the adjustable power-good threshold
- $V_{(PG\_REF)}$ is the internal comparator reference voltage of the PGADJ pin, 1.1 V typical, 2% accuracy specified under all conditions

By setting the power-good threshold $V_{(PG\_ADJ)}$ when V_{OUT} exceeds this threshold, the PG output turns high after the power-good delay has expired. When V_{OUT} falls below $V_{(PG\_ADJ)} - V_{(PG\_HYST)}$, the PG output turns low after a short deglitch time. Figure 21 shows a block diagram of this threshold.

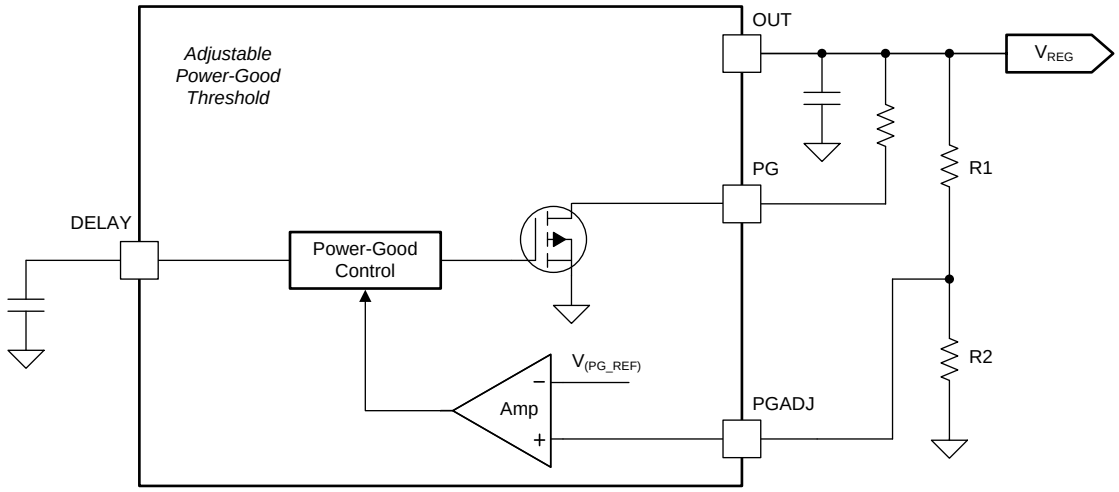


Figure 21. Adjustable Power-Good Threshold

7.3.3 Adjustable Power-Good Delay Timer (DELAY)

The power-good delay, $t_{(DLY)}$, is the time from when PGADJ is greater than $V_{(PG,REF)}$ until the PG pin goes high. The power-good delay is a function of the value of the external capacitor that is connected to the DELAY pin (C_{DELAY}). Connecting an external capacitor from this pin to GND sets the power-good delay. The constant current charges an external capacitor until the voltage exceeds a threshold to trip an internal comparator, and Equation 2 determines the power-good delay. Figure 22 illustrates a timing diagram for power-good power-up conditions.

$$t_{(DLY)} = \frac{C_{DELAY} \times 1\ V}{5\ \mu A} \quad (2)$$

where

- $t_{(DLY)}$ is the adjustable power-good delay
- C_{DELAY} is the value of the power-good delay capacitor

Feature Description (continued)

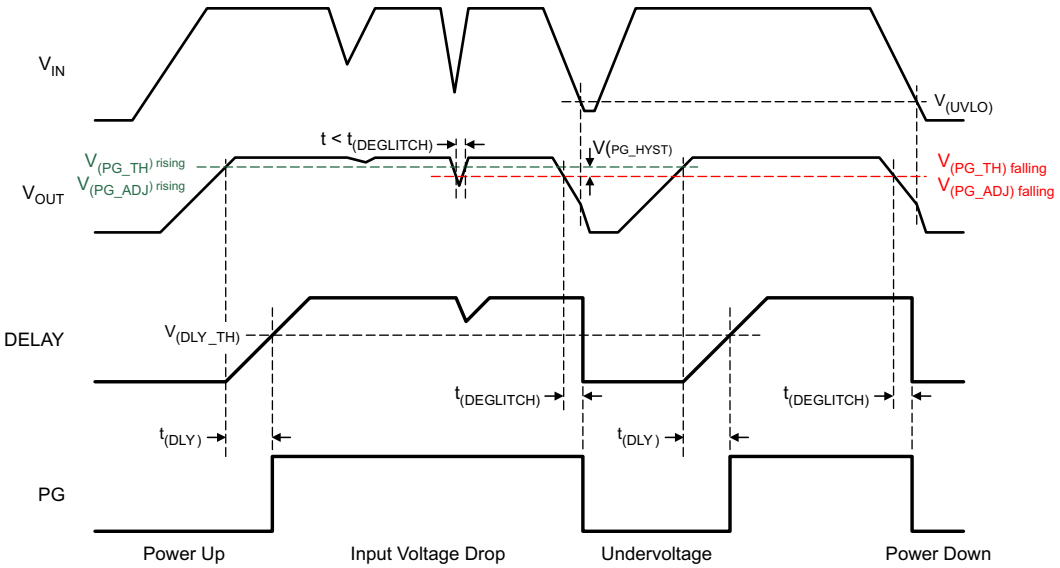


Figure 22. Power-Up and Conditions for Activation of Power Good

If the DELAY pin is open, the default delay time is $t_{(DLY\_FIX)}$.

7.3.4 Undervoltage Shutdown

This device has an integrated undervoltage lockout (UVLO) circuit that shuts down the output if the input voltage falls below an internal UVLO threshold, $V_{(UVLO)}$. The UVLO circuit makes sure that the regulator does not latch into an unknown state during low-input-voltage conditions. If the input voltage has a negative transient that drops below the UVLO threshold and recovers, the regulator shuts down and powers up with a normal power-up sequence after the input voltage rises above the required level.

7.3.5 Current Limit

The TPS7B70-Q1 has current-limit protection to keep the device in a safe operating area when an overload or output short-to-ground condition occurs. This feature protects the device from excessive power dissipation. For example, during a short-circuit condition on the output, fault protection limits the current through the pass element to $I_{(LIM)}$ to protect the device from excessive power dissipation.

7.3.6 Thermal Shutdown

This device incorporates a thermal shutdown (TSD) circuit as a protection from overheating. For continuous normal operation, the junction temperature must not exceed the TSD trip point. If the junction temperature exceeds the TSD trip point, the output turns off. When the junction temperature falls below $T_{(SD)} - T_{(HYST)}$, the output turns on again.

7.4 Device Functional Modes

7.4.1 Operation With Input Voltage Less Than 4 V

The device normally operates with input voltages above 4 V. The device can also operate at lower input voltages; the maximum UVLO voltage is 2.6 V. At input voltages below the actual UVLO voltage, the device does not operate.

7.4.2 Operation With Input Voltage Greater Than 4 V

If the input voltage is greater than the output set value plus the device dropout voltage when the input voltage is greater than 4 V, then the output voltage is equal to the set value. Otherwise, the output voltage is equal to the input voltage minus the dropout voltage.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7B70-Q1 is a 300-mA low-dropout linear regulator with ultra-low quiescent current. The PSpice transient model is available for download on the product folder and can be used to evaluate the basic function of the device.

8.2 Typical Application

Figure 23 shows a typical application circuit for the TPS7B70-Q1. Different values of external components can be used, depending on the end application. An application may require a larger output capacitor during fast load steps to prevent a large drop on the output voltage. Use a low-ESR ceramic capacitor with a dielectric of type X7R.

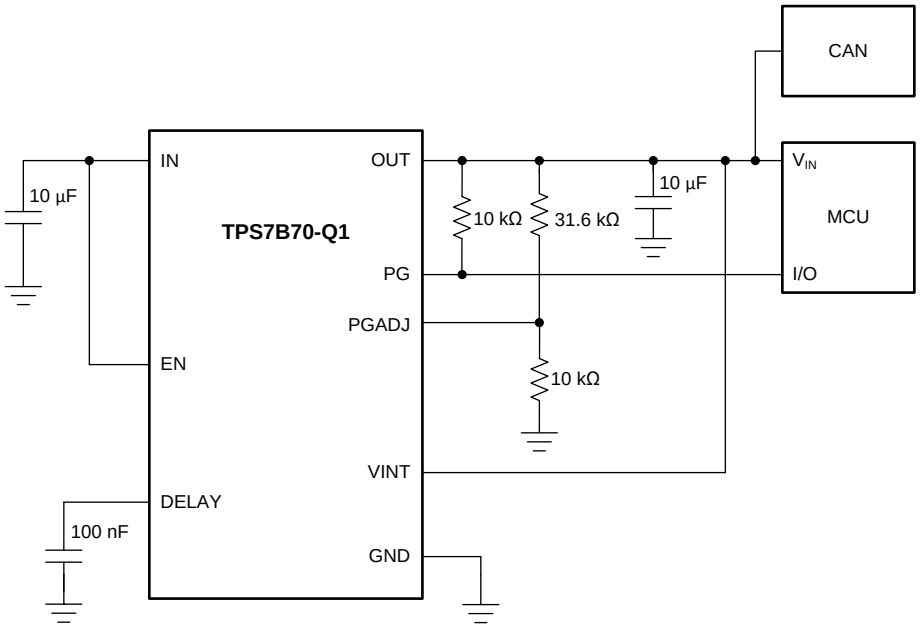


Figure 23. Supply Power to an MCU

Typical Application (continued)

8.2.1 Design Requirements

For this design, the TPS7B70-Q1 must be able to supply a CAN transceiver and an MCU from a 12-V automotive battery. To provide good MCU operation, the PG pin must trip when the output is at 95% of the nominal value. The PG pin must have a 20-ms delay in order to avoid shutting down as a result of temporary glitches.

8.2.2 Detailed Design Procedure

8.2.2.1 Input Capacitor

A 10-µF capacitor in parallel with a 0.1-µF ceramic bypass capacitor is placed at the input in order to keep the input voltage stable. The input can tolerate transients up to 40 V, so the input capacitors have a 50-V voltage rating.

8.2.2.2 Output Capacitor

For this application, a 10-µF X7R ceramic capacitor is used to provide good output transient performance and good loop stability.

8.2.2.3 Power-Good Threshold

The power-good threshold is set by connecting PGADJ to GND, or by connecting PGADJ to a resistor divider from OUT to GND. The *Adjustable Power-Good Threshold (PG, PGADJ)* section provides the method to setup the power-good threshold. Rearranging Equation 1 yields Equation 3, and solves the values of R1 and R2 that are needed to get the 95% falling threshold. In this design, R2 is a 10-kΩ resistor. Solving Equation 3 for R1 gives a value of 33.18 kΩ. This value is not a standard 1% resistor value, so a 31.6-kΩ resistor is chosen for R1.

$$R1 = R2\left(\frac{V_{(PGADJ)falling}}{V_{(PTGADJ\_TH)falling}}\right) \quad (3)$$

8.2.2.4 Power-Good Delay, $t_{(DLY)}$

Set the power-good delay with an external capacitor (C_{DELAY}) to ground. Calculate the correct capacitance with Equation 2. This application requires a delay of 20 ms, so solve for the correct capacitance required to get this delay. As shown in Equation 4, rearrange Equation 2 to solve for C_{DELAY}.

$$C_{DELAY} = t_{DLY} \times 5\mu A \quad (4)$$

8.2.3 Application Curve

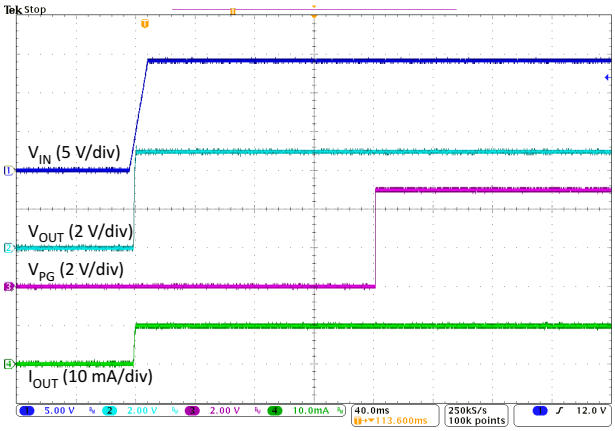


Figure 24. Power-Up Waveform

9 Power Supply Recommendations

The device is designed to operate from an input-voltage supply range from 4 V to 40 V. This input supply must be well regulated. If the input supply is located more than a few inches from the TPS7B70-Q1, add a capacitor with a value of ≥ 10 µF with a 0.1-µF ceramic bypass capacitor in parallel at the input.

10 Layout

10.1 Layout Guidelines

For LDO power supplies, especially high-voltage and high-current supplies, layout is an important step. If the layout is not carefully designed, the regulator cannot deliver enough output current because of thermal limitations. To improve the thermal performance of the device and maximize the current output at high ambient temperature, spread out the thermal pad as much as possible, and put enough thermal vias on the thermal pad. Figure 25 shows an example layout.

10.2 Layout Example

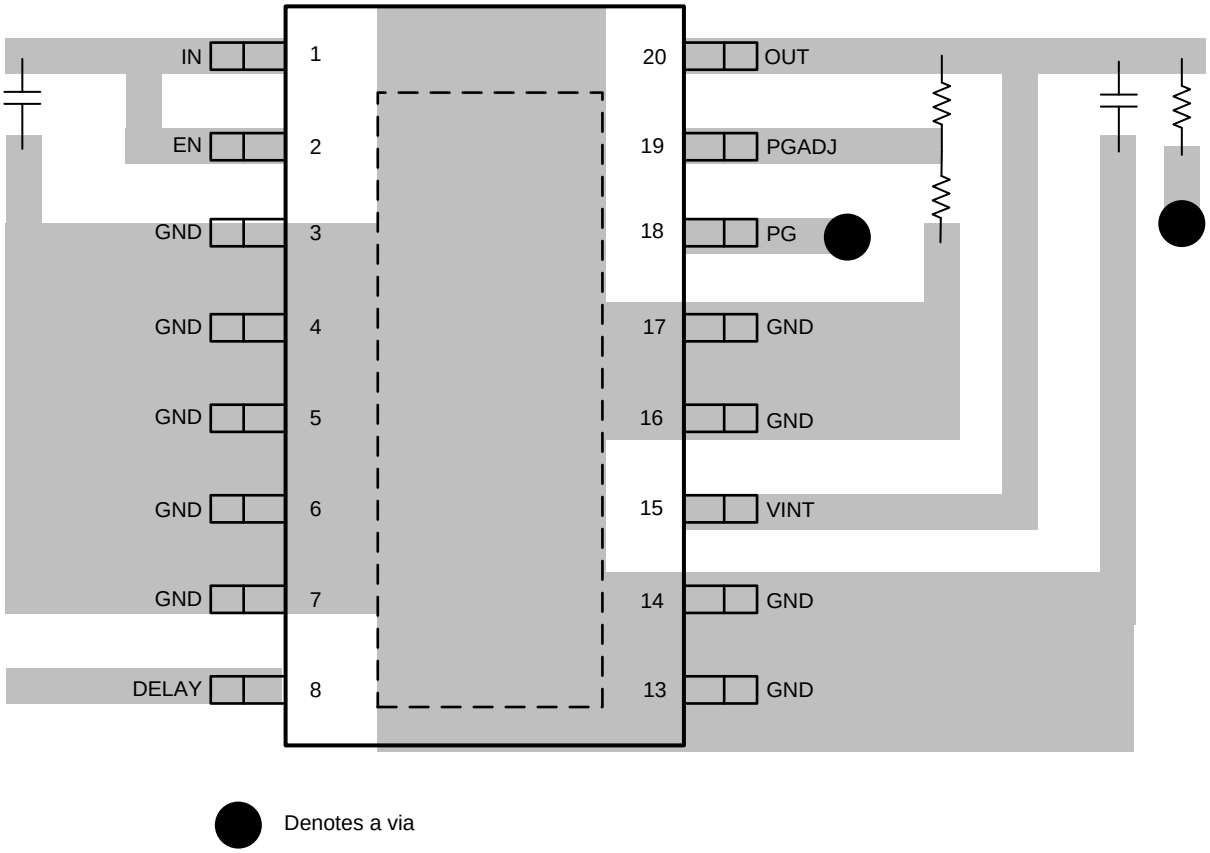


Figure 25. Layout Example

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Texas Instruments, *TPS7B70EVM-008 Evaluation Module* user's guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

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All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated devices. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS7B7033QPWPRQ1	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B7033Q
TPS7B7050QPWPRQ1	Active	Production	HTSSOP (PWP) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 125	7B7050Q

(1) Status: For more details on status, see our product life cycle.

(2) Material type: When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) RoHS values: Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) Lead finish/Ball material: Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

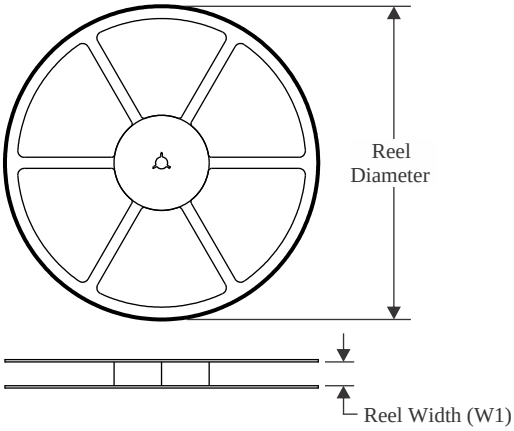
(5) MSL rating/Peak reflow: The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

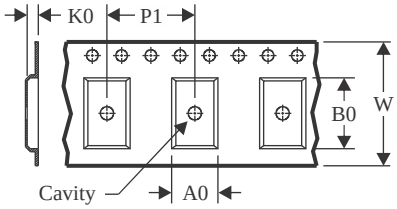
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

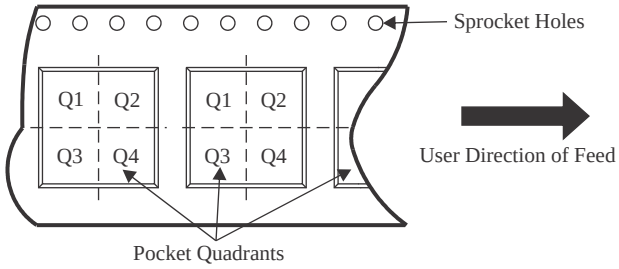


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

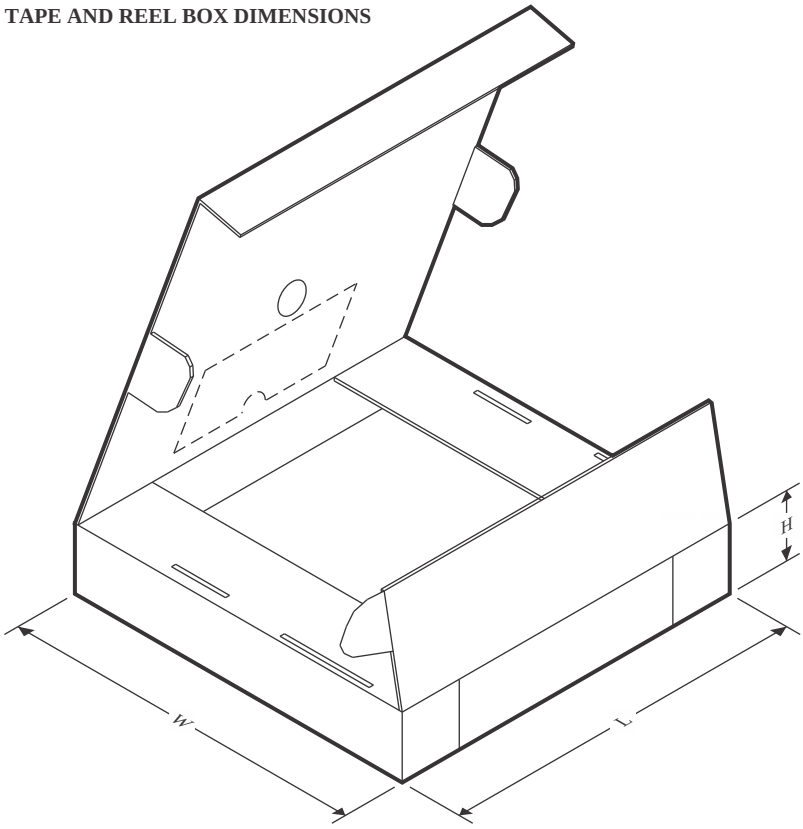
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7B7033QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS7B7050QPWPRQ1	HTSSOP	PWP	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

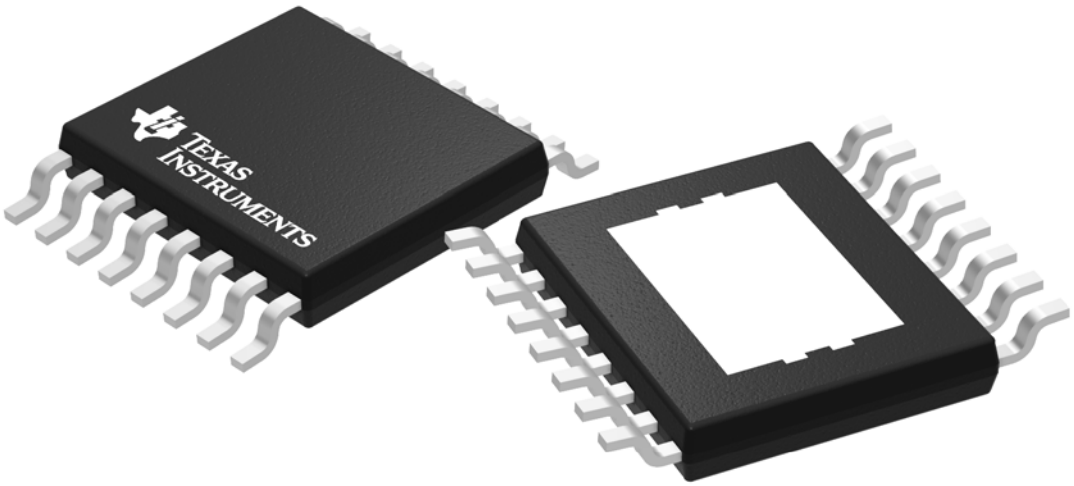


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7B7033QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0
TPS7B7050QPWPRQ1	HTSSOP	PWP	16	2000	350.0	350.0	43.0

PWP 16 PowerPAD™ TSSOP - 1.2 mm max height

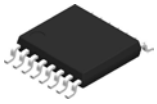
PLASTIC SMALL OUTLINE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

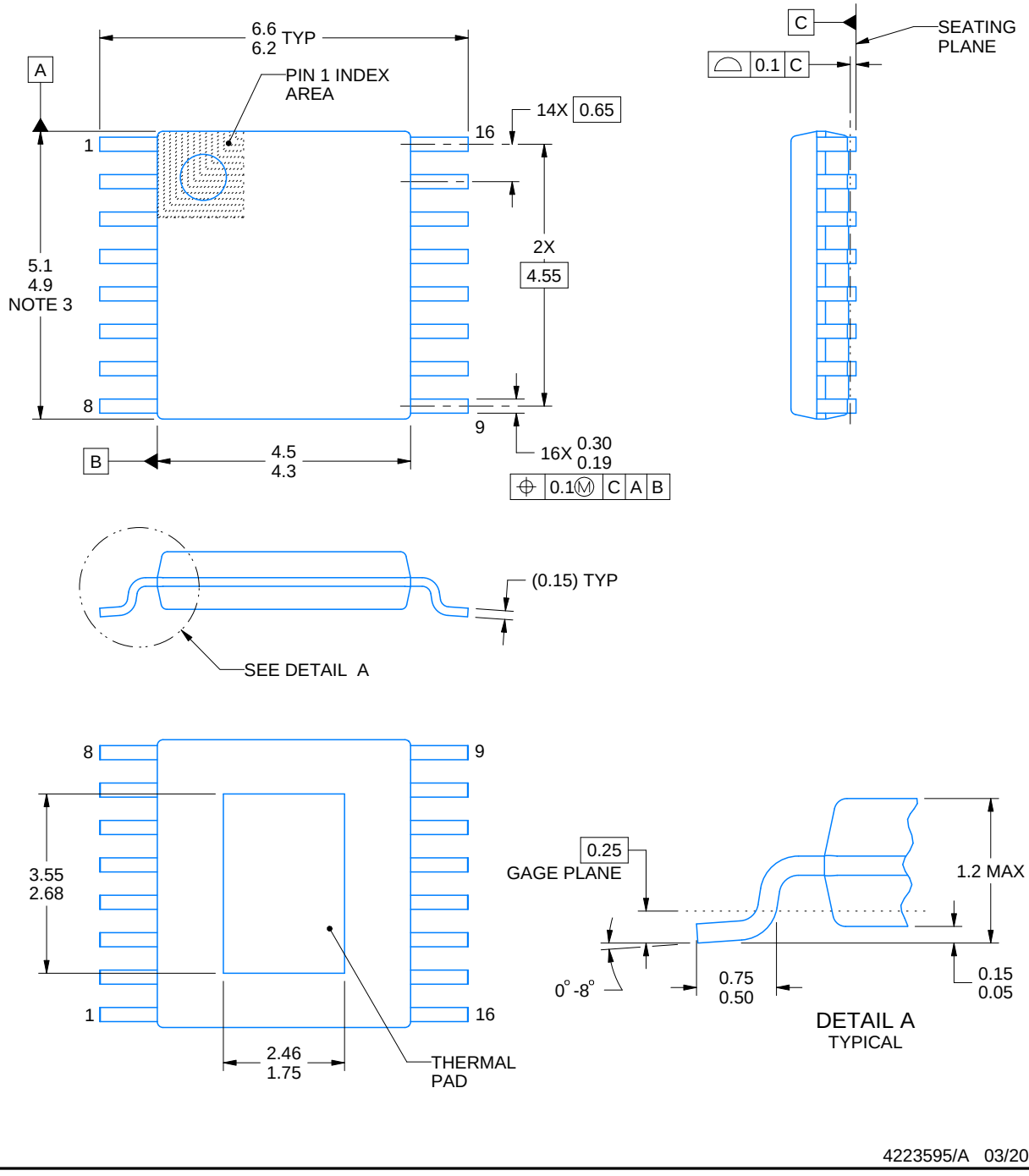
PACKAGE OUTLINE

PWP0016J



PowerPAD™ TSSOP - 1.2 mm max height

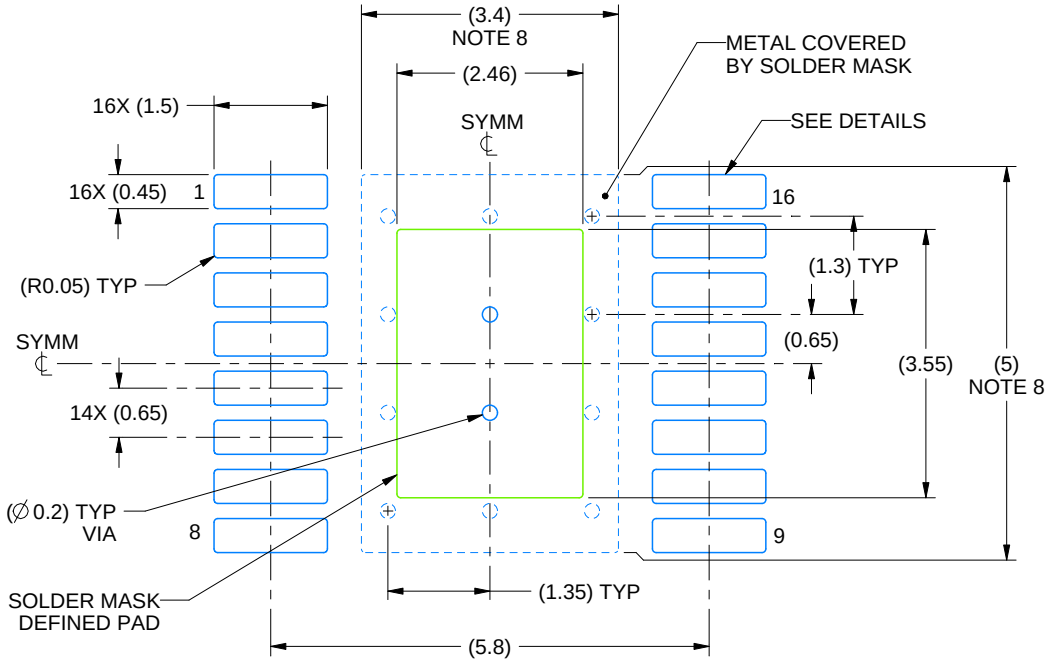
SMALL OUTLINE PACKAGE



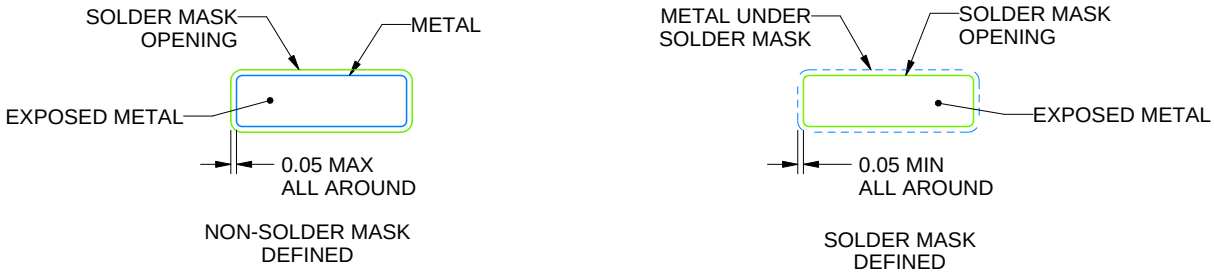
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

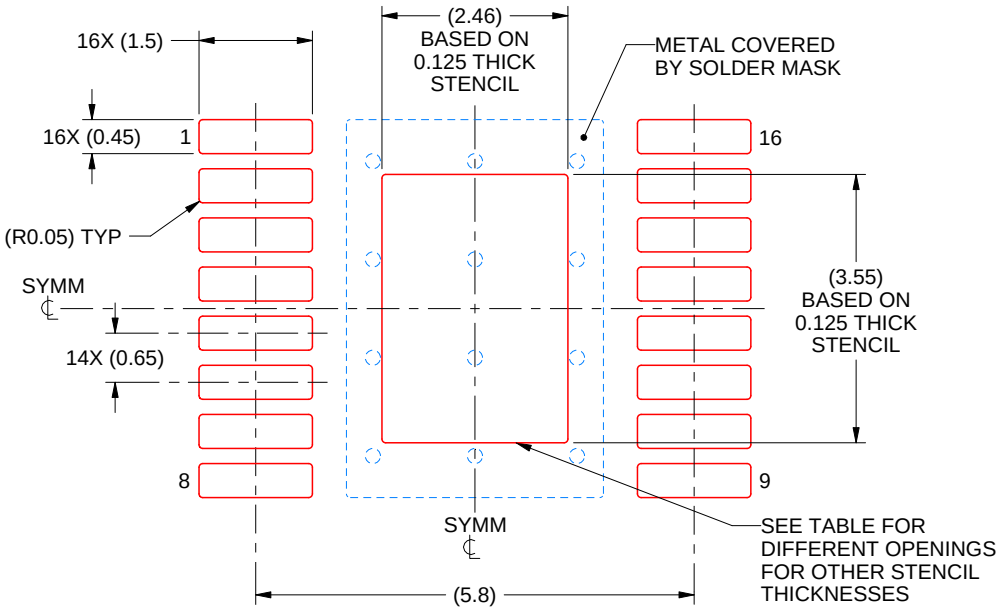


SOLDER MASK DETAILS

4223595/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
8. Size of metal pad may vary due to creepage requirement.
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.75 X 3.97
0.125	2.46 X 3.55 (SHOWN)
0.15	2.25 X 3.24
0.175	2.08 X 3.00

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NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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