1 Features

- 1.6-V to 5.5-V input voltage range
  - Device input voltage > 1.65 V for start-up
- 1.2-V to 5.3-V output voltage range (adjustable)
- High output current capability, 3-A peak switch current
  - 2-A output current for \( V_{\text{IN}} \geq 3 \text{ V} \), \( V_{\text{OUT}} = 3.3 \text{ V} \)
  - 1.5-A output current for \( V_{\text{IN}} \geq 2.7 \text{ V} \), \( V_{\text{OUT}} = 3.3 \text{ V} \)
- High efficiency over the entire load range
  - 8-μA typical quiescent current
  - Power save mode
- 150-mV load-step response at a 1-A current step
- Peak current buck-boost mode architecture
  - Seamless mode transition with < 20-mV output ripple
  - Forward and reverse current operation
  - Start-up into pre-biased outputs
  - Fixed-frequency operation with 2-MHz switching
- Safety and robust operation features
  - Overcurrent protection and short-circuit protection
  - Integrated soft start with active ramp adoption
  - Overtemperature protection and overvoltage protection
  - True shutdown function with load disconnect
  - Forward and backward current limit
- Small solution size
  - Small 1-μH inductor
  - Works with one 0805 output capacitor over the full \( V_{\text{OUT}} \) range
- Create a custom design using the TPS631000 with the WEBENCH® Power Designer

2 Applications

- System pre-regulator (smartphone, tablet, terminal, telematics)
- Point-of-load regulation (wired sensor, port/cable adapter, and dongle)
- Fingerprint, camera sensors (electronic smart lock, IP network camera)
- RF amplifier supply (smart sensors)
- Voltage stabilizer (datacom, optical modules, cooling/heating)

3 Description

The TPS631000 is a constant frequency peak current mode control buck-boost converter. The device has a 3-A peak current limit (typical) and 1.6-V to 5.5-V input voltage range. The TPS631000 provides a power supply solution for system pre-regulators and voltage stabilizers.

Depending on the input voltage, the TPS631000 automatically operates in boost, buck, or in 3-cycle buck-boost mode when the input voltage is approximately equal to the output voltage. The transitions between modes happen at a defined duty cycle and avoid unwanted toggling within the modes to reduce output voltage ripple. 8-μA quiescent current and power save mode power enable the highest efficiency for light to no-load conditions.

The TPS631000 offers a very small solution size with a 1.2-mm \( \times \) 2.1-mm SOT-583 package, a 1-μH inductor, and one 0805 output capacitor.

Device Information

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE(1)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS631000</td>
<td>SOT-583</td>
<td>1.6 mm ( \times ) 2.1 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Efficiency Target vs Output Current (\( V_{\text{OUT}} = 3.3 \text{ V} \))
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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision A (January 2022) to Revision B (June 2022)

<table>
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<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>7</td>
</tr>
<tr>
<td>11</td>
</tr>
<tr>
<td>14</td>
</tr>
</tbody>
</table>

- Removed reference to PSM
- Updated Table 8-2
- Updated Table 8-6

### Changes from Revision * (October 2021) to Revision A (January 2022)

<table>
<thead>
<tr>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

- Changed document status from Advance Information to Production Data
5 Pin Configuration and Functions

![Pin Configuration Diagram](https://www.ti.com/lit/ds/svsf3b/svsf3b.pdf)

**Figure 5-1. 8-Pin DRL SOT-5X3 Package (Top View)**

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOUT</td>
<td>PWR</td>
<td>Power stage output</td>
</tr>
<tr>
<td>LX2</td>
<td>PWR</td>
<td>Inductor switching node of the boost stage</td>
</tr>
<tr>
<td>LX1</td>
<td>PWR</td>
<td>Inductor switching node of the buck stage</td>
</tr>
<tr>
<td>VIN</td>
<td>PWR</td>
<td>Supply input voltage</td>
</tr>
<tr>
<td>EN</td>
<td>I</td>
<td>Device enable. Set High to enable and Low to disable. It must not be left floating.</td>
</tr>
<tr>
<td>MODE</td>
<td>I</td>
<td>PFM/PWM selection. Set Low for power save mode, set High for forced PWM. It must not be left floating.</td>
</tr>
<tr>
<td>GND</td>
<td>PWR</td>
<td>Power ground</td>
</tr>
<tr>
<td>FB</td>
<td>I</td>
<td>Voltage feedback. Sensing pin</td>
</tr>
</tbody>
</table>

(1) PWR = power, I = input
6 Specifications

6.1 Absolute Maximum Ratings
over operating junction temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>(V_{\text{I}})</th>
<th>Input voltage ((\text{VIN}, \text{LX1}, \text{LX2}, \text{VOUT}, \text{EN}, \text{FB}, \text{MODE}))(^{(2)})</th>
<th>(\text{MIN})</th>
<th>(\text{MAX})</th>
<th>(\text{UNIT})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{I}})</td>
<td>Input voltage for less than 10 ns ((\text{LX1}, \text{LX2}))(^{(2)})</td>
<td>–0.3</td>
<td>7</td>
<td>(\text{V})</td>
</tr>
<tr>
<td>(T_{\text{J}})</td>
<td>Operating junction temperature</td>
<td>–40</td>
<td>150</td>
<td>(\text{°C})</td>
</tr>
<tr>
<td>(T_{\text{stg}})</td>
<td>Storage temperature</td>
<td>–65</td>
<td>150</td>
<td>(\text{°C})</td>
</tr>
</tbody>
</table>

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) All voltage values are with respect to network ground terminal, unless otherwise noted.

6.2 ESD Rating

<table>
<thead>
<tr>
<th>(V_{\text{ESD}})</th>
<th>Electrostatic discharge</th>
<th>(\text{VALUE})</th>
<th>(\text{UNIT})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{ESD}})</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(^{(1)})</td>
<td>±1000</td>
<td>(\text{V})</td>
</tr>
<tr>
<td>(V_{\text{ESD}})</td>
<td>Charged-device model (CDM), per JEDEC specification JS-002, all pins(^{(2)})</td>
<td>± 500</td>
<td>(\text{V})</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating junction temperature (unless otherwise noted)

<table>
<thead>
<tr>
<th>(V_{\text{I}})</th>
<th>Supply voltage</th>
<th>(\text{MIN})</th>
<th>(\text{NOM})</th>
<th>(\text{MAX})</th>
<th>(\text{UNIT})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(V_{\text{O}})</td>
<td>Output voltage</td>
<td>1.2</td>
<td>5.3</td>
<td>(\text{V})</td>
<td></td>
</tr>
<tr>
<td>(C_{\text{I}})</td>
<td>Input capacitance (V_{\text{I}} = 1.6 \text{ V to } 5.5 \text{ V})</td>
<td>4.2</td>
<td>(\mu\text{F})</td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{\text{O}})</td>
<td>Output capacitance (1.2 \text{ V} \leq V_{\text{O}} \leq 3.6 \text{ V}, \text{nominal value at } V_{\text{O}} = 3.3 \text{ V})</td>
<td>10.4</td>
<td>16.9</td>
<td>330</td>
<td>(\mu\text{F})</td>
</tr>
<tr>
<td>(C_{\text{O}})</td>
<td>Output capacitance (3.6 \text{ V} &lt; V_{\text{O}} \leq 5.3 \text{ V}, \text{nominal value at } V_{\text{O}} = 5 \text{ V})</td>
<td>7.95</td>
<td>10.6</td>
<td>330</td>
<td>(\mu\text{F})</td>
</tr>
<tr>
<td>(L)</td>
<td>Inductance</td>
<td>0.7</td>
<td>1</td>
<td>1.3</td>
<td>(\mu\text{H})</td>
</tr>
<tr>
<td>(T_{\text{J}})</td>
<td>Operating junction temperature range</td>
<td>–40</td>
<td>125</td>
<td>(\text{°C})</td>
<td></td>
</tr>
</tbody>
</table>

6.4 Thermal Information
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>(\text{THERMAL METRIC}(^{(1)}))</th>
<th>TPS631000 DRL PACKAGE</th>
<th>(\text{UNIT})</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\text{JJA}})</td>
<td>Junction-to-ambient thermal resistance</td>
<td>132.7</td>
</tr>
<tr>
<td>(R_{\text{JJC(top)}})</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>43.8</td>
</tr>
<tr>
<td>(R_{\text{JB}})</td>
<td>Junction-to-board thermal resistance</td>
<td>27.3</td>
</tr>
<tr>
<td>(\Psi_{\text{JT}})</td>
<td>Junction-to-top characterization parameter</td>
<td>1.2</td>
</tr>
<tr>
<td>(\Psi_{\text{JB}})</td>
<td>Junction-to-board characterization parameter</td>
<td>26.6</td>
</tr>
<tr>
<td>(R_{\text{JJC(bot)}})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
### 6.5 Electrical Characteristics

Over operating junction temperature range and recommended supply voltage range (unless otherwise noted). Typical values are at \( V_I = 3.8 \, V \), \( V_O = 3.3 \, V \), and \( T_J = 25^\circ C \) (unless otherwise noted).

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>SUPPLY</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{SD} )</td>
<td>Shutdown current into VIN ( V_I = 3.8 , V ), ( V_O = 3.3 , V ), ( T_J = 25^\circ C )</td>
<td>0.5</td>
<td>0.9</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_Q )</td>
<td>Quiescent current into VIN ( V_I = 2.2 , V ), ( V_O = 3.3 , V ), no switching</td>
<td>0.15</td>
<td>6.1</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td>Quiescent current into VOUT ( V_I = 2.2 , V ), ( V_O = 3.3 , V ), no switching</td>
<td>8</td>
<td></td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( V_{IT^+} )</td>
<td>Positive-going UVLO threshold voltage</td>
<td>1.5</td>
<td>1.55</td>
<td>1.599</td>
<td>V</td>
</tr>
<tr>
<td>( V_{IT^-} )</td>
<td>Negative-going UVLO threshold voltage</td>
<td>0.77</td>
<td>0.98</td>
<td>1.2</td>
<td>V</td>
</tr>
<tr>
<td>( V_{UVLO} )</td>
<td>UVLO threshold voltage hysteresis</td>
<td>0.5</td>
<td>0.66</td>
<td>0.76</td>
<td>V</td>
</tr>
<tr>
<td>( I_{hys} )</td>
<td>Hysteresis voltage</td>
<td>±0.01</td>
<td>±0.25</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{IH} )</td>
<td>High-level input current ( V_I = 1.5 , V ), ( V_O = 3.3 , V ), no pullup resistor</td>
<td>±0.01</td>
<td>±0.1</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{IL} )</td>
<td>Low-level input current ( V_I = 0 , V ), ( V_O = 3.3 , V ), no pullup resistor</td>
<td>±0.01</td>
<td>±0.3</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( I_{BAIS} )</td>
<td>Input bias current ( V_I = 5.5 , V )</td>
<td>±0.01</td>
<td>±0.3</td>
<td></td>
<td>( \mu A )</td>
</tr>
<tr>
<td><strong>POWER SWITCH</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( f_{DS(on)} )</td>
<td>On-state resistance ( V_I = 3.8 , V ), ( V_O = 3.3 , V ), test current = 0.2 A</td>
<td>45</td>
<td></td>
<td></td>
<td>m( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>m( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>50</td>
<td></td>
<td></td>
<td>m( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>85</td>
<td></td>
<td></td>
<td>m( \Omega )</td>
</tr>
<tr>
<td>( I_{REV} )</td>
<td>Reverse current into VOUT ( V_I = 0 , V ), ( V_O = 3.3 , V ), ( V_{EN} = 0 , V )</td>
<td>0.8</td>
<td></td>
<td>2</td>
<td>( \mu A )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( T_J = 25^\circ C )</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>( T_J = -40^\circ C ) to 125°C</td>
</tr>
<tr>
<td><strong>CURRENT LIMIT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( I_{PEAK} )</td>
<td>Switch peak current limit ( 1 ) ( Q1 ), ( V_O = 3.3 , V )</td>
<td>2.6</td>
<td>3</td>
<td>3.35</td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Output sourcing current ( V_I = 3.3 , V )</td>
<td></td>
<td></td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Output sinking current ( V_I = 3.3 , V )</td>
<td>−0.7</td>
<td>−0.55</td>
<td>−0.45</td>
<td>A</td>
</tr>
<tr>
<td>( I_{PFM_entry} )</td>
<td>The output current at PFM mode entry threshold (peak) current ( 1 ) ( I_Q ) falling</td>
<td>145</td>
<td></td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td><strong>OUTPUT</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{FB} )</td>
<td>Reference voltage on feedback pin</td>
<td>495</td>
<td>500</td>
<td>505</td>
<td>mV</td>
</tr>
<tr>
<td><strong>PROTECTION FEATURES</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{T+(OV)} )</td>
<td>Positive-going OVP threshold voltage</td>
<td>5.55</td>
<td>5.75</td>
<td>5.95</td>
<td>V</td>
</tr>
<tr>
<td>( V_{T+(IV)} )</td>
<td>Positive-going IVP threshold voltage</td>
<td>5.55</td>
<td>5.75</td>
<td>5.95</td>
<td>V</td>
</tr>
<tr>
<td><strong>TIMING PARAMETERS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( t_{l(EN)} )</td>
<td>Delay between a rising edge on the EN pin and the start of the output voltage ramp</td>
<td>0.87</td>
<td>1.5</td>
<td></td>
<td>ms</td>
</tr>
<tr>
<td>( t_{l(ramp)} )</td>
<td>Soft-start ramp time</td>
<td>6.42</td>
<td>7.55</td>
<td>8.68</td>
<td>ms</td>
</tr>
<tr>
<td>( f_{SW} )</td>
<td>Switching frequency</td>
<td>1.8</td>
<td></td>
<td>2</td>
<td>2.2</td>
</tr>
</tbody>
</table>

(1) Current limit production test are performed under DC conditions. The current limit in operation will be somewhat higher and depend on propagation delay and the applied external components.
7 Detailed Description

7.1 Overview

The TPS631000 is a constant frequency peak current mode control buck-boost converter. The converter uses a fixed-frequency topology with approximately 2-MHz switching frequency. The modulation scheme has three clearly defined operation modes where the converter enters with defined thresholds over the full operation range of \( V_{IN} \) and \( V_{OUT} \). The maximum output current is determined by the Q1 peak current limit, which is typically 3 A.

7.2 Functional Block Diagram

7.3 Feature Description

7.3.1 Undervoltage Lockout (UVLO)

The input voltage of the VIN pin is continuously monitored if the device is not in shutdown mode. UVLO only stops or starts the converter operation. The UVLO does not impact the core logic of the device. UVLO avoids a brownout of the device during device operation. In case the supply voltage on the VIN pin is lower that the negative-going threshold of UVLO, the converter stops its operation. To avoid a false disturbance of the power conversion, the UVLO falling threshold logic signal is digitally de-glitched.

If the supply voltage on the VIN pin recovers to be higher than the UVLO rising threshold, the converter returns to operation. In this case, the soft-start procedure restarts faster than under start-up without a pre-biased output.
7.3.2 Enable and Soft Start

When the input voltage is above the UVLO rising threshold and the EN pin is pulled to a voltage above 1.2 V, the TPS631000 is enabled and starts up after a short delay time, $t_{d(EN)}$.

The TPS631000 has an inductor peak current clamp to limit inrush current during start-up. When the minimum current clamp ($I_{L(lim_SS)}$) is lower than the current that is necessary to follow the voltage ramp, the current automatically increases to follow the voltage ramp. The minimum current limit ensures as fast as possible soft start if the capacitance is chosen lower than what the ramp time $t_{d(RAMP)}$ was selected for.

In a typical start-up case as shown in Figure 7-1 (low output load, typical output capacitance), the minimum current clamp limits the inrush current and charges the output capacitor. The output voltage then rises faster than the reference voltage ramp (see phase A in Figure 7-1). To avoid an output overshoot, the current clamp is deactivated when the output is close to the target voltage and follows the reference voltage ramp slew value given by the voltage ramp, which is finishing the start up (see phase B in Figure 7-1). The transition from the minimum current clamp operation is sensed by using the threshold $95\% \times V_{OUT\_TARGET}$. After phase B, the output voltage is well regulated to the nominal target voltage. The current waveform depends on the output load and operation mode.

7.3.3 Adjustable Output Voltage

The output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is given by $V_{FB}$. The low-side resistor $R2$ (between FB and GND) must not exceed 100 kΩ. The high-side resistor $R1$ (between FB and VOUT) is calculated by Equation 1.

$$R1 = R2 \times (V_{OUT} / V_{FB} - 1)$$

The typical $V_{FB}$ voltage is 0.5 V.

7.3.4 Mode Selection (PFM/FPWM)

The mode pin is a digital input to enable PFM/FPWM. When the MODE pin is connected to logic low, the device works in auto PFM mode. The device features a power save mode to maintain the highest efficiency over the full operating output current range. PFM automatically changes the converter operation from CCM to pulse frequency modulation.

When the MODE pin is connected to logic high, the device works in forced PWM mode, regardless of the output current, to achieve minimum output ripple.
7.3.5 Reverse Current Operation
The device can support reverse current operation (the current flows from VOUT pin to VIN pin). If the output feedback voltage on the FB pin is higher than the reference voltage, the converter regulation forces a current into the input capacitor. The reverse current operation is independent of the $V_{IN}$ voltage or $V_{OUT}$ voltage ratio, hence it is possible on all device operation modes boost, buck, or buck-boost.

7.3.6 Protection Features
The following sections describe the protection features of the device.

7.3.6.1 Input Overvoltage Protection
The TPS631000 has input overvoltage protection. It avoids any damage to the device in case the current flows from the output to the input and the input source cannot sink current (for example, a diode in the supply path).

If forced PWM mode is active, the current can go negative until it reaches the sink current limit. Once the input voltage threshold, $V_{T+(IVP)}$, is reached on the VIN pin, the protection disables forced PWM mode and only allows current to flow from VIN to VOUT. After the input voltage drops under the input voltage protection threshold, forced PWM mode can be activated again.

7.3.6.2 Output Overvoltage Protection
The TPS631000 has the output overvoltage protection. It avoids any damage to the device in case the external feedback pin is not working properly.

If the output voltage threshold $V_{T+(OVP)}$ is reach on the VOUT pin, the protection disables converter power stage and enter a high impedance at the switch nodes.

7.3.6.3 Short Circuit Protection
The device features peak current limit performance at short circuit protection. Figure 7-2 shows a typical device behavior of an short/overload event of the short circuit protection.

![Figure 7-2. Typical Device Behavior During Short Circuit Protection](image)

7.3.6.4 Thermal Shutdown
To avoid thermal damage of the device, the temperature of the die is monitored. The device stops operation once the sensed temperature rises over the thermal threshold. After the temperature drops below the thermal shutdown hysteresis, the converter returns to normal operation.

7.4 Device Functional Modes
The device has two functional modes: off and on. The device enters the on mode when the voltage on the VIN pin is higher than the UVLO threshold and a high logic level is applied to the EN pin. The device enters the off mode when the voltage on the VIN pin is lower than the UVLO threshold or a low logic level is applied to the EN pin.
Figure 7-3. Device Functional Modes

on

V_i > V_{IT+} && EN pin = high

V_i < V_{IT-} || EN pin = low

off
8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS631000 is a high-efficiency, low-quiescent current, buck-boost converter. The device is suitable for applications needing a regulated output voltage from an input supply that can be higher or lower than the output voltage.

8.2 Typical Application

![Typical Application Diagram](image)

**Figure 8-1. 3.3-V<sub>OUT</sub> Typical Application**

8.2.1 Design Requirements

The design parameters are listed in Table 8-1.

<table>
<thead>
<tr>
<th>PARAMETERS</th>
<th>VALUES</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage</td>
<td>2.7 V to 4.3 V</td>
</tr>
<tr>
<td>Output voltage</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Output current</td>
<td>1.5 A</td>
</tr>
</tbody>
</table>

8.2.2 Detailed Design Procedure

The first step is the selection of the output filter components. To simplify this process, Section 6.3 outlines minimum and maximum values for inductance and capacitance. Tolerance and derating should be taken into account when selecting nominal inductance and capacitance.

8.2.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS631000 device with the WEBENCH® Power Designer.

1. Start by entering your V<sub>IN</sub>, V<sub>OUT</sub> and I<sub>OUT</sub> requirements.
2. Optimize your design for key parameters like efficiency, footprint or cost using the optimizer dial and compare this design with other possible solutions from Texas Instruments.

3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real-time pricing and component availability.

4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.

5. Get more information about WEBENCH tools at [www.ti.com/webench](http://www.ti.com/webench).

### 8.2.2.2 Inductor Selection

The inductor selection is affected by several parameters such as the following:

- Inductor ripple current
- Output voltage ripple
- Transition point into power save mode
- Efficiency

See Table 8-2 for typical inductors.

For high efficiencies, the inductor should have a low DC resistance to minimize conduction losses. Especially at high-switching frequencies, the core material has a high impact on efficiency. When using small chip inductors, the efficiency is reduced mainly due to higher inductor core losses. This needs to be considered when selecting the appropriate inductor. The inductor value determines the inductor ripple current. The larger the inductor value, the smaller the inductor ripple current and the lower the conduction losses of the converter. Conversely, larger inductor values cause a slower load transient response. To avoid saturation of the inductor, the peak current for the inductor in steady state operation is calculated using Equation 3. Only the equation that defines the switch current in boost mode is shown because this provides the highest value of current and represents the critical current value for selecting the right inductor.

\[
D = \frac{V_{OUT} - V_{IN}}{V_{OUT}}
\]  
\[
I_{PEAK} = \frac{I_{out}}{\eta \times (1 - D)} + \frac{V_{IN} \times D}{2 \times f \times L}
\]

where:
- \( D \) = duty cycle in boost mode
- \( f \) = converter switching frequency (typical 2.2 MHz)
- \( L \) = inductor value
- \( \eta \) = estimated converter efficiency (use the number from the efficiency curves or 0.9 as an assumption)

**Note**

The calculation must be done for the minimum input voltage in boost mode. Calculating the maximum inductor current using the actual operating conditions gives the minimum saturation current of the inductor needed. It is recommended to choose an inductor with a saturation current 20% higher than the value calculated using Equation 3. Possible inductors are listed in Table 8-2.
Table 8-2. List of Recommended Inductors

<table>
<thead>
<tr>
<th>INDUCTOR VALUE [µH]</th>
<th>SATURATION CURRENT [A]</th>
<th>DCR [mΩ]</th>
<th>PART NUMBER</th>
<th>MANUFACTURER(1)</th>
<th>SIZE (L × W × H mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>4.3</td>
<td>42</td>
<td>DFE252012P-1R0M=P2</td>
<td>MuRata</td>
<td>2.5 × 2.0 × 1.2</td>
</tr>
<tr>
<td>1</td>
<td>4.2</td>
<td>43</td>
<td>HTEK20161T-1R0MSR</td>
<td>Cyntec</td>
<td>2.0 × 1.6 × 1.0</td>
</tr>
<tr>
<td>1</td>
<td>2.2</td>
<td>75</td>
<td>MAKK2016T1R0M(2)</td>
<td>Taiyo Yuden</td>
<td>2.0 × 1.6 × 1.0</td>
</tr>
<tr>
<td>1</td>
<td>2.0</td>
<td>144</td>
<td>DFE18SAN1R0ME0(2)</td>
<td>Murata</td>
<td>1.6 × 0.8 × 0.8</td>
</tr>
</tbody>
</table>

(1) See the Third-Party Products Disclaimer.
(2) This inductor does not support full output current range.

8.2.2.3 Output Capacitor Selection

For the output capacitor, use small ceramic capacitors placed as close as possible to the VOUT and PGND pins of the IC. The recommended nominal output capacitor value is a single 47 µF. If, for any reason, the application requires the use of large capacitors that cannot be placed close to the IC, use a smaller ceramic capacitor in parallel to the large capacitor. The small capacitor should be placed as close as possible to the VOUT and PGND pins of the IC.

It is important that the effective capacitance is given according to the recommended value in Section 6.3. In general, consider DC bias effects resulting in less effective capacitance. The choice of the output capacitance is mainly a tradeoff between size and transient behavior as higher capacitance reduces transient response over/undershoot and increases transient response time. Possible output capacitors are listed in Table 8-3.

There is no upper limit for the output capacitance value.

Table 8-3. List of Recommended Capacitors

<table>
<thead>
<tr>
<th>CAPACITOR VALUE [µF]</th>
<th>VOLTAGE RATING [V]</th>
<th>ESR [mΩ]</th>
<th>PART NUMBER</th>
<th>MANUFACTURER(1)</th>
<th>SIZE (METRIC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>47</td>
<td>6.3</td>
<td>10</td>
<td>GRM219R60J476ME44</td>
<td>Murata</td>
<td>0805 (2012)</td>
</tr>
<tr>
<td>47</td>
<td>10</td>
<td>40</td>
<td>CL10A476MQ8QRN</td>
<td>Semco</td>
<td>0603 (1608)</td>
</tr>
</tbody>
</table>

(1) See the Third-Party Products Disclaimer.

8.2.2.4 Input Capacitor Selection

A 22-µF input capacitor is recommended to improve line transient behavior of the regulator and EMI behavior of the total power supply circuit. An X5R or X7R ceramic capacitor placed as close as possible to the VIN and PGND pins of the IC is recommended. This capacitance can be increased without limit. If the input supply is located more than a few inches from the TPS631000, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic or tantalum capacitor with a value of 47 µF is a typical choice.

Table 8-4. List of Recommended Capacitors

<table>
<thead>
<tr>
<th>CAPACITOR VALUE [µF]</th>
<th>VOLTAGE RATING [V]</th>
<th>ESR [mΩ]</th>
<th>PART NUMBER</th>
<th>MANUFACTURER(1)</th>
<th>SIZE (METRIC)</th>
</tr>
</thead>
<tbody>
<tr>
<td>22</td>
<td>6.3</td>
<td>43</td>
<td>GRM187R61A226ME15</td>
<td>Murata</td>
<td>0603 (1608)</td>
</tr>
<tr>
<td>10</td>
<td>10</td>
<td>40</td>
<td>GRM188R61A106ME69</td>
<td>Murata</td>
<td>0603 (1608)</td>
</tr>
</tbody>
</table>

(1) See the Third-Party Products Disclaimer.

8.2.2.5 Setting the Output Voltage

The output voltage is set by an external resistor divider. The resistor divider must be connected between VOUT, FB, and GND. The feedback voltage is 500 mV nominal.

The low-side resistor R2 (between FB and GND) should not exceed 100 kΩ. The high-side resistor (between FB and VOUT) R1 is calculated with Equation 4.

---

(1) See the Third-Party Products Disclaimer.
\[ R1 = R2 \times \left( \frac{V_{\text{OUT}}}{V_{\text{FB}}} - 1 \right) \]  

(4)

where

- \( V_{\text{FB}} = 500 \, \text{mV} \)

### Table 8-5. Resistor Selection For Typical Output Voltages

<table>
<thead>
<tr>
<th>( V_{\text{OUT}} )</th>
<th>R1</th>
<th>R2</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.5 V</td>
<td>365</td>
<td>91</td>
</tr>
<tr>
<td>3.3 V</td>
<td>511</td>
<td>91</td>
</tr>
<tr>
<td>3.6 V</td>
<td>562</td>
<td>91</td>
</tr>
<tr>
<td>5 V</td>
<td>806</td>
<td>91</td>
</tr>
</tbody>
</table>
8.2.3 Application Curves

Figure 8-2. Typical Output Current Capability vs Input Voltage

Figure 8-3. Efficiency vs Output Current (FPWM)

Figure 8-4. Load Regulation (FPWM)

Figure 8-5. Efficiency vs Input Voltage (PFM)

Figure 8-6. Load Regulation (PFM)

Figure 8-7. Switching Waveforms, Boost Operation with 1-A Load
8.2.3 Application Curves (continued)

![Switching Waveforms with 1-A Load](image1)

<table>
<thead>
<tr>
<th>Figure 8-8</th>
<th>Figure 8-9</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} = 3.3 , \text{V}, , V_{OUT} = 3.3 , \text{V} )</td>
<td>( V_{IN} = 3.6 , \text{V}, , V_{OUT} = 3.3 , \text{V} )</td>
</tr>
<tr>
<td>( I_{OUT} = 1 , \text{A}, , \text{MODE} = \text{Low} )</td>
<td>( I_{OUT} = 1 , \text{A}, , \text{MODE} = \text{Low} )</td>
</tr>
</tbody>
</table>

![Switching Waveforms, Buck Operation with 1-A Load](image2)

<table>
<thead>
<tr>
<th>Figure 8-10</th>
<th>Figure 8-11</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} = 4.3 , \text{V}, , V_{OUT} = 3.3 , \text{V} )</td>
<td>( V_{IN} = 3.6 , \text{V}, , V_{OUT} = 3.3 , \text{V} )</td>
</tr>
<tr>
<td>( I_{OUT} = 1 , \text{A}, , \text{MODE} = \text{Low} )</td>
<td>( I_{OUT} = 1 , \text{mA}, , \text{MODE} = \text{Low} )</td>
</tr>
</tbody>
</table>

![Start-Up by EN](image3)

<table>
<thead>
<tr>
<th>Figure 8-12</th>
<th>Figure 8-13</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} = 3.6 , \text{V}, , V_{OUT} = 3.3 , \text{V} )</td>
<td>( V_{IN} = 3.6 , \text{V}, , V_{OUT} = 3.3 , \text{V} )</td>
</tr>
<tr>
<td>( R_{load} = 4 , \Omega, , \text{MODE} = \text{Low} )</td>
<td>( R_{load} = 4 , \Omega, , \text{MODE} = \text{Low} )</td>
</tr>
</tbody>
</table>
8.2.3 Application Curves (continued)

*Figure 8-14. Load Transient at 2.7-V Input Voltage*

*Figure 8-15. Load Sweep at 2.7-V Input Voltage*

*Figure 8-16. Load Transient at 3.6-V Input Voltage*

*Figure 8-17. Load Sweep at 3.6-V Input Voltage*

*Figure 8-18. Load Transient at 4.3-V Input Voltage*

*Figure 8-19. Load Sweep at 4.3-V Input Voltage*
8.2.3 Application Curves (continued)

![Inductor Current](image)

**Figure 8-20.** Line Transient at 1-A Load Current

**Figure 8-21.** Line Sweep at 1-A Load Current

**Figure 8-22.** Output Short Protection (Entry)

**Figure 8-23.** Output Short Protection (Recover)

**Table 8-6.** Components for Application Characteristic Curves for $V_{OUT} = 3.3$ V

<table>
<thead>
<tr>
<th>REFERENCE</th>
<th>DESCRIPTION</th>
<th>PART NUMBER</th>
<th>MANUFACTURER</th>
</tr>
</thead>
<tbody>
<tr>
<td>U1</td>
<td>High Power Density 1.5 A Buck-Boost Converter</td>
<td>TPS631000</td>
<td>Texas Instruments</td>
</tr>
<tr>
<td>L1</td>
<td>1.0 µH, 2.5 mm x 2.0 mm, 4.3 A, 42 mΩ</td>
<td>DFE252012P-1R0M=P2</td>
<td>Murata</td>
</tr>
<tr>
<td>C1</td>
<td>22 µF, 0603, Ceramic Capacitor, ±20%, 6.3 V</td>
<td>GRM187R61A226ME15</td>
<td>Murata</td>
</tr>
<tr>
<td>C2</td>
<td>47 µF, 0805, Ceramic Capacitor, ±20%, 6.3 V</td>
<td>GRM219R60J476ME44</td>
<td>Murata</td>
</tr>
<tr>
<td>R1</td>
<td>511 kΩ, 0603 Resistor, 1%, 100 mW</td>
<td>Standard</td>
<td>Standard</td>
</tr>
<tr>
<td>R2</td>
<td>91 kΩ, 0603 Resistor, 1%, 100 mW</td>
<td>Standard</td>
<td>Standard</td>
</tr>
</tbody>
</table>

(1) See the Third-Party Products Disclaimer.
(2) For other output voltages, refer to Table 8-5 for resistor values.

9 Power Supply Recommendations

The TPS631000 device has no special requirements for its input power supply. The input power supply output current needs to be rated according to the supply voltage, output voltage, and output current of the TPS631000.
10 Layout
10.1 Layout Guidelines
The PCB layout is an important step to maintain the high performance of the TPS631000 device.
- Place input and output capacitors as close as possible to the IC. Traces need to be kept short. Route wide and direct traces to the input and output capacitors results in low trace resistance and low parasitic inductance.
- The sense trace connected to FB is signal trace. Keep these traces away from LX1 and LX2 nodes.

10.2 Layout Example

![Layout Example Diagram]

Figure 10-1. Layout Example
11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI’S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT
CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES
OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER
ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Development Support

11.1.2.1 Custom Design with WEBENCH Tools

Click here to create a custom design using the TPS631000 device with the WEBENCH® Power Designer.

1. Start by entering your $V_{IN}$, $V_{OUT}$ and $I_{OUT}$ requirements.
2. Optimize your design for key parameters like efficiency, footprint or cost using the optimizer dial and
   compare this design with other possible solutions from Texas Instruments.
3. WEBENCH Power Designer provides you with a customized schematic along with a list of materials with real
time pricing and component availability.
4. In most cases, you will also be able to:
   - Run electrical simulations to see important waveforms and circuit performance,
   - Run thermal simulations to understand the thermal performance of your board,
   - Export your customized schematic and layout into popular CAD formats,
   - Print PDF reports for the design, and share your design with colleagues.
5. Get more information about WEBENCH tools at www.ti.com/webench.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on
Subscribe to updates to register and receive a weekly digest of any product information that has changed. For
change details, review the revision history included in any revised document.

11.3 Support Resources

TI E2E™ support forums are an engineer’s go-to source for fast, verified answers and design help — straight
from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do
not necessarily reflect TI's views; see TI's Terms of Use.

11.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled
with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may
be more susceptible to damage because very small parametric changes could cause the device not to meet its published
specifications.

11.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.
12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS631000DRLR</td>
<td>ACTIVE</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>8</td>
<td>4000</td>
<td>RoHS &amp; Green</td>
<td>Call TI</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>2N4W</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPS631000DRLR</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>8</td>
<td>4000</td>
<td>180.0</td>
<td>8.4</td>
<td>2.75</td>
<td>1.9</td>
<td>0.8</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
</tr>
</tbody>
</table>
TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
<tbody>
<tr>
<td>TPS631000DRLR</td>
<td>SOT-5X3</td>
<td>DRL</td>
<td>8</td>
<td>4000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
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