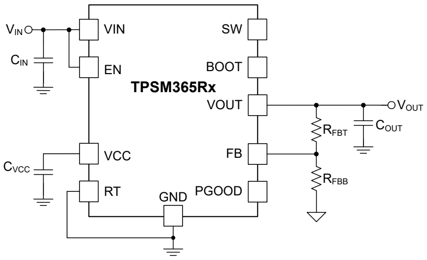
TPSM365R6, TPSM365R3 3-V to 65-V Input, 600-mA/300-mA, 4-μA No-Load I_Q Synchronous Buck Converter Power Module in a HotRod™ QFN Package

1 Features

- Functional Safety-Capable
  - Documentation available to aid functional safety system design
- Versatile synchronous buck DC/DC module:
  - Integrated MOSFETs, inductor, and controller
  - Wide input voltage range: 3 V to 65 V
  - Input transient up to 70 V
  - Junction temperature range –40°C to +125°C
  - 4.5-mm × 3.5-mm × 2-mm overmolded package
  - Frequency adjustable from 200 kHz to 2.2 MHz using the RT pin or an external SYNC signal
- Ultra-high efficiency across the full load range:
  - Greater than 85% efficiency at 12 V_{IN}, 3.3-V_{OUT}
  - Greater than 85% efficiency at 24 V_{IN}, 5-V_{OUT}
  - Ultra-low operating quiescent current at no load: 4 μA at V_{IN} = 24 V to 3.3-V V_{OUT}
- Optimized for ultra-low EMI requirements:
  - Pseudo-random spread spectrum reduces peak emissions
  - Pin selectable FPWM mode for constant frequency at light loads with MODE/SYNC pin
  - FSW synchronization with MODE/SYNC pin
  - CISPR11 class B capable
- Output voltage and current options:
  - Fixed output variants of 3.3-V or 5-V V_{OUT}
  - Adjustable output voltage from 1 V to 13 V
  - Pin compatible with TPSM33625
  - 600-mA output current (TPSM365R6)
  - 300-mA output current (TPSM365R3)
- Inherent protection features for robust design
  - Precision enable input and open-drain PGOOD indicator for sequencing, control, and V_{IN} UVLO
  - Overcurrent and thermal shutdown protections
- Create a custom design using the TPSM365Rx with the WEBENCH® Power Designer



Typical Schematic

2 Applications

- Factory automation and control
- Building automation
- Test equipment
- Appliances

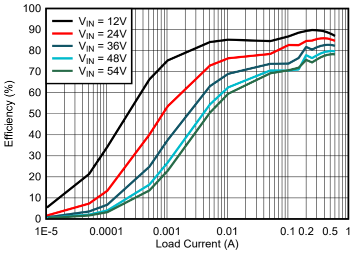
3 Description

The TPSM365R6 or TPSM365R3 is a 600-mA or 300-mA, 65-V input synchronous step-down DC/DC power module that combines power MOSFETs, integrated inductor and boot capacitor in a compact and easy-to-use 3.5-mm × 4.5-mm × 2-mm, 11-pin QFN package. The small HotRod™ QFN package technology enhances the thermal performance and low EMI. The device features the ultra-low operating I_Q of 4 μA at no load (24 V to 3.3-V V_{OUT}). The TPSM365Rx is available in two fixed output voltage option supporting 3.3 V and 5 V, and an adjustable output voltage option supporting 1-V to 13-V range. The module only requires four external components for a 3.3-V and 5-V fixed output solution. The TPSM365Rx is optimized for excellent EMI performance and space constraint applications.

Package Information

PART NUMBER	PACKAGE (1)	BODY SIZE (NOM)
TPSM365R6	RDN (QFN-HR,11)	3.50 mm × 4.50 mm × 2.00 mm
TPSM365R3		

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Efficiency vs Output Current V_{OUT} = 5 V, F_{SW} = 1 MHz

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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (November 2022) to Revision B (February 2023)	Page
• Added TPSM365R3 to the data sheet	1

Changes from Revision * (September 2022) to Revision A (November 2022)	Page
• Changed status from Advance Information to Production Data	1

5 Description (continued)

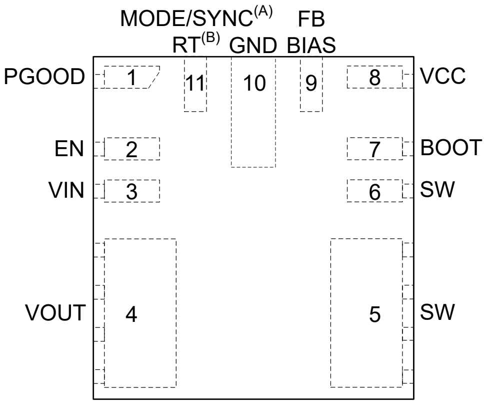
The TPSM365Rx uses a peak current mode control scheme with internal compensation to maintain stable operation with minimal output capacitance. The precision EN feature allows precise control of the device during start-up and shutdown. An open-drain PGOOD output provides a true indication of the output voltage status. The TPSM365Rx includes prebias start up, overcurrent, and temperature protections, making the TPSM365Rx an excellent device for powering a wide range of industrial applications. In the fixed option variants, the MODE/SYNC pin enables seamless transition from FPWM to PFM with a no-load standby quiescent current of less than 4 µA, ensuring high efficiency and superior transient response for the entire load-current range.

6 Device Comparison Table

DEVICE	ORDERABLE PART NUMBER (1)	F_{SW}	OUTPUT VOLTAGE	EXTERNAL SYNC	SPREAD SPECTRUM
TPSM365R6	TPSM365R6FRDNR	Adjustable with RT resistor	Adjustable (1 V to 13 V)	No (FPWM only)	Yes
TPSM365R6V3	TPSM365R6V3RDNR	Fixed 1 MHz	3.3-V Fixed	Yes (PFM/PWM Selectable)	Yes
TPSM365R6V5	TPSM365R6V5RDNR	Fixed 1 MHz	5-V Fixed	Yes (PFM/PWM Selectable)	Yes
TPSM365R6	TPSM365R6RDNR	Adjustable with RT resistor	Adjustable (1 V to 13 V)	No (Default PFM at light load)	Yes
TPSM365R3	TPSM365R3FRDNR	Adjustable with RT resistor	Adjustable (1 V to 13 V)	No (FPWM only)	Yes
TPSM365R3	TPSM365R3RDNR	Adjustable with RT resistor	Adjustable (1 V to 13 V)	No (Default PFM at light load)	Yes

(1) For more information on device orderable part numbers, see *Device Nomenclature*.

7 Pin Configuration and Functions



A. Pin 11 factory-set for fixed switching frequency MODE/SYNC variants only.

B. See *Device Comparison Table* for more details. Pin 11 trimmed and factory-set for externally adjustable switching frequency RT variants only.

Figure 7-1. RDN Package, 11-Pin QFN-HR, Top View (All Variants)

Table 7-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	PGOOD	A	Power-good monitor. Open-drain output that asserts low if the feedback voltage is not within the specified window thresholds. A 10-kΩ to 100-kΩ pullup resistor is required to a suitable pullup voltage. If not used, this pin can be left open or connected to GND. High = power OK, Low = power bad. PGOOD pin goes low when EN = Low.
2	EN	A	Precision enable input pin. High = ON, Low = OFF. Can be connected to VIN. Precision enable allows the pin to be used as an adjustable UVLO. Can be connected directly to VIN. The module can be turned off by using an open-drain or collector device to connect this pin to GND. An external voltage divider can be placed between this pin, GND, and VIN to create an external UVLO.*Do not float this pin.*
3	VIN	P	Input supply voltage. Connect the input supply to these pins. Connect a high-quality bypass capacitor or capacitors directly to this pin and GND in close proximity to the module. Refer to *Section 10.4.2* for input capacitor placement example.
4	VOUT	P	Output voltage. The pin is connected to the internal output inductor. Connect the pin to the output load and connect external output capacitors between the pin and GND. Fixed output options are available. For fixed output variants, connect the FB pin to VOUT. Check *Section 6* for more details.
5, 6	SW	P	Power module switch node. Do not place any external component on this pin or connect to any signal. The amount of copper placed on these pins must be kept to a minimum to prevent issues with noise and EMI.
7	BOOT	P	Bootstrap pin for internal high-side driver circuitry. A 100-nF bootstrap capacitor is internally connected from this pin to SW within the module to provide the bootstrap voltage.
8	VCC	P	Internal LDO output. Used as supply to internal control circuits. Do not connect to external loads. Can be used as logic supply for power-good flag. Connect a high-quality 1-µF capacitor from this pin to GND.
9	FB or BIAS	A	Feedback input. For the adjustable output version, connect the mid-point of the feedback resistor divider to this pin. Connect the upper resistor (R_{FBT}) of the feedback divider to VOUT at the desired point of regulation. Connect the lower resistor (R_{FBB}) of the feedback divider to GND. When connecting with feedback resistor divider, keep this FB trace short and as small as possible to avoid noise coupling. See *Section 10.4.2* for a feedback resistor placement. For a fixed output version, connect BIAS directly to VOUT pin. Do not leave open or connect to ground.
10	GND	G	Power ground terminal. Connect to system ground. Connect to C_{IN} with short, wide traces.
11	RT or MODE/SYNC	A	When the part is trimmed as the RT pin variant, the switching frequency in the part can be adjusted from 200 kHz to 2.2 MHz based on the resistor value connected between RT and GND. When the pin is trimmed as the MODE/SYNC variant, the part can operate in user-selectable PFM/FPWM operation. In FPWM, the part can be synchronized to an external clock. Clock triggers on rising edge of applied external clock. *Do not float this pin..*
A = Analog, P = Power, G = Ground			

8 Specifications

8.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range (unless otherwise noted) (1)

PARAMETER		MIN	MAX	UNIT
Voltage	VIN to GND	–0.3	70	V
Voltage	EN to GND	–0.3	70	V
Voltage	SW to GND	–0.3	70.3	V
Voltage	MODE/SYNC to GND (MODE/SYNC variant)	–0.3	5.5	V
Voltage	RT to GND (RT variant)	–0.3	5.5	V
Voltage	BIAS to GND (Fixed V_{OUT} variant)	–0.3	13	V
Voltage	FB to GND (Adjustable V_{OUT} variant)	–0.3	13	V
Voltage	PGOOD to GND	0	20	V
Voltage	BOOT to SW	–0.3	5.5	V
Voltage	VCC to GND	–0.3	5.5	V
T_J (2)	Junction temperature	–40	125	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The ambient temperature is the air temperature of the surrounding environment. The junction temperature is the temperature of the internal power IC when the device is powered. Operating below the maximum ambient temperature, as shown in the safe operating area (SOA) curves in the Typical Applications sections, ensures that the maximum junction temperature of any component inside the module is never exceeded.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to 125°C (unless otherwise noted) (1) (2)

		MIN	TYP	MAX	UNIT
Input voltage	Input voltage, V_{IN} (Input voltage range after startup)	3.6		65	V
Output voltage	Output Adjustment Range for adjustable output versions, V_{OUT}	1		13	V
Output current	(TPSM365R3X) Load current range (3)	0		0.3	A
Output current	(TPSM365R6X) Load current range (3)	0		0.6	A
Frequency setting	Selectable Frequency Range with RT (RT variant)	0.2		2.2	MHz
Frequency setting	External Sync CLK (with MODE/SYNC variant)	0.2		2.2	MHz
Temperature	T_J junction temperature	–40		125	°C

(1) Recommended operating conditions indicate conditions for which the device is intended to be functional, but do not ensure specific performance limits. For ensured specifications, see Electrical Characteristics table.
(2) High junction temperatures degrade operating lifetimes. Operating lifetime is de-rated for junction temperatures greater than 125℃
(3) Maximum continuous DC current may be derated when operating with high switching frequency or high ambient temperature. See Application section for details.

8.4 Thermal Information

THERMAL METRIC (1)		TPSM365R6 / TPSM365R3	UNIT
		RDN	
		11 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	56.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	53.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.3	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	10.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.2	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report. The value of $R_{\Theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. This value was calculated in accordance with JESD 51-7, and simulated on a 4-layer JEDEC board. It does not represent the performance obtained in an actual application.

8.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)						
V_{IN_R}	Minimum operating Input Voltage (Rising)	Rising Threshold		3.4	3.6	V
V_{IN_F}	Minimum operating Input Voltage (Falling)	Once Operating; Falling Threshold	2.45	3.0		V
$I_{Q\_13p5\_Fixed}$	Non-switching input current; measured at V_{IN} pin (2)	V_{IN} = V_{EN} = 13.5 V; V_{BIAS} = 5.25 V, $V_{MODE/SYNC}$ = 0 V; Fixed Output Option	0.25	0.672	1.05	µA
$I_{Q\_13p5\_Adj}$	Non-switching input current; measured at V_{IN} pin (2)	V_{IN} = V_{EN} = 13.5 V; V_{FB} = 1.5 V, V_{RT} = 0 V; Adjustable Output Option	11	17	24	µA
$I_{Q\_24p0\_Fixed}$	Non-switching input current; measured at V_{IN} pin (2)	V_{IN} = V_{EN} = 24 V; V_{BIAS} = 5.25 V, $V_{MODE/SYNC}$ = 0 V; Fixed Output Option	0.8	1.2	1.7	µA
$I_{Q\_24p0\_Adj}$	Non-switching input current; measured at V_{IN} pin (2)	V_{IN} = V_{EN} = 24 V; V_{FB} = 1.5 V, V_{RT} = 0 V; Adjustable Output Option	11	18	24	µA
I_{B_13p5}	Current into BIAS pin (not switching) (2)	V_{IN} = V_{EN} = 13.5 V, V_{BIAS} = 5.25 V, $V_{MODE/SYNC}$ = 0 V; Fixed Output Option	14	17	22	µA
I_{B_24p0}	Current into BIAS pin (not switching) (2)	V_{IN} = V_{EN} = 24 V, V_{BIAS} = 5.25 V, $V_{MODE/SYNC}$ = 0 V; Fixed Output Option	14	18	22	µA
I_{SD_13p5}	Shutdown quiescent current; measured at V_{IN} pin (2)	V_{EN} = 0 V; V_{IN} = 13.5 V		0.5	1.3	µA
I_{SD_24p0}	Shutdown quiescent current; measured at V_{IN} pin (2)	V_{EN} = 0 V; V_{IN} = 24 V		1	1.8	µA
ENABLE (EN PIN)						
$V_{EN-WAKE}$	Enable wake-up threshold		0.4			V
$V_{EN-VOUT}$	Precision enable high level for V_{OUT}		1.16	1.263	1.36	V
$V_{EN-HYST}$	Enable threshold hysteresis below $V_{EN-VOUT}$		0.3	0.35	0.4	V
I_{LKG-EN}	Enable input leakage current	V_{EN} = 3.3 V		0.3	10	nA
INTERNAL LDO						
V_{CC}	Internal VCC voltage	Adjustable or Fixed Output Option; Auto mode	3.125	3.15	3.22	V
I_{CC}	Bias regulator current limit			65	240	mA
$V_{CC-UVLO}$	Internal VCC undervoltage lockout	VCC rising under voltage threshold	3	3.3	3.65	V
$V_{CC-UVLO-HYST}$	Internal VCC under voltage lock-out hysteresis	Hysteresis below $V_{CC-UVLO}$	0.4	0.8	1.2	V
CURRENT LIMITS						
I_{SC-0p3}	Short circuit high side current limit (2)	0.3 A version (TPSM365R3)	0.42	0.5	0.575	A
$I_{LS-LIMIT-0p3}$	Low side current limit (2)	0.3 A version (TPSM365R3)	0.27	0.35	0.42	A
$I_{PEAK-MIN-0p3}$	Minimum Peak Inductor Current (2)	Auto operation, 0.3 A version; Duty Cycle = 0%; (TPSM365R3)	0.065	0.09	0.113	A
I_{SC-0p6}	Short circuit high side current limit (2)	0.6 A version (TPSM365R6)	0.87	1	1.11	A
$I_{LS-LIMIT-0p6}$	Low side current limit (2)	0.6 A version (TPSM365R6)	0.6	0.7	0.8	A
$I_{PEAK-MIN-0p6}$	Minimum Peak Inductor Current (2)	Auto operation, 0.6 A version; Duty Cycle = 0%; (TPSM365R6)	0.127	0.19	0.227	A
I_{ZC}	Zero Cross Current (2)	Auto mode operation; (TPSM365R3) and (TPSM365R6)		0.01	0.025	A
I_{L-NEG}	Negative current limit (2)	FPWM operation; (TPSM365R3) and (TPSM365R6)	–0.8	–0.7	–0.6	A

8.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER GOOD						
$V_{PG\text{-}OV}$	PGOOD upper threshold - Rising	% of BIAS or FB (adjustable or fixed output)	106	107	110	%
$V_{PG\text{-}UV}$	PGOOD lower threshold - Falling	% of BIAS or FB (adjustable or fixed output)	93	94	96.5	%
$V_{PG\text{-}HYS}$	PGOOD hysteresis	% of BIAS or FB (adjustable or fixed output)	1.3	1.8	2.3	%
$V_{PG\text{-}VALID}$	Minimum input voltage for proper PGOOD function		0.72	1	2	V
$R_{PG\text{-}EN5p0}$	$R_{DS(ON)}$ PGOOD output	V_{EN} = 5 V, 1 mA pull-up current	20	40	70	Ω
$R_{PG\text{-}EN0}$	$R_{DS(ON)}$ PGOOD output	V_{EN} = 0 V, 1 mA pull-up current	10	18	31	Ω
t_{RESET_FILTER}	PGOOD deglitch delay at falling edge		15	25	40	µs
t_{PGOOD_ACT}	Delay time to PGOOD high signal		1.7	1.956	2.16	ms
SOFT START						
t_{SS}	Time from first SW pulse to V_{OUT}/FB at 90% of set point		1.95	2.58	3.2	ms
OSCILLATOR (MODE/SYNC)						
$V_{SYNC\text{-}H}$	SYNC input and mode high level threshold		1.8			V
$V_{SYNC\text{-}L}$	SYNC input and mode low level threshold				0.8	V
$V_{SYNC\text{-}HYS}$	SYNC input hysteresis		230	300	380	mV
t_{PULSE_H}	High duration needed to be recognized as a pulse		100			ns
t_{PULSE_L}	Low duration needed to be recognized as a pulse		100			ns
t_{SYNC}	High/Low signal duration to be recognized as a valid synchronization signal		6	9	12	µs
t_{MODE}	Time at one level needed to indicate FPWM or Auto Mode		18			µs
OSCILLATOR (RT)						
f_{OSC_2p2MHz}	Internal oscillator frequency	RT = GND	2.1	2.2	2.3	MHz
f_{OSC_1p0MHz}	Internal oscillator frequency	RT = VCC	0.93	1	1.05	MHz
f_{ADJ_400kHz}		RT = 39.2 kΩ (with RT variant only)	0.34	0.4	0.46	MHz
SWITCH NODE (SW)						
$t_{ON\text{-}MIN}$	Minimum switch on-time	V_{IN} = 24 V, I_{OUT} = 0.6 A	40	57	86	ns
$t_{OFF\text{-}MIN}$	Minimum switch off-time		40	58	77	ns
$t_{ON\text{-}MAX}$	Maximum switch on-time	High-side timeout in dropout	7.6	9	9.8	µs
MOSFETS						
$R_{DSON\text{-}HS}$	High-side MOSFET on-resistance	Load = 0.3 A		560	920	mΩ
$R_{DSON\text{-}LS}$	Low-side MOSFET on-resistance	Load = 0.3 A		280	480	mΩ
$V_{BOOT\text{-}UVLO}$	BOOT - SW UVLO threshold (3)		2.14	2.3	2.42	V

8.5 Electrical Characteristics (continued)

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 24 V. (1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOLTAGE REFERENCE						
$V_{OUT\_Fixed3p3}$	Initial V_{OUT} voltage accuracy for 3.3-V	3.3-V $V_{OUT;}$ V_{IN} = 3.6 V to 65 V; FPWM Mode	3.25	3.3	3.34	V
$V_{OUT\_Fixed5p0}$	Initial V_{OUT} voltage accuracy for 5-V	5-V $V_{OUT;}$ V_{IN} = 5.5 V to 65 V; FPWM Mode	4.93	5	5.07	V
V_{FB}	Internal reference voltage accuracy	V_{IN} = 3.6 V to 65 V; FPWM Mode	0.985	1	1.01	V
I_{FB}	FB input current	Adjsutable output, FB = 1 V		85	115	nA

(1) MIN and MAX limits are 100% production tested at 25ºC. Limits over the operating temperature range verified through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) This is the current used by the device open loop. It does not represent the total input current of the system when in regulation.
(3) When the voltage across the C_{BOOT} capacitor falls below this voltage, the low side MOSFET is turn to recharge the boot capacitor

8.6 System Characteristics

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 125°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN)						
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 13.5 V, V_{BIAS} = 3.3-V V_{OUT}, I_{OUT} = 0 A, PFM mode (fixed output voltage)		6.5		µA
I_{SUPPLY}	Input supply current when in regulation	V_{IN} = 24 V, V_{BIAS} = 3.3-V V_{OUT}, I_{OUT} = 0 A, FPWM mode (fixed output voltage)		4		µA
D_{MAX}	Maximum switch duty cycle (1)			98		%
VOLTAGE REFERENCE (FB or BIAS)						
$V_{OUT\_5p0V\_ACC}$	V_{OUT} = 5 V, V_{IN} = 5.5 V to 65 V, I_{OUT} = 0 A to full load (2)	FPWM mode	–1.5		1.5	%
$V_{OUT\_5p0V\_ACC}$	V_{OUT} = 5 V, V_{IN} = 5.5 V to 65 V, I_{OUT} = 0 A to full load (2)	Auto mode	–1.5		2.5	%
$V_{OUT\_3p3V\_ACC}$	V_{OUT} = 3.3 V, V_{IN} = 3.6 V to 65 V, I_{OUT} = 0 A to full load (2)	FPWM mode	–1.5		1.5	%
$V_{OUT\_3p3V\_ACC}$	V_{OUT} = 3.3 V, V_{IN} = 3.6 V to 65 V, I_{OUT} = 0 A to full load (2)	Auto mode	–1.5		2.5	%
SPREAD SPECTRUM						
f_{SSS}	Frequency span of spread spectrum operation - largest deviation from center frequency (3)	Spread spectrum active		±2		%
f_{PSS}	Spread spectrum pseudo random pattern frequency (3)			0.98	1.5	Hz
EFFICIENCY						
η	Efficiency	V_{IN} = 12 V, V_{OUT} = 3.3 V, I_{OUT} = 0.6 A, F_{SW} = 1 MHz		82.7		%
η	Efficiency	V_{IN} = 24 V, V_{OUT} = 3.3 V, I_{OUT} = 0.6 A, F_{SW} = 1 MHz		80.2		%
η	Efficiency	V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 0.6 A, F_{SW} = 1 MHz		84.7		%
η	Efficiency	V_{IN} = 36 V, V_{OUT} = 5 V, I_{OUT} = 0.6 A, F_{SW} = 1 MHz		82.3		%
η	Efficiency	V_{IN} = 24 V, V_{OUT} = 12 V, I_{OUT} = 0.4 A, F_{SW} = 2.2 MHz		88.4		%
η	Efficiency	V_{IN} = 48 V, V_{OUT} = 12 V, I_{OUT} = 0.4 A, F_{SW} = 2.2 MHz		78.5		%

8.6 System Characteristics (continued)

The following specifications apply only to the typical applications circuit, with nominal component values. Specifications in the typical (TYP) column apply to T_J = 25°C only. Specifications in the minimum (MIN) and maximum (MAX) columns apply to the case of typical components over the temperature range of T_J = –40°C to 125°C. These specifications are not ensured by production testing.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
THERMAL SHUTDOWN						
T_{SD-R}	Thermal shutdown rising	Shutdown threshold	158	168	180	°C
T_{SD-F}	Thermal shutdown falling	Recovery threshold	150	158	165	°C
T_{SD-HYS}	Thermal shutdown hysteresis		8	10	15	°C

(1) In dropout the switching frequency drops to increase the effective duty cycle. The lowest frequency is clamped at approximately: f_{MIN} = 1 / (t_{ON-MAX} + $T_{OFF-MIN}$). D_{MAX} = t_{ON-MAX} /(t_{ON-MAX} + $t_{OFF-MIN}$).
(2) Deviation is with respect to V_{IN} = 13.5 V
(3) Specified by design. Not production tested.

8.7 Typical Characteristics

Unless otherwise specified, the following conditions apply: T_A = 25°C, V_{IN} = 24 V

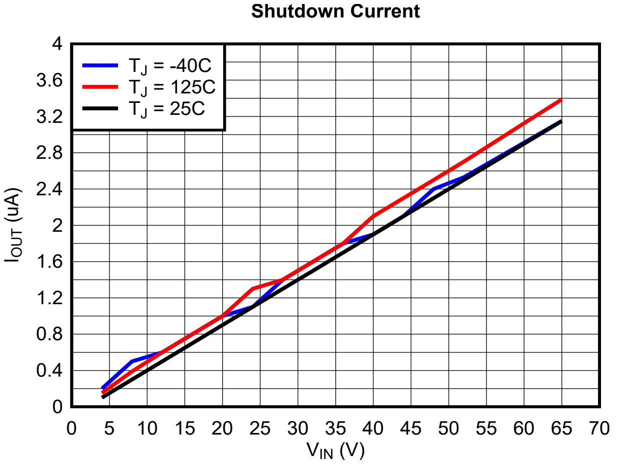


Figure 8-1. Shutdown Supply Current

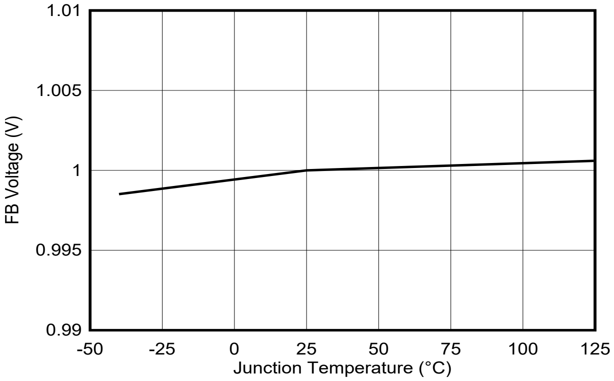


Figure 8-2. Feedback Voltage

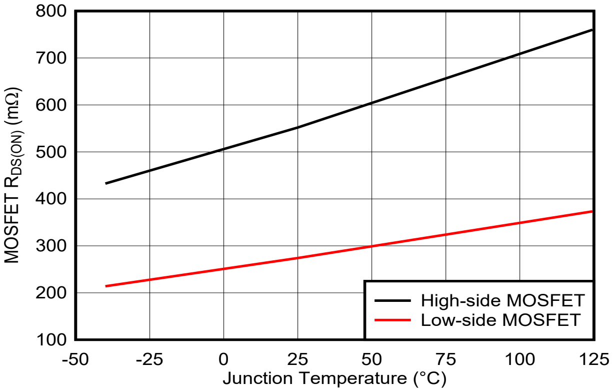


Figure 8-3. High-Side and Low-Side MOSFET $R_{DS(on)}$

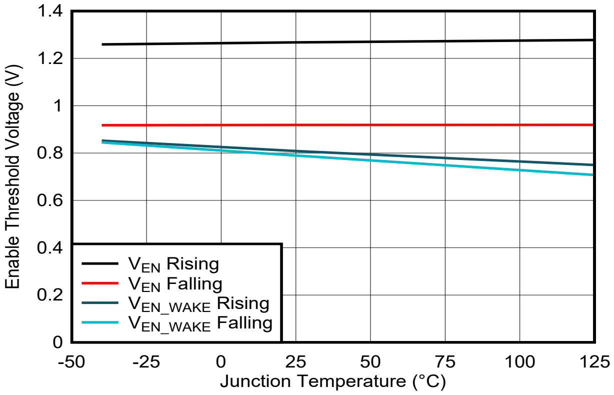


Figure 8-4. Enable Thresholds

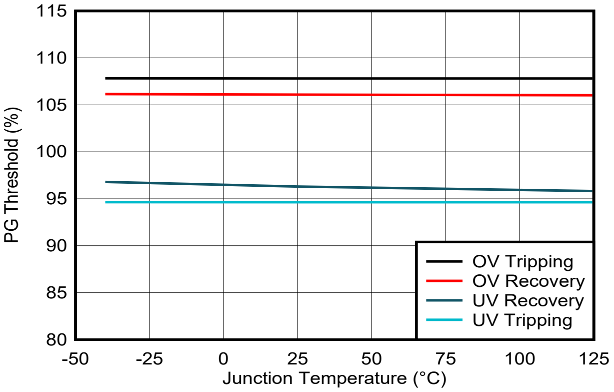


Figure 8-5. Power-Good (PG) Thresholds

8.8 Typical Characteristics: V_{IN} = 12 V

Unless otherwise specified, the following condition apply: T_A = 25°C

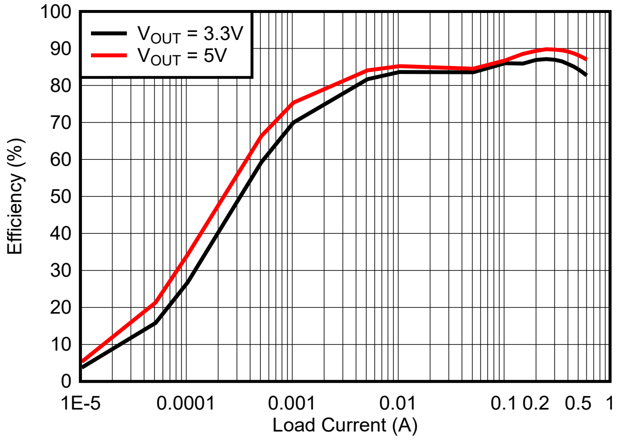


Figure 8-6. Efficiency in Auto Mode

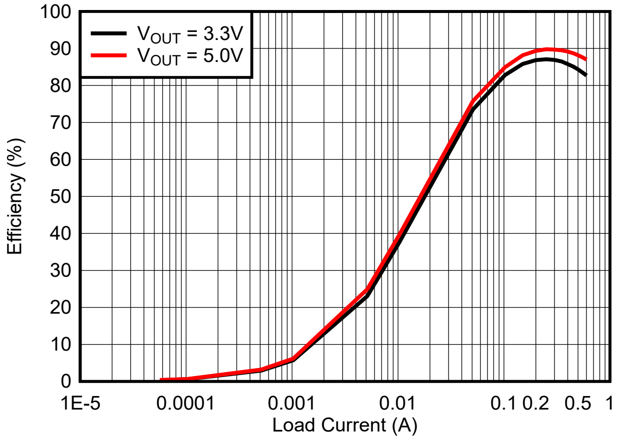


Figure 8-7. Efficiency in FPWM Mode

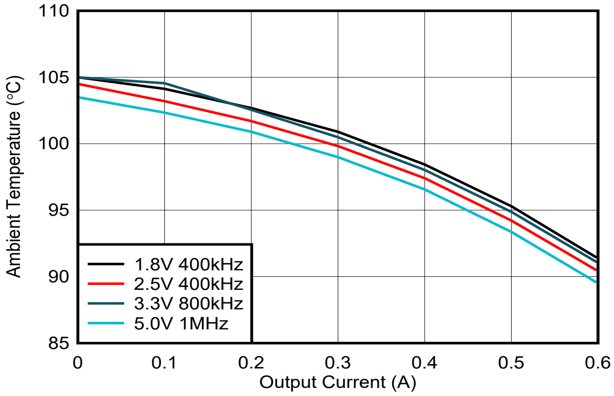


Figure 8-8. Safe Operating Area (Standard EVM Layout and Board Size)

8.9 Typical Characteristics: V_{IN} = 24 V

Unless otherwise specified, the following condition apply: T_A = 25°C

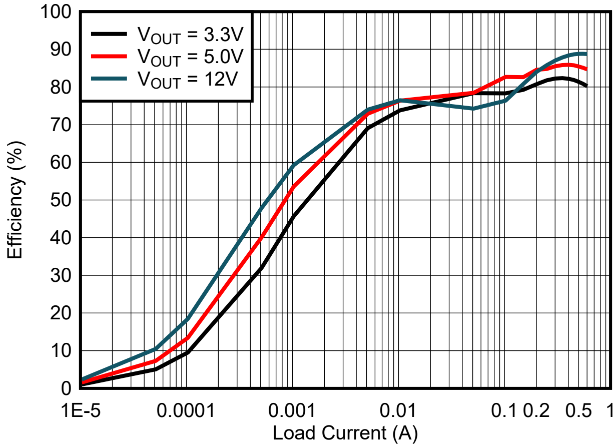


Figure 8-9. Efficiency in Auto Mode

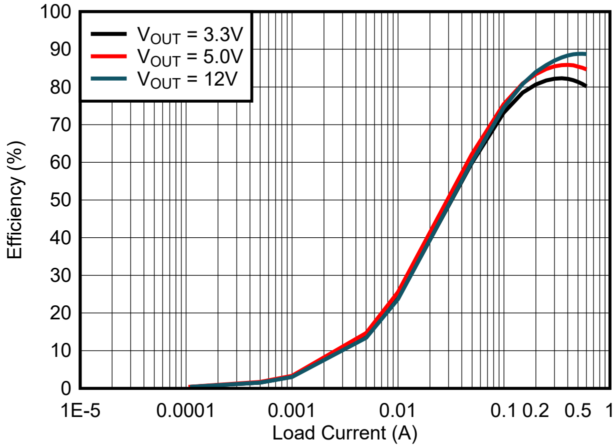


Figure 8-10. Efficiency in FPWM Mode

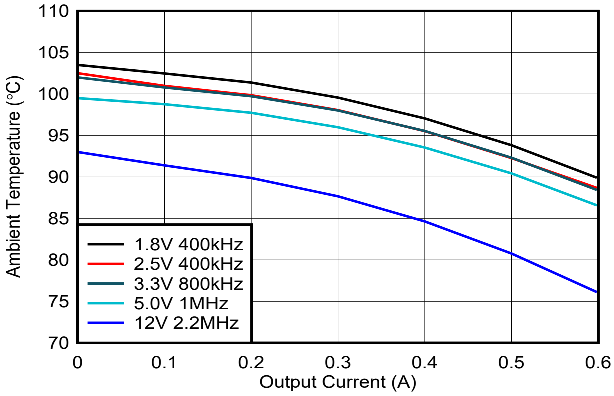


Figure 8-11. Safe Operating Area (Standard EVM Layout and Board Size)

8.10 Typical Characteristics: V_{IN} = 48 V

Unless otherwise specified, the following condition apply: T_A = 25°C

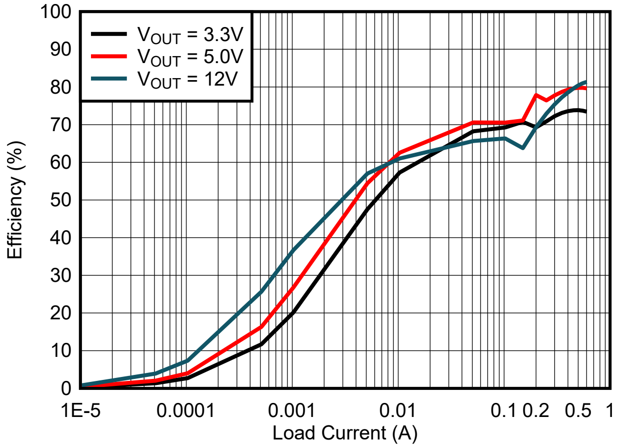


Figure 8-12. Efficiency in Auto Mode

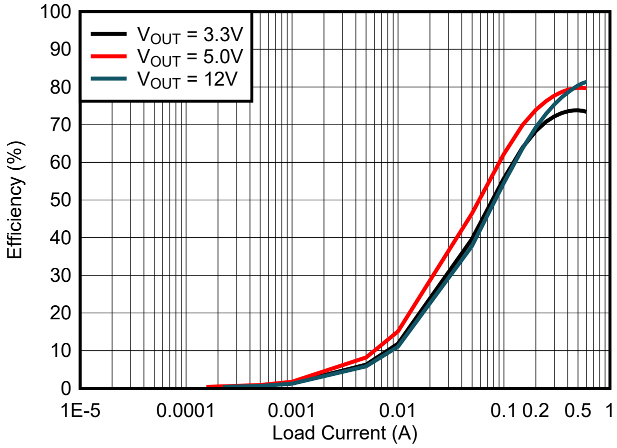


Figure 8-13. Efficiency in FPWM Mode

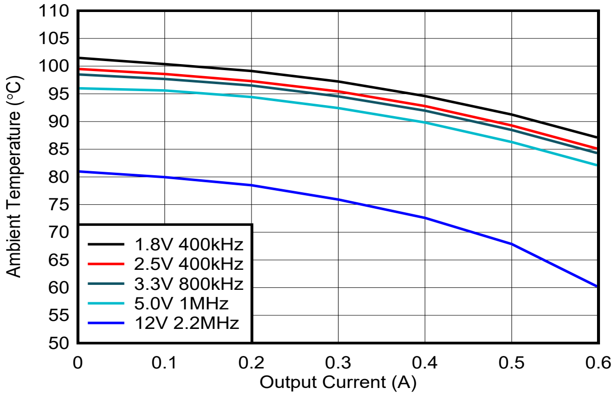


Figure 8-14. Safe Operating Area (Standard EVM Layout and Board Size)

9 Detailed Description

9.1 Overview

The TPSM365R6 or TPSM365R3 is an easy-to-use, synchronous buck, DC-DC power module that operates from a 3-V to 65-V supply voltage. The device is intended for step-down conversions from 5-V, 12-V, 24-V, and 48-V supply rails. With an integrated power controller, inductor, and MOSFETs, the TPSM365R6 or TPSM365R3 delivers up to 600-mA or 300-mA DC load current with high efficiency and ultra-low input quiescent current in a very small solution size. Although designed for simple implementation, this device offers flexibility to optimize its usage according to the target application. Control-loop compensation is not required, reducing design time and external component count.

The TPSM365Rx can operate over a wide range of switching frequencies and duty ratios. If the minimum ON-time or OFF-time cannot support the desired duty ratio, the switching frequency gets reduced automatically, maintaining the output voltage regulation. With the right internal loop compensation the system design time with the TPSM365Rx reduces significantly with minimal external components. In addition, the PGOOD output feature with built-in delayed release allows the elimination of the reset supervisor in many applications.

With a programmable switching frequency from 200 kHz to 2.2 MHz using its RT pin or an external clock signal, the TPSM365Rx incorporates specific features to improve EMI performance in noise-sensitive applications:

- An optimized package that incorporates flip chip on lead (FCOL) technology and pinout design enables a shielded switch-node layout that mitigates radiated EMI.
- Pseudo-Random Spread Spectrum (PRSS) modulation reduces peak emissions.
- Clock synchronization and FPWM mode enable constant switching frequency across the load current range.

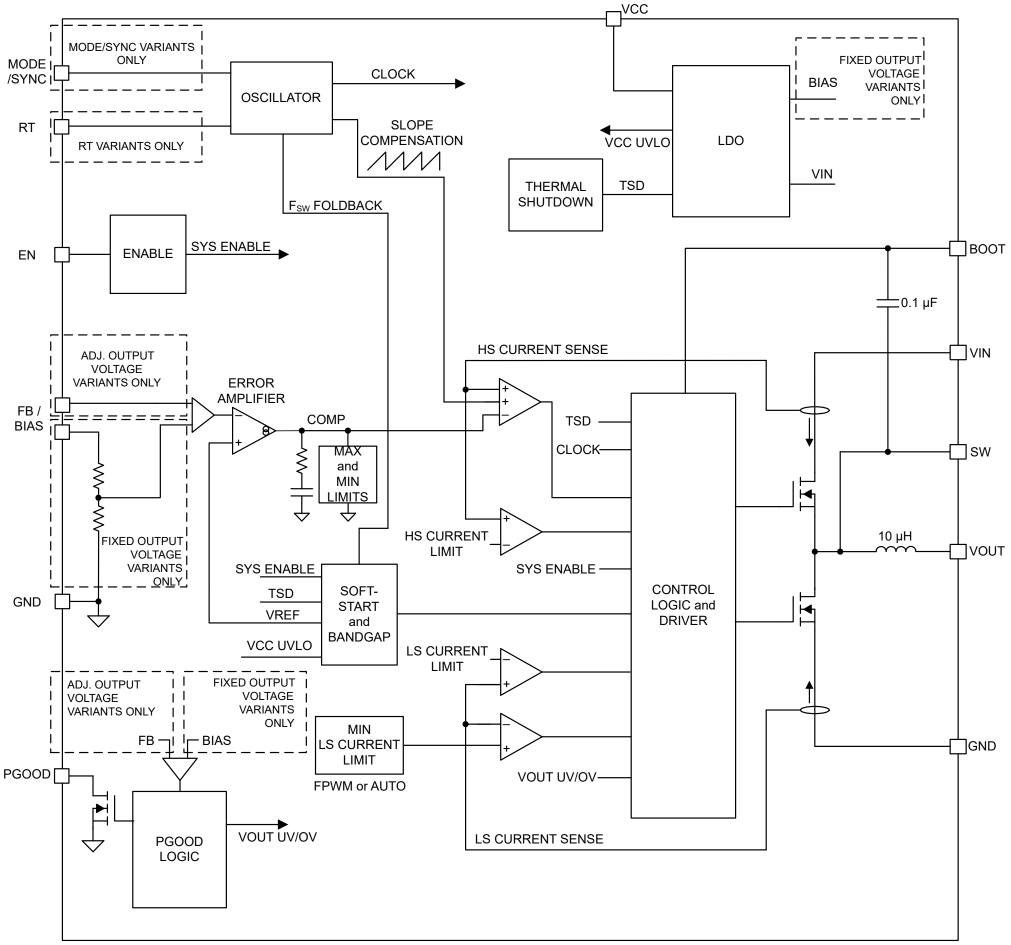
Together, these features eliminate the need for any common-mode choke, shielding, and input filter inductor, greatly reducing the complexities and cost of the EMI/EMC mitigation measures.

The TPSM365Rx module also includes inherent protection features for robust system requirements:

- An open-drain PGOOD indicator for power-rail sequencing and fault reporting
- Precision enable input with hysteresis, providing:
  - Programmable line undervoltage lockout (UVLO)
  - Remote ON and OFF capability
- Internally fixed output-voltage soft start with monotonic start-up into prebiased loads
- Hiccup-mode overcurrent protection with cycle-by-cycle peak and valley current limits
- Thermal shutdown with automatic recovery

These features enable a flexible and easy-to-use platform for a wide range of applications. The pin arrangement is designed for a simple layout, requiring few external components. See Section 10.4 for a layout example.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Input Voltage Range

With a steady-state input voltage range from 3 V to 65 V, the TPSM365Rx module is intended for step-down conversions from typical 12-V to 48-V input supply rails. The schematic circuit in Figure 9-1 shows all the necessary components to implement a TPSM365Rx-based buck regulator using a single input supply.

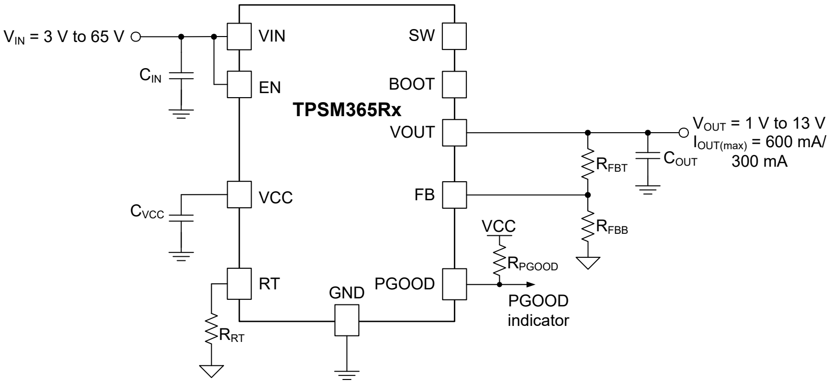


Figure 9-1. TPSM365Rx Schematic Diagram with Input Voltage Operating Range of 3 V to 65 V

Take extra care to ensure that the voltage at the VIN pin does not exceed the absolute maximum voltage rating of 70 V during line or load transient events. Voltage ringing at the VIN pins that exceeds the absolute maximum ratings can damage the IC.

9.3.2 Output Voltage Selection

Adjustable Output Voltage Variants

For adjustable output voltage variants, the TPSM365Rx has an adjustable output voltage range from 1.0 V to 13 V. Setting the output voltage requires two resistors, R_{FBT} and R_{FBB} (see Figure 9-2). Connect R_{FBT} between VOUT at the regulation point and the FB pin. Connect R_{FBB} between the FB pin and AGND. The variants with adjustable output voltage option in the TPSM365Rx family are designed with a 1-V internal reference voltage. The value for R_{FBT} can be calculated using Equation 1.

$$R_{FBT}[\text{k}\Omega] = R_{FBB}[\text{k}\Omega] \times \left(\frac{V_{OUT}[\text{V}]}{1\ \text{V}} - 1\right) \tag{1}$$

For adjustable output options, an addition feedforward capacitor, C_{FF}, in parallel with the R_{FBT} can be needed to optimize the transient response. See Section 10.2.1.2.7 for additional information. No additional resistor divider or feedforward capacitor, C_{FF}, is needed in case of fixed-output variants.

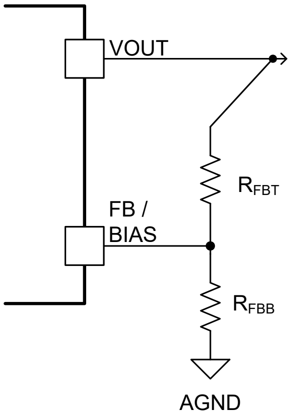


Figure 9-2. Setting Output Voltage for Adjustable Output Variant

Table 9-1. Standard R_{FBT} Values, Recommended F_{SW} and Minimum C_{OUT}

V_{OUT} (V)	R_{FBT} (kΩ) (1)	RECOMMENED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)	V_{OUT} (V)	R_{FBT} (kΩ) (1)	RECOMMENED F_{SW} (kHz)	$C_{OUT(MIN)}$ (µF) (EFFECTIVE)
1.0	Short	400	300	3.3	23.2	800	40
1.2	2	500	200	5.0	40.2	1000	25
1.5	4.99	500	160	7.5	64.9	1300	20
1.8	8.06	600	120	10	90.9	1500	15
2.0	10	600	100	12	110	2000	5
2.5	15	750	65	13	120	2200	5
3.0	20	750	50				

(1) R_{FBB} = 10 kΩ

Select an R_{FBB} value of 10 kΩ for most applications. A larger R_{FBT} value consumes less DC current, which is mandatory if light-load efficiency is critical. However, TI does not recommend R_{FBT} larger than 1 MΩ because the feedback path becomes more susceptible to noise. High feedback resistance generally requires more careful layout of the feedback path. Keep the feedback trace as short as possible while keeping the feedback trace away from the noisy area of the PCB. For more layout recommendations, see Section 10.4.

Fixed Output Voltage Variants

When using the TPSM365Rx as fixed-output options (no external resistors), simply connect the FB/BIAS to the output (VOUT). The 3.3-V or 5-V fixed output options are factory trimmed and are unique to a specific device. See *Section 6* for more details about the fixed-output variants.

9.3.3 Input Capacitors

Input capacitors are required to limit the input ripple voltage to the module due to switching-frequency AC currents. TI recommends using ceramic capacitors to provide low impedance and high RMS current rating over a wide temperature range. Equation 2 gives the input capacitor RMS current. The highest input capacitor RMS current occurs at D = 0.5, at which point, the RMS current rating of the capacitors must be greater than half the output current.

$$I_{CIN,rms} = \sqrt{D \times \left[I_{out}^2 \times (1 - D) + \frac{\Delta I_L^2}{12}\right]} \tag{2}$$

where

- D = V_{OUT} / V_{IN} is the module duty cycle.

Ideally, the DC and AC components of the input current to the buck stage are provided by the input voltage source and the input capacitors, respectively. Neglecting inductor ripple current, the input capacitors source current of amplitude (I_{OUT} – I_{IN}) during the D interval and sink I_{IN} during the 1 – D interval. Thus, the input capacitors conduct a square-wave current of peak-to-peak amplitude equal to the output current. The resulting capacitive component of the AC ripple voltage is a triangular waveform. Together with the ESR-related ripple component, Equation 3 gives the peak-to-peak ripple voltage amplitude.

$$\Delta V_{IN} = \frac{I_{OUT} \times D \times (1 - D)}{F_{SW} \times C_{IN}} + I_{OUT} \times R_{ESR} \tag{3}$$

Equation 4 gives the input capacitance required for a particular load current.

$$C_{IN} \geq \frac{D \times (1 - D) \times I_{OUT}}{F_{SW} \times (\Delta V_{IN} - R_{ESR} \times I_{OUT})} \tag{4}$$

where

- ΔV_{IN} is the input voltage ripple specification.

The TPSM365Rx requires a minimum of a 2.2-µF ceramic type input capacitance. Only use high-quality ceramic type capacitors with sufficient voltage and temperature rating. The ceramic input capacitors provide a low impedance source to the power module in addition to supplying the ripple current and isolating switching noise from other circuits. Additional capacitance can be required for applications with transient load requirements. The voltage rating of the input capacitors must be greater than the maximum input voltage. To compensate for the derating of ceramic capacitors, TI recommends a voltage rating of twice the maximum input voltage or placing multiple capacitors in parallel. Table 9-2 includes a preferred list of capacitors by vendor.

Table 9-2. Recommended Input Capacitors

VENDOR [1]	DIELECTRIC	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE RATING (V)	CAPACITANCE (µF) [2]
TDK	X7R	C3225X7R2A225K230AM	1210	100	2.2
Kemet	X7R	C1210C225K1RAC	1210	100	2.2
Kyocera / AVX	X7R	12061C225KAT4A	1206	100	2.2
Sansung Electro-Mechanics	X7R	CL32B225KCJSNNE	1210	100	2.2
Taiyo Yuden	X7R	MSASH32MSB7225KPNA01	1210	100	2.2

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

9.3.4 Output Capacitors

Table 9-1 lists the TPSM365Rx minimum amount of required output capacitance. The effects of DC bias and temperature variation must be considered when using ceramic capacitance. For ceramic capacitors, the package size, voltage rating, and dielectric material contribute to differences between the standard rated value and the actual effective value of the capacitance.

When adding additional capacitance above $C_{OUT(MIN)}$, the capacitance can be ceramic type, low-ESR polymer type, or a combination of the two. See Table 9-3 for a preferred list of output capacitors by vendor.

Table 9-3. Recommended Output Capacitors

VENDOR [1]	TEMPERATURE COEFFICIENT	PART NUMBER	CASE SIZE	CAPACITOR CHARACTERISTICS	
				VOLTAGE (V)	CAPACITANCE (µF) [2]
TDK	X7R	CGA5L1X7R1C106K160AC	1206	16	10
Murata	X7R	GCM31CR71C106KA64L	1206	16	10
TDK	X7R	C3216X7R1E106K160AB	1206	25	10
Murata	X7R	GRM32ER71E226M	1210	25	22
TDK	X7R	C3225X7R1E226M250AB	1210	25	22

(1) Consult capacitor suppliers regarding availability, material composition, RoHS and lead-free status, and manufacturing process requirements for any capacitors identified in this table. See the *Third-Party Products Disclaimer*.
(2) Nameplate capacitance values (the effective values are lower based on the applied DC voltage and temperature).

9.3.5 Enable, Start-Up, and Shutdown

Voltage at the EN pin controls the start-up or remote shutdown of the TPSM365Rx. The part stays shut down as long as the EN pin voltage is less than $V_{EN\text{-}WAKE}$ = 0.4 V. During the shutdown, the input current drawn by the device typically drops down to 0.5 µA (V_{IN} = 13.5 V). With the voltage at the EN pin greater than $V_{EN\text{-}WAKE}$, the device enters device standby mode and the internal LDO powers up to generate VCC. As the EN voltage increases further, approaching $V_{EN\text{-}VOUT}$, the device finally starts to switch, entering start-up mode with a soft start. During the device shutdown process, when the EN input voltage measures less than ($V_{EN\text{-}VOUT}$–$V_{EN\text{-}HYST}$), the regulator stops switching and re-enters device standby mode. Any further decrease in the EN pin voltage, below $V_{EN\text{-}WAKE}$, and the device is then firmly shut down. The high-voltage compliant EN input pin can be connected directly to the VIN input pin if remote precision control is not needed. The EN input pin must not be allowed to float.

The various EN threshold parameters and their values are listed in the *Section 8.5*. Figure 9-3 shows the precision enable behavior and Figure 9-4 shows a typical remote EN start-up waveform in an application. After EN goes high, after a delay of about 1 ms, the output voltage begins to rise with a soft start and reaches close to the final value in about 2.58 ms (t_{ss}). After a delay of about 1.956 ms (t_{PGOOD_ACT}), the PG flag goes high. During start-up, the device is not allowed to enter FPWM mode until the soft-start time has elapsed. This time is measured from the rising edge of EN.

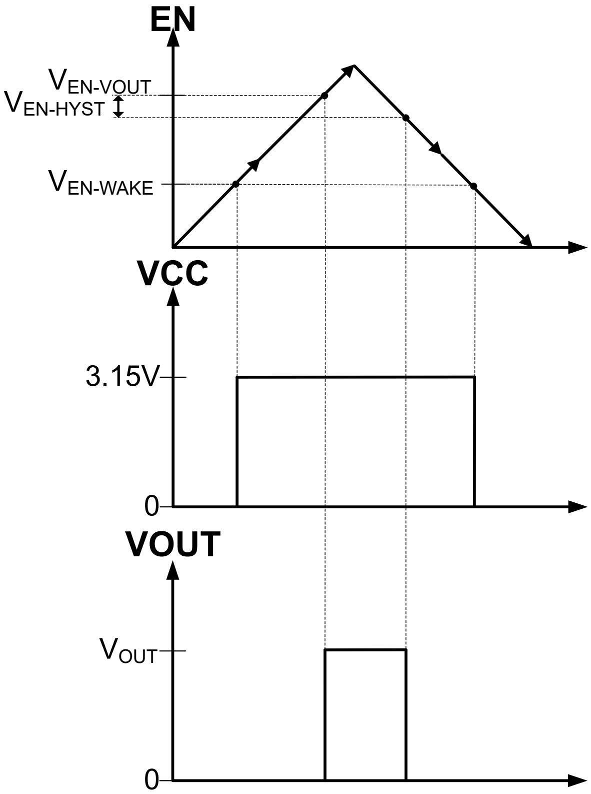


Figure 9-3. Precision Enable Behavior

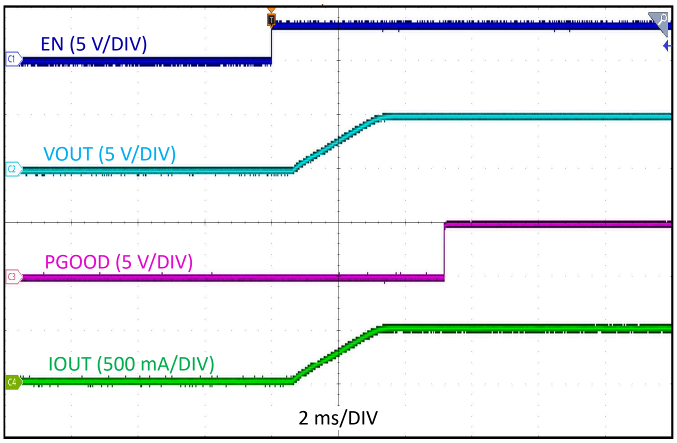


Figure 9-4. Enable Start-Up V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 0.5 A

External UVLO via EN pin

In some cases, an input UVLO level different than that provided internal to the device is needed. This can be accomplished by using the circuit shown in Figure 9-5. The input voltage at which the device turns on is designated as V_{ON} while the turn-off voltage is V_{OFF}. First, a value for R_{ENB} is chosen in the range of 10 kΩ to 100 kΩ, then Equation 5 and Equation 6 are used to calculate R_{ENT} and V_{OFF}, respectively.

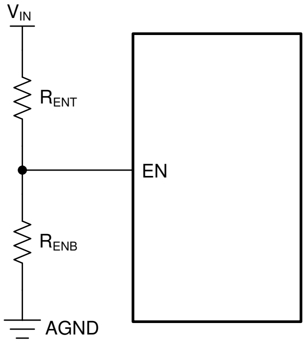


Figure 9-5. Setup for External UVLO Application

$$R_{ENT} = \left(\frac{V_{ON}}{V_{EN-VOUT}} - 1\right) \times R_{ENB} \tag{5}$$

$$V_{OFF} = V_{ON} \times \left(1 - \frac{V_{EN-HYST}}{V_{EN-VOUT}}\right) \tag{6}$$

where

- V_{ON} is the V_{IN} turn-on voltage.
- V_{OFF} is the V_{IN} turn-off voltage.

9.3.6 External CLK SYNC (with MODE/SYNC)

It is often desirable to synchronize the operation of multiple regulators in a single system, resulting in a well-defined system level performance. The select variants in the TPSM365Rx with the MODE/SYNC pin allow the power designer to synchronize the device to a common external clock. An in-phase locking scheme where the rising edge of the clock signal, provided to the MODE/SYNC pin, corresponds to the turning on of the high-side device. The external clock synchronization is implemented using a phase locked loop (PLL) eliminating any large glitches. The external clock fed into the TPSM365Rx replaces the internal free-running clock, but does not affect any frequency foldback operation. Output voltage continues to be well-regulated. The device remains in FPWM mode and operates in CCM for light loads when synchronization input is provided.

The MODE/SYNC input pin in the TPSM365Rx can operate in one of three selectable modes:

- Auto Mode: Pulse frequency modulation (PFM) operation is enabled during light load and diode emulation prevents reverse current through the inductor.
- FPWM Mode: In FPWM mode, diode emulation is disabled, allowing current to flow backwards through the inductor. This allows operation at full frequency even without load current.
- SYNC Mode: The internal clock locks to an external signal applied to the MODE/SYNC pin. As long as output voltage can be regulated at full frequency and is not limited by minimum off-time or minimum on-time, clock frequency is matched to the frequency of the signal applied to the MODE/SYNC pin. While the device is in SYNC mode, it operates as though in FPWM mode: diode emulation is disabled allowing the frequency applied to the MODE/SYNC pin to be matched without a load.

9.3.6.1 Pulse-Dependent MODE/SYNC Pin Control

Most systems that require more than a single mode of operation from the device are controlled by digital circuitry such as a microprocessor. These systems can generate dynamic signals easily but have difficulty generating multi-level signals. Pulse-dependent MODE/SYNC pin control is useful with these systems. To initiate pulse-dependent MODE/SYNC pin control, a valid sync signal must be applied. Table 9-4 shows a summary of the pulse dependent mode selection settings.

Table 9-4. Pulse-Dependent Mode Selection Settings

MODE/SYNC INPUT	MODE
> V_{MODE_H}	FPWM with spread spectrum factory setting
< V_{MODE_L}	Auto mode with spread spectrum factory setting
Synchronization Clock	SYNC mode

Figure 9-6 shows the transition between auto mode and FPWM mode while in pulse-dependent MODE/SYNC control. The device transitions to a new mode of operation after the time, t_{MODE}. Figure 9-6 and Figure 9-7 show the details.

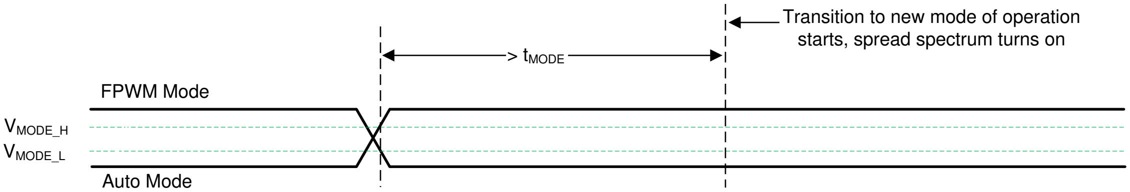


Figure 9-6. Transition from Auto Mode and FPWM Mode

If MODE/SYNC voltage remains constant longer than t_{MODE}, the device enters either auto mode or FPWM mode with spread spectrum turned on (if factory setting is enabled) and MODE/SYNC continues to operate in pulse-dependent scheme.

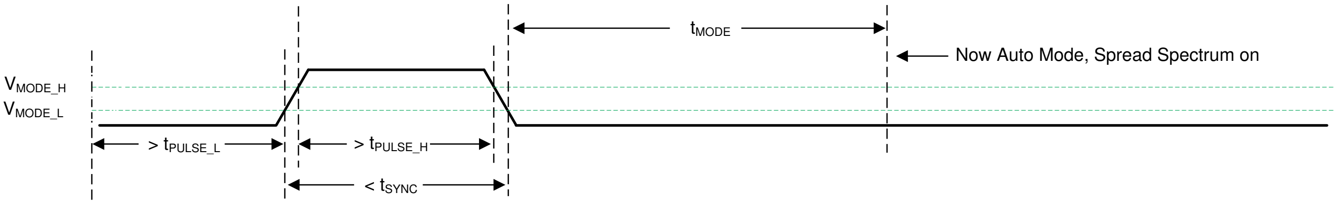


Figure 9-7. Transition from SYNC Mode to Auto Mode

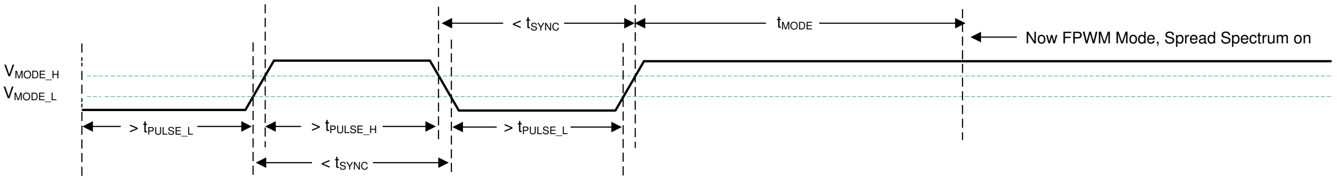


Figure 9-8. Transition from SYNC Mode to FPWM Mode

9.3.7 Switching Frequency (RT)

The select variants in the TPSM365Rx family with the RT pin allows the power designers to set any desired operating frequency between 200 kHz and 2.2 MHz in their applications. See Figure 9-9 to determine the resistor value needed for the desired switching frequency or simply select from Table 9-6. The RT pin and the MODE/SYNC pin variants share the same pin location. The power supply designer can either use the RT pin variant and adjust the switching frequency of operation as warranted by the application or use the MODE/SYNC variant and synchronize to an external clock signal. See Table 9-5 for selection on programming the RT pin.

Table 9-5. RT Pin Setting

RT INPUT	SWITCHING FREQUENCY
VCC	1 MHz
GND	2.2 MHz
RT to GND	Adjustable according to Figure 9-9
Float (not recommended)	No switching

$$RT = \frac{18286}{Fsw^{1.021}} \quad (7)$$

where

- RT is the frequency setting resistor value (kΩ).
- F_{SW} is the switching frequency (kHz).

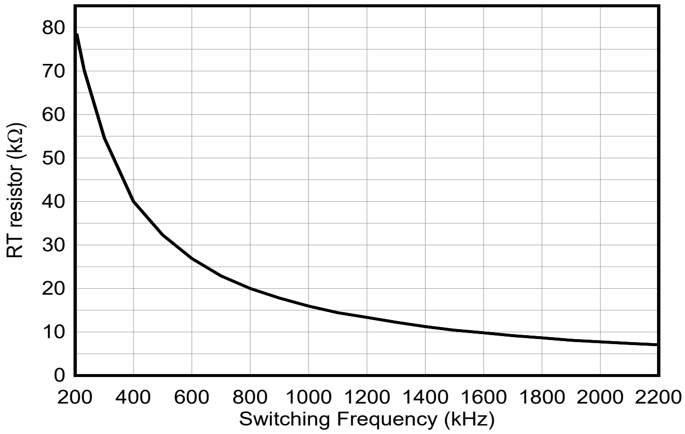


Figure 9-9. RT Values vs Frequency

The switching frequency must be selected based on the output voltage setting of the device. See Table 9-6 for R_{RT} resistor values and the allowable output voltage range for a given switching frequency for common input voltages.

Table 9-6. Switching Frequency Versus Output Voltage (I_{OUT} = 600 mA)

F_{SW} (kHz)	R_{RT} (kΩ)	V_{IN} = 5 V		V_{IN} = 12 V		V_{IN} = 24 V		V_{IN} = 36 V		V_{IN} = 48 V	
		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)		V_{OUT} RANGE (V)	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
200	81.6	1	1	-	-	-	-	-	-	-	-
400	40.2	1	2.4	1	2	1	1.9	1.1	1.8	1.4	1.8
600	26.7	1	2.7	1	4	1.1	3	1.6	2.8	2.1	2.8
800	19.8	1	3.1	1	6	1.4	4.4	2.1	3.9	2.7	3.8
1000	15.8	1	3.5	1	6	1.7	5.8	2.6	5.1	3.4	4.9
1200	13.2	1	3.9	1.1	6	2.1	8	3.1	6.4	4.1	6
1400	11.3	1	4	1.2	6.4	2.4	12	3.6	7.9	4.8	7.3
1600	9.76	1	4	1.4	7	2.7	12	4.1	9.7	5.4	8.6
1800	8.66	1	4	1.6	7.4	3.1	12	4.6	11.9	6.1	10.1
2000	7.77	1	4	1.7	7.8	3.4	12	5.1	13	6.8	11.7
2200	7.06	1	4	1.9	8.2	3.7	12	5.6	13	7.4	13

9.3.8 Power-Good Output Operation

The power-good feature using the PGOOD pin of the TPSM365Rx can be used to reset a system microprocessor whenever the output voltage is out of regulation. This open-drain output remains low under device fault conditions, such as current limit and thermal shutdown, as well as during normal start-up. A glitch filter prevents false flag operation for any short duration excursions in the output voltage, such as during line and load transients. Output voltage excursions lasting less than t_{RESET_FILTER} do not trip the power-good flag. Power-good operation can best be understood in reference to Figure 9-10. Table 9-7 gives a more detailed breakdown of the PGOOD operation. Here, $V_{PG_{UV}}$ is defined as the PG_{UV} scaled version of V_{OUT} (target regulated output voltage) and $V_{PG_{HYS}}$ as the PG_{HYS} scaled version of V_{OUT}, where both PG_{UV} and PG_{HYS} are listed in Section 8.5. During the initial power up, a total delay of 5 ms (typical) is encountered from the time $V_{EN\text{-}VOUT}$ is triggered to the time that the power-good is flagged high. This delay only occurs during the device start-up and is not encountered during any other normal operation of the power-good function. When EN is pulled low, the power-good flag output is also forced low. With EN low, power-good remains valid as long as the input voltage ($V_{PGD\text{-}VALID}$ is ≥ 1 V (typical)).

The power-good output scheme consists of an open-drain n-channel MOSFET, which requires an external pullup resistor connected to a suitable logic supply. It can also be pulled up to either V_{CC} or V_{OUT} through an appropriate resistor, as desired. If this function is not needed, the PGOOD pin can be open or grounded. Limit the current into this pin to ≤ 4 mA.

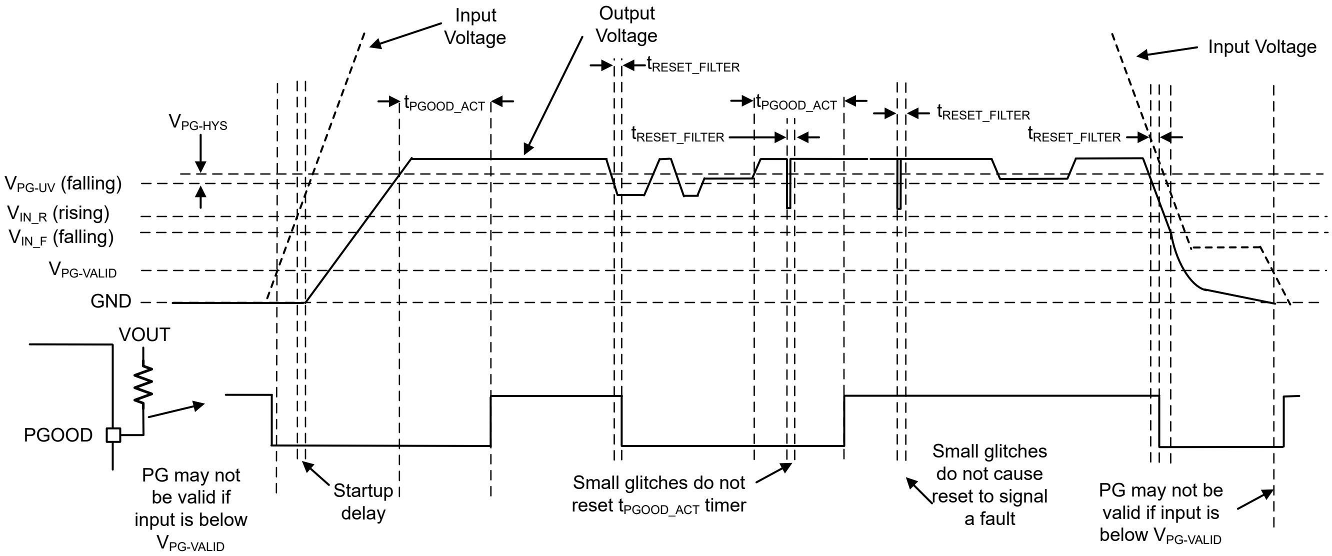


Figure 9-10. Power-Good Operation (OV Events Not Included)

Table 9-7. Fault Conditions for PGOOD (Pull Low)

FAULT CONDITION INITIATED	FAULT CONDITION ENDS (AFTER WHICH t_{PGOOD_ACT} MUST PASS BEFORE PGOOD OUTPUT IS RELEASED)
$V_{OUT} < V_{PG_{UV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation: $V_{PG_{UV}} + V_{PG_{HYS}} < V_{OUT} < V_{PG_{OV}} - V_{PG_{HYS}}$
$V_{OUT} > V_{PG_{OV}}$ AND $t > t_{RESET\_FILTER}$	Output voltage in regulation
$T_J > T_{SD\text{-}R}$	$T_J < T_{SD\text{-}R}\text{-}T_{SD\text{-}HYS}$ AND output voltage in regulation
$EN < V_{EN\text{-}VOUT} - V_{EN\text{-}HYST}$	$EN > V_{EN\text{-}VOUT}$ AND output voltage in regulation
$V_{CC} < V_{CC\text{-}UVLO} - V_{CC\text{-}UVLO\text{-}HYST}$	$V_{CC} > V_{CC\text{-}UVLO}$ AND output voltage in regulation

9.3.9 Internal LDO, VCC UVLO, and BIAS Input

The TPSM365Rx uses the internal LDO output and the VCC pin for all internal power supply. The VCC pin draws power either from the VIN (in adjustable output variants) or the BIAS (in fixed-output variants). In the fixed output variants, after the TPSM365Rx is active but has yet to regulate, the VCC rail continues to draw power from the input voltage, VIN, until the BIAS voltage reaches > 3.15 V (or when the device has reached steady-state regulation post the soft start). The VCC rail typically measures 3.15 V in both adjustable and fixed output variants. To prevent unsafe operation, VCC has an undervoltage lockout, which prevents switching if the internal voltage is too low. See $V_{VCC\text{-}UVLO}$ and $V_{VCC\text{-}UVLO\text{-}HYST}$ in *Section 8.5*. During start-up, VCC momentarily exceeds the normal operating voltage until $V_{VCC\text{-}UVLO}$ is exceeded, then drops to the normal operating voltage. Note that these undervoltage lockout values, when combined with the LDO dropout, drives the minimum input voltage rising and falling thresholds.

9.3.10 Bootstrap Voltage and $V_{BOOT\text{-}UVLO}$ (BOOT Terminal)

The high-side switch driver circuit requires a bias voltage higher than VIN to ensure the HS switch is turned ON. There is an internal 0.1-µF capacitor connected between BOOT and SW that operates as a charge pump to boost the voltage on the BOOT terminal to (SW + VCC). The boot diode is integrated on the TPSM365Rx die to minimize physical solution size. The BOOT rail has an UVLO setting. This UVLO has a threshold of $V_{BOOT\text{-}UVLO}$ and is typically set at 2.3 V. If the BOOT capacitor is not charged above this voltage with respect to the SW pin, then the part initiates a charging sequence, turning on the low-side switch before attempting to turn on the high-side device.

9.3.11 Spread Spectrum

The purpose of spread spectrum is to eliminate peak emissions at specific frequencies by spreading these peaks across a wider range of frequencies than a part with fixed-frequency operation. In most systems containing the TPSM365Rx, low-frequency conducted emissions from the first few harmonics of the switching frequency can be easily filtered. A more difficult design criterion is reduction of emissions at higher harmonics, which fall in the FM band. These harmonics often couple to the environment through electric fields around the switch node and inductor. The TPSM365Rx uses a ±2% spread of frequencies which can spread energy smoothly across the FM and TV bands, but is small enough to limit subharmonic emissions below the switching frequency of the part. Peak emissions at the switching frequency of the part are only reduced slightly, by less than 1 dB, while peaks in the FM band are typically reduced by more than 6 dB.

The TPSM365Rx uses a cycle-to-cycle frequency hopping method based on a linear feedback shift register (LFSR). This intelligent pseudo-random generator limits cycle-to-cycle frequency changes to limit output ripple. The pseudo-random pattern repeats at less than 1.5 Hz, which is below the audio band.

The spread spectrum is only available while the clock of the TPSM365Rx device is free running at its natural frequency. Any of the following conditions overrides spread spectrum, turning it off:

- The clock is slowed due to operation at low-input voltage – this is operation in dropout.
- The clock is slowed under light load in auto mode. Note that if you are operating in FPWM mode, spread spectrum can be active, even if there is no load.
- The clock is slowed due to high input to output voltage ratio. This mode of operation is expected if on-time reaches minimum on-time. See *Electrical Characteristics*.
- The clock is synchronized with an external clock.

9.3.12 Soft Start and Recovery from Dropout

When designing with the TPSM365Rx, slow rise in output voltage due to recovery from dropout and soft start must be considered as a two separate operating conditions, as shown in Figure 9-11 and Figure 9-12. Soft start is triggered by any of the following conditions:

- Power is applied to the VIN pin of the device, releasing undervoltage lockout.
- EN is used to turn on the device.
- Recovery from shutdown due to overtemperature protection.

After soft start is triggered, the power module takes the following actions:

- The reference used by the power module to regulate the output voltage is slowly ramped up. The net result is that output voltage, if previously 0 V, takes t_{SS} to reach 90% of the desired value.
- Operating mode is set to auto mode of operation, activating the diode emulation mode for the low-side MOSFET. This allows start-up without pulling the output low. This is true even when there is a voltage already present at the output during a pre-bias start-up.

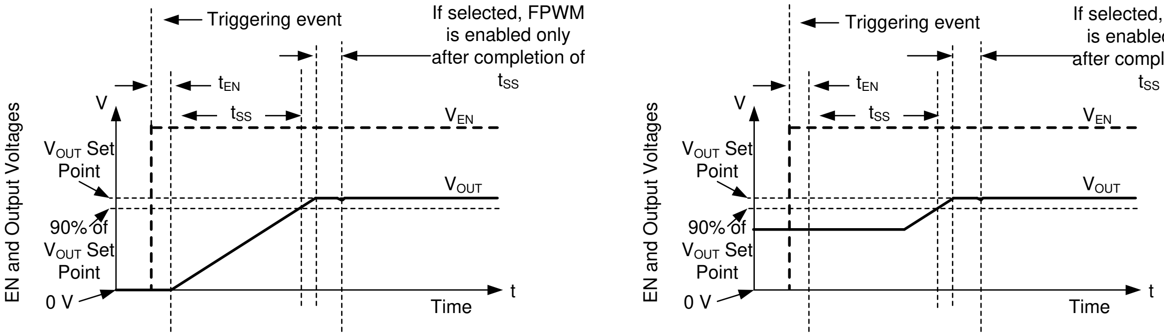


Figure 9-11. Soft Start with and without Prebias Voltage

9.3.12.1 Recovery from Dropout

Any time the output voltage falls more than a few percent, output voltage ramps up slowly. This condition, called graceful recovery from dropout in this document, differs from soft start in two important ways:

- The reference voltage is set to approximately 1% above what is needed to achieve the existing output voltage.
- If the device is set to FPWM, it continues to operate in that mode during its recovery from dropout. If output voltage were to suddenly be pulled up by an external supply, the TPSM365Rx can pull down on the output. Note that all protections that are present during normal operation are in place, preventing any catastrophic failure if output is shorted to a high voltage or ground.

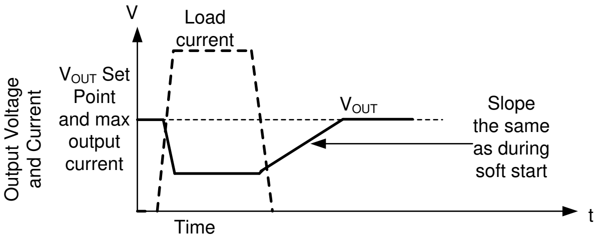


Figure 9-12. Recovery from Dropout

Whether the output voltage falls due to high load or low input voltage, after the condition that causes the output to fall below its set point is removed, the output climbs at the same speed as during start-up. Figure 9-12 shows an example of this behavior.

9.3.13 Overcurrent Protection (OCP)

The TPSM365Rx is protected from overcurrent conditions by using cycle-by-cycle current limiting circuitry on both the high-side and low-side MOSFETs. The current is compared every switching cycle to the current limit threshold. During an overcurrent condition, the output voltage decreases.

High-side MOSFET overcurrent protection is implemented by the typical peak-current mode control scheme. The HS switch current is sensed when the HS is turned on after a short blanking time. The HS switch current is compared to either the minimum of a fixed current set point or the output of the internal error amplifier loop minus the slope compensation every switching cycle. Because the output of the internal error amplifier loop has a maximum value and slope compensation increases with duty cycle, HS current limit decreases with increased duty factor if duty factor is typically above 35%.

When the LS switch is turned on, the current going through it is also sensed and monitored. Like the high-side device, the low-side device has a turnoff commanded by the internal error amplifier loop. In the case of the lowside device, turn-off is prevented if the current exceeds this value, even if the oscillator normally starts a new switching cycle. Also like the high-side device, there is a limit on how high the turn-off current is allowed to be. This is called the low-side current limit. If the LS current limit is exceeded, the LS MOSFET stays on and the HS switch is not to be turned on. The LS switch is turned off after the LS current falls below this limit and the HS switch is turned on again as long as at least one clock period has passed since the last time the HS device has turned on.

9.3.14 Thermal Shutdown

Thermal shutdown limits total power dissipation by turning off the internal switches when the device junction temperature exceeds 168°C (typical). Thermal shutdown does not trigger below 158°C (minimum). After thermal shutdown occurs, hysteresis prevents the part from switching until the junction temperature drops to approximately 158°C (typical). When the junction temperature falls below 158°C (typical), the TPSM365Rx attempts another soft start.

While the TPSM365Rx is shut down due to high junction temperature, power continues to be provided to VCC. To prevent overheating due to a short circuit applied to VCC, the LDO that provides power for VCC has reduced current limit while the part is disabled due to high junction temperature. The LDO only provides a few milliamperes during thermal shutdown.

9.4 Device Functional Modes

9.4.1 Shutdown Mode

The EN pin provides electrical ON and OFF control of the device. When the EN pin voltage is below 0.4 V, the power module does not have any output voltage and the device is in shutdown mode. In shutdown mode, the quiescent current drops to typically 0.5 μA.

9.4.2 Standby Mode

The internal LDO has a lower EN threshold than the output of the power module. When the EN pin voltage is above $V_{EN\text{-}WAKE}$ and below the precision enable threshold for the output voltage, the internal LDO regulates the VCC voltage at 3.15 V typical. The precision enable circuitry is ON after VCC is above its UVLO. The internal power MOSFETs of the SW node remain off unless the voltage on EN pin goes above its precision enable threshold. The TPSM365Rx also employs UVLO protection. If the VCC voltage is below its UVLO level, the output of the module is turned off.

9.4.3 Active Mode

The TPSM365Rx is in active mode whenever the EN pin is above $V_{EN\text{-}VOUT}$, V_{IN} is high enough to satisfy V_{IN_R}, and no other fault conditions are present. The simplest way to enable the operation is to connect the EN pin to V_{IN}, which allows self start-up when the applied input voltage exceeds the minimum V_{IN_R}.

In active mode, depending on the load current, input voltage, and output voltage, the TPSM365Rx is in one of five modes:

- Continuous conduction mode (CCM) with fixed switching frequency when the load current is above half of the inductor current ripple.
- Auto Mode - Light Load Operation: PFM when switching frequency is decreased at very light load.
- FPWM Mode - Light Load Operation: Discontinuous conduction mode (DCM) when the load current is lower than half of the inductor current ripple.
- Minimum on-time: At high input voltage and low output voltages, the switching frequency is reduced to maintain regulation.
- Dropout mode: When switching frequency is reduced to minimize voltage dropout.

9.4.3.1 CCM Mode

The following operating description of the TPSM365Rx refers to *Section 9.2*. In CCM, the TPSM365Rx supplies a regulated output voltage by turning on the internal high-side (HS) and low-side (LS) switches with varying duty cycle (D). During the HS switch on-time, the SW pin voltage, V_{SW}, swings up to approximately V_{IN}, and the inductor current increases with a linear slope. The HS switch is turned off by the control logic. During the HS switch off-time, t_{OFF}, the LS switch is turned on. Inductor current discharges through the LS switch, which forces the V_{SW} to swing below ground by the voltage drop across the LS switch. The buck module converter loop adjusts the duty cycle to maintain a constant output voltage. D is defined by the on-time of the HS switch over the switching period:

$$D = T_{ON} / T_{SW} \tag{8}$$

In an ideal buck module converter where losses are ignored, D is proportional to the output voltage and inversely proportional to the input voltage:

$$D = V_{OUT} / V_{IN} \tag{9}$$

9.4.3.2 AUTO Mode - Light Load Operation

The TPSM365Rx can have two behaviors while lightly loaded. One behavior, called auto mode operation, allows for seamless transition between normal current mode operation while heavily loaded and highly efficient light load operation. The other behavior, called FPWM Mode, maintains full frequency even when unloaded. Which mode the TPSM365Rx operates in depends on which variant from this family is selected. Note that all parts operate in FPWM mode when synchronizing frequency to an external signal.

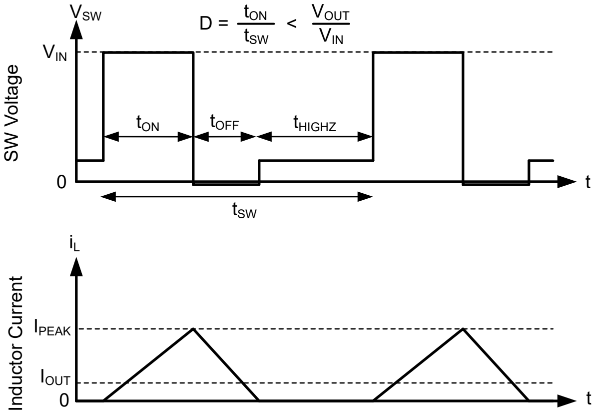
The light load operation is employed in the TPSM365Rx only in the auto mode. The light load operation employs two techniques to improve efficiency:

- Diode emulation, which allows DCM operation (See Figure 9-13)
- Frequency reduction (See Figure 9-14)

Note that while these two features operate together to improve light load efficiency, they operate independent of each other.

9.4.3.2.1 Diode Emulation

Diode emulation prevents reverse current through the inductor which requires a lower frequency needed to regulate given a fixed peak inductor current. Diode emulation also limits ripple current as frequency is reduced. With a fixed peak current, as output current is reduced to zero, frequency must be reduced to near zero to maintain regulation.



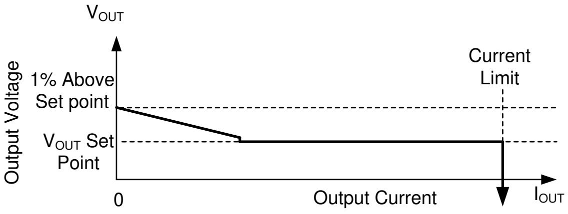
In auto mode, the low-side device is turned off after SW node current is near zero. As a result, after output current is less than half of what inductor ripple can be in CCM, the part operates in DCM which is equivalent to the statement that diode emulation is active.

Figure 9-13. PFM Operation

The TPSM365Rx has a minimum peak inductor current setting (see $I_{PEAK-MIN}$ in *Section 8.5*) while in auto mode. After current is reduced to a low value with fixed input voltage, on-time is constant. Regulation is then achieved by adjusting frequency. This mode of operation is called PFM mode regulation.

9.4.3.2.2 Frequency Reduction

The TPSM365Rx reduces frequency whenever output voltage is high. This function is enabled whenever the internal error amplifier compensation output, COMP, an internal signal, is low and there is an offset between the regulation set point of FB/BIAS and the voltage applied to FB/BIAS. The net effect is that there is larger output impedance while lightly loaded in auto mode than in normal operation. Output voltage must be approximately 1% high when the part is completely unloaded.



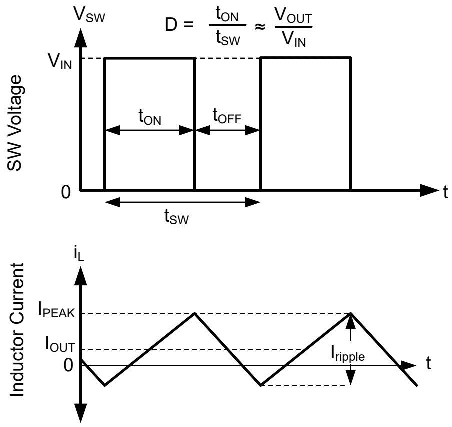
In auto mode, after output current drops below approximately 1/10th the rated current of the part, output resistance increases so that output voltage is 1% high while the buck is completely unloaded.

Figure 9-14. Steady State Output Voltage versus Output Current in Auto Mode

In PFM operation, a small DC positive offset is required on the output voltage to activate the PFM detector. The lower the frequency in PFM, the more DC offset is needed on VOUT. If the DC offset on VOUT is not acceptable, a dummy load at VOUT or FPWM Mode can be used to reduce or eliminate this offset.

9.4.3.3 FPWM Mode - Light Load Operation

In FPWM Mode, frequency is maintained while the output is lightly loaded. To maintain frequency, a limited reverse current is allowed to flow through the inductor. Reverse current is limited by reverse current limit circuitry, see *Section 8.5* for reverse current limit values.



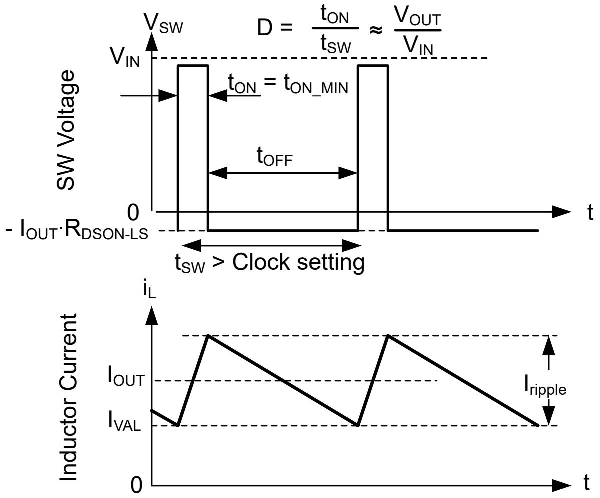
In FPWM mode, Continuous Conduction (CCM) is possible even if I_{OUT} is less than half of I_{ripple}.

Figure 9-15. FPWM Mode Operation

For all devices, in FPWM mode, frequency reduction is still available if output voltage is high enough to command minimum on-time even while lightly loaded, allowing good behavior during faults which involve output being pulled up.

9.4.3.4 Minimum On-time (High Input Voltage) Operation

The TPSM365Rx continues to regulate output voltage even if the input-to-output voltage ratio requires an on-time less than the minimum on-time of the chip with a given clock setting. This is accomplished using valley current control. At all times, the compensation circuit dictates both a maximum peak inductor current and a maximum valley inductor current. If for any reason, valley current is exceeded, the clock cycle is extended until valley current falls below that determined by the compensation circuit. If the power module is not operating in current limit, the maximum valley current is set above the peak inductor current, preventing valley control from being used unless there is a failure to regulate using peak current only. If the input-to-output voltage ratio is too high, such that the inductor current peak value exceeds the peak command dictated by compensation, the high-side device cannot be turned off quickly enough to regulate output voltage. As a result, the compensation circuit reduces both peak and valley current. After a low enough current is selected by the compensation circuit, valley current matches that being commanded by the compensation circuit. Under these conditions, the low-side device is kept on and the next clock cycle is prevented from starting until inductor current drops below the desired valley current. Because on-time is fixed at its minimum value, this type of operation resembles that of a device using a Constant On-Time (COT) control scheme; see Figure 9-16.

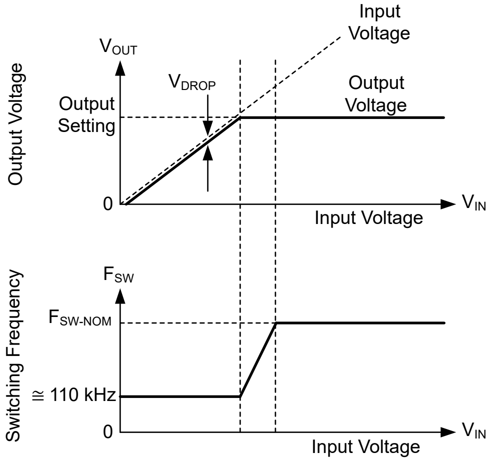


In valley control mode, minimum inductor current is regulated, not peak inductor current.

Figure 9-16. Valley Current Mode Operation

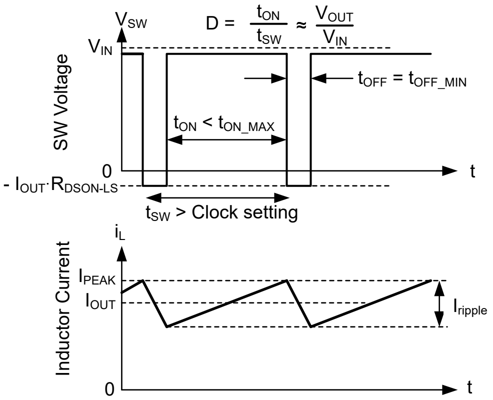
9.4.4 Dropout

Dropout operation is defined as any input-to-output voltage ratio that requires frequency to drop to achieve the required duty cycle. At a given clock frequency, duty cycle is limited by the minimum off-time. After this limit is reached as shown in Figure 9-18 if clock frequency was to be maintained, the output voltage can fall. Instead of allowing the output voltage to drop, the TPSM365Rx extends the high side switch on-time past the end of the clock cycle until the needed peak inductor current is achieved. The clock is allowed to start a new cycle after peak inductor current is achieved or after a pre-determined maximum on-time, $t_{ON\text{-}MAX}$, of approximately 9 µs passes. As a result, after the needed duty cycle cannot be achieved at the selected clock frequency due to the existence of a minimum off-time, frequency drops to maintain regulation. As shown in Figure 9-17 if input voltage is low enough so that output voltage cannot be regulated even with an on-time of $t_{ON\text{-}MAX}$, output voltage drops to slightly below the input voltage by V_{DROP}. For additional information on recovery from dropout, refer back to Section 9.3.12.1.



Output voltage and frequency versus input voltage: If there is little difference between input voltage and output voltage setting, the IC reduces frequency to maintain regulation. If input voltage is too low to provide the desired output voltage at approximately 110 kHz, input voltage tracks output voltage.

Figure 9-17. Frequency and Output Voltage in Dropout



Switching waveforms while in dropout. Inductor current takes longer than a normal clock to reach the desired peak value. As a result, frequency drops. This frequency drop is limited by $t_{ON\text{-}MAX}$.

Figure 9-18. Dropout Waveforms

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Application Information

The TPSM365Rx only requires a few external components to convert from a wide range of supply voltages to a fixed output voltage. To expedite and streamline the process of designing of a TPSM365Rx, WEBENCH® online software is available to generate complete designs, leveraging iterative design procedures and access to comprehensive component databases. The following section describes the design procedure to configure the TPSM365Rx power module.

As mentioned previously, the TPSM365Rx also integrates several optional features to meet system design requirements, including precision enable, UVLO, and PGOOD indicator. The application circuit detailed below shows TPSM365Rx configuration options suitable for several application use cases. Refer to the *TPSM365R6EVM User's Guide* for more detail.

Note

All of the capacitance values given in the following application information refer to *effective* values unless otherwise stated. The *effective* value is defined as the actual capacitance under DC bias and temperature, not the rated or nameplate values. Use high-quality, low-ESR, ceramic capacitors with an X7R or better dielectric throughout. All high value ceramic capacitors have a large voltage coefficient in addition to normal tolerances and temperature effects. Under DC bias the capacitance drops considerably. Large case sizes and higher voltage ratings are better in this regard. To help mitigate these effects, multiple capacitors can be used in parallel to bring the minimum *effective* capacitance up to the required value. This can also ease the RMS current requirements on a single capacitor. A careful study of bias and temperature variation of any capacitor bank must be made to ensure that the minimum value of *effective* capacitance is provided.

10.2 Typical Application

The following design is a sample typical application and design procedure to implement the TPSM365Rx.

10.2.1 600-mA and 300-mA Synchronous Buck Regulator for Industrial Applications

Figure 10-1 and Figure 10-2 shows respectively the TPSM365R6 and TPSM365R3 setup in a typical application with an output voltage of 5-V with a switching frequency of 1 MHz. The nominal input voltage is 24 V. The RT pin is tied to VCC which sets the free-running switching frequency at 1 MHz.

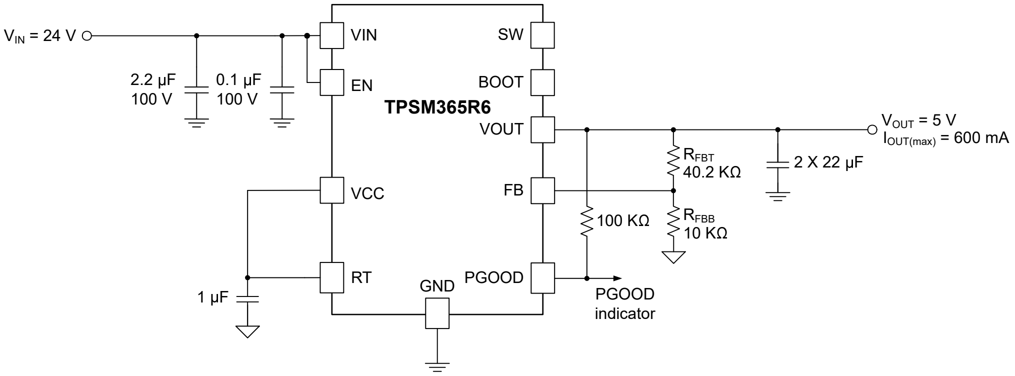


Figure 10-1. Example Application Circuit

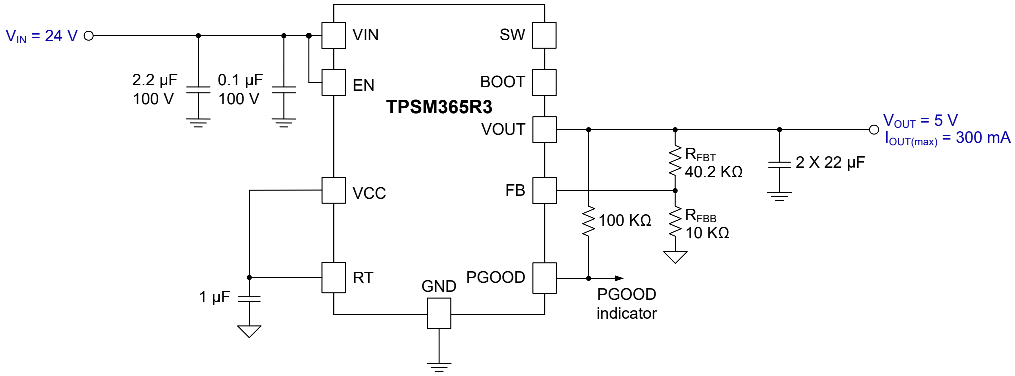


Figure 10-2. Example Application Circuit

10.2.1.1 Design Requirements

For this design example, use the parameters listed in Table 10-1 as the input parameters and follow the design procedures in *Detailed Design Procedure*.

Table 10-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage	24 V
Output voltage	5 V
Output current	0 A to 600 mA
Switching frequency	1 MHz

Table 10-2 gives the selected buck module power-stage components with availability from multiple vendors. This design uses an all-ceramic output capacitor implementation.

Table 10-2. List of Materials for Application Circuit 1

REFERENCE DESIGNATOR	QTY	SPECIFICATION	MANUFACTURER (1)	PART NUMBER
C_{IN}	1	2.2 µF, 100 V, X7R, 1210, ceramic	TDK	C3225X7R2A225K230AB
	1	100 nF, 100 V, X7R, 0603, ceramic	Murata	GRM188R72A104KA35J
C_{OUT}	2	22 µF, 25 V, X7R, 1210, ceramic	TDK	C3225X7R1E226M250AB
C_{VCC}	1	1 µF, 16 V, X7R, 0603, ceramic	TDK	C1608X7R1C105K080AC
U_1	1	TPSM365R6 65-V, 600-mA synchronous buck module	Texas Instruments	TPSM365R6FRDNR

(1) See the *Third-Party Products Disclaimer*

More generally, the TPSM365Rx module is designed to operate with a wide range of external components and system parameters. However, the integrated loop compensation is optimized for a certain range of output capacitance.

10.2.1.2 Detailed Design Procedure

10.2.1.2.1 Custom Design With WEBENCH® Tools

To create a custom design using the TPSM365Rx device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.

- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

10.2.1.2.2 Output Voltage Setpoint

The output voltage of the TPSM365Rx device is externally adjustable using a resistor divider. The recommended value of R_{FBB} is 10 kΩ. The value for R_{FBT} can be selected from Table 9-1 or calculated using Equation 10:

$$R_{FBT}[\text{k}\Omega] = R_{FBB}[\text{k}\Omega] \times \left(\frac{V_{OUT}[\text{V}]}{1\ \text{V}} - 1\right) \tag{10}$$

For the desired output voltage of 5 V, the formula yields a value of 40.2 kΩ. Choose the closest available standard value of 40.2 kΩ for R_{FBT}. Alternatively, if a fixed 3.3-V or 5-V output voltage power module variant is used, the user can connect the FB/BIAS pin directly to the output capacitor.

10.2.1.2.3 Switching Frequency Selection

The recommended switching frequency for standard output voltages can be found in Table 9-1. For a 5-V output, the recommended switching frequency is 1 MHz. To set the switching frequency to 1 MHz, connect the RT pin to VCC.

10.2.1.2.4 Input Capacitor Selection

The TPSM365Rx requires a minimum input capacitance of 1 × 2.2-μF and 1 × 0.1-μF ceramic type. High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. The voltage rating of input capacitors must be greater than the maximum input voltage.

For this design, select a 2.2-μF, 100-V, 1210 case size, and a 0.1-μF, 100-V, 0603 case size ceramic capacitors.

10.2.1.2.5 Output Capacitor Selection

For a 5-V output, the TPSM365Rx requires a minimum of 25 μF of effective output capacitance for proper operation (see Table 9-1). High-quality ceramic type capacitors with sufficient voltage and temperature rating are required. Additional output capacitance can be added to reduce ripple voltage or for applications with transient load requirements.

For this design example, select 2 × 22-μF, 25-V, 1210 case size, ceramic capacitors, which have a total effective capacitance of approximately 42 μF at 5 V.

10.2.1.2.6 VCC

The VCC pin is the output of the internal LDO used to supply the control circuits of the regulator. This output requires a 1-μF, 16-V ceramic capacitor connected from VCC to GND for proper operation. In general, this output must not be loaded with any external circuitry. However, this output can be used to supply the pullup for the power-good function (see Section 9.3.8). A value in the range of 10 kΩ to 100 kΩ is a good choice in this case. The nominal output voltage on VCC is 3.15 V; see Section 8.5 for limits.

10.2.1.2.7 C_{FF} Selection

In some cases, a feedforward capacitor can be used across R_{FBT} to improve the load transient response or improve the loop-phase margin. This is especially true when values of R_{FBT} > 100 kΩ are used. Large values of R_{FBT}, in combination with the parasitic capacitance at the FB pin, can create a small signal pole that interferes with the loop stability. A C_{FF} can help mitigate this effect. Use Equation 11 to estimate the value of C_{FF}. The value found with Equation 11 is a starting point; use lower values to determine if any advantage is gained by the use of a C_{FF} capacitor. The *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed forward Capacitor application report* is helpful when experimenting with a feedforward capacitor.

$$C_{FF} < \frac{V_{OUT} \times C_{OUT}}{120 \times R_{FBT} \times \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{11}$$

10.2.1.2.8 Power-Good Signal

Applications requiring a power good signal to indicate that the output voltage is present and in regulation must use a pullup resistor between the PGOOD pin and a valid voltage source.

For this design, a 100-kΩ resistor is placed between the PGOOD pin and the VCC pin (the internal 3.15-V LDO output).

10.2.1.2.9 Maximum Ambient Temperature

As with any power conversion module, the TPSM365Rx dissipates internal power while operating. The effect of this power dissipation is to raise the internal temperature of the power module above ambient. The internal die and inductor temperature (T_J) is a function of the ambient temperature, the power loss, and the effective thermal resistance, $R_{\theta JA}$, of the module and PCB combination. The maximum junction temperature for the TPSM365Rx must be limited to 125°C. This establishes a limit on the maximum module power dissipation and, therefore, the load current. Equation 12 shows the relationships between the important parameters. It is easy to see that larger ambient temperatures (T_A) and larger values of $R_{\theta JA}$ reduce the maximum available output current. The power module efficiency can be estimated by using the curves provided in this data sheet. If the desired operating conditions cannot be found in one of the curves, interpolation can be used to estimate the efficiency. Alternatively, the EVM can be adjusted to match the desired application requirements and the efficiency can be measured directly. The correct value of $R_{\theta JA}$ is more difficult to estimate. As stated in the *Semiconductor and IC Package Thermal Metrics application report* the values given in *Thermal Information* section are not valid for design purposes and must not be used to estimate the thermal performance of the application. The values reported in that table were measured under a specific set of conditions that are rarely obtained in an actual application.

$$I_{OUT}|_{MAX} = \frac{(T_J - T_A)}{R_{\theta JA}} \times \frac{\eta}{1-\eta} \times \frac{1}{V_{OUT}} \tag{12}$$

where

- η is the efficiency.

The effective $R_{\theta JA}$ is a critical parameter and depends on many factors such as the following:

- Power dissipation
- Air temperature/flow
- PCB area
- Copper heat-sink area
- Number of thermal vias under the package
- Adjacent component placement

As a reference, the effective $R_{\theta JA}$ on the EVM for typical 24-V V_{IN} 5-V V_{OUT} full-load condition is around 30 °C/W. Use the following resources as guides to optimal thermal PCB design and estimating $R_{\theta JA}$ for a given application environment:

- *Thermal Design by Insight not Hindsight Application Report*
- *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages Application Report*
- *Semiconductor and IC Package Thermal Metrics Application Report*
- *Thermal Design Made Simple with LM43603 and LM43602 Application Report*
- *PowerPAD™ Thermally Enhanced Package Application Report*
- *PowerPAD™ Made Easy Application Report*
- *Using New Thermal Metrics Application Report*
- *PCB Thermal Calculator*

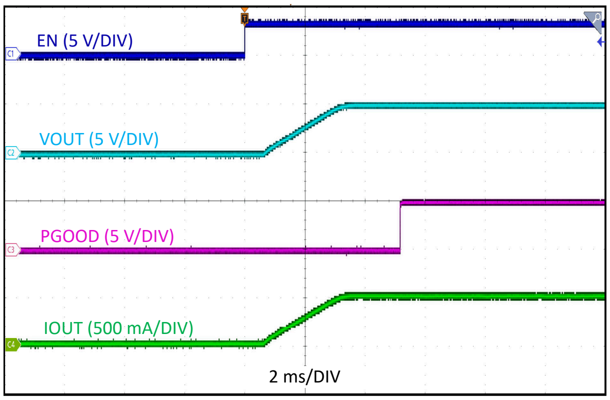
10.2.1.2.10 Other Connections

- The RT pin can be connected to AGND for a switching frequency of 2.2 MHz or tied to VCC for a switching frequency of 1 MHz. A resistor connected between the RT pin and GND can be used to set the desired operating frequency between 200 kHz and 2.2 MHz.
- For the MODE/SYNC pin variant, connecting this pin to an external clock forces the device into SYNC operation. Connecting the MODE/SYNC pin low allows the device to operate in PFM mode at light load. Connecting the MODE/SYNC pin high puts the device into FPWM mode and allows full frequency operation independent of load current.
- A resistor divider network on the EN pin can be added for a precision input undervoltage lockout (UVLO)
- For fixed output voltage variants, connect FB/BIAS pin to VOUT.
- Place a 1-µF capacitor between the VCC pin and PGND, located near to the device.

- A pullup resistor between the PGOOD pin and a valid voltage source to generate a power-good signal.

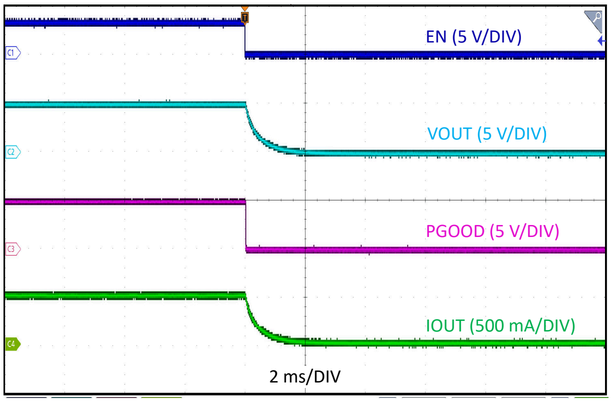
10.2.1.3 Application Curves

Unless otherwise indicated, V_{IN} = 24 V, V_{OUT} = 5 V, I_{OUT} = 0.5 A, and F_{SW} = 1 MHz



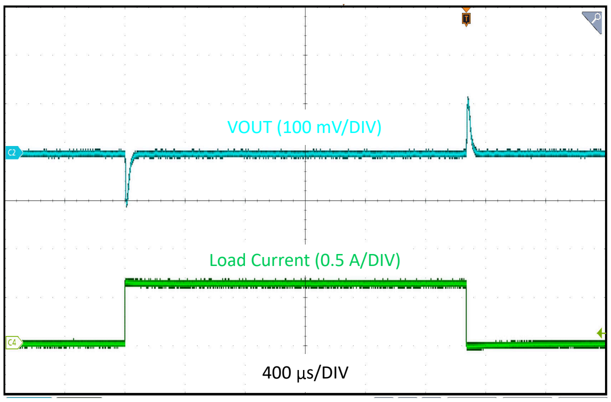
V_{IN} = 24 V V_{OUT} = 5 V

Figure 10-3. Start-Up Waveforms



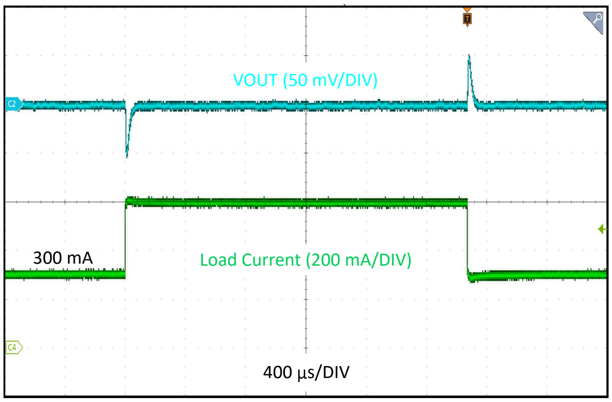
V_{IN} = 24 V V_{OUT} = 5 V

Figure 10-4. Shutdown Waveforms



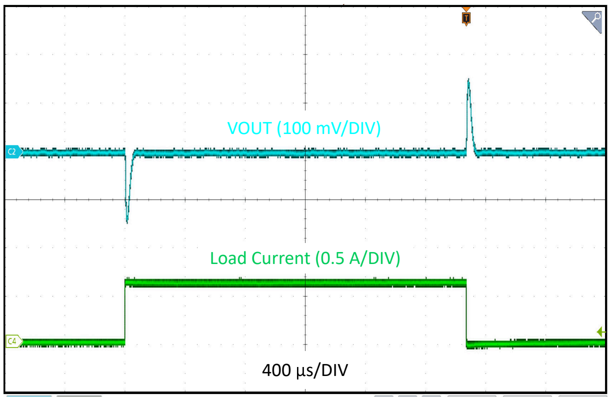
V_{IN} = 24 V V_{OUT} = 3.3 V F_{SW} = 1 MHz
C_{OUT} = 2 × 22 µF

Figure 10-5. Load Transient, 0 A to 0.6 A, 1 A/µs



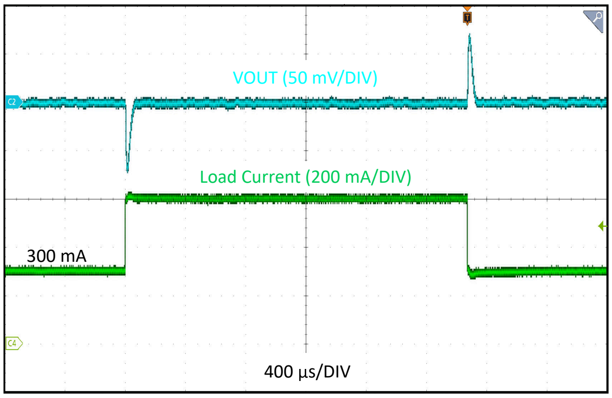
V_{IN} = 24 V V_{OUT} = 3.3 V F_{SW} = 1 MHz
C_{OUT} = 2 × 22 µF

Figure 10-6. Load Transient, 0.3 A to 0.6 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 22 µF

Figure 10-7. Load Transient, 0 A to 0.6 A, 1 A/µs



V_{IN} = 24 V V_{OUT} = 5 V F_{SW} = 1 MHz
C_{OUT} = 2 × 22 µF

Figure 10-8. Load Transient, 0.3 A to 0.6 A, 1 A/µs

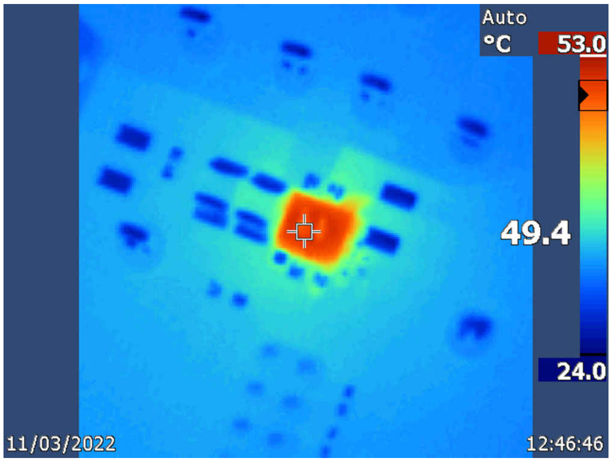


Figure 10-9. Thermal Image, V_{IN} = 24 V, V_{OUT} = 12 V, F_{SW} = 2.2 MHz, I_{OUT} = 0.6 A (Standard EVM and BOM)

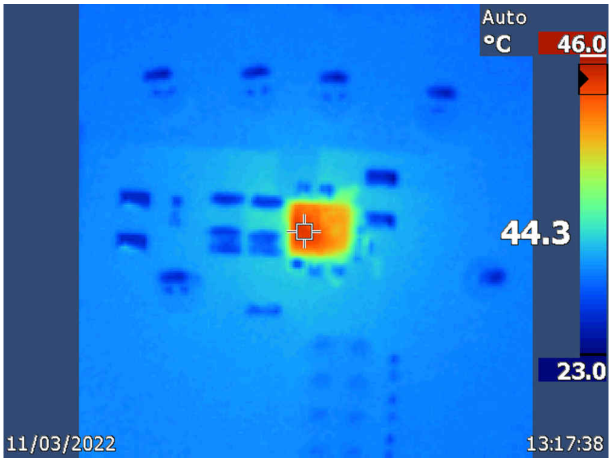


Figure 10-10. Thermal Image, V_{IN} = 24 V, V_{OUT} = 5 V, F_{SW} = 1 MHz, I_{OUT} = 0.6 A (Standard EVM and BOM)

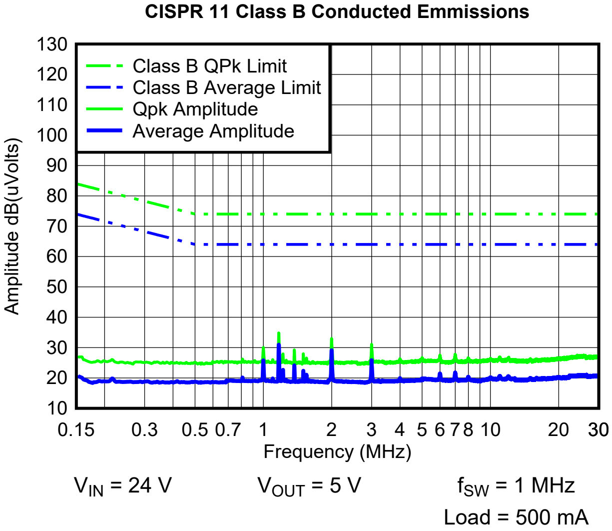


Figure 10-11. Typical CISPR 11 Class B Conducted EMI 150 kHz - 30 MHz with EMI Filter (Standard EVM Layout and BOM)

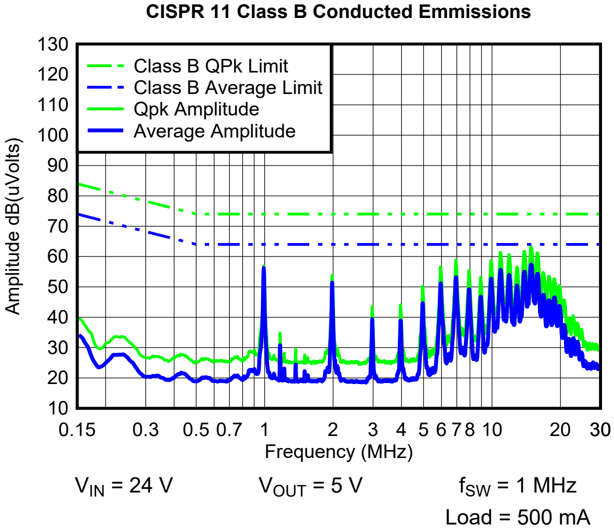
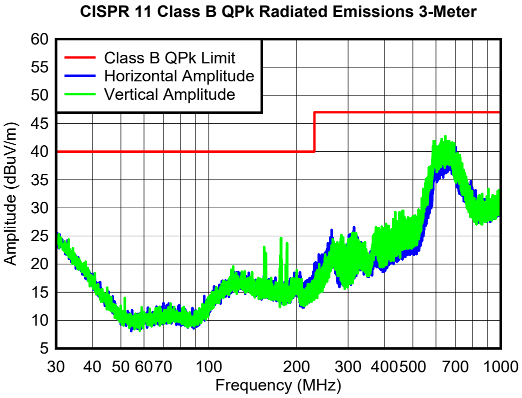


Figure 10-12. Typical CISPR 11 Class B Conducted EMI 150 kHz - 30 MHz without EMI Filter (Standard EVM Layout and BOM)



V_{IN} = 24 V

V_{OUT} = 5 V

f_{SW} = 1 MHz

Load = 500 mA

Figure 10-13. Typical CISPR 11 Class B Radiated EMI 30 kHz - 1000 MHz (Standard EVM Layout and BOM, Input Filter Removed)

10.3 Power Supply Recommendations

The TPSM365Rx buck module is designed to operate over a wide input voltage range of 3 V to 65 V. The characteristics of the input supply must be compatible with the *Absolute Maximum Ratings* and *Recommended Operating Conditions* in this data sheet. In addition, the input supply must be capable of delivering the required input current to the loaded regulator circuit. Estimate the average input current with Equation 13.

$$I_{IN} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta} \tag{13}$$

where

- η is the efficiency

If the module is connected to an input supply through long wires or PCB traces with a large impedance, take special care to achieve stable performance. The parasitic inductance and resistance of the input cables can have an adverse affect on module operation. More specifically, the parasitic inductance in combination with the low-ESR ceramic input capacitors form an underdamped resonant circuit, possibly resulting in instability, voltage transients, or both, each time the input supply is cycled ON and OFF. The parasitic resistance causes the input voltage to dip during a load transient. If the module is operating close to the minimum input voltage, this dip can cause false UVLO triggering and a system reset.

The best way to solve such issues is to reduce the distance from the input supply to the module and use an electrolytic input capacitor in parallel with the ceramics. The moderate ESR of the electrolytic capacitor helps damp the input resonant circuit and reduce any overshoot or undershoot at the input. A capacitance in the range of 47 µF to 100 µF is usually sufficient to provide input parallel damping and helps hold the input voltage steady during large load transients. A typical ESR of 0.1 Ω to 0.4 Ω provides enough damping for most input circuit configurations.

10.4 Layout

The performance of any switching power supply depends as much upon the layout of the PCB as the component selection. Use the following guidelines to design a PCB with the best power conversion performance, optimal thermal performance, and minimal generation of unwanted EMI.

10.4.1 Layout Guidelines

The PCB layout of any DC/DC module is critical to the optimal performance of the design. Poor PCB layout can disrupt the operation of an otherwise good schematic design. Even if the module regulates correctly, bad PCB layout can mean the difference between a robust design and one that cannot be mass produced. Furthermore, to a great extent, the EMI performance of the regulator is dependent on the PCB layout. In a buck converter module, the most critical PCB feature is the loop formed by the input capacitor or capacitors and power ground, as shown in Figure 10-14. This loop carries large transient currents that can cause large transient voltages when reacting with the trace inductance. These unwanted transient voltages disrupt the proper operation of the power module. Because of this, the traces in this loop must be wide and short, and the loop area as small as possible to reduce the parasitic inductance. Figure 10-15 shows a recommended layout for the critical components of the TPSM365Rx.

1. *Place the input capacitors as close as possible to the VIN and GND terminals.* VIN and GND pins are adjacent, simplifying the input capacitor placement.
2. *Place bypass capacitor for VCC close to the VCC pin.* This capacitor must be placed close to the device and routed with short, wide traces to the VCC and GND pins.
3. *Place the feedback divider as close as possible to the FB pin of the device.* Place R_{FBB}, R_{FBT}, and C_{FF}, if used, physically close to the device. The connections to FB and GND must be short and close to those pins on the device. The connection to V_{OUT} can be somewhat longer. However, the latter trace must not be routed near any noise source (such as the SW node) that can capacitively couple into the feedback path of the regulator.
4. *Use at least one ground plane in one of the middle layers.* This plane acts as a noise shield and as a heat dissipation path.

5. *Provide wide paths for VIN, VOUT, and GND.* Making these paths as wide and direct as possible reduces any voltage drops on the input or output paths of the power module and maximizes efficiency.
6. *Provide enough PCB area for proper heat-sinking.* Sufficient amount of copper area must be used to ensure a low $R_{\theta JA}$, commensurate with the maximum load current and ambient temperature. The top and bottom PCB layers must be made with two ounce copper and no less than one ounce. If the PCB design uses multiple copper layers (recommended), these thermal vias can also be connected to the inner layer heat-spreading ground planes.
7. *Use multiple vias* to connect the power planes to internal layers.

See the following PCB layout resources for additional important guidelines:

- *Layout Guidelines for Switching Power Supplies Application Report*
- *Simple Switcher PCB Layout Guidelines Application Report*
- *Construction Your Power Supply- Layout Considerations Seminar*
- *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x Application Report*

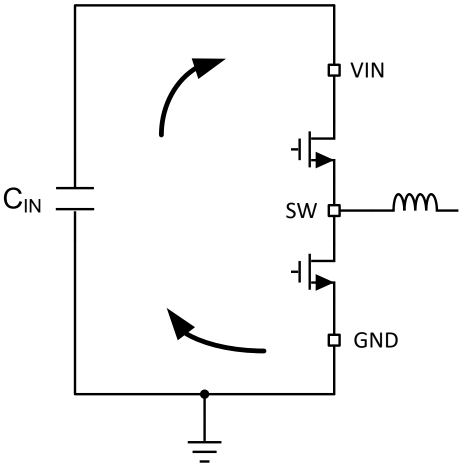


Figure 10-14. Current Loops with Fast Edges

10.4.1.1 Ground and Thermal Considerations

As previously mentioned, TI recommends using one of the middle layers as a solid ground plane. A ground plane provides shielding for sensitive circuits and traces as well as a quiet reference potential for the control circuitry. Connect the GND pin to the ground planes using vias next to the bypass capacitors. The GND trace, as well as the VIN and SW traces, must be constrained to one side of the ground planes. The other side of the ground plane contains much less noise; use for sensitive routes.

TI recommends providing adequate device heat-sinking by having enough copper near the GND pin. See Figure 10-15 for example layout. Use as much copper as possible, for system ground plane, on the top and bottom layers for the best heat dissipation. Use a four-layer board with the copper thickness for the four layers, starting from the top as: 2 oz / 1 oz / 1 oz / 2 oz. A four-layer board with enough copper thickness, and proper layout, provides low current conduction impedance, proper shielding and lower thermal resistance.

10.4.2 Layout Example

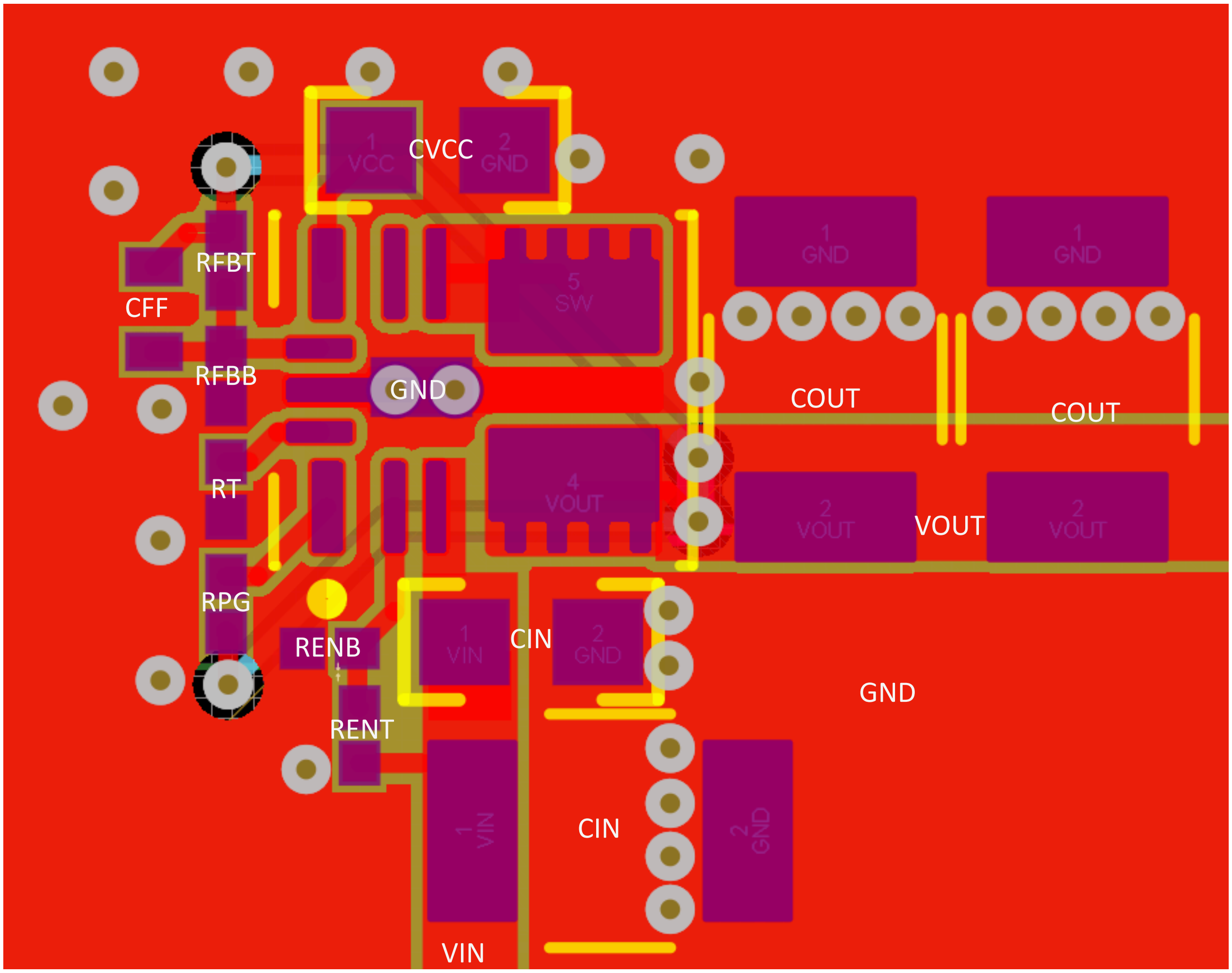


Figure 10-15. Example Layout

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

11.1.2 Device Nomenclature

Figure 11-1 shows the device naming nomenclature of the TPSM365Rx. See Section 6 for the availability of each variant. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options; minimum order quantities apply.

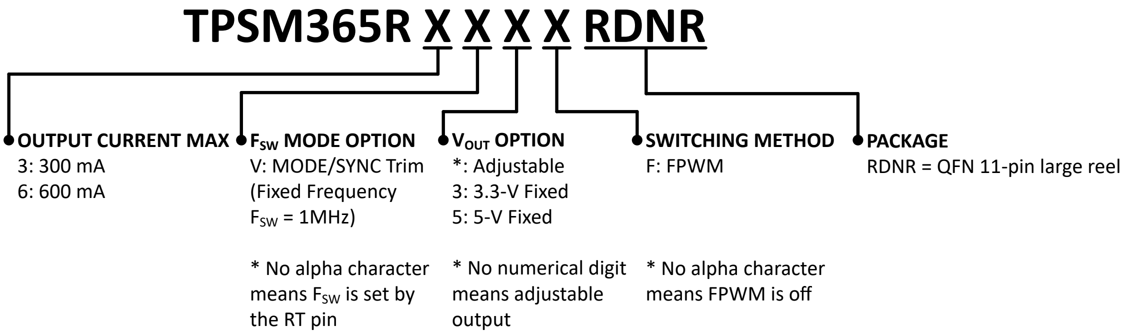


Figure 11-1. Device Naming Nomenclature

11.1.3 Development Support

11.1.3.1 Custom Design With WEBENCH® Tools

To create a custom design using the TPSM365R3 device with the WEBENCH Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance.
- Run thermal simulations to understand board thermal performance.
- Export customized schematic and layout into popular CAD formats.
- Print PDF reports for the design, and share the design with colleagues.

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Innovative DC/DC Power Modules* selection guide
- Texas Instruments, *Enabling Small, Cool and Quiet Power Modules with Enhanced HotRod™ QFN Package Technology* white paper
- Texas Instruments, *Benefits and Trade-offs of Various Power-Module Package Options* white paper
- Texas Instruments, *Simplify Low EMI Design with Power Modules* white paper

- Texas Instruments, *Power Modules for Lab Instrumentation* white paper
- Texas Instruments, *An Engineer's Guide To EMI In DC/DC Regulators* e-book
- Texas Instruments, *Soldering Considerations for Power Modules* application report
- Texas Instruments, *Practical Thermal Design With DC/DC Power Modules* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *Thermal Design by Insight not Hindsight* application report
- Texas Instruments, *A Guide to Board Layout for Best Thermal Resistance for Exposed Pad Packages* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *Thermal Design Made Simple with LM43603 and LM43602* application report
- Texas Instruments, *PowerPAD™ Thermally Enhanced Package* application report
- Texas Instruments, *PowerPAD™ Made Easy* application report
- Texas Instruments, *Using New Thermal Metrics* application report
- Texas Instruments, *PCB Thermal Calculator*
- Texas Instruments, *Layout Guidelines for Switching Power Supplies* application report
- Texas Instruments, *Simple Switcher PCB Layout Guidelines* application report
- Texas Instruments, *Construction Your Power Supply- Layout Considerations Seminar*
- Texas Instruments, *Low Radiated EMI Layout Made Simple with LM4360x and LM4600x* application report
- Texas Instruments, *TPSM365R6EVM User's Guide*
- Texas Instruments, *AN-2020 Thermal Design By Insight, Not Hindsight* application report
- *Optimizing Transient Response of Internally Compensated DC-DC Converters with Feed forward Capacitor* application report

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

11.5 Trademarks

HotRod™, PowerPAD™, and TI E2E™ are trademarks of Texas Instruments.
All trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPSM365R3FRDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R3F
TPSM365R3FRDNR.Z	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R3F
TPSM365R3RDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R3
TPSM365R3RDNR.Z	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R3
TPSM365R6FRDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R6F
TPSM365R6FRDNR.Z	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R6F
TPSM365R6RDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R6
TPSM365R6RDNR.Z	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R6
TPSM365R6V3RDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R6V3
TPSM365R6V3RDNR.Z	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R6V3
TPSM365R6V5RDNR	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R6V5
TPSM365R6V5RDNR.Z	Active	Production	QFN-FCMOD (RDN) | 11	3000 | LARGE T&R	Yes	SN	Level-3-260C-168 HR	-40 to 125	365R6V5

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

[4] **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

[5] **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

[6] **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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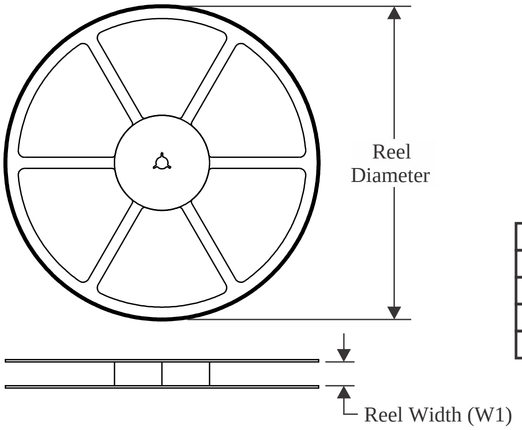
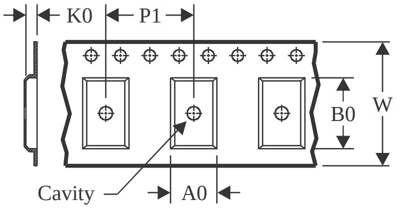
TAPE AND REEL INFORMATION

REEL DIMENSIONS

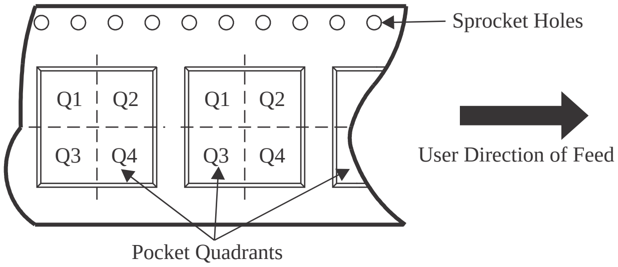


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

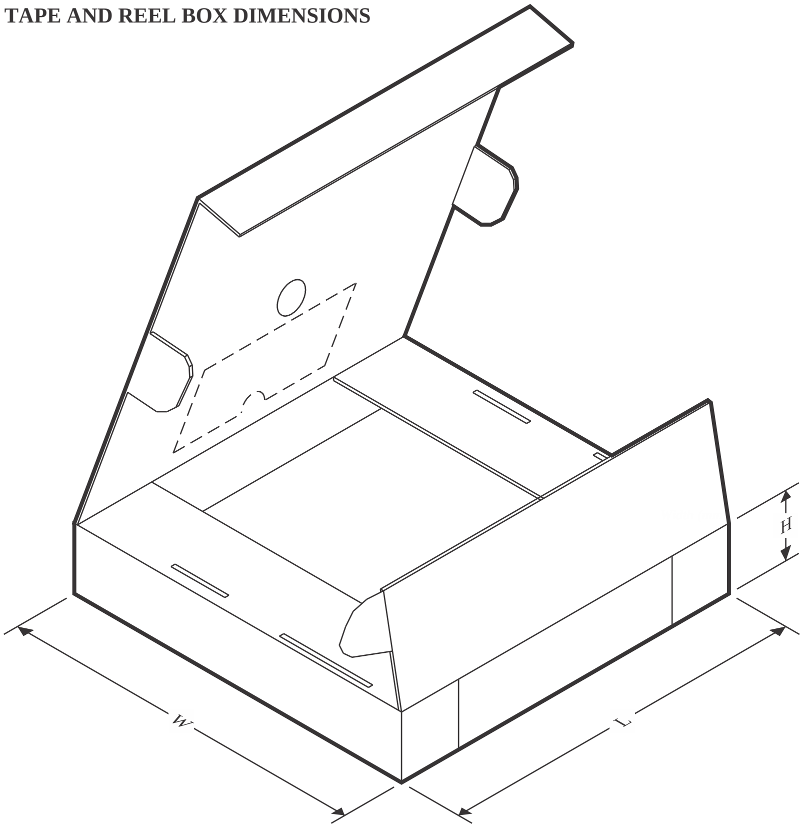
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

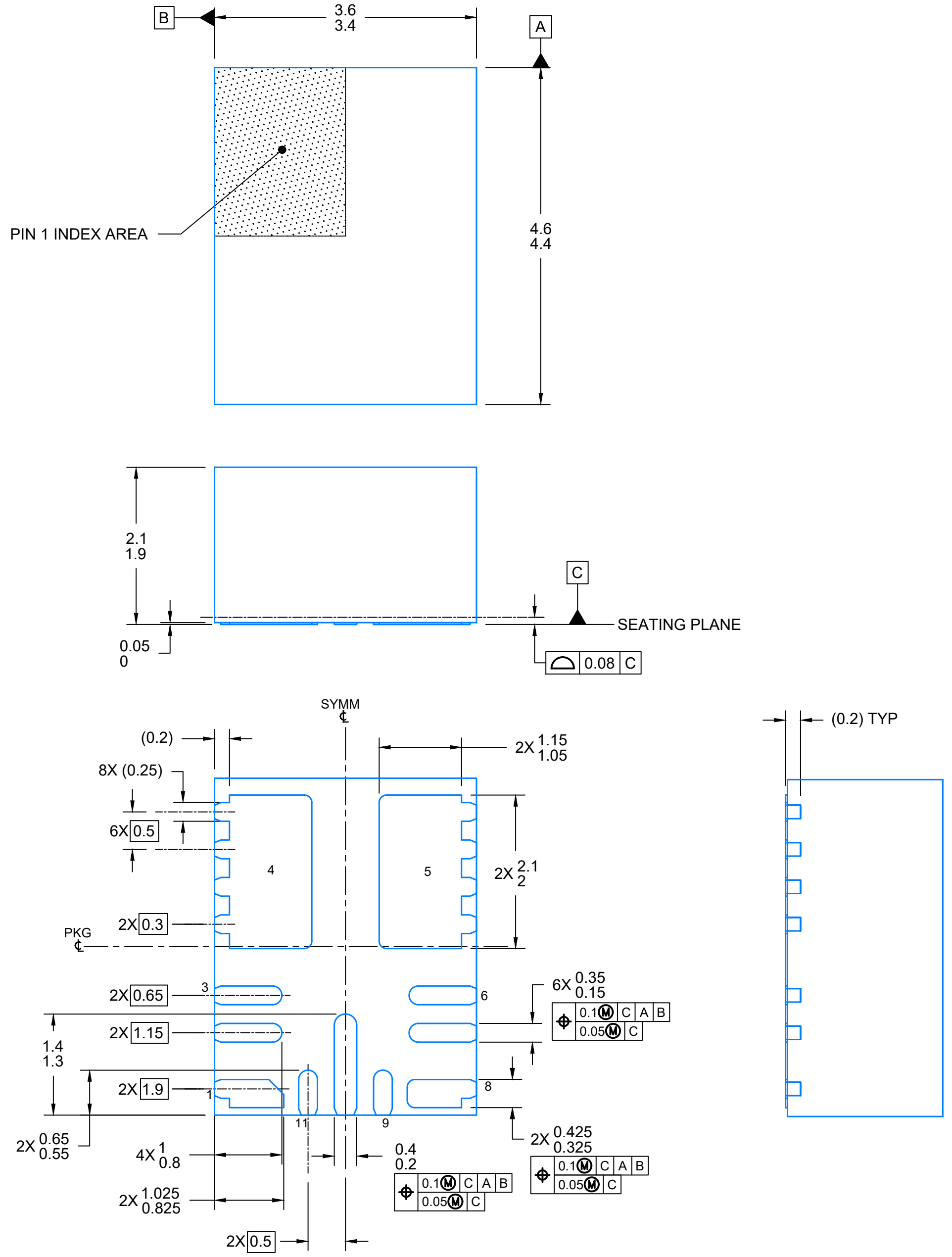
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPSM365R3FRDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1
TPSM365R3RDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1
TPSM365R6FRDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1
TPSM365R6RDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1
TPSM365R6V3RDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1
TPSM365R6V5RDNR	QFN-FCMOD	RDN	11	3000	330.0	17.6	3.8	4.8	2.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPSM365R3FRDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0
TPSM365R3RDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0
TPSM365R6FRDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0
TPSM365R6RDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0
TPSM365R6V3RDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0
TPSM365R6V5RDNR	QFN-FCMOD	RDN	11	3000	336.0	336.0	48.0



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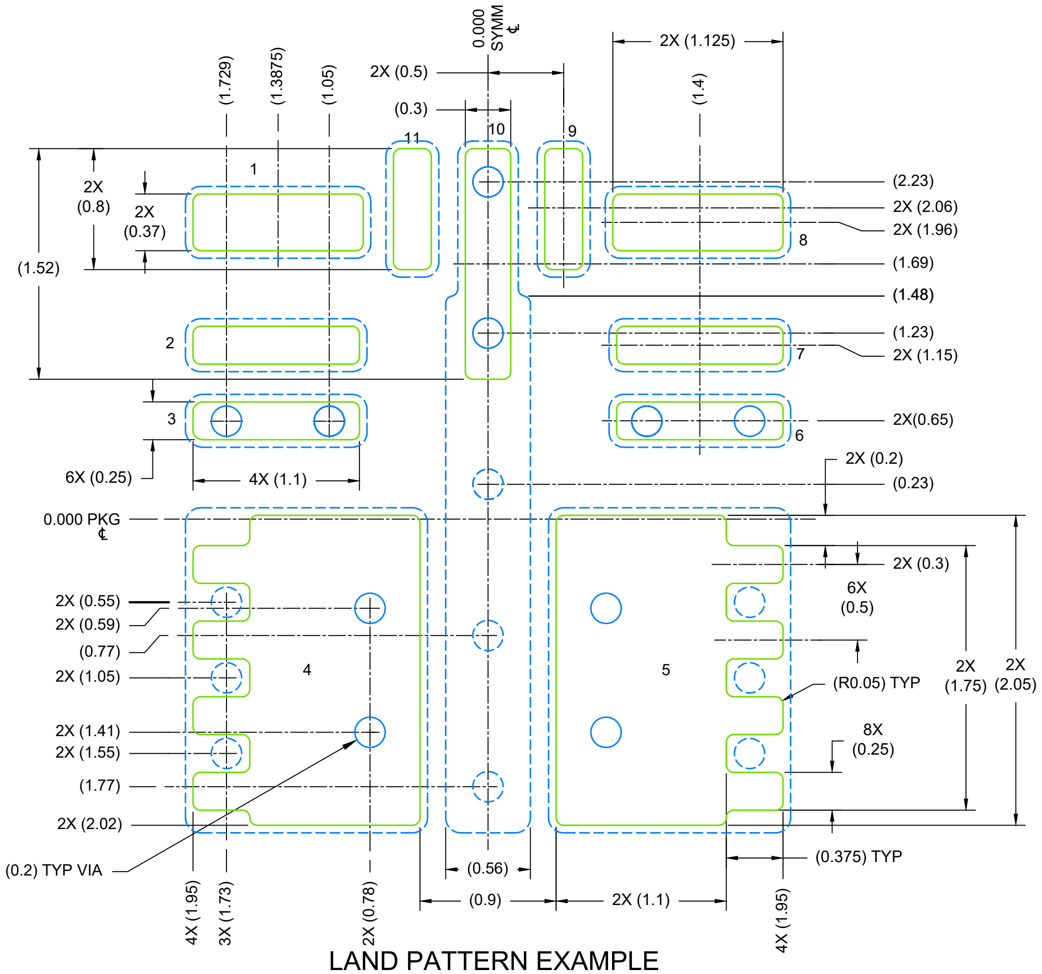
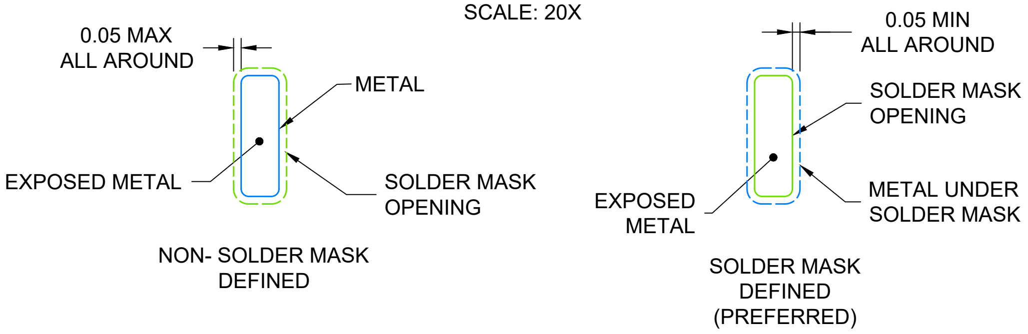
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



NON- SOLDER MASK
DEFINED

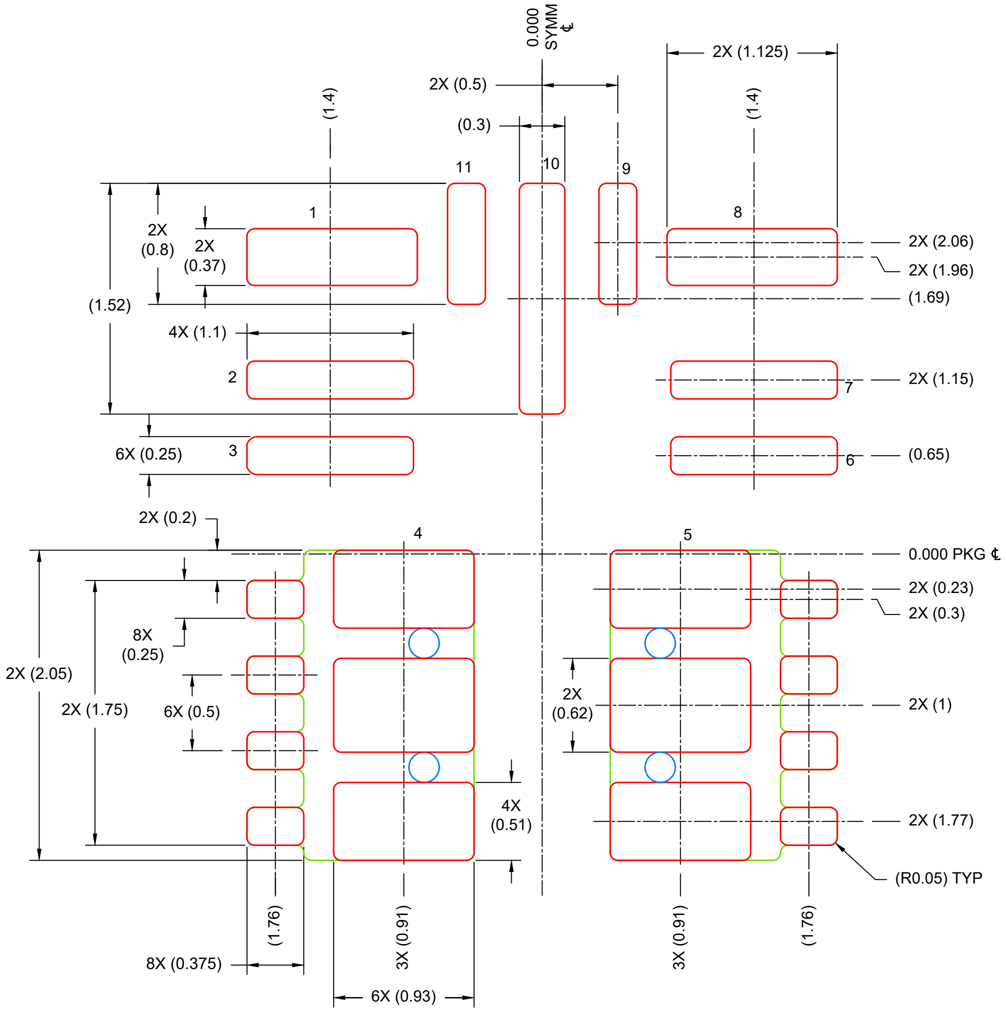
SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK DETAILS

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).

5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

PIN 4 & 5:
72% SOLDER COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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