ADC121S101x Single-Channel, 0.5 to 1-Msps, 12-Bit Analog-to-Digital Converter

1 Features
- Specified Over a Range of Sample Rates
- 6-Pin WSON and SOT-23 Packages
- Variable Power Management
- Single Power Supply With 2.7 V to 5.25 V Range
- SPI™, QSPI™, MICROWIRE, and DSP Compatible
- AEC-Q100 Grade 1 Qualified
- DNL: +0.5 / −0.3 LSB (Typical)
- INL: ±0.40 LSB (Typical)
- Power Consumption:
  - 3-V Supply: 2 mW (Typical)
  - 5-V Supply: 10 mW (Typical)

2 Applications
- Portable Systems
- Remote Data Acquisition
- Instrumentation and Control Systems
- Automotive

3 Description
The ADC121S101 is a low-power, single-channel CMOS 12-bit analog-to-digital converter with a high-speed serial interface. Unlike the conventional practice of specifying performance at a single sample rate only, the ADC121S101 is fully specified over a sample rate range of 500 ksps to 1 Msps. The converter is based upon a successive-approximation register architecture with an internal track-and-hold circuit.

The output serial data is straight binary, and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces.

The ADC121S101 operates with a single supply with a range from 2.7 V to 5.25 V. Normal power consumption using a 3 V or 5 V supply is 2 mW and 10 mW, respectively. The power-down feature reduces the power consumption to as low as 2.6 µW using a 5-V supply.

The ADC121S101 is packaged in 6-pin WSON and SOT-23 packages. Operation over the temperature range of −40°C to 125°C is specified.

Device Information (1)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC121S101</td>
<td>WSON (6)</td>
<td>2.50 mm × 2.20 mm</td>
</tr>
<tr>
<td></td>
<td>SOT-23 (6)</td>
<td>2.90 mm × 1.60 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.
Table of Contents

1 Features ................................................................. 1
2 Applications .......................................................... 1
3 Description .............................................................. 1
4 Revision History ....................................................... 2
5 Device Comparison Table ............................................. 3
6 Pin Configuration and Functions ................................. 3
7 Specifications .......................................................... 4
   7.1 Absolute Maximum Ratings ................................. 4
   7.2 ESD Ratings: ADC121S101 .................................. 4
   7.3 ESD Ratings: ADC121S101-Q1 ............................ 4
   7.4 Recommended Operating Conditions ..................... 4
   7.5 Thermal Information .......................................... 5
   7.6 Electrical Characteristics ................................... 5
   7.7 Timing Requirements ......................................... 7
   7.8 Typical Characteristics ....................................... 9
8 Detailed Description .................................................. 12
   8.1 Overview .......................................................... 12
   8.2 Functional Block Diagram .................................... 13
9 Application and Implementation ................................ 17
   9.1 Application Information ......................................... 17
   9.2 Typical Application ........................................... 17
10 Power Supply Recommendations ................................. 19
   10.1 Power Management ........................................... 19
   10.2 Power Supply Noise Considerations .................... 19
11 Layout ...................................................................... 20
   11.1 Layout Guidelines ............................................. 20
   11.2 Layout Example ................................................. 20
12 Device and Documentation Support ............................ 21
   12.1 Device Support ................................................ 21
   12.2 Community Resources ....................................... 22
   12.3 Trademarks ...................................................... 22
   12.4 Electrostatic Discharge Caution ........................... 22
   12.5 Glossary .......................................................... 22
13 Mechanical, Packaging, and Orderable Information ....... 22

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision G (January 2014) to Revision H Page

• Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1

Changes from Revision F (May 2013) to Revision G Page

• Changed sentence in the Using the ADC121S101 section ......................................................... 13

Changes from Revision E (May 2013) to Revision F Page

• Changed layout of National Data Sheet to TI format ................................................................. 1
5 Device Comparison Table

<table>
<thead>
<tr>
<th>RESOLUTION</th>
<th>SPECIFIED SAMPLE RATE RANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>50 TO 200 KSPS</td>
</tr>
<tr>
<td>12 Bits</td>
<td>ADC121S021</td>
</tr>
<tr>
<td>10 Bits</td>
<td>ADC101S021</td>
</tr>
<tr>
<td>8 Bits</td>
<td>ADC081S021</td>
</tr>
</tbody>
</table>

(1) All devices are fully pin and function compatible.

6 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN NO.</th>
<th>PIN NAME</th>
<th>TYPE(1)</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_A</td>
<td>P</td>
<td>Positive supply pin. This pin must be connected to a quiet 2.7-V to 5.25-V source and bypassed to GND with a 1-µF capacitor and a 0.1-µF monolithic capacitor located within 1 cm of the power pin.</td>
</tr>
<tr>
<td>2</td>
<td>GND</td>
<td>G</td>
<td>The ground return for the supply and signals.</td>
</tr>
<tr>
<td>3</td>
<td>V_IN</td>
<td>I</td>
<td>Analog input. This signal can range from 0 V to V_A.</td>
</tr>
<tr>
<td>4</td>
<td>SCLK</td>
<td>I</td>
<td>Digital clock input. This clock directly controls the conversion and readout processes.</td>
</tr>
<tr>
<td>5</td>
<td>SDATA</td>
<td>O</td>
<td>Digital data output. The output samples are clocked out of this pin on falling edges of the SCLK pin.</td>
</tr>
<tr>
<td>6</td>
<td>CS</td>
<td>I</td>
<td>Chip select. On the falling edge of CS, a conversion process begins.</td>
</tr>
<tr>
<td>PAD</td>
<td>GND</td>
<td>G</td>
<td>For package suffix CISD(X) only. TI recommends connecting the center pad to ground.</td>
</tr>
</tbody>
</table>

(1) G = Ground, I = Input, O = Output, P = Power
7 Specifications

7.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)(1)(2)(3)

<table>
<thead>
<tr>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog supply voltage, $V_A$</td>
<td>–0.3</td>
<td>6.5</td>
</tr>
<tr>
<td>Voltage on any digital pin to GND</td>
<td>–0.3</td>
<td>6.5</td>
</tr>
<tr>
<td>Voltage on any analog pin to GND</td>
<td>–0.3</td>
<td>$V_A + 0.3$</td>
</tr>
<tr>
<td>Input current at any pin(4)</td>
<td>±10</td>
<td>mA</td>
</tr>
<tr>
<td>Package input current(4)</td>
<td>±20</td>
<td>mA</td>
</tr>
<tr>
<td>Power consumption at $T_A = 25^\circ C$</td>
<td>See(5)</td>
<td></td>
</tr>
<tr>
<td>Junction temperature, $T_J$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature, $T_{stg}$</td>
<td>–65</td>
<td>150</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltages are measured with respect to GND = 0 V (unless otherwise specified).

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(4) When the input voltage at any pin exceeds the power supply (that is, $V_{IN} < GND$ or $V_{IN} > V_A$), the current at that pin must be limited to 10 mA. The 20 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to two. The Absolute Maximum Ratings do not apply to the $V_A$ pin. The current into the $V_A$ pin is limited by the Analog Supply Voltage specification.

(5) The absolute maximum junction temperature ($T_{J\text{max}}$) for this device is 150°C. The maximum allowable power dissipation is dictated by $T_{J\text{max}}$, the junction-to-ambient thermal resistance ($\theta_{JA}$), and the ambient temperature ($T_A$), and can be calculated using the formula $P_{D\text{max}} = (T_{J\text{max}} - T_A) / \theta_{JA}$. The values for maximum power dissipation listed above will be reached only when the device is operated in a severe fault condition (that is, when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions must always be avoided.

7.2 ESD Ratings: ADC121S101

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±3500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

7.3 ESD Ratings: ADC121S101-Q1

<table>
<thead>
<tr>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>±3500</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.4 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>MIN</th>
<th>NOM</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_A$</td>
<td>Supply voltage</td>
<td>2.7</td>
<td>5.25</td>
</tr>
<tr>
<td>Digital input pins voltage (regardless of supply voltage)</td>
<td>–0.3</td>
<td>5.25</td>
<td>V</td>
</tr>
<tr>
<td>Analog input pins voltage</td>
<td>0</td>
<td>$V_A$</td>
<td>V</td>
</tr>
<tr>
<td>Clock frequency</td>
<td>25</td>
<td>20000</td>
<td>kHz</td>
</tr>
<tr>
<td>Sample rate</td>
<td>Up to 1 Msps</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$T_A$</td>
<td>Operating temperature</td>
<td>–40</td>
<td>125</td>
</tr>
</tbody>
</table>

(1) All voltages are measured with respect to GND = 0 V (unless otherwise specified).
## 7.5 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(1)</th>
<th>ADC121S101</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>NGF (WSON)</td>
<td>6 PINS</td>
</tr>
<tr>
<td>Junction-to-ambient thermal resistance</td>
<td>94</td>
<td>69</td>
</tr>
<tr>
<td>Junction-to-case (top) thermal resistance</td>
<td>118</td>
<td>69</td>
</tr>
<tr>
<td>Junction-to-board thermal resistance</td>
<td>69</td>
<td>69</td>
</tr>
<tr>
<td>Junction-to-top characterization parameter</td>
<td>6.5</td>
<td>N/A</td>
</tr>
<tr>
<td>Junction-to-board characterization parameter</td>
<td>69</td>
<td>N/A</td>
</tr>
<tr>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>15</td>
<td>N/A</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.

## 7.6 Electrical Characteristics

$V_A = 2.7 \text{ V to } 5.25 \text{ V}, \ GND = 0 \text{ V}, f_{SCLK} = 10 \text{ MHz to } 20 \text{ MHz}, \ C_L = 15 \text{ pF}, f_{SAMPLE} = 500 \text{ kspst to } 1 \text{ Msps, and } T_A = 25^\circ \text{C}$ (unless otherwise noted)(1)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(2)</th>
<th>TYP</th>
<th>MAX(2)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution with no missing codes</td>
<td>$V_A = 2.7 \text{ V to } 3.6 \text{ V}, -40^\circ \text{C} \leq T_A \leq 125^\circ \text{C}$</td>
<td>12</td>
<td>12</td>
<td>12</td>
<td>Bits</td>
</tr>
<tr>
<td>INL</td>
<td>$-40^\circ \text{C} \leq T_A \leq 85^\circ \text{C}, \ V_A = 2.7 \text{ V to } 3.6 \text{ V}$</td>
<td>-1</td>
<td>±0.4</td>
<td>1</td>
<td>LSB</td>
</tr>
<tr>
<td>DNL</td>
<td>$-40^\circ \text{C} \leq T_A \leq 85^\circ \text{C}, \ V_A = 2.7 \text{ V to } 3.6 \text{ V}$</td>
<td>0.5</td>
<td>±0.1</td>
<td>1</td>
<td>LSB</td>
</tr>
<tr>
<td>$V_{OFF}$</td>
<td>Offset error</td>
<td>$-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C}, \ V_A = 2.7 \text{ V to } 3.6 \text{ V}$</td>
<td>-1.2</td>
<td>±0.1</td>
<td>1.2</td>
</tr>
<tr>
<td>$GE$</td>
<td>Gain error</td>
<td>$-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C}, \ V_A = 2.7 \text{ V to } 3.6 \text{ V}$</td>
<td>-1.2</td>
<td>±0.2</td>
<td>1.2</td>
</tr>
</tbody>
</table>

### DYNAMIC CONVERTER

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(2)</th>
<th>TYP</th>
<th>MAX(2)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>Signal-to-noise plus distortion ratio</td>
<td>$V_A = 2.7 \text{ V to } 5.25 \text{ V}, -40^\circ \text{C} \leq T_A \leq 125^\circ \text{C}$</td>
<td>70</td>
<td>72</td>
<td>dB</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-noise ratio</td>
<td>$V_A = 2.7 \text{ V to } 5.25 \text{ V}, -40^\circ \text{C} \leq T_A \leq 125^\circ \text{C}$</td>
<td>70.8</td>
<td>72.5</td>
<td>dB</td>
</tr>
<tr>
<td>THD</td>
<td>Total harmonic distortion</td>
<td>$V_A = 2.7 \text{ V to } 5.25 \text{ V}, f_{IN} = 100 \text{ kHz}, -0.02 \text{ dBFs}$</td>
<td>-80</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious-free dynamic range</td>
<td>$V_A = 2.7 \text{ V to } 5.25 \text{ V}, f_{IN} = 100 \text{ kHz}, -0.02 \text{ dBFs}$</td>
<td>82</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective number of bits</td>
<td>$V_A = 2.7 \text{ V to } 5.25 \text{ V}, f_{IN} = 100 \text{ kHz}, -0.02 \text{ dBFs}$</td>
<td>11.3</td>
<td>11.6</td>
<td>Bits</td>
</tr>
<tr>
<td>IMD</td>
<td>Intermodulation distortion, second order terms</td>
<td>$V_A = 5.25 \text{ V}, f_a = 103.5 \text{ kHz}, f_b = 113.5 \text{ kHz}$</td>
<td>-78</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>IMD</td>
<td>Intermodulation distortion, third order terms</td>
<td>$V_A = 5.25 \text{ V}, f_a = 103.5 \text{ kHz}, f_b = 113.5 \text{ kHz}$</td>
<td>-78</td>
<td>dB</td>
<td></td>
</tr>
<tr>
<td>FPBW</td>
<td>–3 dB full power bandwidth</td>
<td>$V_A = 5 \text{ V}$</td>
<td>11</td>
<td>MHz</td>
<td></td>
</tr>
</tbody>
</table>

(1) Tested limits are guaranteed to TI's AOQL (Average Outgoing Quality Level).
(2) Data sheet minimum and maximum specification limits are guaranteed by design, test, or statistical analysis.
Electrical Characteristics (continued)

\( V_A = 2.7 \) V to 5.25 V, GND = 0 V, \( f_{SCLK} = 10 \) MHz to 20 MHz, \( C_L = 15 \) pF, \( f_{SAMPLE} = 500 \) ksp to 1 Msps, and \( T_A = 25^\circ \)C (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN(^{(2)})</th>
<th>TYP</th>
<th>MAX(^{(2)})</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( V_{IN} )</td>
<td>Input range</td>
<td>0 to ( V_A )</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{DQC} )</td>
<td>DC leakage current</td>
<td>(-40^\circ )C ≤ ( T_A ) ≤ 125°C</td>
<td>–1</td>
<td>1</td>
<td>( \mu A )</td>
</tr>
<tr>
<td>( C_{IN} )</td>
<td>Input capacitance</td>
<td>Track mode</td>
<td>30</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Hold mode</td>
<td></td>
<td>4</td>
<td>pF</td>
</tr>
</tbody>
</table>

**DIGITAL INPUT**

| \( V_{IH} \) | Input high voltage | \( V_A = 5.25 \) V, \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 2.4 | | V |
| | | \( V_A = 3.6 \) V, \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 2.1 | | |
| \( V_{IL} \) | Input low voltage | \( V_A = 5 \) V, \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 0.8 | | V |
| | | \( V_A = 3 \) V, \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 0.4 | | |
| \( I_{IN} \) | Input current | \( V_{IN} = 0 \) V or \( V_A \), \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | –1 | ±0.1 | 1 | \( \mu A \) |
| \( C_{IND} \) | Digital input capacitance | \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 2 | 4 | pF |

**DIGITAL OUTPUT**

| \( V_{OH} \) | Output high voltage | \( I_{SOURCE} = 200 \) \( \mu A \), \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | \( V_A - 0.2 \) | \( V_A - 0.07 \) | V |
| | | \( I_{SOURCE} = 1 \) mA | \( V_A - 0.1 \) | | |
| \( V_{OL} \) | Output low voltage | \( I_{SINK} = 200 \) \( \mu A \), \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 0.03 | 0.4 | V |
| | | \( I_{SINK} = 1 \) mA | 0.1 | | |
| \( I_{OZH}, I_{OZL} \) | TRI-STATE leakage current | \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | –10 | ±0.1 | 10 | \( \mu A \) |
| \( C_{OUT} \) | TRI-STATE output capacitance | \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 2 | 4 | pF |
| | | Output coding | Straight (natural) binary | | |

**POWER SUPPLY**

| \( V_A \) | Supply voltage | \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 2.7 | 5.25 | V |
| \( I_A \) | Supply current, normal mode (operational, CS low) | \( V_A = 5.25 \) V, \( f_{SAMPLE} = 1 \) Msps, \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 2.0 | 3.2 | mA |
| | | \( V_A = 3.6 \) V, \( f_{SAMPLE} = 1 \) Msps, \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 0.6 | 1.5 | |
| | | Supply current, shutdown (CS high) | \( f_{SCLK} = 0 \) MHz, \( V_A = 5 \) V, \( f_{SAMPLE} = 0 \) ksp | 500 | | nA |
| | | | \( f_{SCLK} = 20 \) MHz, \( V_A = 5 \) V, \( f_{SAMPLE} = 0 \) ksp | 60 | | \( \mu A \) |
| \( P_D \) | Power consumption, normal mode (operational, CS low) | \( V_A = 5 \) V, \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 10 | 16 | mW |
| | | \( V_A = 3 \) V, \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 2.0 | 4.5 | |
| | | Power consumption, shutdown (CS high) | \( f_{SCLK} = 0 \) MHz, \( V_A = 5 \) V, \( f_{SAMPLE} = 0 \) ksp | 2.5 | | \( \mu W \) |
| | | | \( f_{SCLK} = 20 \) MHz, \( V_A = 5 \) V, \( f_{SAMPLE} = 0 \) ksp | 300 | | |

**AC**

| \( f_{SCLK} \) | Clock frequency\(^{(3)}\) | \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C\(^{(4)}\) | 10 | 20 | MHz |
| \( f_S \) | Sample rate | \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C\(^{(4)}\) | 500 | 1000 | ksp |
| \( DC \) | SCLK duty cycle | \( f_{SCLK} = 20 \) MHz, \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 40% | 50% | 60% |
| \( t_{ACQ} \) | Minimum time required for acquisition | \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C | 350 | | ns |
| \( t_{QUIET} \) | Quiet time | \(-40^\circ \)C ≤ \( T_A \) ≤ 125°C\(^{(5)}\) | 50 | | ns |
| \( t_{AD} \) | Aperture delay | 3 | | ns |
| \( t_{AJ} \) | Aperture jitter | 30 | | ps |

\(^{(3)}\) This condition is for \( f_{SCLK} = 20 \) MHz.

\(^{(4)}\) This is the frequency range over which the electrical performance is guaranteed. The device is functional over a wider range which is specified under Operating Ratings.

\(^{(5)}\) Minimum quiet time required by bus relinquish and the start of the next conversion.
7.7 Timing Requirements

\( V_A = 2.7 \text{ V} \) to \( 5.25 \text{ V} \), \( GND = 0 \text{ V} \), \( f_{SCLK} = 10 \text{ MHz} \) to \( 20 \text{ MHz} \), \( C_L = 25 \text{ pF} \), \( f_{\text{SAMPLE}} = 500 \text{ ksp} \) to \( 1 \text{ Msps} \), and \( T_A = 25^\circ \text{C} \)
(unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( t_{CS} )</td>
<td>Minimum ( CS ) pulse width</td>
<td>(-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>10 ns</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td>( t_{SU} )</td>
<td>( CS ) to ( SCLK ) setup time</td>
<td>(-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>10 ns</td>
<td>10 ns</td>
<td>10 ns</td>
</tr>
<tr>
<td>( t_{EN} )</td>
<td>Delay from ( CS ) until ( SDATA ) TRI-STATE disabled(1)</td>
<td>(-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>20 ns</td>
<td>20 ns</td>
<td>20 ns</td>
</tr>
<tr>
<td>( t_{ACC} )</td>
<td>Data access time after ( SCLK ) falling edge(2)</td>
<td>( V_A = 2.7 \text{ V} ) to ( 3.6 \text{ V} ), (-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>40 ns</td>
<td>40 ns</td>
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</tr>
<tr>
<td></td>
<td></td>
<td>( V_A = 4.75 \text{ V} ) to ( 5.25 \text{ V} ), (-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>20 ns</td>
<td>20 ns</td>
<td>20 ns</td>
</tr>
<tr>
<td>( t_{CL} )</td>
<td>( SCLK ) low pulse width</td>
<td>(-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>0.4 \times t_{SCLK}</td>
<td>0.4 \times t_{SCLK}</td>
<td>0.4 \times t_{SCLK}</td>
</tr>
<tr>
<td>( t_{CH} )</td>
<td>( SCLK ) high pulse width</td>
<td>(-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>0.4 \times t_{SCLK}</td>
<td>0.4 \times t_{SCLK}</td>
<td>0.4 \times t_{SCLK}</td>
</tr>
<tr>
<td>( t_H )</td>
<td>( SCLK ) to data valid hold time</td>
<td>( V_A = 2.7 \text{ V} ) to ( 3.6 \text{ V} ), (-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>7 ns</td>
<td>7 ns</td>
<td>7 ns</td>
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<td></td>
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<td>( V_A = 4.75 \text{ V} ) to ( 5.25 \text{ V} ), (-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>5 ns</td>
<td>5 ns</td>
<td>5 ns</td>
</tr>
<tr>
<td>( t_{DIS} )</td>
<td>( SCLK ) falling edge to ( SDATA ) high impedance(3)</td>
<td>( V_A = 2.7 \text{ V} ) to ( 3.6 \text{ V} ), (-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>6 ns</td>
<td>6 ns</td>
<td>6 ns</td>
</tr>
<tr>
<td></td>
<td></td>
<td>( V_A = 4.75 \text{ V} ) to ( 5.25 \text{ V} ), (-40^\circ \text{C} \leq T_A \leq 125^\circ \text{C} )</td>
<td>5 ns</td>
<td>5 ns</td>
<td>5 ns</td>
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<tr>
<td>( t_{POWER-UP} )</td>
<td>Power-up time from full power down</td>
<td></td>
<td>1 \mu s</td>
<td>1 \mu s</td>
<td>1 \mu s</td>
</tr>
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</table>

(1) Measured with the timing test circuit and defined as the time taken by the output signal to cross 1 V.
(2) Measured with the timing test circuit and defined as the time taken by the output signal to cross 1 V or 2 V.
(3) \( t_{DIS} \) is derived from the time taken by the outputs to change by 0.5 V with the timing test circuit. The measured number is then adjusted to remove the effects of charging or discharging the output capacitance. This means that \( t_{DIS} \) is the true bus relinquish time, independent of the bus loading.

Figure 1. Timing Test Circuit
Figure 2. Serial Timing Diagram
7.8 Typical Characteristics

$T_A = 25^\circ C$, $f_{\text{SAMPLE}} = 500 \text{ ksp} s$ to $1 \text{ Msp} s$, $f_{\text{SCLK}} = 10 \text{ MHz}$ to $20 \text{ MHz}$, and $f_{\text{IN}} = 100 \text{ kHz}$ (unless otherwise noted)

![Figure 3. DNL, $f_{\text{SCLK}} = 10 \text{ MHz}$](image)

![Figure 4. INL, $f_{\text{SCLK}} = 10 \text{ MHz}$](image)

![Figure 5. DNL, $f_{\text{SCLK}} = 20 \text{ MHz}$](image)

![Figure 6. INL, $f_{\text{SCLK}} = 20 \text{ MHz}$](image)

![Figure 7. DNL vs Clock Frequency](image)

![Figure 8. INL vs Clock Frequency](image)
Typical Characteristics (continued)

\[ T_A = 25^\circ C, \ f_{\text{SAMPLE}} = 500 \text{ ksp} \text{s} \text{ to } 1 \text{ Msps}, \ f_{\text{SCLK}} = 10 \text{ MHz} \text{ to } 20 \text{ MHz}, \text{ and } f_{\text{IN}} = 100 \text{ kHz} \text{ (unless otherwise noted)} \]

- **Figure 9. SNR vs Clock Frequency**
- **Figure 10. SINAD vs Clock Frequency**
- **Figure 11. SFDR vs Clock Frequency**
- **Figure 12. THD vs Clock Frequency**
- **Figure 13. Spectral Response**
  \( V_A = 5.25 \text{ V}, \ f_{\text{SCLK}} = 10 \text{ MHz} \)
- **Figure 14. Spectral Response**
  \( V_A = 5.25 \text{ V}, \ f_{\text{SCLK}} = 20 \text{ MHz} \)
Typical Characteristics (continued)

$T_A = 25^\circ C$, $f_{\text{SAMPLE}} = 500$ ksp/s to 1 Msps, $f_{\text{SCLK}} = 10$ MHz to 20 MHz, and $f_{\text{IN}} = 100$ kHz (unless otherwise noted)

![Figure 15. Power Consumption vs Throughput, $f_{\text{SCLK}} = 20$ MHz]
8 Detailed Description

8.1 Overview

The ADC121S101 is a successive-approximation analog-to-digital converter designed around a charge-redistribution digital-to-analog converter core. Simplified schematics of the ADC121S101 in both track and hold modes are shown in Figure 16 and Figure 17, respectively. In Figure 16, the device is in track mode: switch SW1 connects the sampling capacitor to the input, and SW2 balances the comparator inputs. The device is in this state until CS is brought low, at which point the device moves to hold mode.

Figure 17 shows the device in hold mode: switch SW1 connects the sampling capacitor to ground, maintaining the sampled voltage, and switch SW2 unbalances the comparator. The control logic then instructs the charge-redistribution DAC to add or subtract fixed amounts of charge from the sampling capacitor until the comparator is balanced. When the comparator is balanced, the digital word supplied to the DAC is the digital representation of the analog input voltage. The device moves from hold mode to track mode on the 13th rising edge of SCLK.

Figure 16. ADC121S101 in Track Mode

Figure 17. ADC121S101 in Hold Mode
8.2 Functional Block Diagram

![Functional Block Diagram](image)

8.3 Feature Description

See the Functional Block Diagram for the serial interface timing diagram for the ADC. CS is chip select, which initiates conversions on the ADC and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. SDATA is the serial data out pin, where a conversion result is found as a serial data stream.

Basic operation of the ADC begins with CS going low, which initiates a conversion process and data transfer. Subsequent rising and falling edges of SCLK are labelled with reference to the falling edge of CS; for example, the third falling edge of SCLK shall refer to the third falling edge of SCLK after CS goes low.

At the fall of CS, the SDATA pin comes out of TRI-STATE, and the converter moves from track mode to hold mode. The input signal is sampled and held for conversion on the falling edge of CS. The converter moves from hold mode to track mode on the 13th rising edge of SCLK (see Figure 2). The interval for the \( t_{ACQ} \) specification begins at this point. At least 350 ns must pass between the 13th rising edge of SCLK and the next falling edge of CS. The SDATA pin is placed back into TRI-STATE after the 16th falling edge of SCLK, or at the rising edge of CS, whichever occurs first. After a conversion is completed, the quiet time \( t_{QUIET} \) must be satisfied before bringing CS low again to begin another conversion.

Sixteen SCLK cycles are required to read a complete sample from the ADC. The sample bits (including leading zeroes) are clocked out on falling edges of SCLK, and are intended to be clocked in by a receiver on subsequent falling edges of SCLK. The ADC produces three leading zero bits on SDATA, followed by twelve data bits, most significant first.

If CS goes low before the rising edge of SCLK, an additional (fourth) zero bit may be captured by the next falling edge of SCLK.

8.3.1 Determining Throughput

Throughput depends on the frequency of SCLK and how much time is allowed to elapse between the end of one conversion and the start of another. At the maximum specified SCLK frequency, the maximum guaranteed throughput is obtained by using a 20-SCLK frame. As shown in Figure 2, the minimum allowed time between CS falling edges is determined by 1) 12.5 SCLKs for Hold mode, 2) the larger of two quantities: either the minimum required time for Track mode (\( t_{ACQ} \)) or 2.5 SCLKs to finish reading the result and 3) 0, 1/2 or 1 SCLK padding to ensure an even number of SCLK cycles so there is a falling SCLK edge when CS next falls.

For example, at the fastest rate for this family of parts, SCLK is 20MHz and 2.5 SCLKs are 125 ns, so calculate the minimum time between CS falling edges using Equation 1.

\[
12.5 \times 50 \text{ ns} + 350 \text{ ns} + 0.5 \times 50 \text{ ns} = 1000 \text{ ns}
\]

(12.5 SCLKs + \( t_{ACQ} \) + 1/2 SCLK) which corresponds to a maximum throughput of 1 MSPS. At the slowest rate for this family, SCLK is 1 MHz. Using a 20 cycle conversion frame as shown in Figure 2 yields a 20-µs time between CS falling edges for a throughput of 50 KSPS.
Feature Description (continued)

It is possible, however, to use fewer than 20 clock cycles provided the timing parameters are met. With a 1-MHz SCLK, there are 2500 ns in 2.5-SCLK cycles, which is greater than $t_{ACQ}$. After the last data bit has come out, the clock requires one full cycle to return to a falling edge. Thus the total time between falling edges of CS is $12.5 \times 1 \, \mu s + 2.5 \times 1 \, \mu s + 1 \times 1 \, \mu s = 16 \, \mu s$, which is a throughput of 62.5 KSPS.

8.3.2 ADC Transfer Function

The output format of the ADC is straight binary. Code transitions occur midway between successive integer LSB values. The LSB width for the ADC is $V_A/4096$. Figure 18 shows the ideal transfer characteristic. The transition from an output code of 0000 0000 0000 to a code of 0000 0000 0001 is at 1/2 LSB, or a voltage of $V_A/8192$. Other code transitions occur at steps of one LSB.

8.3.3 Analog Inputs

Figure 19 shows an equivalent circuit for the ADC's input. Diodes D1 and D2 provide ESD protection for the analog inputs. At no time must the analog input go beyond $(V_A + 300 \, mV)$ or $(GND - 300 \, mV)$, as these ESD diodes will begin conducting, which could result in erratic operation. For this reason, the ESD diodes must not be used to clamp the input signal.

The capacitor C1 in Figure 19 has a typical value of 4 pF, and is mainly the package pin capacitance. Resistor R1 is the on resistance of the track or hold switch, and is typically 500 Ω. Capacitor C2 is the ADC sampling capacitor and is typically 26 pF. The ADC delivers the best performance when driven by a low-impedance source to eliminate distortion caused by the charging of the sampling capacitance. This is especially important when using the ADC to sample AC signals. Also important when sampling dynamic signals is an anti-aliasing filter.

Figure 18. Ideal Transfer Characteristic

Figure 19. Equivalent Input Circuit
Feature Description (continued)

8.3.4 Digital Inputs and Outputs

The ADC digital inputs (SCLK and CS) are not limited by the same maximum ratings as the analog inputs. The
digital input pins are instead limited to 5.25 V with respect to GND, regardless of $V_A$, the supply voltage. This
allows the ADC to be interfaced with a wide range of logic levels, independent of the supply voltage.

8.4 Device Functional Modes

The ADC has two possible modes of operation: normal mode, and shutdown mode. The ADC enters normal
mode (and a conversion process is begun) when CS is pulled low. The device enters shutdown mode if CS is
pulled high before the tenth falling edge of SCLK after CS is pulled low, or stays in normal mode if CS remains
low. Once in shutdown mode, the device stays there until CS is brought low again. By varying the ratio of time
spent in the normal and shutdown modes, a system may trade off throughput for power consumption, with a
sample rate as low as zero.

8.4.1 Normal Mode

The fastest possible throughput is obtained by leaving the ADC in normal mode at all times, so there are no
power-up delays. To keep the device in normal mode continuously, CS must be kept low until after the 10th
falling edge of SCLK after the start of a conversion (remember that a conversion is initiated by bringing CS low).

If CS is brought high after the 10th falling edge, but before the 16th falling edge, the device will remain in normal
mode, but the current conversion will be aborted, and SDATA will return to TRI-STATE (truncating the output
word).

Sixteen SCLK cycles are required to read all of a conversion word from the device. After sixteen SCLK cycles
have elapsed, CS may be idled either high or low until the next conversion. If CS is idled low, it must be brought
high again before the start of the next conversion, which begins when CS is again brought low.

After sixteen SCLK cycles, SDATA returns to TRI-STATE. Another conversion may be started, after $t_{QUIET}$ has
elapsed, by bringing CS low again.

8.4.2 Shutdown Mode

Shutdown mode is appropriate for applications that either do not sample continuously, or it is acceptable to trade
throughput for power consumption. When the ADC is in shutdown mode, all of the analog circuitry is turned off.

To enter shutdown mode, a conversion must be interrupted by bringing CS high anytime between the second
and tenth falling edges of SCLK, as shown in Figure 20. Once CS has been brought high in this manner, the
device will enter shutdown mode; the current conversion will be aborted and SDATA will enter TRI-STATE. If CS
is brought high before the second falling edge of SCLK, the device will not change mode; this is to avoid
accidentally changing mode as a result of noise on the CS line.
Device Functional Modes (continued)

To exit shutdown mode, bring CS back low. Upon bringing CS low, the ADC begins powering up (see Timing Requirements for power-up time specifications). This power-up delay results in the first conversion result being unusable. The second conversion performed after power up, however, is valid, as shown in Figure 21.

If CS is brought back high before the 10th falling edge of SCLK, the device returns to shutdown mode. This is done to avoid accidentally entering normal mode as a result of noise on the CS line. To exit shutdown mode and remain in normal mode, CS must be kept low until after the 10th falling edge of SCLK. The ADC is fully powered up after 16 SCLK cycles.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Figure 22 shows a typical application of the ADC. In this example, power is provided by TI’s LP2950 low-dropout voltage regulator, available in a variety of fixed and adjustable output voltages. The power supply pin is bypassed with a capacitor network placed close to the ADC. Because the reference for the ADC is the supply voltage, any noise on the supply degrades the noise performance of the device. To keep noise off the supply, use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC supply pin. Because of the ADC’s low power requirements, it is also possible to use a precision reference as a power supply to maximize performance. The three-wire interface is shown in Figure 22 connected to a microprocessor or DSP.

9.2 Typical Application

9.2.1 Design Requirements

A positive supply-only, data acquisition system is capable of digitizing a single-ended input signal ranging from 0 V to 5 V with a throughput up to 1 Msps. The ADC121S101 must interface to an MCU whose supply is set at 5 V.

9.2.2 Detailed Design Procedure

The signal range requirement forces the design to use 5-V analog supply at $V_A$, analog supply. This follows from the fact that $V_A$ is also a reference potential for the ADC. The maximum sampling rate of the ADC121S101 $F_s = F_{SCLK} / 20$.

Noise consideration must be given to the SPI interface, especially when the master MCU is capable of producing fast rising edges on the digital bus signals. Inserting small resistances in the digital signal path may help in reducing the ground bounce, and thus improve the overall noise performance of the system.

Take care when the signal source is capable of producing voltages beyond $V_A$. In such instances, the internal ESD diodes may start conducting. The ESD diodes are not intended as input signal clamps. To provide the desired clamping action use Schottky diodes.

A 0.1-µF capacitor must be placed close to the supply pin of the ADC121S101.
Typical Application (continued)

A small capacitor (1 nF to 10 nF) placed on the input pin can help the internal sampling capacitor settle. If the ADC121S101 is driven by an operational amplifier, a small resistor (50 Ω to 200 Ω) must be placed between the output of the operational amplifier and the junction of the capacitor and the ADC121S101 input pin.

9.2.3 Application Curve

![ADC Transfer Characteristic](image)

**Figure 23. ADC Transfer Characteristic**
10 Power Supply Recommendations

The power supply pin is bypassed with a capacitor network located close to the ADC. Because the reference for the ADC is the supply voltage, any noise on the supply degrades device noise performance. To keep noise off the supply, use a dedicated linear regulator for this device, or provide sufficient decoupling from other circuitry to keep noise off the ADC supply pin. Because of the ADC's low power requirements, it is also possible to use a precision reference as a power supply to maximize performance.

10.1 Power Management

The ADC takes time to power up, either after first applying $V_A$, or after returning to normal mode from shutdown mode. This corresponds to one dummy conversion for any SCLK frequency within the specifications in this document. After this first dummy conversion, the ADC performs conversions properly. Note that the $t_{QUIET}$ time must still be included between the first dummy conversion and the second valid conversion.

When the $V_A$ supply is first applied, the ADC may power up in either of the two modes: normal or shutdown. As such, one dummy conversion must be performed after start-up, as described in the previous paragraph. The part may then be placed into either normal mode or the shutdown mode, as described in Normal Mode and Shutdown Mode.

When the ADC is operated continuously in normal mode, the maximum throughput is $f_{SCLK} / 20$ at the maximum specified $f_{SCLK}$. Throughput may be traded for power consumption by running $f_{SCLK}$ at its maximum specified rate and performing fewer conversions per unit time, raising the ADC CS line after the 10th and before the 15th fall of SCLK of each conversion. Figure 15 shows a plot of typical power consumption versus throughput. To calculate the power consumption for a given throughput, multiply the fraction of time spent in the normal mode by the normal mode power consumption and add the fraction of time spent in shutdown mode multiplied by the shutdown mode power consumption. Note that the curve of power consumption vs throughput is essentially linear. This is because the power consumption in the shutdown mode is so small that it can be ignored for all practical purposes.

10.2 Power Supply Noise Considerations

The charging of any output load capacitance requires current from the power supply, $V_A$. The current pulses required from the supply to charge the output capacitance causes voltage variations on the supply. If these variations are large enough, they could degrade SNR and SINAD performance of the ADC. Furthermore, discharging the output capacitance when the digital output goes from a logic high to a logic low dumps current into the die substrate, which is resistive. Load discharge currents causes ground bounce noise in the substrate that degrades noise performance if that current is large enough. The larger the output capacitance, the more current flows through the die substrate and the greater is the noise coupled into the analog channel, degrading noise performance.

To keep noise out of the power supply, keep the output load capacitance as small as practical. It is good practice to use a 100-$\Omega$ series resistor at the ADC output, placed as close to the ADC output pin as practical. This limits the charge and discharge current of the output capacitance and improves noise performance.
11 Layout

11.1 Layout Guidelines

Capacitive coupling between the noisy digital circuitry and the sensitive analog circuitry can lead to poor performance. The solution is to keep the analog circuitry separated from the digital circuitry.

Generally, analog and digital lines must cross each other at 90° to avoid crosstalk. However, to maximize accuracy in high resolution systems, avoid crossing analog and digital lines altogether.

The analog input must be isolated from noisy signal traces to avoid coupling of spurious signals into the input. Any external component (for example, a filter capacitor) connected between the converter's input pins and ground must be connected to a clean point of the ground.

A 0.1-µF capacitor must be placed close to the supply pin of the ADC121S101.

11.2 Layout Example

![ADC121S101 Sample Layout](image-url)
12 Device and Documentation Support

12.1 Device Support

12.1.1 Device Nomenclature

**ACQUISITION TIME** is the time required to acquire the input voltage. That is, it is time required for the hold capacitor to charge up to the input voltage. Acquisition time is measured backwards from the falling edge of CS when the signal is sampled and the part moves from Track to Hold. The start of the time interval that contains \( t_{ACQ} \) is the 13th rising edge of SCLK of the previous conversion when the part moves from hold to track. The user must ensure that the time between the 13th rising edge of SCLK and the falling edge of the next CS is not less than \( t_{ACQ} \) to meet performance specifications.

**APERTURE DELAY** is the time after the falling edge of CS to when the input signal is acquired or held for conversion.

**APERTURE JITTER (APERTURE UNCERTAINTY)** is the variation in aperture delay from sample to sample. Aperture jitter manifests itself as noise in the output.

**CONVERSION TIME** is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word. This is from the falling edge of CS when the input signal is sampled to the 16th falling edge of SCLK when the SDATA output goes into TRI-STATE.

**DIFFERENTIAL NON-LINEARITY (DNL)** is the measure of the maximum deviation from the ideal step size of 1 LSB.

**DUTY CYCLE** is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

**EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS)** is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as \( (\text{SINAD} - 1.76) / 6.02 \) and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

**FULL POWER BANDWIDTH** is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

**GAIN ERROR** is the deviation of the last code transition (111...110) to (111...111) from the ideal \( (V_{\text{REF}} - 1.5 \text{ LSB}) \), after adjusting for offset error.

**INTEGRAL NON-LINEARITY (INL)** is a measure of the deviation of each individual code from a line drawn from negative full scale \( (\frac{1}{2} \text{ LSB below the first code transition}) \) through positive full scale \( (\frac{1}{2} \text{ LSB above the last code transition}) \). The deviation of any given code from this straight line is measured from the center of that code value.

**INTERMODULATION DISTORTION (IMD)** is the creation of additional spectral components as a result of two sinusoidal frequencies being applied to the ADC input at the same time. It is defined as the ratio of the power in the second and third order intermodulation products to the sum of the power in both of the original frequencies. IMD is usually expressed in dB.

**MISSING CODES** are those output codes that will never appear at the ADC outputs. The ADC121S101 is guaranteed not to have any missing codes.

**OFFSET ERROR** is the deviation of the first code transition (000...000) to (000...001) from the ideal (i.e. GND + 0.5 LSB).

**SIGNAL TO NOISE RATIO (SNR)** is the ratio, expressed in dB, of the rms value of the input signal to the rms value of the sum of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

**SIGNAL TO NOISE PLUS DISTORTION (S/N+D or SINAD)** is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.

**SPURIOUS FREE DYNAMIC RANGE (SFDR)** is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.
Device Support (continued)

TOTAL HARMONIC DISTORTION (THD) is the ratio, expressed in dB or dBC, of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output. THD is calculated as

$$\text{THD} = 20 \log_{10} \sqrt[2]{\frac{A_{f_2}^2 + \cdots + A_{f_6}^2}{A_{f_1}^2}}$$

where $A_{f_1}$ is the RMS power of the input frequency at the output and $A_{f_2}$ through $A_{f_6}$ are the RMS power in the first 5 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion. It is the acquisition time plus the conversion time.

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

E2E is a trademark of Texas Instruments.

All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
# Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
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<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
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<td>SOT-23</td>
<td>DBV</td>
<td>6</td>
<td>1000</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-40 to 125</td>
<td>X07Q</td>
<td>Samples</td>
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<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBsolete**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
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In no event shall TI’s liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF ADC121S101, ADC121S101-Q1:

- Catalog: ADC121S101
- Automotive: ADC121S101-Q1

NOTE: Qualified Version Definitions:

- Catalog - TI’s standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
**TAPE AND REEL INFORMATION**

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
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<td>178.0</td>
<td>8.4</td>
<td>3.2</td>
<td>3.2</td>
<td>1.4</td>
<td>4.0</td>
<td>8.0</td>
<td>Q3</td>
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<td>Q3</td>
</tr>
</tbody>
</table>
## TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC121S101CIMF/NOPB</td>
<td>SOT-23</td>
<td>DBV</td>
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<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
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<td>35.0</td>
</tr>
</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.
9. Board assembly site may have different recommendations for stencil design.
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