ADC121S705 12-Bit, 500 kSPS to 1 MSPS, Differential Input, Micro Power A/D Converter

Check for Samples: ADC121S705

**FEATURES**
- True Differential Inputs
- Ensured performance from 500 kSPS to 1 MSPS
- External Reference
- Wide Input Common-Mode Voltage Range
- SPI™/QSPI™/MICROWIRE/DSP Compatible Serial Interface

**APPLICATIONS**
- Automotive Navigation
- Portable Systems
- Medical Instruments
- Instrumentation and Control Systems
- Motor Control
- Direct Sensor Interface

**KEY SPECIFICATIONS**
- Conversion Rate: 500 kSPS to 1 MSPS
- INL: ± 0.95 LSB (Max)
- DNL: ±0.95 LSB (Max)
- Offset Error: ±3.0 LSB (Max)
- Gain Error: ±6.5 LSB (Max)
- SINAD: 69.5 db (Min)
- Power Consumption at \( V_A = 5V \)
  - Active, 1 MSPS: 11.5 mW (Typ)
  - Active, 500 kSPS: 9.0 mW (Typ)
  - Power-Down: 1.5 µW (Typ)

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

**DESCRIPTION**

The ADC121S705 is a 12-bit, 500 kSPS to 1 MSPS sampling Analog-to-Digital (A/D) converter that features a fully differential, high impedance analog input and an external reference. The reference voltage can be varied from 1.0V to \( V_A \), with a corresponding resolution between 244µV and \( V_A \) divided by 4096.

The output serial data is binary 2’s complement and is compatible with several standards, such as SPI™, QSPI™, MICROWIRE, and many common DSP serial interfaces. The differential input, low power consumption, and small size make the ADC121S705 ideal for direct connection to transducers in battery operated systems or remote data acquisition applications.

Operating from a single 5V supply, the supply current when operating at 1 MSPS is typically 2.3 mA. The supply current drops down to 0.3 µA typically when the ADC121S705 enters power-down mode. The ADC121S705 is available in the VSSOP-8 package. Operation is ensured over the industrial temperature range of −40°C to +105°C and clock rates of 8 MHz to 16 MHz.

**Connection Diagram**

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Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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### Block Diagram

![Block Diagram](image)

### PIN DESCRIPTIONS

<table>
<thead>
<tr>
<th>Pin No.</th>
<th>Symbol</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>V_REF</td>
<td>Voltage Reference Input. A voltage reference between 1V and $V_A$ must be applied to this input. $V_{REF}$ must be decoupled to GND with a minimum ceramic capacitor value of 0.1 $\mu$F. A bulk capacitor value of 1.0 $\mu$F to 10 $\mu$F in parallel with the 0.1 $\mu$F is recommended for enhanced performance.</td>
</tr>
<tr>
<td>2</td>
<td>+IN</td>
<td>Non-Inverting Input. +IN is the positive analog input for the differential signal applied to the ADC121S705.</td>
</tr>
<tr>
<td>3</td>
<td>−IN</td>
<td>Inverting Input. −IN is the negative analog input for the differential signal applied to the ADC121S705.</td>
</tr>
<tr>
<td>4</td>
<td>GND</td>
<td>Ground. GND is the ground reference point for all signals applied to the ADC121S705.</td>
</tr>
<tr>
<td>5</td>
<td>CS</td>
<td>Chip Select Bar. CS is active low. The ADC121S705 is in Normal Mode when CS is LOW and Power-Down Mode when CS is HIGH. A conversion begins on the fall of CS.</td>
</tr>
<tr>
<td>6</td>
<td>D_OUT</td>
<td>Serial Data Output. The conversion result is provided on D_OUT. The serial data output word is comprised of 4 null bits and 12 data bits (MSB first). During a conversion, the data is outputted on the falling edges of SCLK and is valid on the rising edges.</td>
</tr>
<tr>
<td>7</td>
<td>SCLK</td>
<td>Serial Clock. SCLK is used to control data transfer and serves as the conversion clock.</td>
</tr>
<tr>
<td>8</td>
<td>$V_A$</td>
<td>Power Supply input. A voltage source between 4.5V and 5.5V must be applied to this input. $V_A$ must be decoupled to GND with a ceramic capacitor value of 0.1 $\mu$F in parallel with a bulk capacitor value of 1.0 $\mu$F to 10 $\mu$F.</td>
</tr>
</tbody>
</table>
Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Analog Supply Voltage (V_A)</td>
<td>(-0.3) to 6.5V</td>
</tr>
<tr>
<td>Voltage on Any Pin to GND</td>
<td>(-0.3) to (V_A+0.3) V</td>
</tr>
<tr>
<td>Input Current at Any Pin ((4))</td>
<td>(\pm 10) mA</td>
</tr>
<tr>
<td>Package Input Current ((4))</td>
<td>(\pm 50) mA</td>
</tr>
<tr>
<td>Power Consumption at (T_A = 25^\circ) C</td>
<td>See ((5))</td>
</tr>
<tr>
<td>ESD Susceptibility ((6))</td>
<td></td>
</tr>
<tr>
<td>Human Body Model</td>
<td>2500V</td>
</tr>
<tr>
<td>Machine Model</td>
<td>250V</td>
</tr>
<tr>
<td>Charge Device Model</td>
<td>750V</td>
</tr>
<tr>
<td>Junction Temperature</td>
<td>(+150^\circ) C</td>
</tr>
<tr>
<td>Storage Temperature</td>
<td>(-65^\circ) C to (+150^\circ) C</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.

(4) When the input voltage at any pin exceeds the power supplies (that is, \(V_IN < GND\) or \(V_IN > V_A\)), the current at that pin should be limited to 10 mA. The 50 mA maximum package input current rating limits the number of pins that can safely exceed the power supplies with an input current of 10 mA to five.

(5) The absolute maximum junction temperature \(T_{J,max}\) for this device is 150\(^\circ\) C. The maximum allowable power dissipation is dictated by \(T_{J,max}\), the junction-to-ambient thermal resistance \(\theta_{JA}\), and the ambient temperature \(T_A\), and can be calculated using the formula \(P_{D\text{MAX}} = (T_{J,max} - T_A)/\theta_{JA}\). The values for maximum power dissipation listed above will be reached only when the ADC121S705 is operated in a severe fault condition (e.g. when input or output pins are driven beyond the power supply voltages, or the power supply polarity is reversed). Such conditions should always be avoided.

(6) Human body model is a 100 pF capacitor discharged through a 1.5 k\(\Omega\) resistor. Machine model is a 220 pF capacitor discharged through 0 \(\Omega\). Charge device model simulates a pin slowly acquiring charge (such as from a device sliding down the feeder in an automated assembler) then rapidly being discharged.

Operating Ratings

<table>
<thead>
<tr>
<th>Description</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Operating Temperature Range</td>
<td>(-40^\circ) C \leq T_A \leq +105^\circ) C</td>
</tr>
<tr>
<td>Supply Voltage, (V_A)</td>
<td>(+4.5) to (+5.5) V</td>
</tr>
<tr>
<td>Reference Voltage, (V_{REF})</td>
<td>1.0V to (V_A)</td>
</tr>
<tr>
<td>Input Common-Mode Voltage, (V_{CM})</td>
<td>See Figure 59</td>
</tr>
<tr>
<td>Digital Input Pins Voltage Range</td>
<td>0 to (V_A)</td>
</tr>
<tr>
<td>Clock Frequency</td>
<td>8 MHz to 16 MHz</td>
</tr>
<tr>
<td>Differential Analog Input Voltage</td>
<td>(-V_{REF}) to (+V_{REF})</td>
</tr>
</tbody>
</table>

(1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits. For ensured specifications and test conditions, see the Electrical Characteristics. The ensured specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions. Operation of the device beyond the maximum Operating Ratings is not recommended.

(2) All voltages are measured with respect to GND = 0V, unless otherwise specified.

Package Thermal Resistance

<table>
<thead>
<tr>
<th>Package</th>
<th>(\theta_{JA})</th>
</tr>
</thead>
<tbody>
<tr>
<td>8-lead VSSOP</td>
<td>200(^\circ) C / W</td>
</tr>
</tbody>
</table>

(1) Soldering process must comply with Texas Instruments’ Reflow Temperature Profile specifications. Refer to www.ti.com/packaging.

(2) Reflow temperature profiles are different for lead-free packages.
ADC121S705 Converter Electrical Characteristics

The following specifications apply for \( V_A = +4.5 \text{V to } 5.5 \text{V}, V_{REF} = 2.5 \text{V}, f_{SCLK} = 8 \text{ to } 16 \text{ MHz}, f_{IN} = 100 \text{ kHz}, C_L = 25 \text{ pF}, \) unless otherwise noted. **Boldface limits apply for** \( T_A = T_{MIN} \text{ to } T_{MAX} \); all other limits are at \( T_A = 25^\circ \text{C}. \)

### STATIC CONVERTER CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical</th>
<th>Limits</th>
<th>Units(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>INL</td>
<td>Integral Non-Linearity</td>
<td>( f_{IN} = 100 \text{ kHz}, -0.1 \text{ dBFS} )</td>
<td>( \pm 0.6 )</td>
<td>( \pm 0.95 )</td>
<td>LSB (max)</td>
</tr>
<tr>
<td>DNL</td>
<td>Differential Non-Linearity</td>
<td>( f_{IN} = 100 \text{ kHz}, -0.1 \text{ dBFS} )</td>
<td>( \pm 0.4 )</td>
<td>( \pm 0.95 )</td>
<td>LSB (max)</td>
</tr>
<tr>
<td>OE</td>
<td>Offset Error</td>
<td></td>
<td>( -0.4 )</td>
<td>( \pm 3 )</td>
<td>LSB (max)</td>
</tr>
<tr>
<td>FSE</td>
<td>Positive Full-Scale Error</td>
<td>( f_{IN} = 100 \text{ kHz}, -0.1 \text{ dBFS} )</td>
<td>( +0.1 )</td>
<td>( \pm 2 )</td>
<td>LSB (max)</td>
</tr>
<tr>
<td>GE</td>
<td>Gain Error</td>
<td></td>
<td>( -1.0 )</td>
<td>( \pm 6 )</td>
<td>LSB (max)</td>
</tr>
</tbody>
</table>

### DYNAMIC CONVERTER CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical</th>
<th>Limits</th>
<th>Units(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SINAD</td>
<td>Signal-to-Noise Plus Distortion Ratio</td>
<td>( f_{IN} = 100 \text{ kHz}, -0.1 \text{ dBFS} )</td>
<td>72.2</td>
<td>69.5</td>
<td>dBc (min)</td>
</tr>
<tr>
<td>SNR</td>
<td>Signal-to-Noise Ratio</td>
<td>( f_{IN} = 100 \text{ kHz}, -0.1 \text{ dBFS} )</td>
<td>72.8</td>
<td>71</td>
<td>dBc (min)</td>
</tr>
<tr>
<td>THD</td>
<td>Total Harmonic Distortion</td>
<td>( f_{IN} = 100 \text{ kHz}, -0.1 \text{ dBFS} )</td>
<td>-81.6</td>
<td>-72</td>
<td>dBc (max)</td>
</tr>
<tr>
<td>SFDR</td>
<td>Spurious-Free Dynamic Range</td>
<td>( f_{IN} = 100 \text{ kHz}, -0.1 \text{ dBFS} )</td>
<td>83.9</td>
<td>72</td>
<td>dBc (min)</td>
</tr>
<tr>
<td>ENOB</td>
<td>Effective Number of Bits</td>
<td></td>
<td>11.7</td>
<td>11.25</td>
<td>bits (min)</td>
</tr>
</tbody>
</table>

### ANALOG INPUT CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical</th>
<th>Limits</th>
<th>Units(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Differential Input Range</td>
<td>( V_{IN} = V_{REF} \text{ or } V_{IN} = -V_{REF} )</td>
<td>( \pm 1 )</td>
<td>( \mu A \text{ (max)} )</td>
<td></td>
</tr>
<tr>
<td>IDC</td>
<td>DC Leakage Current</td>
<td>( V_{IN} = V_{REF} \text{ or } V_{IN} = -V_{REF} )</td>
<td>( 17 )</td>
<td>( \mu F \text{ (pF)} )</td>
<td></td>
</tr>
<tr>
<td>CNA</td>
<td>Input Capacitance</td>
<td>In Track Mode</td>
<td>( 3 )</td>
<td>( \mu F \text{ (pF)} )</td>
<td></td>
</tr>
<tr>
<td>CMRR</td>
<td>Common Mode Rejection Ratio</td>
<td>See Specification Definitions for the test condition</td>
<td>( 76 )</td>
<td>( dB \text{ (dB)} )</td>
<td></td>
</tr>
<tr>
<td>VREF</td>
<td>Reference Voltage Range</td>
<td>( V_A \text{ (max)} )</td>
<td>( 0.2 )</td>
<td>( \mu A \text{ (max)} )</td>
<td></td>
</tr>
</tbody>
</table>

### DIGITAL INPUT CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical</th>
<th>Limits</th>
<th>Units(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VIN</td>
<td>Input High Voltage</td>
<td>( V_{IN} = 0 \text{V or } V_A )</td>
<td>( 2.6 )</td>
<td>( 3.6 )</td>
<td>( V \text{ (min)} )</td>
</tr>
<tr>
<td>VIL</td>
<td>Input Low Voltage</td>
<td>( V_{IN} = 0 \text{V or } V_A )</td>
<td>( 2.5 )</td>
<td>( 1.5 )</td>
<td>( V \text{ (max)} )</td>
</tr>
<tr>
<td>IIN</td>
<td>Input Current</td>
<td>( V_{IN} = 0 \text{V or } V_A )</td>
<td>( \pm 1 )</td>
<td>( \mu A \text{ (max)} )</td>
<td></td>
</tr>
</tbody>
</table>

### DIGITAL OUTPUT CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical</th>
<th>Limits</th>
<th>Units(2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>VOH</td>
<td>Output High Voltage</td>
<td>( I_{SOURCE} = 200 \mu A )</td>
<td>( V_A - 0.12 )</td>
<td>( V_A - 0.2 )</td>
<td>( V \text{ (min)} )</td>
</tr>
<tr>
<td>VIL</td>
<td>Output Low Voltage</td>
<td>( I_{SOURCE} = 1 \text{mA} )</td>
<td>( V_A - 0.16 )</td>
<td>( V \text{ (max)} )</td>
<td></td>
</tr>
<tr>
<td>IOZH</td>
<td>TRI-STATE Leakage Current</td>
<td>Force 0V or ( V_A )</td>
<td>( 0.05 )</td>
<td>( V \text{ (max)} )</td>
<td></td>
</tr>
<tr>
<td>COU</td>
<td>TRI-STATE Output Capacitance</td>
<td>Force 0V or ( V_A )</td>
<td>( 2 )</td>
<td>( 4 )</td>
<td>( \mu F \text{ (max)} )</td>
</tr>
</tbody>
</table>

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(1) Data sheet min/max specification limits are specified by design, test, or statistical analysis.
(2) Tested limits are specified to AOQL (Average Outgoing Quality Level).
ADC121S705 Converter Electrical Characteristics (1) (continued)
The following specifications apply for $V_A = +4.5$V to 5.5V, $V_{REF} = 2.5$V, $f_{SCLK} = 8$ to 16 MHz, $f_{IN} = 100$ kHz, $C_L = 25$ pF, unless otherwise noted. **Boldface limits apply for $T_A = T_{MIN}$ to $T_{MAX}$:** all other limits are at $T_A = 25^\circ$C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical</th>
<th>Limits</th>
<th>Units (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_A$</td>
<td>Analog Supply Voltage</td>
<td></td>
<td>4.5 V (min)</td>
<td>5.5 V (max)</td>
<td></td>
</tr>
<tr>
<td>$I_{VA}$ (Normal)</td>
<td>Supply Current, Normal Mode (Operational)</td>
<td>$f_{SCLK} = 16$ MHz, $f_S = 1$ MSPS, $f_{IN} = 100$ kHz</td>
<td>2.3</td>
<td>3 mA (max)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{SCLK} = 8$ MHz, $f_S = 500$ kSPS, $f_{IN} = 100$ kHz</td>
<td>1.8</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>$I_{VA}$ (PD)</td>
<td>Supply Current, Power Down Mode (CS high)</td>
<td>$f_{SCLK} = 16$ MHz</td>
<td>56</td>
<td>μA (max)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{SCLK} = 0$ (3)</td>
<td>0.3</td>
<td>2 μA (max)</td>
<td></td>
</tr>
<tr>
<td>PWR (Normal)</td>
<td>Power Consumption, Normal Mode (Operational)</td>
<td>$f_{SCLK} = 16$ MHz, $f_S = 1$ MSPS, $f_{IN} = 100$ kHz, $V_A = 5.0$V</td>
<td>11.5</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{SCLK} = 8$ MHz, $f_S = 500$ kSPS, $f_{IN} = 100$ kHz, $V_A = 5.0$V</td>
<td>9.0</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td>PWR (PD)</td>
<td>Power Consumption, Power Down Mode (CS high)</td>
<td>$f_{SCLK} = 16$ MHz, $V_A = 5.0$V</td>
<td>280</td>
<td>μW</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$f_{SCLK} = 0$, $V_A = 5.0$V</td>
<td>1.5</td>
<td>μW</td>
<td></td>
</tr>
<tr>
<td>PSRR</td>
<td>Power Supply Rejection Ratio</td>
<td>See the Specification Definitions for the test condition</td>
<td>–85</td>
<td>dB</td>
<td></td>
</tr>
</tbody>
</table>

**AC ELECTRICAL CHARACTERISTICS**

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical</th>
<th>Limits</th>
<th>Units (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$f_{SCLK}$</td>
<td>Maximum Clock Frequency</td>
<td></td>
<td>20</td>
<td>16 MHz (min)</td>
<td></td>
</tr>
<tr>
<td>$f_{SCLK}$</td>
<td>Minimum Clock Frequency</td>
<td></td>
<td>0.8</td>
<td>8 MHz (max)</td>
<td></td>
</tr>
<tr>
<td>$f_S$</td>
<td>Maximum Sample Rate (4)</td>
<td></td>
<td>1.25</td>
<td>1 MSPS (min)</td>
<td></td>
</tr>
<tr>
<td>$t_{ACQ}$</td>
<td>Track/Hold Acquisition Time</td>
<td></td>
<td>2.5</td>
<td>SCLK cycles (min)</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>3.0</td>
<td>SCLK cycles (max)</td>
<td></td>
</tr>
<tr>
<td>$t_{CONV}$</td>
<td>Conversion Time</td>
<td></td>
<td>13</td>
<td>SCLK cycles</td>
<td></td>
</tr>
<tr>
<td>$t_{AD}$</td>
<td>Aperture Delay</td>
<td>See Specification Definitions</td>
<td>6</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

(3) Data sheet min/max specification limits are specified by design, test, or statistical analysis.

ADC121S705 Timing Specifications (1)
The following specifications apply for $V_A = +4.5$V to 5.5V, $V_{REF} = 2.5$V, $f_{SCLK} = 8$ MHz to 16 MHz, $C_L = 25$ pF, **Boldface limits apply for $T_A = T_{MIN}$ to $T_{MAX}$:** all other limits $T_A = 25^\circ$C.

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>Conditions</th>
<th>Typical</th>
<th>Limits</th>
<th>Units (2)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{CSH}$</td>
<td>CS Hold Time after an SCLK rising edge</td>
<td></td>
<td>5</td>
<td>ns (min)</td>
<td></td>
</tr>
<tr>
<td>$t_{CSSU}$</td>
<td>CS Setup Time prior to an SCLK rising edge</td>
<td></td>
<td>5</td>
<td>ns (min)</td>
<td></td>
</tr>
<tr>
<td>$t_{DH}$</td>
<td>$D_{OUT}$ Hold time after an SCLK Falling edge</td>
<td></td>
<td>7</td>
<td>2.5 ns (min)</td>
<td></td>
</tr>
<tr>
<td>$t_{DA}$</td>
<td>$D_{OUT}$ Access time after an SCLK Falling edge</td>
<td></td>
<td>18</td>
<td>22 ns (max)</td>
<td></td>
</tr>
<tr>
<td>$t_{DIS}$</td>
<td>$D_{OUT}$ Disable Time after the rising edge of CS (2)</td>
<td></td>
<td>20</td>
<td>20 ns (max)</td>
<td></td>
</tr>
<tr>
<td>$t_{EN}$</td>
<td>$D_{OUT}$ Enable Time after the falling edge of CS</td>
<td></td>
<td>8</td>
<td>20 ns (max)</td>
<td></td>
</tr>
<tr>
<td>$t_{CH}$</td>
<td>SCLK High Time</td>
<td></td>
<td>25</td>
<td>ns (min)</td>
<td></td>
</tr>
<tr>
<td>$t_{CL}$</td>
<td>SCLK Low Time</td>
<td></td>
<td>25</td>
<td>ns (min)</td>
<td></td>
</tr>
<tr>
<td>$t_r$</td>
<td>$D_{OUT}$ Rise Time</td>
<td></td>
<td>7</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>$t_f$</td>
<td>$D_{OUT}$ Fall Time</td>
<td></td>
<td>7</td>
<td>ns</td>
<td></td>
</tr>
</tbody>
</table>

(1) Data sheet min/max specification limits are specified by design, test, or statistical analysis.

(2) $t_{DIS}$ is the time for $D_{OUT}$ to change 10% while being loaded by the Timing Test Circuit.
Timing Diagrams

Figure 1. ADC121S705 Single Conversion Timing Diagram

Figure 2. ADC121S705 Continuous Conversion Timing Diagram

Figure 3. Timing Test Circuit

Figure 4. Rise and Fall Times

Figure 5. Hold and Access Times

Figure 6. Valid CS Assertion Times

Figure 7. Voltage Waveform for tDIS
Specification Definitions

APERTURE DELAY is the time between the fourth falling edge of SCLK and the time when the input signal is acquired or held for conversion.

COMMON MODE REJECTION RATIO (CMRR) is a measure of how well in-phase signals common to both input pins are rejected.

To calculate CMRR, the change in output offset is measured while the common mode input voltage is changed from 2V to 3V.

\[
\text{CMRR} = 20 \log \left( \frac{\Delta \text{Common Input}}{\Delta \text{Output Offset}} \right) \quad (1)
\]

CONVERSION TIME is the time required, after the input voltage is acquired, for the ADC to convert the input voltage to a digital word.

DIFFERENTIAL NON-LINEARITY (DNL) is the measure of the maximum deviation from the ideal step size of 1 LSB.

DUTY CYCLE is the ratio of the time that a repetitive digital waveform is high to the total time of one period. The specification here refers to the SCLK.

EFFECTIVE NUMBER OF BITS (ENOB, or EFFECTIVE BITS) is another method of specifying Signal-to-Noise and Distortion or SINAD. ENOB is defined as \((\text{SINAD} - 1.76) / 6.02\) and says that the converter is equivalent to a perfect ADC of this (ENOB) number of bits.

FULL POWER BANDWIDTH is a measure of the frequency at which the reconstructed output fundamental drops 3 dB below its low frequency value for a full scale input.

GAIN ERROR is the deviation from the ideal slope of the transfer function. It is the difference between Positive Full-Scale Error and Negative Full-Scale Error and can be calculated as:

\[
\text{Gain Error} = \text{Positive Full-Scale Error} - \text{Negative Full-Scale Error} \quad (2)
\]

INTEGRAL NON-LINEARITY (INL) is a measure of the deviation of each individual code from a line drawn from negative full scale (½ LSB below the first code transition) through positive full scale (½ LSB above the last code transition). The deviation of any given code from this straight line is measured from the center of that code value.

MISSING CODES are those output codes that will never appear at the ADC outputs. The ADC121S705 is ensured not to have any missing codes.

NEGATIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions from negative full scale to the next code and \(-V_{\text{REF}} + 0.5 \text{ LSB}\).

OFFSET ERROR is the difference between the differential input voltage at which the output code transitions from code 000h to 001h and 1/2 LSB.

POSITIVE FULL-SCALE ERROR is the difference between the differential input voltage at which the output code transitions to positive full scale and \(V_{\text{REF}} - 1.5 \text{ LSB}\).

POWER SUPPLY REJECTION RATIO (PSRR) is a measure of how well a change in supply voltage is rejected. PSRR is calculated from the ratio of the change in offset error for a given change in supply voltage, expressed in dB. For the ADC121S705, \(V_A\) is changed from 4.5V to 5.5V.

\[
\text{PSRR} = 20 \log \left( \frac{\Delta \text{Offset}}{\Delta V_A} \right) \quad (3)
\]

SIGNAL TO NOISE RATIO (SNR) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all other spectral components below one-half the sampling frequency, not including harmonics or d.c.

SIGNAL TO NOISE PLUS DISTORTION (S+N+D or SINAD) is the ratio, expressed in dB, of the rms value of the input signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c.
SPURIOUS FREE DYNAMIC RANGE (SFDR) is the difference, expressed in dB, between the desired signal amplitude to the amplitude of the peak spurious spectral component, where a spurious spectral component is any signal present in the output spectrum that is not present at the input and may or may not be a harmonic.

TOTAL HARMONIC DISTORTION (THD) is the ratio of the rms total of the first five harmonic components at the output to the rms level of the input signal frequency as seen at the output, expressed in dB. THD is calculated as

\[
\text{THD} = 20 \cdot \log_{10} \left( \frac{A_{12}^2 + \cdots + A_{16}^2}{A_{11}^2} \right)
\]

where \(A_{11}\) is the RMS power of the input frequency at the output and \(A_{12}\) through \(A_{16}\) are the RMS power in the first 5 harmonic frequencies.

THROUGHPUT TIME is the minimum time required between the start of two successive conversion.
Typical Performance Characteristics

\[ V_A = 5.0 \text{V}, \; V_{\text{REF}} = 2.5 \text{V}, \; T_A = +25^\circ \text{C}, \; f_{\text{SAMPLE}} = 1 \text{ MSPS}, \; f_{\text{SCLK}} = 16 \text{ MHz}, \; f_{\text{IN}} = 100 \text{ kHz} \text{ unless otherwise stated.} \]
Typical Performance Characteristics (continued)

V_A = 5.0V, V_REF = 2.5V, T_A = +25°C, f_{SAMPLE} = 1 MSPS, f_{SCLK} = 16 MHz, f_{IN} = 100 kHz unless otherwise stated.

![DNL vs. V_REF](image1)

![INL vs. V_REF](image2)

![OFFSET ERROR vs. V_REF](image3)

![GAIN ERROR vs. V_REF](image4)

![DNL vs. SCLK FREQUENCY](image5)

![INL vs. SCLK FREQUENCY](image6)
Typical Performance Characteristics (continued)

$V_A = 5.0\text{V}, V_{\text{REF}} = 2.5\text{V}, T_A = +25^\circ\text{C}, f_{\text{SAMPLE}} = 1\ \text{MSPS}, f_{\text{SCLK}} = 16\ \text{MHz}, f_{\text{IN}} = 100\ \text{kHz}$ unless otherwise stated.

OFFSET ERROR vs. SCLK FREQUENCY

GAIN ERROR vs. SCLK FREQUENCY

OFFSET ERROR vs. SCLK DUTY CYCLE

GAIN ERROR vs. SCLK DUTY CYCLE

DNL vs. SCLK DUTY CYCLE

INL vs. SCLK DUTY CYCLE

Figure 20.

Figure 21.

Figure 22.

Figure 23.

Figure 24.

Figure 25.
Typical Performance Characteristics (continued)

$V_A = 5.0\, \text{V}, \quad V_{\text{REF}} = 2.5\, \text{V}, \quad T_A = +25^\circ\, \text{C}, \quad f_{\text{SAMPLE}} = 1\, \text{MSPS}, \quad f_{\text{SCLK}} = 16\, \text{MHz}, \quad f_{\text{IN}} = 100\, \text{kHz}$ unless otherwise stated.

DNL vs. TEMPERATURE

\begin{figure}
\centering
\includegraphics[width=0.4\textwidth]{DNLvsTEMP}
\caption{DNL vs. TEMPERATURE}
\end{figure}

INL vs. TEMPERATURE

\begin{figure}
\centering
\includegraphics[width=0.4\textwidth]{INLvsTEMP}
\caption{INL vs. TEMPERATURE}
\end{figure}

OFFSET ERROR vs. TEMPERATURE

\begin{figure}
\centering
\includegraphics[width=0.4\textwidth]{OFFSETERRORvsTEMP}
\caption{OFFSET ERROR vs. TEMPERATURE}
\end{figure}

GAIN ERROR vs. TEMPERATURE

\begin{figure}
\centering
\includegraphics[width=0.4\textwidth]{GAINERRORvsTEMP}
\caption{GAIN ERROR vs. TEMPERATURE}
\end{figure}

SNR vs. $V_A$

\begin{figure}
\centering
\includegraphics[width=0.4\textwidth]{SNRvsVA}
\caption{SNR vs. $V_A$}
\end{figure}

THD vs. $V_A$

\begin{figure}
\centering
\includegraphics[width=0.4\textwidth]{THDvsVA}
\caption{THD vs. $V_A$}
\end{figure}
Typical Performance Characteristics (continued)

$V_A = 5.0\, \text{V}$, $V_{\text{REF}} = 2.5\, \text{V}$, $T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 1\, \text{MSPS}$, $f_{\text{SCLK}} = 16\, \text{MHz}$, $f_{\text{IN}} = 100\, \text{kHz}$ unless otherwise stated.

**SINAD vs. $V_A$**

Figure 32.

**SFDR vs. $V_A$**

Figure 33.

**SNR vs. $V_{\text{REF}}$**

Figure 34.

**THD vs. $V_{\text{REF}}$**

Figure 35.

**SINAD vs. $V_{\text{REF}}$**

Figure 36.

**SFDR vs. $V_{\text{REF}}$**

Figure 37.
Typical Performance Characteristics (continued)

$V_A = 5.0\text{V}$, $V_{\text{REF}} = 2.5\text{V}$, $T_A = +25^\circ\text{C}$, $f_{\text{SAMPLE}} = 1\ \text{MSPS}$, $f_{\text{SCLK}} = 16\ \text{MHz}$, $f_{\text{IN}} = 100\ \text{kHz}$ unless otherwise stated.

- **SNR vs. SCLK FREQUENCY**
- **THD vs. SCLK FREQUENCY**
- **SINAD vs. SCLK FREQUENCY**
- **SFDR vs. SCLK FREQUENCY**
- **SNR vs. SCLK DUTY CYCLE**
- **THD vs. SCLK DUTY CYCLE**

![SNR vs. SCLK FREQUENCY](Figure 38.)

![THD vs. SCLK FREQUENCY](Figure 39.)

![SINAD vs. SCLK FREQUENCY](Figure 40.)

![SFDR vs. SCLK FREQUENCY](Figure 41.)

![SNR vs. SCLK DUTY CYCLE](Figure 42.)

![THD vs. SCLK DUTY CYCLE](Figure 43.)
Typical Performance Characteristics (continued)

$V_A = 5.0\, \text{V}, V_{\text{REF}} = 2.5\, \text{V}, T_A = +25^\circ\, \text{C}, f_{\text{SAMPLE}} = 1\, \text{MSPS}, f_{\text{SCLK}} = 16\, \text{MHz}, f_{\text{IN}} = 100\, \text{kHz}$ unless otherwise stated.

![SINAD vs. SCLK DUTY CYCLE](image1)

Figure 44.

![SFDR vs. SCLK DUTY CYCLE](image2)

Figure 45.

![SNR vs. INPUT FREQUENCY](image3)

Figure 46.

![THD vs. INPUT FREQUENCY](image4)

Figure 47.

![SINAD vs. INPUT FREQUENCY](image5)

Figure 48.

![SFDR vs. INPUT FREQUENCY](image6)

Figure 49.
Typical Performance Characteristics (continued)

$V_A = 5.0 \text{V}, V_{\text{REF}} = 2.5 \text{V}, T_A = +25 \degree \text{C}, f_{\text{SAMPLE}} = 1 \text{ MSPS}, f_{\text{SCLK}} = 16 \text{ MHz}, f_{\text{IN}} = 100 \text{ kHz}$ unless otherwise stated.

**SNR vs. TEMPERATURE**

![SNR vs. TEMPERATURE graph]

**THD vs. TEMPERATURE**

![THD vs. TEMPERATURE graph]

**SINAD vs. TEMPERATURE**

![SINAD vs. TEMPERATURE graph]

**SFDR vs. TEMPERATURE**

![SFDR vs. TEMPERATURE graph]

**SUPPLY CURRENT vs. SCLK FREQUENCY**

![SUPPLY CURRENT vs. SCLK FREQUENCY graph]

**SUPPLY CURRENT vs. TEMPERATURE**

![SUPPLY CURRENT vs. TEMPERATURE graph]
Typical Performance Characteristics (continued)

$V_A = 5.0\text{V}, V_{\text{REF}} = 2.5\text{V}, T_A = +25^\circ\text{C}, f_{\text{SAMPLE}} = 1\text{ MSPS}, f_{\text{SCLK}} = 16\text{ MHz}, f_{\text{IN}} = 100\text{ kHz}$ unless otherwise stated.

**Figure 56.** REF. CURRENT vs. SCLK FREQUENCY

**Figure 57.** REF. CURRENT vs. TEMPERATURE

**Figure 58.** SPECTRAL RESPONSE - 1 MSPS
Functional Description

The ADC121S705 analog-to-digital converter uses a successive approximation register (SAR) architecture based upon capacitive redistribution containing an inherent sample/hold function. The architecture and process allow the ADC121S705 to acquire and convert an analog signal at sample rates up to 1 MSPS while consuming very little power.

The ADC121S705 requires an external reference, external clock, and a single +5V power source that can be as low as +4.5V. The external reference can be any voltage between 1V and \( V_A \). The value of the reference voltage determines the range of the analog input, while the reference input current depends upon the conversion rate.

The external clock can take on values as indicated in the Electrical Characteristics of this data sheet. The duty cycle of the clock is essentially unimportant, provided the minimum clock high and low times are met. The minimum clock frequency is set by internal capacitor leakage. Each conversion requires 16 SCLK cycles to complete. If less than 12 bits of conversion data are required, CS can be brought high at any point during the conversion. This procedure of terminating a conversion prior to completion is often referred to as short cycling.

The analog input is presented to the two input pins: +IN and –IN. Upon initiation of a conversion, the differential input at these pins is sampled on the internal capacitor array. The inputs are disconnected from the internal circuitry while a conversion is in progress.

The digital conversion result is clocked out by the SCLK input and is provided serially, most significant bit first, at the D\(_{OUT}\) pin. The digital data that is provided at the D\(_{OUT}\) pin is that of the conversion currently in progress. With CS held low after the conversion is complete, the ADC121S705 continuously converts the analog input. The digital data on D\(_{OUT}\) can be clocked into the receiving device on the SCLK rising edges. See Serial Digital Interface and Timing Diagrams for more information.

REFERENCE INPUT

The externally supplied reference voltage sets the analog input range. The ADC121S705 will operate with a reference voltage in the range of 1V to \( V_A \).

As the reference voltage is reduced, the range of input voltages corresponding to each digital output code is reduced. That is, a smaller analog input range corresponds to one LSB (Least Significant Bit). The size of one LSB is equal to twice the reference voltage divided by 4096. When the LSB size goes below the noise floor of the ADC121S705, the noise will span an increasing number of codes and overall performance will suffer. For example, dynamic signals will have their SNR degrade, while D.C. measurements will have their code uncertainty increase. Since the noise is Gaussian in nature, the effects of this noise can be reduced by averaging the results of a number of consecutive conversions.

Additionally, since offset and gain errors are specified in LSB, any offset and/or gain errors inherent in the A/D converter will increase in terms of LSB size as the reference voltage is reduced.

The reference input and the analog inputs are connected to the capacitor array through a switch matrix when the input is sampled. Hence, the only current required at the reference and at the analog inputs is a series of transient spikes.

Lower reference voltages will decrease the current pulses at the reference input and will slightly decrease the average input current. The reference current changes only slightly with temperature. See Figure 56 and Figure 57 in Typical Performance Characteristics for additional details.
ANALOG SIGNAL INPUTS

The ADC121S705 has a differential input, and the effective input voltage that is digitized is (+IN) − (−IN). As is the case with all differential input A/D converters, operation with a fully differential input signal or voltage will provide better performance than with a single-ended input. Yet, the ADC121S705 can be presented with a single-ended input.

The current required to recharge the input sampling capacitor will cause voltage spikes at +IN and −IN. Do not try to filter out these noise spikes. Rather, ensure that the transient settles out during the acquisition period (three SCLK cycles after the fall of CS).

Differential Input Operation

With a fully differential input voltage or signal, a positive full scale output code (0111 1111 1111b or 7FFh) will be obtained when (+IN) − (−IN) ≥ V_REF − 1.5 LSB. A negative full scale code (1000 0000 0000b or 800h) will be obtained when (+IN) − (−IN) ≤ −V_REF + 0.5 LSB. This ignores gain, offset and linearity errors, which will affect the exact differential input voltage that will determine any given output code.

Single-Ended Input Operation

For single-ended operation, the non-inverting input (+IN) of the ADC121S705 should be driven with a signal or voltages that have a maximum to minimum value range that is equal to or less than twice the reference voltage. The inverting input (−IN) should be biased at a stable voltage that is halfway between these maximum and minimum values.

Since the design of the ADC121S705 is optimized for a differential input, the performance degrades slightly when driven with a single-ended input. Linearity characteristics such as INL and DNL typically degrade by 0.1 LSB and dynamic characteristics such as SINAD typically degrade by 2 dB. Note that single-ended operation should only be used if the performance degradation (compared with differential operation) is acceptable.

Input Common Mode Voltage

The allowable input common mode voltage (V_CM) range depends upon the supply and reference voltages used for the ADC121S705. The ranges of V_CM are depicted in Figure 59 and Figure 60. The minimum and maximum common mode voltages for differential and single-ended operation are shown in Table 1.

![Figure 59. V_CM range for Differential Input operation](image1)

![Figure 60. V_CM range for single-ended operation](image2)

<table>
<thead>
<tr>
<th>Table 1. Allowable V_CM Range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Signal</td>
</tr>
<tr>
<td>--------------</td>
</tr>
<tr>
<td>Differential</td>
</tr>
<tr>
<td>Single-Ended</td>
</tr>
</tbody>
</table>
SERIAL DIGITAL INTERFACE

The ADC121S705 communicates via a synchronous 3-wire serial interface as shown in Timing Diagrams. CS, chip select, initiates conversions and frames the serial data transfers. SCLK (serial clock) controls both the conversion process and the timing of serial data. DOUT is the serial data output pin, where a conversion result is sent as a serial data stream, MSB first.

A serial frame is initiated on the falling edge of CS and ends on the rising edge of CS. The ADC121S705's DOUT pin is in a high impedance state when CS is high and is active when CS is low; thus CS acts as an output enable.

During the first three cycles of SCLK, the ADC121S705 is in acquisition mode ($t_{ACQ}$), acquiring the input voltage. For the next thirteen SCLK cycles ($t_{CONV}$), the conversion is accomplished and the data is clocked out. SCLK falling edges one through four clock out leading zeros while falling edges five through sixteen clock out the conversion result, MSB first. If there is more than one conversion in a frame (continuous conversion mode), the ADC121S705 will re-enter acquisition mode on the falling edge of SCLK after the N*16th rising edge of SCLK and re-enter the conversion mode on the N*16+4th falling edge of SCLK as shown in Figure 2. "N" is an integer value.

The ADC121S705 can enter acquisition mode under three different conditions. The first condition involves CS going low (asserted) with SCLK high. In this case, the ADC121S705 enters acquisition mode on the first falling edge of SCLK after CS is asserted. In the second condition, CS goes low with SCLK low. Under this condition, the ADC121S705 automatically enters acquisition mode and the falling edge of CS is seen as the first falling edge of SCLK. In the third condition, CS and SCLK go low simultaneously and the ADC121S705 enters acquisition mode. While there is no timing restriction with respect to the falling edges of CS and SCLK, see Figure 6 for setup and hold time requirements for the falling edge of CS with respect to the rising edge of SCLK.

CS Input

The CS (chip select bar) input is CMOS compatible and is active low. The ADC121S705 is in normal mode when CS is low and power-down mode when CS is high. CS frames the conversion window. The falling edge of CS marks the beginning of a conversion and the rising of CS marks the end of a conversion window. Multiple conversions can occur within a given conversion frame with each conversion requiring sixteen SCLK cycles.

SCLK Input

The SCLK (serial clock) is used as the conversion clock and to clock out the conversion results. This input is CMOS compatible. Internal settling time requirements limit the maximum clock frequency while internal capacitor leakage limits the minimum clock frequency. The ADC121S705 offers ensured performance with the clock rates indicated in the electrical table.

Data Output

The output data format of the ADC121S705 is two's complement, as shown in Table 2. This table indicates the ideal output code for the given input voltage and does not include the effects of offset, gain error, linearity errors, or noise. Each data output bit is sent on the falling edge of SCLK.

While most receiving systems will capture the digital output bits on the rising edge of SCLK, the falling edge of SCLK may be used to capture each bit if the minimum hold time ($t_{DH}$) for DOUT is acceptable. See Figure 5 for DOUT hold and access times.

DOUT is enabled on the falling edge of CS and disabled on the rising edge of CS. If CS is raised prior to the 16th falling edge of SCLK, the current conversion is aborted and DOUT will go into its high impedance state. A new conversion will begin when CS is taken LOW.

<table>
<thead>
<tr>
<th>Description</th>
<th>Analog Input, (+IN) – (-IN)</th>
<th>2’s Complement Binary Output</th>
<th>2’s Comp. Hex Code</th>
</tr>
</thead>
<tbody>
<tr>
<td>+ Full Scale</td>
<td>$V_{REF} - 1.5$ LSB</td>
<td>0111 1111 1111</td>
<td>7FF</td>
</tr>
<tr>
<td>Midscale</td>
<td>0V</td>
<td>0000 0000 0000</td>
<td>000</td>
</tr>
<tr>
<td>Midscale – 1 LSB</td>
<td>$0V - 1$ LSB</td>
<td>1111 1111 1111</td>
<td>FFF</td>
</tr>
<tr>
<td>– Full Scale</td>
<td>$-V_{REF} - 0.5$ LSB</td>
<td>1000 0000 0000</td>
<td>800</td>
</tr>
</tbody>
</table>

Table 2. Ideal Output Code vs. Input Voltage
APPLICATIONS INFORMATION

OPERATING CONDITIONS
We recommend that the following conditions be observed for operation of the ADC121S705:

\[-40 °C \leq T_A \leq +105 °C\]

\[+4.5V \leq V_A \leq +5.5V\]

\[1V \leq V_{REF} \leq V_A\]

\[8 MHz \leq f_{CLK} \leq 16 MHz\]

\[V_{CM}: \text{See Input Common Mode Voltage}\]

POWER CONSUMPTION
The architecture, design, and fabrication process allow the ADC121S705 to operate at conversion rates up to 1 MSPS while consuming very little power. The ADC121S705 consumes the least amount of power while operating in power down mode. For applications where power consumption is critical, the ADC121S705 should be operated in power down mode as often as the application will tolerate. To further reduce power consumption, stop the SCLK while CS is high.

Short Cycling
Another way of saving power is to short cycle the conversion process. This is done by pulling CS high after the last required bit is received from the ADC121S705 output. This is possible because the ADC121S705 places the latest converted data bit on \(D_{OUT}\) as it is generated. If only 8-bits of the conversion result are needed, for example, the conversion can be terminated by pulling CS high after the 8th bit has been clocked out. Halting the conversion after the last needed bit is outputted is called short cycling.

Short cycling can be used to lower the power consumption in those applications that do not need a full 12-bit resolution, or where an analog signal is being monitored until some condition occurs. For example, it may not be necessary to use the full 12-bit resolution of the ADC121S705 as long as the signal being monitored is within certain limits. In some circumstances, the conversion could be terminated after the first few bits. This will lower power consumption in the converter since the ADC121S705 spends more time in power down mode and less time in the conversion mode.

Burst Mode Operation
Normal operation of the ADC121S705 requires the SCLK frequency to be sixteen times the sample rate and the CS rate to be the same as the sample rate. However, in order to minimize power consumption in applications requiring sample rates below 500 kSPS, the ADC121S705 should be run with an SCLK frequency of 16 MHz and a CS rate as slow as the system requires. When this is accomplished, the ADC121S705 is operating in burst mode. The ADC121S705 enters into power down mode at the end of each conversion, minimizing power consumption. This causes the converter to spend the longest possible time in power down mode. Since power consumption scales directly with conversion rate, minimizing power consumption requires determining the lowest conversion rate that will satisfy the requirements of the system.

TIMING CONSIDERATIONS
Proper operation requires that the fall of \(\overline{CS}\) not occur simultaneously with a rising edge of SCLK. If the fall of \(\overline{CS}\) occurs during the rising edge of SCLK, the data might be clocked out one bit early. Whether or not the data is clocked out early depends upon how close the \(\overline{CS}\) transition is to the SCLK transition, the device temperature, and characteristics of the individual device. To ensure that the data is always clocked out at a given time (the 5th falling edge of SCLK), it is essential that the fall of \(\overline{CS}\) always meet the timing requirement specified in the Timing Specifications.
PCB LAYOUT AND CIRCUIT CONSIDERATIONS

For best performance, care should be taken with the physical layout of the printed circuit board. This is especially true with a low reference voltage or when the conversion rate is high. At high clock rates there is less time for settling, so it is important that any noise settles out before the conversion begins.

Power Supply

Any ADC architecture is sensitive to spikes on the power supply, reference, and ground pins. These spikes may originate from switching power supplies, digital logic, high power devices, and other sources. Power to the ADC121S705 should be clean and well bypassed. A 0.1 µF ceramic bypass capacitor and a 1 µF to 10 µF capacitor should be used to bypass the ADC121S705 supply, with the 0.1 µF capacitor placed as close to the ADC121S705 package as possible.

Voltage Reference

The reference source must have a low output impedance and needs to be bypassed with a minimum capacitor value of 0.1 µF. A larger capacitor value of 1 µF to 10 µF placed in parallel with the 0.1 µF is preferred. While the ADC121S705 draws very little current from the reference on average, there are higher instantaneous current spikes at the reference input that must settle out while SCLK is high. Since these transient spikes can be as high as 20 mA, it is important that the reference circuit be capable of providing this much current and settle out during the first three clock periods (acquisition time).

The reference input of the ADC121S705, like all A/D converters, does not reject noise or voltage variations. Keep this in mind if the reference voltage is derived from the power supply. Any noise and/or ripple from the supply that is not rejected by the external reference circuitry will appear in the digital results. The use of an active reference source is recommended. The LM4040 and LM4050 shunt reference families and the LM4132 and LM4140 series reference families are excellent choices for a reference source.

Power and Ground Planes

A single ground plane and the use of two or more power planes is recommended. The power planes should all be in the same board layer and will define the analog, digital, and high power board areas. Lines associated with these areas should always be routed within their respective areas.

The GND pin on the ADC121S705 should be connected to the ground plane at a quiet point. Avoid connecting the GND pin too close to the ground point of a microprocessor, microcontroller, digital signal processor, or other high power digital device.
APPLICATION CIRCUITS

The following figures are examples of the ADC121S705 in typical application circuits. These circuits are basic and will generally require modification for specific circumstances.

Data Acquisition

Figure 61 shows a basic low cost, low power data acquisition circuit. Maximum clock rate with a minimum sample rate can reduce the power consumption further.

![Figure 61. Low cost, low power Data Acquisition System](image)

Pressure Sensor

Figure 62 shows an example of interfacing a pressure sensor to the ADC121S705. A digital-to-analog converter (DAC) is used to bias the pressure sensor. The DAC081S101 provides a means for dynamically adjusting the sensitivity of the sensor. A shunt reference voltage of 2.5V is used as the reference for the ADC121S705. The ADC121S705, DAC081S101, and the LM4040 are all powered from the same voltage source.

![Figure 62. Interfacing the ADC121S705 for a Pressure Sensor](image)
## REVISION HISTORY

Changes from Revision A (March 2013) to Revision B

<table>
<thead>
<tr>
<th>Change Description</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>Changed layout of National Data Sheet to TI format</td>
<td>23</td>
</tr>
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</table>
## PACKAGING INFORMATION

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<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead/Ball Finish</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC121S705CIMM/NOPB</td>
<td>NRND</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU SN</td>
<td>Level-1-260C-UNLIM</td>
<td>0 to 0</td>
<td>X1AC</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION

### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

### REEL DIMENSIONS

<table>
<thead>
<tr>
<th>Reel Diameter</th>
<th>Reel Width (W1)</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- **Schematic**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width (W1) (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin 1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC121S705CIMM/NOPB</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>1000</td>
<td>178.0</td>
<td>12.4</td>
<td>5.3</td>
<td>3.4</td>
<td>1.4</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*
**TAPE AND REEL BOX DIMENSIONS**

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC121S705CIMM/NOPB</td>
<td>VSSOP</td>
<td>DGK</td>
<td>8</td>
<td>1000</td>
<td>210.0</td>
<td>185.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
DGK (S-PDSO-G8) PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO-187 variation AA, except interlead flash.

4073329/E 05/06
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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