ADC3421-Q1 Automotive, Quad-Channel, 12-Bit, 25-MSPS Analog-to-Digital Converter

1 Features

- AEC-Q100 Qualified for automotive applications
  - Temperature grade 1: –40°C to 125°C T_A
- Quad channel
- 12-Bit resolution
- Single supply: 1.8 V
- Serial LVDS interface
- Flexible input clock buffer with divide-by-1, -2, -4
- SNR = 71.1 dBFS, SFDR = 90 dBc at f_{IN} = 10 MHz
- Ultra-low power consumption:
  - 44 mW/Ch at 25 MSPS
- Channel isolation: 105 dB
- Internal dither and chopper
- Support for multichip synchronization

2 Applications

- Solid state LiDAR
- Motor control feedback
- Nondestructive testing
- Radar and smart antenna arrays
- Munitions guidance

3 Description

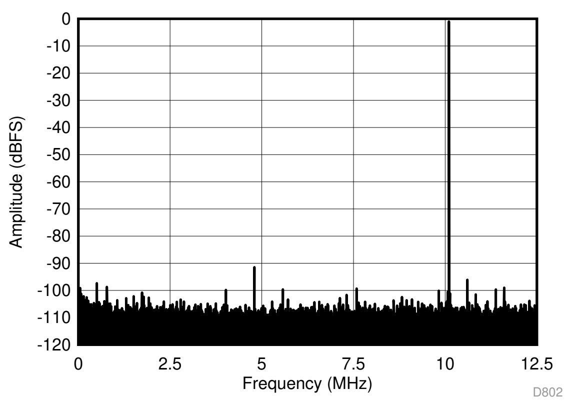
The ADC3421-Q1 is an automotive-grade, high-linearity, ultra-low power, quad-channel, 12-bit, 25-MSPS analog-to-digital converter (ADC). The device is designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider gives more flexibility for system clock architecture design, and the SYSREF input enables complete system synchronization. The ADC3421-Q1 supports serial low-voltage differential signaling (LVDS) in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 12-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ADC3421-Q1	VQFNP (56)	8.00 mm × 8.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Spectrum at 10-MHz IF
SFDR = 90 dBc, SNR = 71.2 dBFS,
SINAD = 71.1 dBFS, THD = 89 dBc



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (December 2019) to Revision A	Page
• Changed the *Register Initialization* section	27
• Changed Figure 50	29

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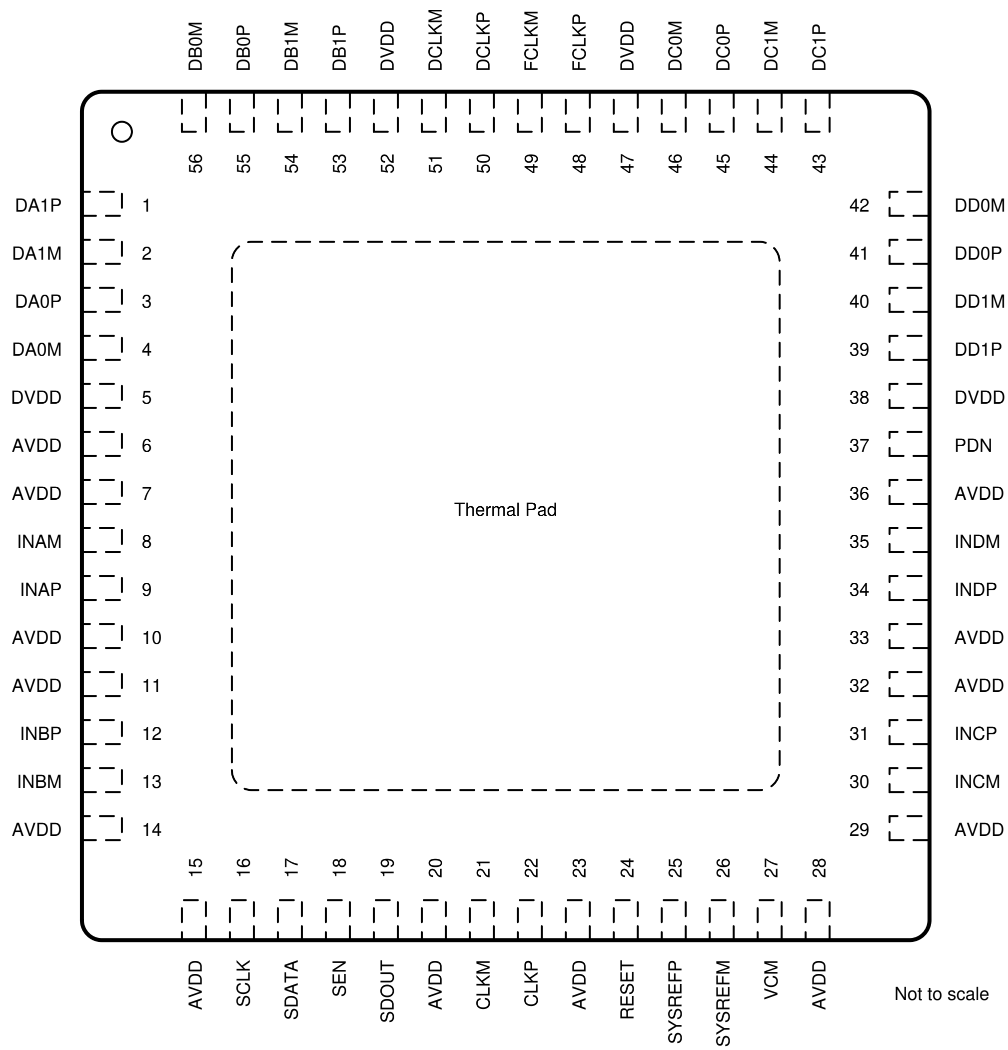
5 Pin Configuration and Functions

RWE Package
VQFNP-56
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	6, 7, 10, 11, 14, 15, 20, 23, 28, 29, 32, 33, 36	I	Analog 1.8-V power supply
CLKM	21	I	Negative differential clock input for the ADC
CLKP	22	I	Positive differential clock input for the ADC
DA0M	4	O	Negative serial LVDS output for wire-0 of channel A
DA0P	3	O	Positive serial LVDS output for wire-0 of channel A
DA1M	2	O	Negative serial LVDS output for wire-1 of channel A
DA1P	1	O	Positive serial LVDS output for wire-1 of channel A
DB0M	56	O	Negative serial LVDS output for wire-0 of channel B
DB0P	55	O	Positive serial LVDS output for wire-0 of channel B
DB1M	54	O	Negative serial LVDS output for wire-1 of channel B
DB1P	53	O	Positive serial LVDS output for wire-1 of channel B
DC0M	46	O	Negative serial LVDS output for wire-0 of channel C
DC0P	45	O	Positive serial LVDS output for wire-0 of channel C
DC1M	44	O	Negative serial LVDS output for wire-1 of channel C
DC1P	43	O	Positive serial LVDS output for wire-1 of channel C
DD0M	42	O	Negative serial LVDS output for wire-0 of channel D
DD0P	41	O	Positive serial LVDS output for wire-0 of channel D
DD1M	40	O	Negative serial LVDS output for wire-1 of channel D
DD1P	39	O	Positive serial LVDS output for wire-1 of channel D
DCLKM	51	O	Negative bit clock output
DCLKP	50	O	Positive bit clock output
DVDD	5, 38, 47, 52	I	Digital 1.8-V power supply
FCLKM	49	O	Negative frame clock output
FCLKP	48	O	Positive frame clock output
INAM	8	I	Negative differential analog input for channel A
INAP	9	I	Positive differential analog input for channel A
INBM	13	I	Negative differential analog input for channel B
INBP	12	I	Positive differential analog input for channel B
INCM	30	I	Negative differential analog input for channel C
INCP	31	I	Positive differential analog input for channel C
INDM	35	I	Negative differential analog input for channel D
INDP	34	I	Positive differential analog input for channel D
PDN	37	I	Power-down control. This pin can be configured using the SPI. This pin has an internal 150-kΩ pulldown resistor.
RESET	24	I	Hardware reset; active high. This pin has an internal 150-kΩ pulldown resistor.
SCLK	16	I	Serial interface clock input. This pin has an internal 150-kΩ pulldown resistor.
SDATA	17	I	Serial interface data input. This pin has an internal 150-kΩ pulldown resistor.
SDOUT	19	O	Serial interface data output
SEN	18	I	Serial interface enable; active low. This pin has an internal 150-kΩ pullup resistor to AVDD.
SYSREFM	26	I	Negative external SYSREF input
SYSREFP	25	I	Positive external SYSREF input
VCM	27	O	Common-mode voltage for analog inputs
Thermal Pad	—	—	Connect thermal pad to ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Analog supply voltage range, AVDD		–0.3	2.1	V
Digital supply voltage range, DVDD		–0.3	2.1	V
Voltage applied to input pins	INAP, INBP, INCP, INDP, INAM, INBM, INCM, INDM	–0.3	min (1.9, AVDD + 0.3)	V
	CLKP, CLKM	–0.3	AVDD + 0.3	
	SYSREFP, SYSREFM	–0.3	AVDD + 0.3	
	SCLK, SEN, SDATA, RESET, PDN	–0.3	3.9	
Temperature	Operating junction, T_J		150	ºC
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C5	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
Supplies						
AVDD	Analog supply voltage range		1.7	1.8	1.9	V
DVDD	Digital supply voltage range		1.7	1.8	1.9	V
Analog Input						
V_{ID}	Differential input voltage	For input frequencies < 450 MHz			2	V_{PP}
		For input frequencies < 600 MHz			1	
V_{IC}	Input common-mode voltage			VCM ± 0.025		V
Clock Input						
	Input clock frequency	Sampling clock frequency	15(2)		25	MSPS
	Input clock amplitude (differential)	Sine wave, ac-coupled	0.2	1.5		V_{PP}
		LPECL, ac-coupled		1.6		
		LVDS, ac-coupled		0.7		
	Input clock duty cycle		35%	50%	65%	
	Input clock common-mode voltage			0.95		V
Digital Outputs						
C_{LOAD}	Maximum external load capacitance from each output pin to GND			3.3		pF
R_{LOAD}	Single-ended load resistance			100		Ω
Temperature						
T_J	Operating Junction Temperature		–40		125	°C

(1) After power-up, use only the RESET pin to reset the device for the first time; see the *Register Initialization* section for details.
(2) See Table 1 for details.

6.4 Thermal Information

THERMAL METRIC[1]		ADC3421-Q1 RWE (VQFNP) 56 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	20.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	8.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	5.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	5.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics: General

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 125°C, maximum sampling rate, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
	ADC clock frequency					25	MSPS
	Resolution			12			Bits
	1.8-V analog supply current				54	71	mA
	1.8-V digital supply current				45	71	mA
	Total power dissipation				177	240	mW
	Global power-down dissipation				5	17	mW
	Standby power-down dissipation				34	75	mW
Analog Input							
	Differential input full-scale				2.0		V_{PP}
r_i	Input resistance	Differential at dc			6.6		kΩ
c_i	Input capacitance	Differential at dc			3.7		pF
$V_{OC(VCM)}$	VCM common-mode voltage output				0.95		V
	VCM output current capability				10		mA
	Input common-mode current	Per analog input pin			1.5		µA/MSPS
	Analog input bandwidth (3 dB)	50-Ω differential source driving 50-Ω termination across INP and INM			540		MHz
DC accuracy							
E_O	Offset error			–25		25	mV
α_{EO}	Temperature coefficient of offset error				± 0.024		mV/°C
$E_{G(REF)}$	Gain error as a result of internal reference inaccuracy alone			–2		2	%FS
$E_{G(CHAN)}$	Gain error of channel alone				–2		%FS
$\alpha_{(EGCHAN)}$	Temperature coefficient of $E_{G(CHAN)}$				±0.008		Δ%FS/Ch
Channel-to-channel Isolation							
	Crosstalk[1]	f_{IN} = 10 MHz	Near channel		105		dB
			Far channel		105		
		f_{IN} = 100 MHz	Near channel		95		
			Far channel		105		
		f_{IN} = 200 MHz	Near channel		94		
			Far channel		105		
		f_{IN} = 230 MHz	Near channel		92		
			Far channel		105		
		f_{IN} = 300 MHz	Near channel		85		
			Far channel		105		

(1) Crosstalk is measured with a –1-dBFS input signal on the aggressor channel and no input on the victim channel.

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6.6 Electrical Characteristics: AC Performance

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 125°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DITHER ON			DITHER OFF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
SNR	Signal-to-noise ratio (from 1-MHz offset)	f_{IN} = 10 MHz		70.9			71.1		dBFS
		f_{IN} = 20 MHz	68.9	70.7			70.9		
		f_{IN} = 70 MHz		70.4			70.6		
		f_{IN} = 100 MHz		70.3			70.5		
		f_{IN} = 170 MHz		69.7			69.9		
		f_{IN} = 230 MHz		68.9			69.1		
	Signal-to-noise ratio (full Nyquist band)	f_{IN} = 10 MHz		70.2			70.5		dBFS
		f_{IN} = 20 MHz		70.1			70.3		
		f_{IN} = 70 MHz		69.8			70.0		
		f_{IN} = 100 MHz		69.6			69.8		
		f_{IN} = 170 MHz		69.2			69.3		
		f_{IN} = 230 MHz		68.3			68.5		
NSD(1)	Noise spectral density (averaged across Nyquist zone)	f_{IN} = 10 MHz		–141.5			–141.7		dBFS/Hz
		f_{IN} = 20 MHz		–141.3	–139.5		–141.5		
		f_{IN} = 70 MHz		–141.0			–141.2		
		f_{IN} = 100 MHz		–140.9			–141.1		
		f_{IN} = 170 MHz		–140.3			–140.5		
		f_{IN} = 230 MHz		–139.5			–139.7		
SINAD(1)	Signal-to-noise and distortion ratio	f_{IN} = 10 MHz		71			71.1		dBFS
		f_{IN} = 20 MHz	67.9	70.8			70.9		
		f_{IN} = 70 MHz		69.5			70		
		f_{IN} = 100 MHz		70.5			70.7		
		f_{IN} = 170 MHz		69.6			69.8		
		f_{IN} = 230 MHz		68.7			68.7		
ENOB(1)	Effective number of bits	f_{IN} = 10 MHz		11.5			11.5		Bits
		f_{IN} = 20 MHz	11	11.4			11.4		
		f_{IN} = 70 MHz		11.4			11.4		
		f_{IN} = 100 MHz		11.4			11.4		
		f_{IN} = 170 MHz		11.3			11.3		
		f_{IN} = 230 MHz		11.1			11.1		
SFDR	Spurious-free dynamic range	f_{IN} = 10 MHz		93			90		dBc
		f_{IN} = 20 MHz	84	91			85		
		f_{IN} = 70 MHz		93			88		
		f_{IN} = 100 MHz		85			82		
		f_{IN} = 170 MHz		86			85		
		f_{IN} = 230 MHz		82			82		

(1) Reported from a 1-MHz offset.

Electrical Characteristics: AC Performance (continued)

Typical values are over the operating free-air temperature range, at T_A = 25°C, full temperature range is T_{MIN} = –40°C to T_{MAX} = 125°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER		TEST CONDITIONS	DITHER ON			DITHER OFF			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
HD2	Second-order harmonic distortion	f_{IN} = 10 MHz		93			92		dBc
		f_{IN} = 20 MHz	83	100			94		
		f_{IN} = 70 MHz		93			92		
		f_{IN} = 100 MHz		94			93		
		f_{IN} = 170 MHz		86			85		
		f_{IN} = 230 MHz		86			82		
HD3	Third-order harmonic distortion	f_{IN} = 10 MHz		96			90		dBc
		f_{IN} = 20 MHz	82	91			85		
		f_{IN} = 70 MHz		93			88		
		f_{IN} = 100 MHz		85			82		
		f_{IN} = 170 MHz		89			89		
		f_{IN} = 230 MHz		82			82		
Non HD2, HD3	Spurious-free dynamic range (excluding HD2, HD3)	f_{IN} = 10 MHz		99			92		dBc
		f_{IN} = 20 MHz	86	98			91		
		f_{IN} = 70 MHz		96			92		
		f_{IN} = 100 MHz		95			93		
		f_{IN} = 170 MHz		92			90		
		f_{IN} = 230 MHz		97			91		
THD	Total harmonic distortion	f_{IN} = 10 MHz		90			86		dBc
		f_{IN} = 20 MHz	78	90			83		
		f_{IN} = 70 MHz		89			85		
		f_{IN} = 100 MHz		84			80		
		f_{IN} = 170 MHz		84			83		
		f_{IN} = 230 MHz		80			79		
IMD3	Two-tone, third-order intermodulation distortion	f_{IN1} = 45 MHz, f_{IN2} = 50 MHz		–98			–98		dBFS
		f_{IN1} = 185 MHz, f_{IN2} = 190 MHz		–91			–91		

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6.7 Digital Characteristics

The dc specifications refer to the condition where the digital outputs are not switching, but are permanently at a valid logic level 0 or 1. AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted.

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
Digital Inputs (RESET, SCLK, SDATA, SEN, PDN)							
V_{IH}	High-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels	1.3			V
V_{IL}	Low-level input voltage		All digital inputs support 1.8-V and 3.3-V CMOS logic levels			0.4	V
I_{IH}	High-level input current	RESET, SDATA, SCLK, PDN	V_{HIGH} = 1.8 V		10		µA
		SEN(1)	V_{HIGH} = 1.8 V		0		µA
I_{IL}	Low-level input current	RESET, SDATA, SCLK, PDN	V_{LOW} = 0 V		0		µA
		SEN	V_{LOW} = 0 V		10		µA
DigitaL Inputs (SYSREFP, SYSREFM)							
V_{IH}	High-level input voltage				1.3		V
V_{IL}	Low-level input voltage				0.5		V
	Common-mode voltage for SYSREF				0.9		V
Digital Outputs (CMOS Interface, SDOUT)							
V_{OH}	High-level output voltage			DVDD – 0.1	DVDD		V
V_{OL}	Low-level output voltage				0	0.1	V
Digital Outputs (LVDS Interface)							
V_{ODH}	High-level output differential voltage		With an external 100-Ω termination	280	350	460	mV
V_{ODL}	Low-level output differential voltage		With an external 100-Ω termination	–460	–350	–280	mV
V_{OCM}	Output common-mode voltage				1.05		V

(1) SEN has an internal 150-kΩ pullup resistor to AVDD. SPI pins (SEN, SCLK, SDATA) can be driven by 1.8 V or 3.3 V CMOS buffers.

6.8 Timing Requirements: General

Typical values are at T_A = 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, unless otherwise noted. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 125°C.

			MIN	TYP	MAX	UNIT
t_A	Aperture delay		1.24	1.44	1.64	ns
	Aperture delay matching between two channels of the same device			±70		ps
	Aperture delay variation between two devices at same temperature and supply voltage			±150		ps
t_J	Aperture jitter			130		f_S rms
	Wake-up time:	Time to valid data after exiting standby power-down mode		35	200	µs
		Time to valid data after exiting global power-down mode (in this mode, both channels power down)		85	450	µs
	ADC latency(1):	2-wire mode (default)		9		Clock cycles
		1-wire mode		8		Clock cycles
t_{SU_SYSREF}	SYSREF reference time:	Setup time for SYSREF referenced to input clock rising edge	1000			ps
t_{H_SYSREF}		Hold time for SYSREF referenced to input clock rising edge	100			ps

(1) Overall latency = ADC latency + t_{PDI}.

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6.9 Timing Requirements: LVDS Output(1)(2)

Typical values are at T_A = 25°C, AVDD = DVDD = 1.8 V, and –1-dBFS differential input, 6x Serialization (2-Wire Mode), C_{LOAD} = 3.3 pF(3), and R_{LOAD} = 100 Ω(4), unless otherwise noted.. Minimum and maximum values are across the full temperature range: T_{MIN} = –40°C to T_{MAX} = 125°C.

			MIN	TYP	MAX	UNIT
t_{SU}	Data setup time: data valid to zero-crossing of differential output clock (CLKOUTP – CLKOUTM)(5)(6)	1-wire mode	1.3	1.48		ns
		2-wire mode	2.61	3.06		
t_{HO}	Data hold time: zero-crossing of differential output clock (CLKOUTP – CLKOUTM) to data becoming invalid(5)(6)	1-wire mode	1.32	1.57		ns
		2-wire mode	2.75	3.12		
t_{PDI}	Clock propagation delay: input clock falling edge cross-over to frame clock rising edge cross-over (15 MSPS < sampling frequency < 25 MSPS)	1-wire mode		$0.1 \times t_S + t_{DELAY}$		ns
		2-wire mode		$0.61 \times t_S + t_{DELAY}$		ns
t_{DELAY}	Delay time		3	4.5	5.9	ns
	LVDS bit clock duty cycle: duty cycle of differential clock (CLKOUTP – CLKOUTM)			49%		
t_{FALL}, t_{RISE}	Data fall time, data rise time: rise time measured from –100 mV to 100 mV, *15 MSPS ≤ Sampling frequency ≤ 25 MSPS*			0.11		ns
$t_{CLKRISE}$, $t_{CLKFALL}$	Output clock rise time, output clock fall time: rise time measured from –100 mV to 100 mV, *15 MSPS ≤ Sampling frequency ≤ 25 MSPS*			0.11		ns

(1) Measurements are done with a transmission line of a 100-Ω characteristic impedance between the device and load. Setup and hold time specifications take into account the effect of jitter on the output data and clock.
(2) Timing parameters are ensured by design and characterization and are not tested in production.
(3) C_{LOAD} is the effective external single-ended load capacitance between each output pin and ground.
(4) R_{LOAD} is the differential load resistance between the LVDS output pair.
(5) Data valid refers to a logic high of 100 mV and a logic low of –100 mV.
(6) Write relevant register settings as mentioned in Table 22.

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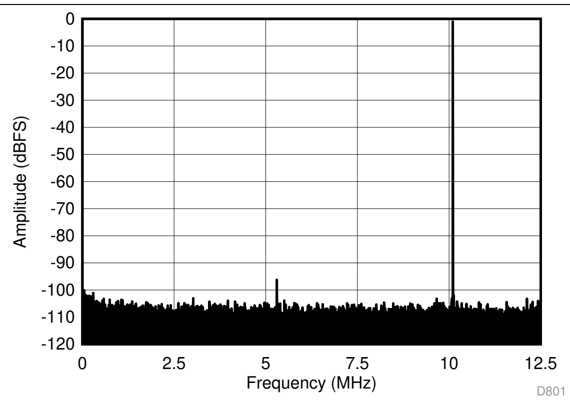
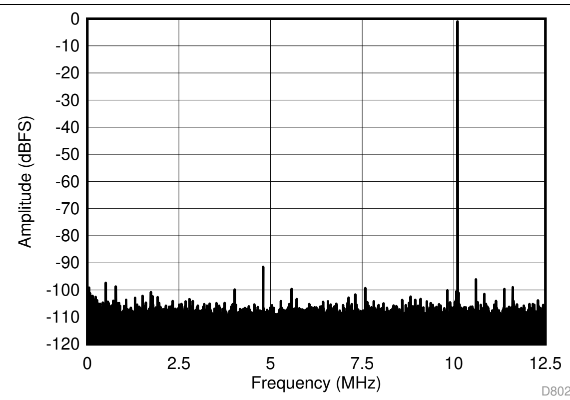
6.10 Typical Characteristics

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted).



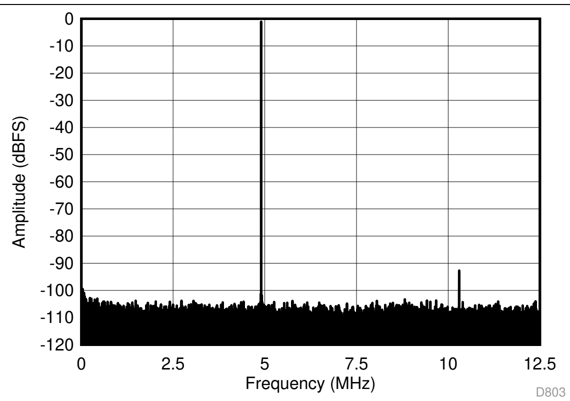
SFDR = 95 dBc, SNR = 71 dBFS, SINAD = 71 dBFS,
THD = 94 dBc, HD2 = 106 dBc, HD3 = 95 dBc

Figure 1. FFT for 10-MHz Input Signal (Dither On)



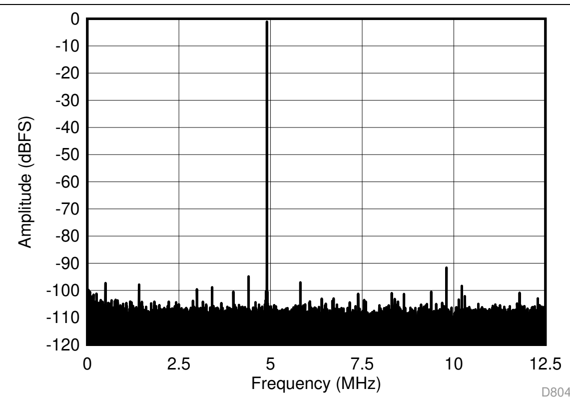
SFDR = 90 dBc, SNR = 71.2 dBFS, SINAD = 71.1 dBFS,
THD = 89 dBc, HD2 = 90 dBc, HD3 = 106 dBc

Figure 2. FFT for 10-MHz Input Signal (Dither Off)



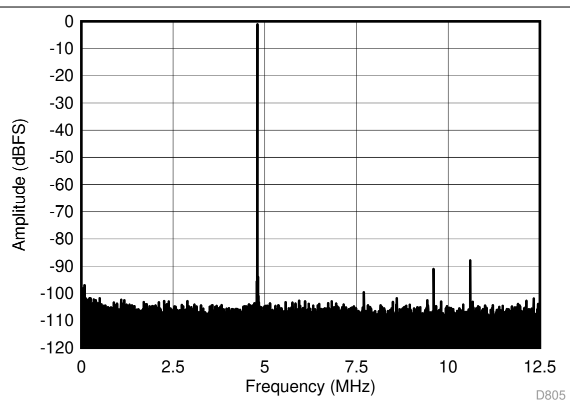
SFDR = 92 dBc, SNR = 70.5 dBFS, SINAD = 70.3 dBFS,
THD = 91 dBc, HD2 = 105 dBc, HD3 = 92 dBc

Figure 3. FFT for 70-MHz Input Signal (Dither On)



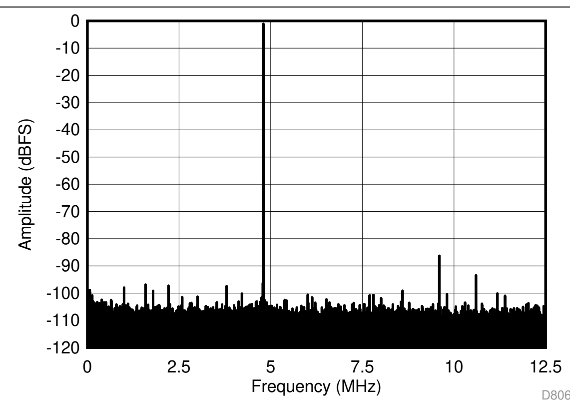
SFDR = 91 dBc, SNR = 70.7 dBFS, SINAD = 70.6 dBFS,
THD = 88 dBc, HD2 = 91 dBc, HD3 = 101 dBc

Figure 4. FFT for 70-MHz Input Signal (Dither Off)



SFDR = 87 dBc, SNR = 69.8 dBFS, SINAD = 69.7 dBFS,
THD = 85 dBc, HD2 = 90 dBc, HD3 = 87 dBc

Figure 5. FFT for 170-MHz Input Signal (Dither On)



SFDR = 85 dBc, SNR = 70 dBFS, SINAD = 69.8 dBFS,
THD = 86 dBc, HD2 = 85 dBc, HD3 = 92 dBc

Figure 6. FFT for 170-MHz Input Signal (Dither Off)

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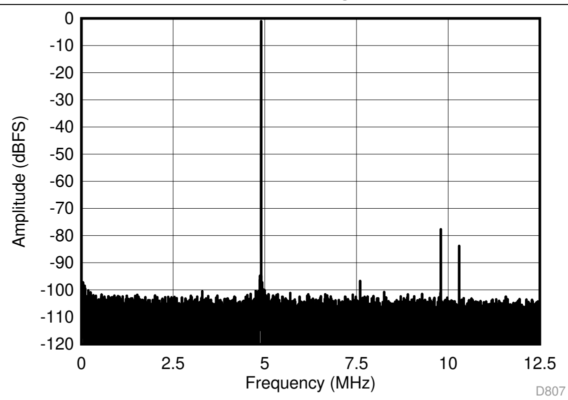
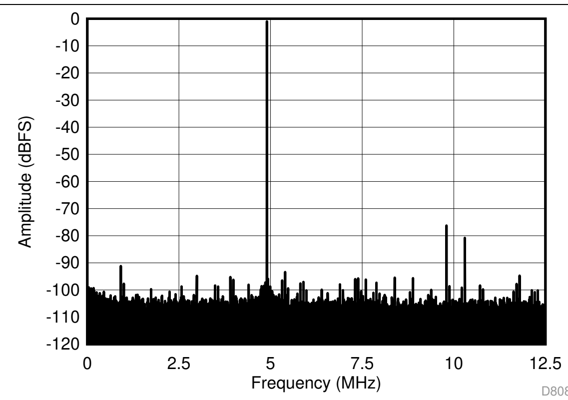
Typical Characteristics (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted).



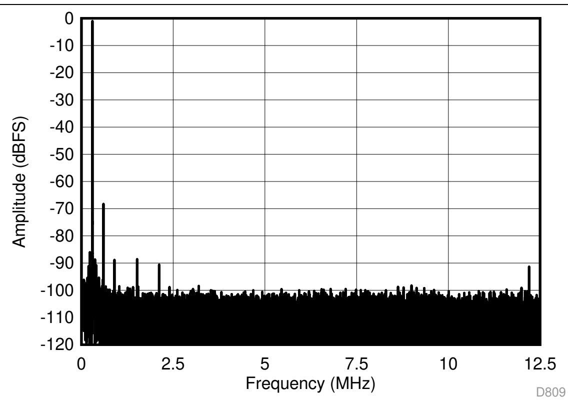
SFDR = 77 dBc, SNR = 68.2 dBFS, SINAD = 67.7 dBFS,
THD = 75 dBc, HD2 = 77 dBc, HD3 = 83 dBc

Figure 7. FFT for 270-MHz Input Signal (Dither On)



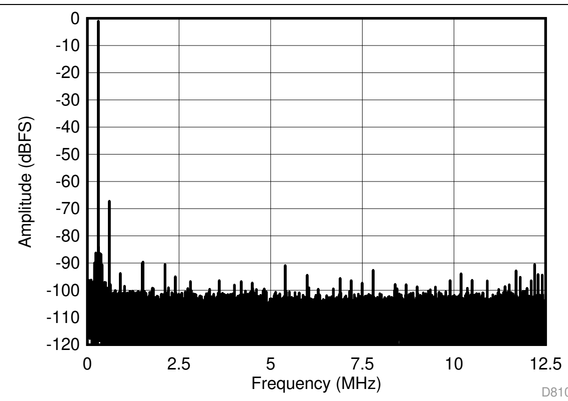
SFDR = 75 dBc, SNR = 68.4 dBFS, SINAD = 67.5 dBFS,
THD = 74 dBc, HD2 = 75 dBc, HD3 = 80 dBc

Figure 8. FFT for 270-MHz Input Signal (Dither Off)



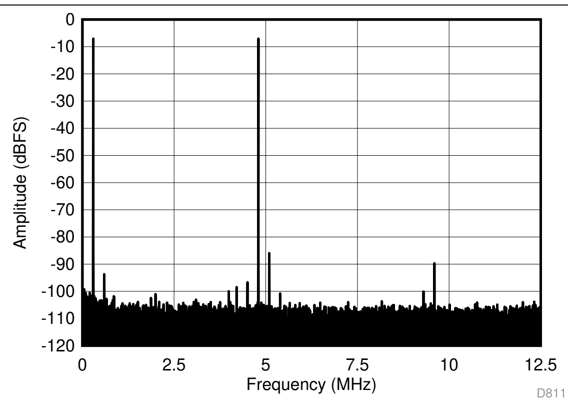
SFDR = 67 dBc, SNR = 66.4 dBFS, SINAD = 66.4 dBFS,
THD = 93 dBc, HD2 = 67 dBc, HD3 = 88 dBc

Figure 9. FFT for 450-MHz Input Signal (Dither On)



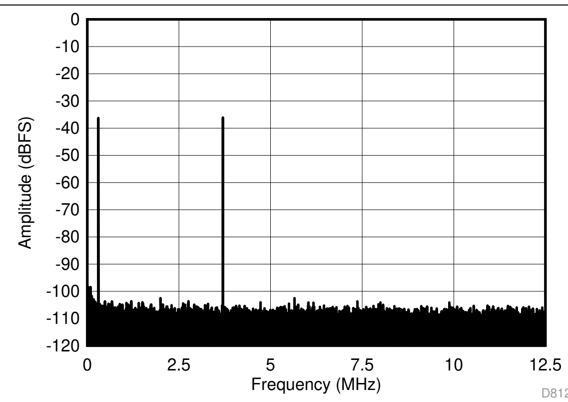
SFDR = 66 dBc, SNR = 66.5 dBFS, SINAD = 66.5 dBFS,
THD = 87 dBc, HD2 = 66 dBc, HD3 = 93 dBc

Figure 10. FFT for 450-MHz Input Signal (Dither Off)



f_{IN1} = 46 MHz, f_{IN2} = 50 MHz, IMD3 = 90,
each tone at = –7 dBFS

Figure 11. FFT for Two-Tone Input Signal (–7 dBFS at 46 MHz and 50 MHz)



f_{IN1} = 46 MHz, f_{IN2} = 50 MHz, IMD3 = 105,
each tone at = –36 dBFS

Figure 12. FFT for Two-Tone Input Signal (–36 dBFS at 46 MHz and 50 MHz)

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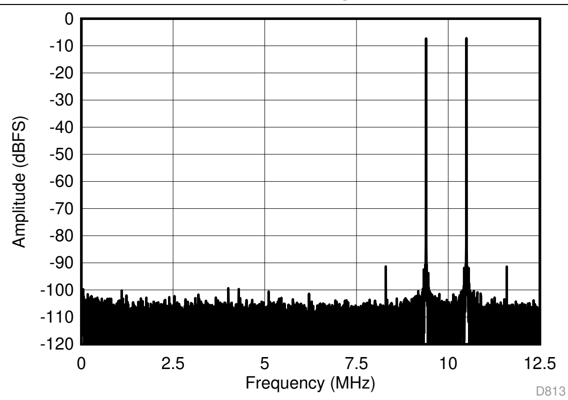
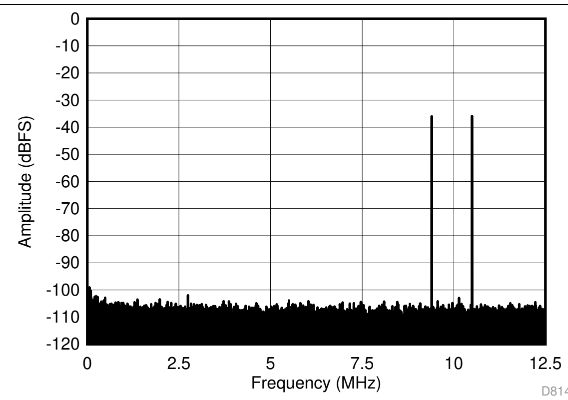
Typical Characteristics (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted).



f_{IN1} = 184.5 MHz, f_{IN2} = 189.5 MHz, IMD3 = 91, each tone at = –7 dBFS

Figure 13. FFT for Two-Tone Input Signal (–7 dBFS at 185 MHz and 190 MHz)



f_{IN1} = 184.5 MHz, f_{IN2} = 189.5 MHz, IMD3 = 98 dBFS, each tone at –36 dBFS

Figure 14. FFT for Two-Tone Input Signal (–36 dBFS at 185 MHz and 190 MHz)

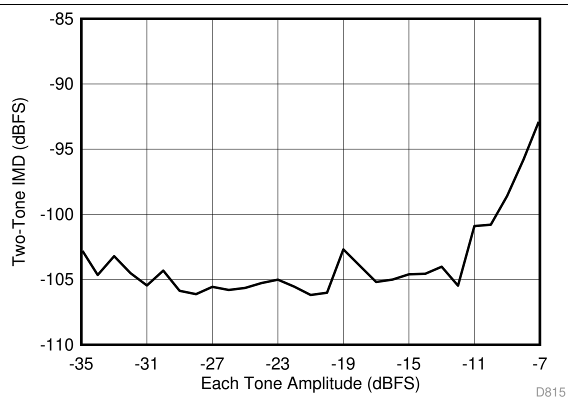


Figure 15. Intermodulation Distortion vs Input Amplitude (46 MHz and 50 MHz)

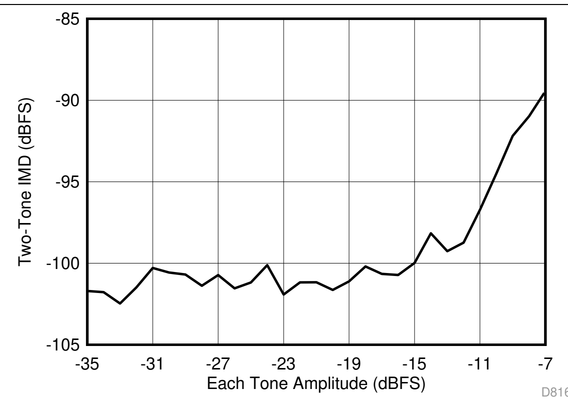


Figure 16. Intermodulation Distortion vs Input Amplitude (185 MHz and 190 MHz)

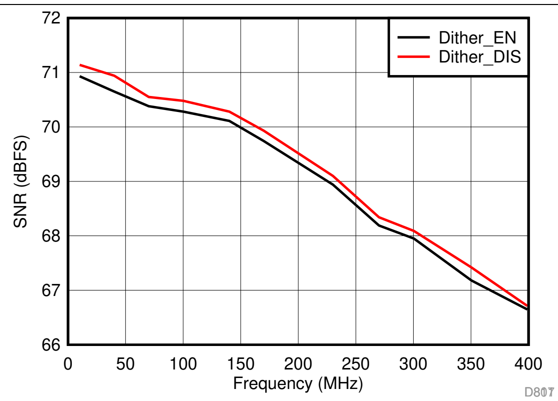


Figure 17. Signal-to-Noise Ratio vs Input Frequency

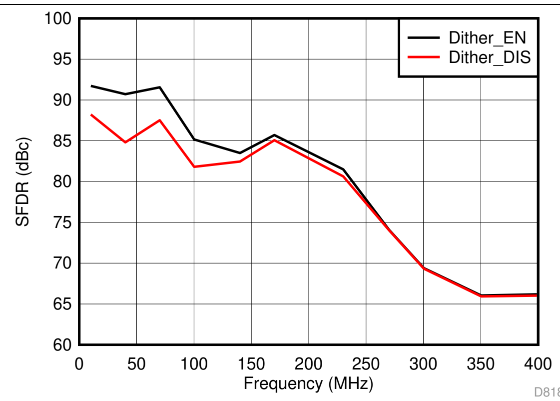


Figure 18. Spurious-Free Dynamic Range vs Input Frequency

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Typical Characteristics (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted).

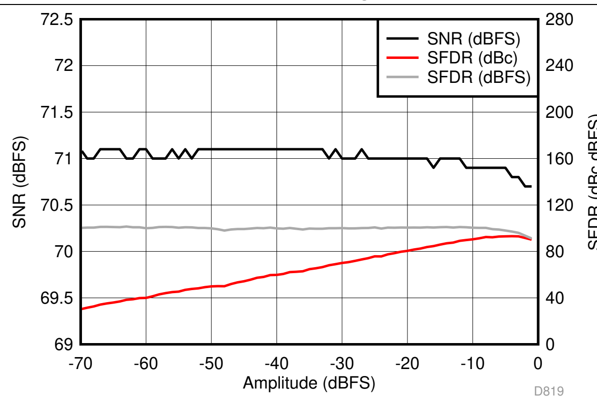

Figure 19. Performance vs Input Amplitude (30 MHz)

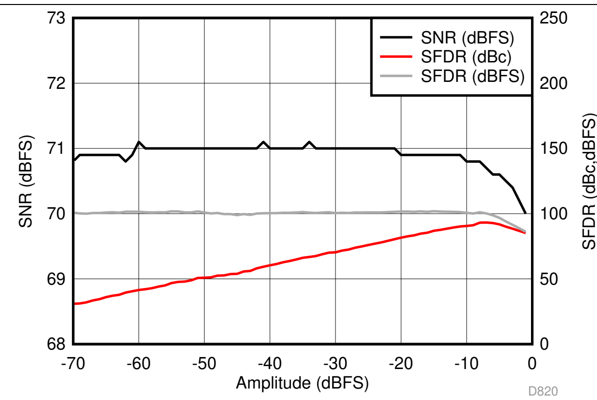

Figure 20. Performance vs Input Amplitude (170 MHz)

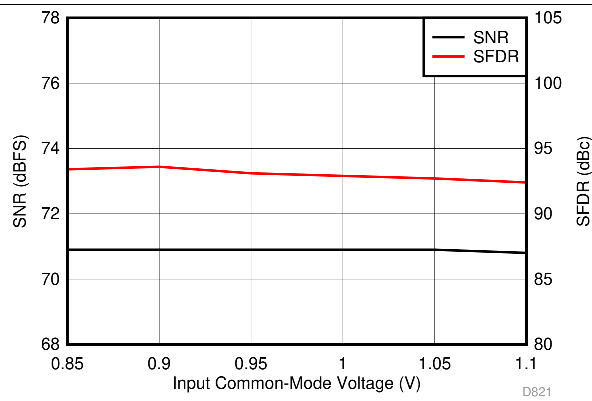

Figure 21. Performance vs Input Common-Mode Voltage (30 MHz)

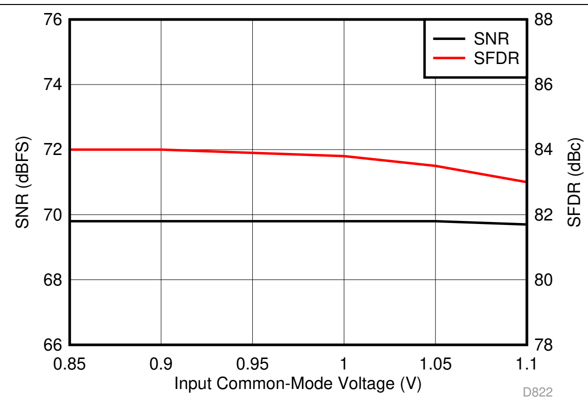

Figure 22. Performance vs Input Common-Mode Voltage (170 MHz)

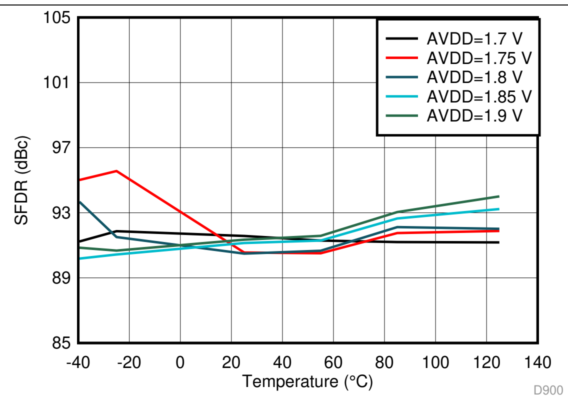

Figure 23. Spurious-Free Dynamic Range vs AVDD Supply and Temperature (30 MHz)

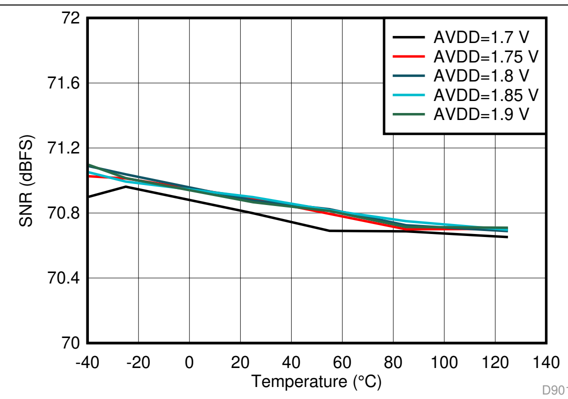

Figure 24. Signal-to-Noise Ratio vs AVDD Supply and Temperature (30 MHz)

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Typical Characteristics (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted).

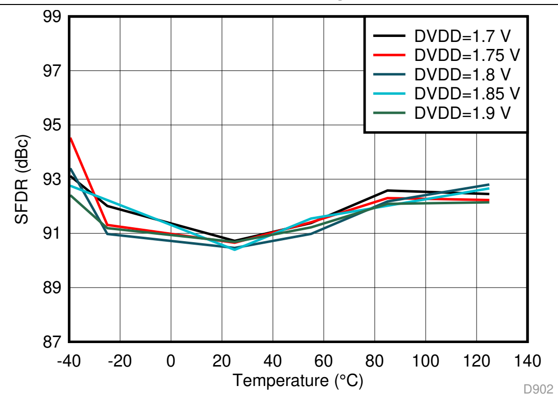


Figure 25. Spurious-Free Dynamic Range vs DVDD Supply and Temperature (30 MHz)

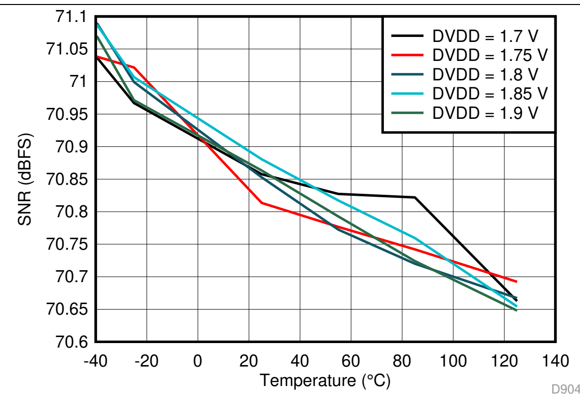


Figure 26. Signal-to-Noise Ratio vs DVDD Supply and Temperature (30 MHz)

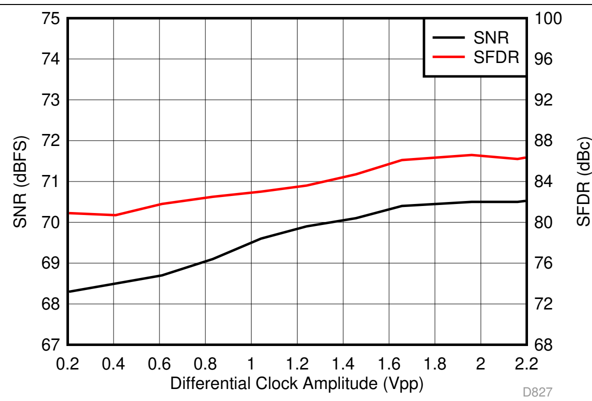


Figure 27. Performance vs Clock Amplitude (40 MHz)

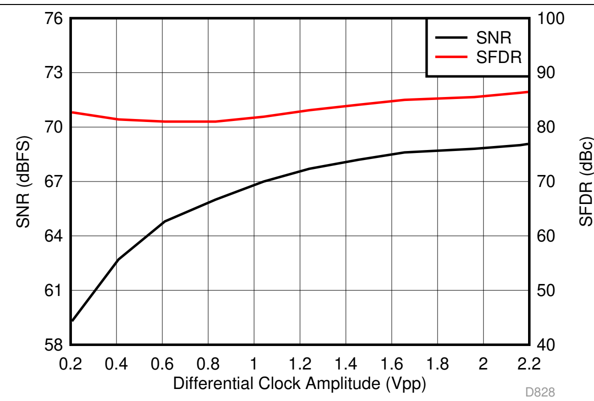


Figure 28. Performance vs Clock Amplitude (150 MHz)

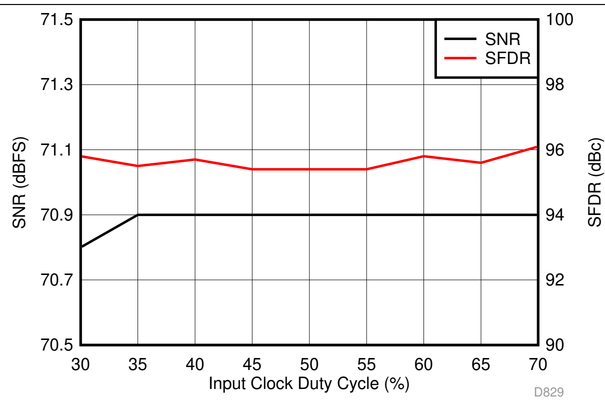


Figure 29. Performance vs Clock Duty Cycle (30 MHz)

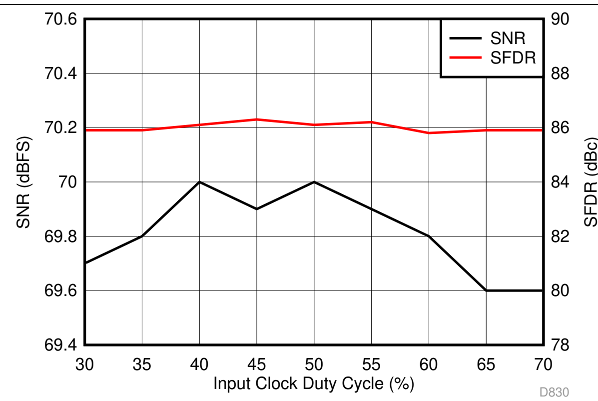


Figure 30. Performance vs Clock Duty Cycle (150 MHz)

Typical Characteristics (continued)

typical values are at T_A = 25°C, ADC sampling rate = 25 MSPS, 50% clock duty cycle, AVDD = 1.8 V, DVDD = 1.8 V, –1-dBFS differential input, 2-V_{PP} full-scale, 32k-point FFT, chopper disabled, and SNR reported with a 1-MHz offset from dc when chopper is disabled and from f_S / 2 when chopper is enabled (unless otherwise noted).

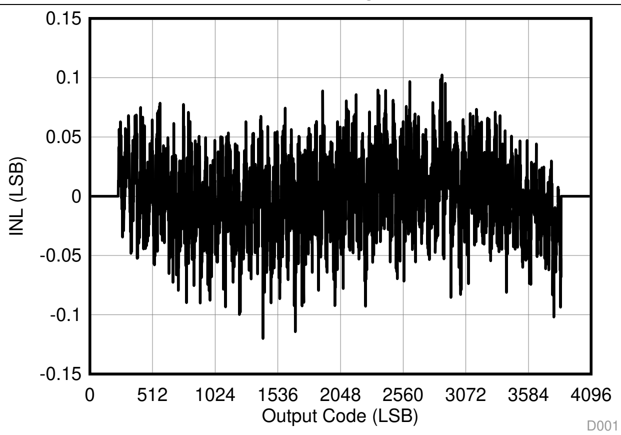


Figure 31. Integral Nonlinearity for a 20-MHz Input

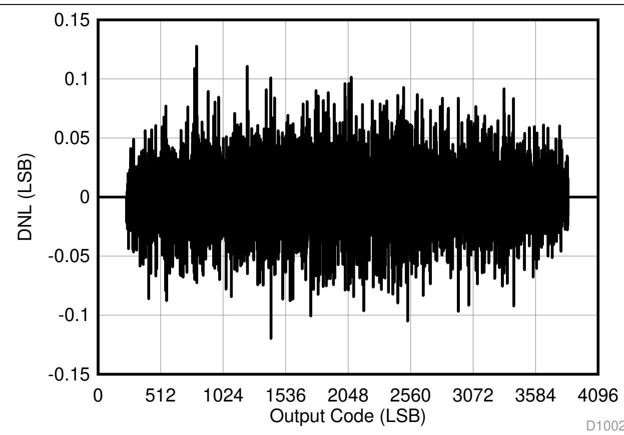
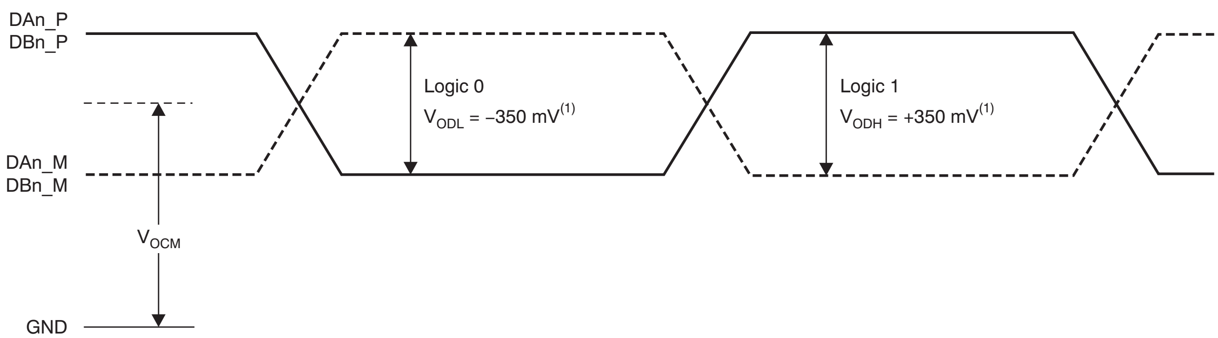


Figure 32. Differential Nonlinearity for a 20-MHz Input

7 Parameter Measurement Information

7.1 Timing Diagrams



(1) With an external 100-Ω termination.

Figure 33. Serial LVDS Output Voltage Levels

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Timing Diagrams (continued)

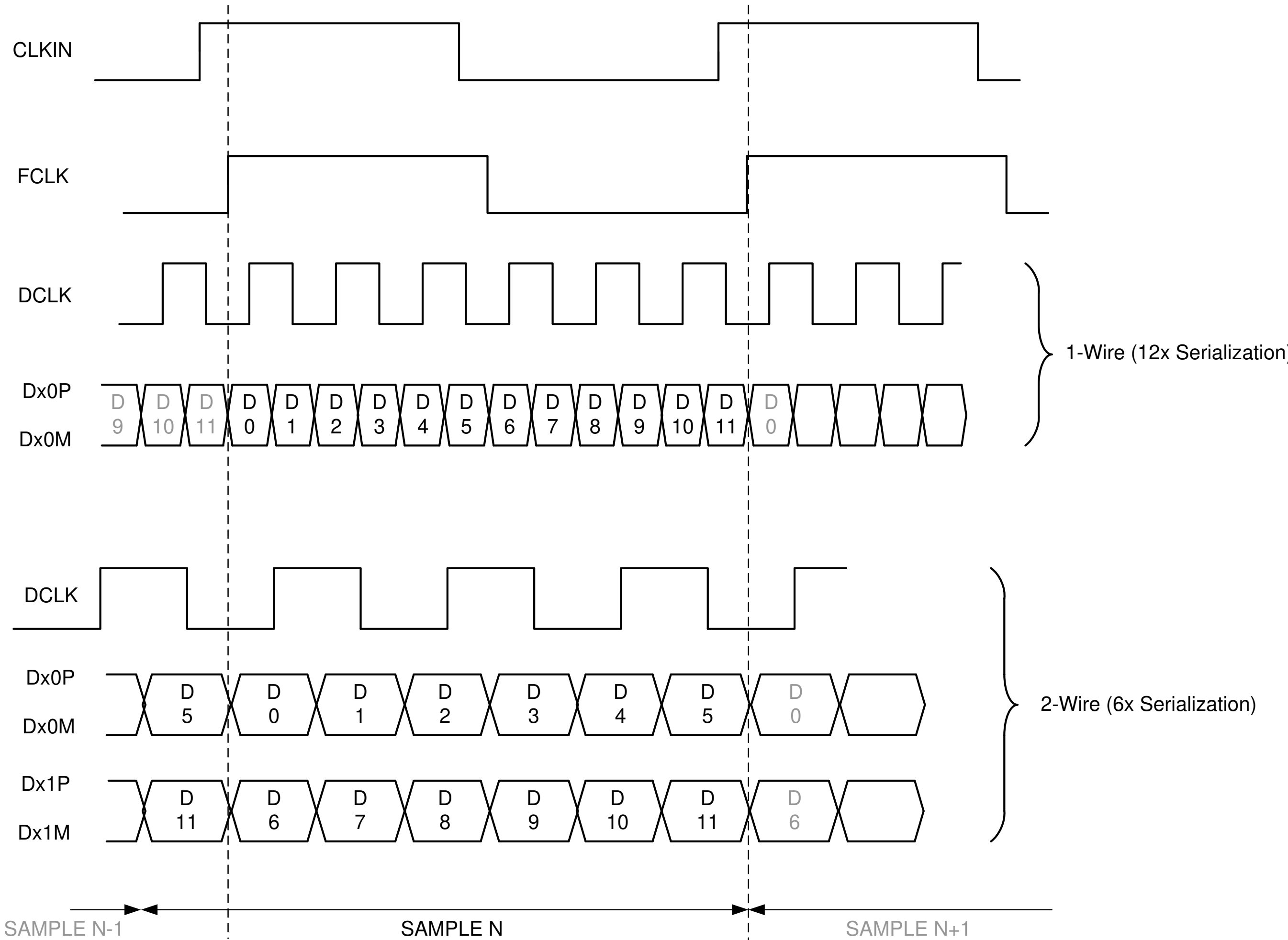


Figure 34. Output Timing Diagram

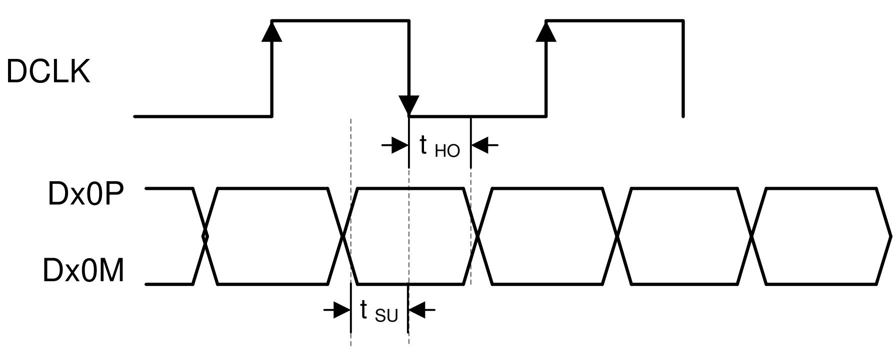


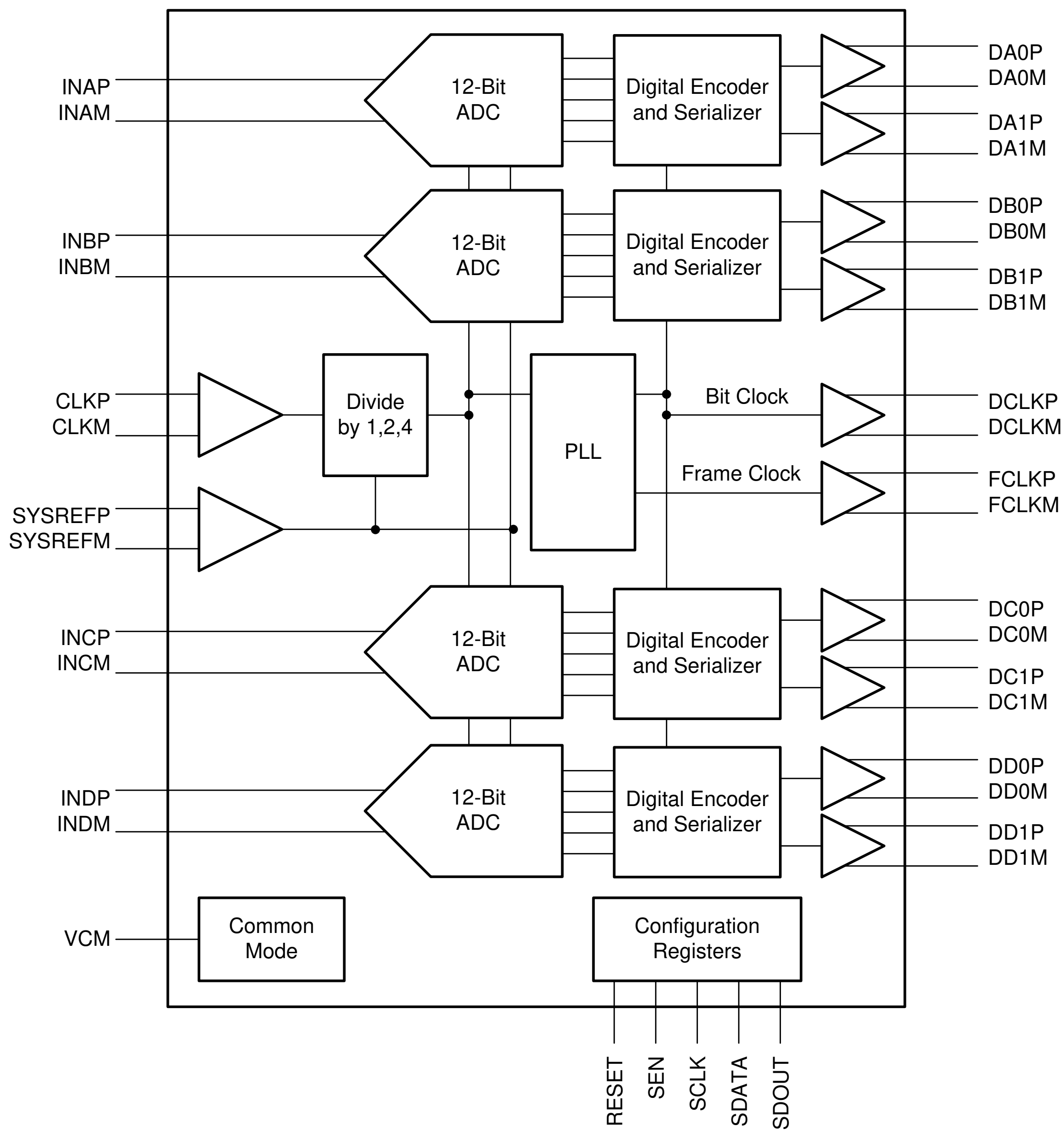
Figure 35. Setup and Hold Time

8 Detailed Description

8.1 Overview

The ADC3421-Q1 is an automotive-grade, high-linearity, ultra-low power, quad-channel, 12-bit, 25-MSPS analog-to-digital converter (ADC). The device is designed specifically to support demanding, high input frequency signals with large dynamic range requirements. An input clock divider gives more flexibility for system clock architecture design, and the SYSREF input enables complete system synchronization. The ADC3421-Q1 supports a serial low-voltage differential signaling (LVDS) interface in order to reduce the number of interface lines, thus allowing for high system integration density. The serial LVDS interface is two-wire, where each ADC data are serialized and output over two LVDS pairs. An internal phase-locked loop (PLL) multiplies the incoming ADC sampling clock to derive the bit clock that is used to serialize the 12-bit output data from each channel. In addition to the serial data streams, the frame and bit clocks are also transmitted as LVDS outputs.

8.2 Functional Block Diagram



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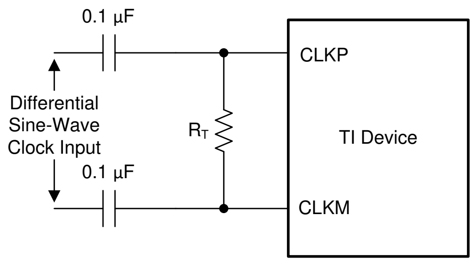
8.3 Feature Description

8.3.1 Analog Inputs

The ADC3421-Q1 analog signal inputs are designed to be driven differentially. Each input pin (INP, INM) must swing symmetrically between (VCM + 0.5 V) and (VCM – 0.5 V), resulting in a 2-V_{PP} (default) differential input swing. The input sampling circuit has a 3-dB bandwidth that extends up to 540 MHz (50-Ω source driving 50-Ω termination between INP and INM).

8.3.2 Clock Input

The device clock inputs can be driven differentially (sine, LVPECL, or LVDS) or single-ended (LVCMOS), with little or no difference in performance between them. The common-mode voltage of the clock inputs is set to 0.95 V using internal 5-kΩ resistors. The self-bias clock inputs of the ADC3421-Q1 can be driven by the transformer-coupled, sine-wave clock source or by the ac-coupled, LVPECL and LVDS clock sources, as shown in Figure 36, Figure 37, and Figure 38. See Figure 39 for details regarding the internal clock buffer.



NOTE: R_T = termination resistor, if necessary.

Figure 36. Differential Sine-Wave Clock Driving Circuit

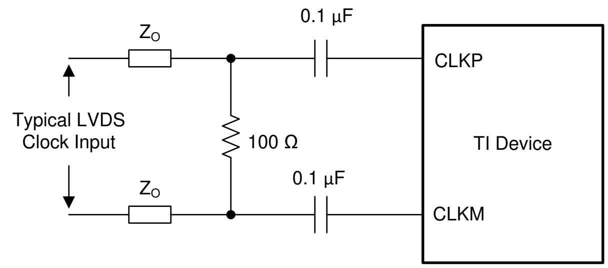


Figure 37. LVDS Clock Driving Circuit

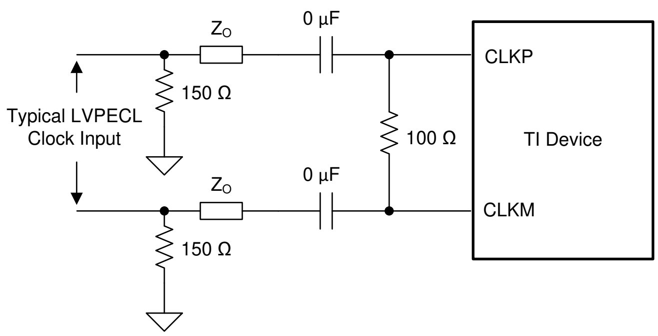
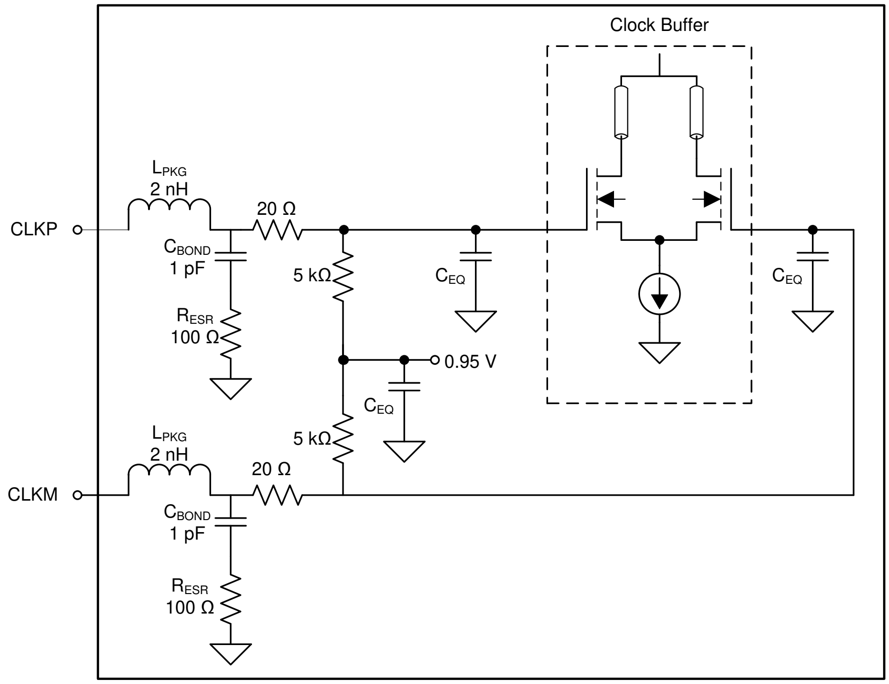


Figure 38. LVPECL Clock Driving Circuit



NOTE: C_{EQ} is 1 pF to 3 pF and is the equivalent input capacitance of the clock buffer.

Figure 39. Internal Clock Buffer

A single-ended CMOS clock can be ac-coupled to the CLKP input, with CLKM connected to ground with a 0.1-µF capacitor, as shown in Figure 40. However, for best performance the clock inputs must be driven differentially, thereby reducing susceptibility to common-mode noise. For high input frequency sampling, TI recommends using a clock source with very low jitter. Band-pass filtering of the clock source can help reduce the effects of jitter. There is no change in performance with a non-50% duty cycle clock input.

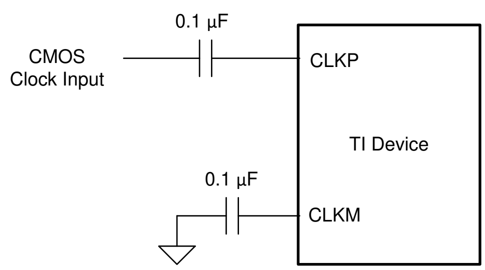


Figure 40. Single-Ended Clock Driving Circuit

8.3.2.1 SNR and Clock Jitter

The signal-to-noise ratio of the ADC is limited by three different factors, as shown in Equation 1. Quantization noise (typically 74 dB for a 12-bit ADC) and thermal noise limit SNR at low input frequencies, and the clock jitter sets SNR for higher input frequencies.

$$SNR_{ADC}[dBc] = -20 \cdot \log \sqrt{\left(10^{-\frac{SNR_{Quantization\_Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Thermal\_Noise}}{20}}\right)^2 + \left(10^{-\frac{SNR_{Jitter}}{20}}\right)^2} \quad (1)$$

The SNR limitation resulting from sample clock jitter can be calculated with Equation 2.

$$SNR_{Jitter}[dBc] = -20 \cdot \log\left(2\pi \cdot f_{in} \cdot t_{Jitter}\right) \quad (2)$$

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The total clock jitter (T_{Jitter}) has two components: the internal aperture jitter (130 fs for the device) which is set by the noise of the clock input buffer and the external clock. T_{Jitter} can be calculated with Equation 3.

$$t_{Jitter} = \sqrt{\left(t_{Jitter,Ext.Clock\_Input}\right)^2 + \left(t_{Aperture\_ADC}\right)^2} \quad (3)$$

External clock jitter can be minimized by using high-quality clock sources and jitter cleaners as well as band-pass filters at the clock input; a faster clock slew rate improves the ADC aperture jitter. The devices have a typical thermal noise of 70.6 dBFS and internal aperture jitter of 130 fs. The SNR, depending on the amount of external jitter for different input frequencies, is shown in Figure 41.

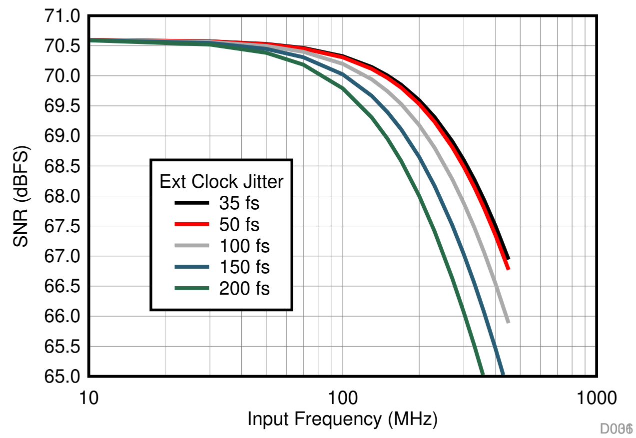

Figure 41. SNR vs Frequency for Different Clock Jitter

8.3.3 Digital Output Interface

The devices offer two different output format options, thus making interfacing to a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC) easy. Each option can be easily programmed using the serial interface, as shown in Table 1. The output interface options are:

- One-wire, 1x frame clock, 12x serialization with the DDR bit clock and
- Two-wire, 1x frame clock, 6x serialization with the DDR bit clock.

Table 1. Interface Rates

INTERFACE OPTIONS	SERIALIZATION	RECOMMENDED SAMPLING FREQUENCY (MSPS)		BIT CLOCK FREQUENCY (MHz)	FRAME CLOCK FREQUENCY (MHz)	SERIAL DATA RATE PER WIRE (Mbps)
		MINIMUM	MAXIMUM			
One-wire	12x	15		90	15	180
			25	150	25	300
Two-wire (Default after Reset)	6x	20 (1)		60	20	120
			25	75	25	150

(1) Use the LOW SPEED ENABLE register bits for low speed operation; see .

8.3.3.1 One-Wire Interface: 12x Serialization

In this interface option, the device outputs the data of each ADC serially on a single LVDS pair (one-wire). The data are available at the rising and falling edges of the bit clock (DDR bit clock). The ADC outputs a new word at the rising edge of every frame clock, starting with the LSB. The data rate is 12x sample frequency (12x serialization).

8.3.3.2 Two-Wire Interface: 6x Serialization

In two-wire interface ,the output data rate is 6x sample frequency because six data bits are output every clock cycle on each differential pair. Each ADC sample is sent over the two wires with the six MSBs on Dx1P, Dx1M and the six LSBs on Dx0P, Dx0M, as shown in Figure 42.

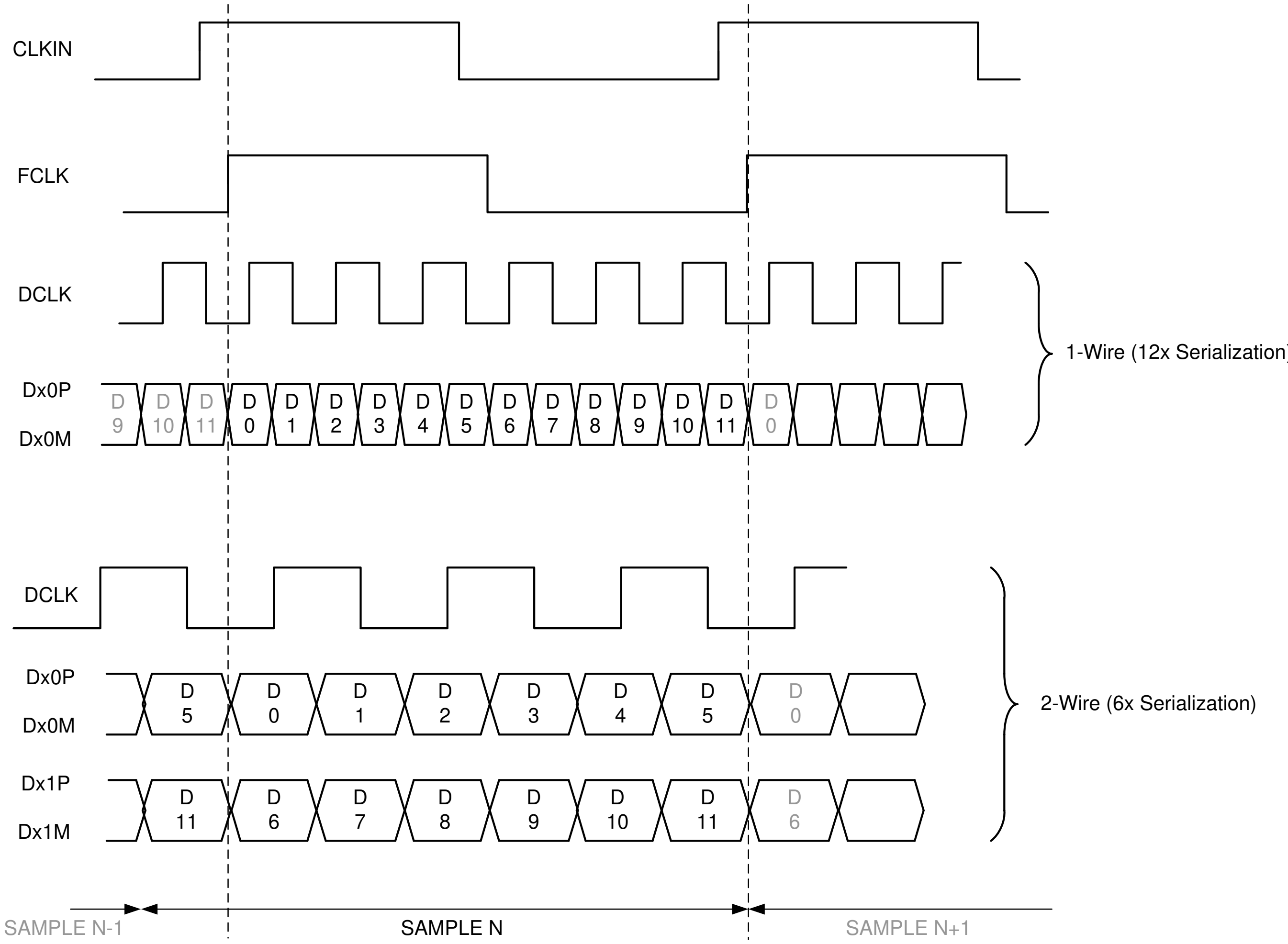

Figure 42. Output Timing Diagram

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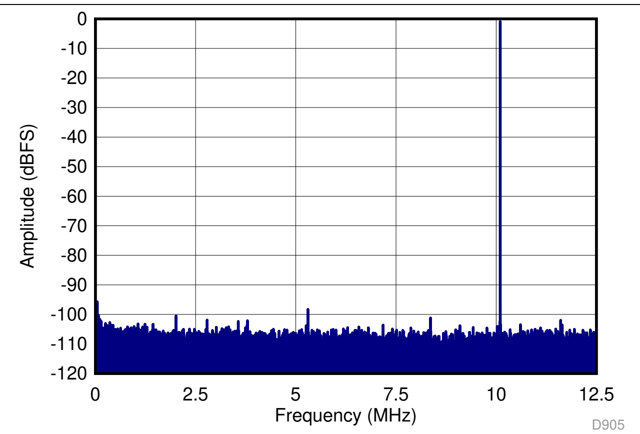
8.4 Device Functional Modes

8.4.1 Input Clock Divider

The devices are equipped with an optional internal divider on the clock input. The clock divider allows operation with a faster input clock (divide by 2 and divide by 4 options programmable using SPI), thus simplifying the system clock distribution design.

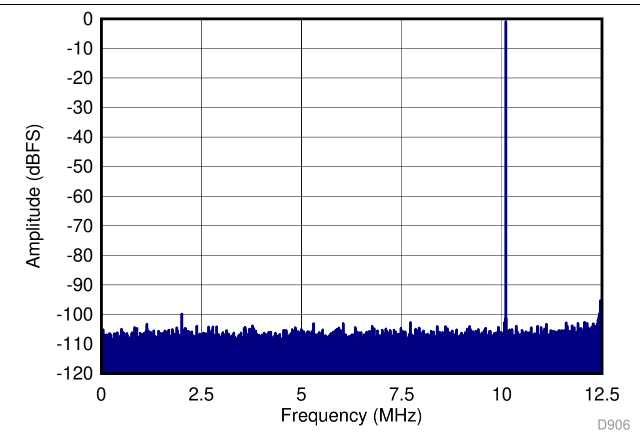
8.4.2 Chopper Functionality

The devices are equipped with an internal chopper front-end. Enabling the chopper function swaps the ADC noise spectrum by shifting the 1/f noise from dc to f_S / 2. Figure 43 shows the noise spectrum with the chopper off and Figure 44 shows the noise spectrum with the chopper on. This function is especially useful in applications requiring good ac performance at low input frequencies or in dc-coupled applications. The chopper can be enabled via SPI register writes and is recommended for input frequencies below 30 MHz. The chopper function creates a spur at f_S / 2 that must be filtered out digitally.



SNR = 71.1 dBFS, SINAD = 71.1 dBFS
SFDR = 97 dBc ,THD = 95 dBc

Figure 43. Chopper Off



SNR = 71 dBFS, SINAD = 71 dBFS
SFDR = 96 dBc, THD = 97 dBc

Figure 44. Chopper On

8.4.3 Power-Down Control

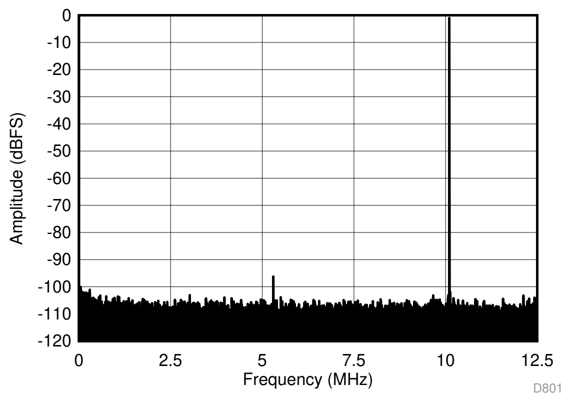
The power-down functions of the ADC3421-Q1 can be controlled either through the parallel control pin (PDN) or through an SPI register setting (see register 15h). The PDN pin can also be configured via SPI to a global power-down or standby functionality, as shown in Table 2.

Table 2. Power-Down Modes

FUNCTION	POWER CONSUMPTION (mW)	WAKE-UP TIME (µs)
Global power-down	5	85
Standby	34	35

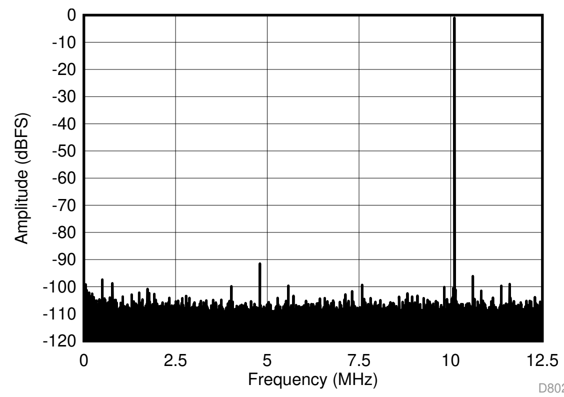
8.4.4 Internal Dither Algorithm

The ADC3421-Q1 uses an internal dither algorithm to achieve high SFDR and a clean spectrum. However, the dither algorithm marginally degrades SNR, creating a trade-off between SNR and SFDR. If desired, the dither algorithm can be turned off by using the DIS DITH CHx registers bits. Figure 45 and Figure 46 show the effect of using dither algorithms.



SFDR = 95 dBc, SNR = 71 dBFS, SINAD = 71 dBFS,
THD = 94 dBc, HD2 = 106 dBc, HD3 = 95 dBc

Figure 45. FFT for 10-MHz Input Signal (Chopper On, Dither On)



SFDR = 90 dBc, SNR = 71.2 dBFS, SINAD = 71.1 dBFS,
THD = 89 dBc, HD2 = 90 dBc, HD3 = 106 dBc

Figure 46. FFT for 10-MHz Input Signal (Chopper On, Dither Off)

8.4.5 Summary of Performance Mode Registers

Table 3 lists the location, value, and functions of performance mode registers in the device.

Table 3. Performance Modes

MODE	REGISTER SETTINGS	DESCRIPTION
Special modes	Registers 139 (bit 3), 239 (bit 3), 439 (bit 3), and 539 (bit 3)	Always write 1 for best performance
Disable dither	Registers 1 (bits 7:0), 134 (bits 5 and 3), 234 (bits 5 and 3), 434 (bits 5 and 3), and 534 (bits 5 and 3)	Disable dither to improve SNR
Disable chopper	Registers 122 (bit 1), 222 (bit 1), 422 (bit 1), and 522 (bit 1)	Disable chopper (shifts 1/f noise floor at dc)
High IF modes	Registers 11Dh (bit 1), 21Dh (bit 1), 31Dh (bit 7 and bit 1), 41Dh (bit 1), 51Dh (bit 1), 308h (bits 7-6), 608h (bits 7-6) and 61Dh (bit 7 and bit 1)	Improves HD3 by a couple of dB for IF > 100 MHz

8.4.6 Device Diagnostic Modes

The device offers various diagnostic modes to check proper device operation at system level. These modes can be enabled using the SPI. Outputs of these modes are stored in diagnostic read-only registers.

8.4.6.1 Internal Reference and Clock Status Check

Device is equipped with a mode to verify presence of a valid input clock, as well as status of on-chip ADC reference. When a valid clock input clock is absent at input clock pins (CLKP,CLKM) of ADC, device sets register bit CLK STATUS to '1'. Similarly, if internal reference block is malfunctioning for a channel, device sets register bits REF STATUS CHx to '1'. To read the status of internal reference from these pins:

1. First enable reference status check by setting register bit EN REF STATUS CHECK to '1'.
2. Read back register bits REF STATUS CHx on SDATA pin for desired channel (x = A, B, C or D).

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8.4.6.2 DC Input check

In this mode, an internally generated DC voltage can be forced by device to its analog inputs. Before forcing internal DC voltage, analog inputs must float. To enable forcing internal DC voltage, register bit EN DC FORCE must be set HIGH. Forced voltage is programmable by register bits DC FORCE[2:0], applied to all four channels together. In terms of output code, typical value of programmed DC voltage is given by equation mentioned below:

Output code= 368 × DC FORCE[2:0] + 745.

Output code is available on LVDS data outputs.

8.4.6.3 Mean and Variance Measurement

Mean and variance values of the ADC output can be analyzed using the on-chip statistical module available for individual channel for a programmable length of samples. These values are stored in register bits MEAN[11:0] and VAR[11:0] in 2s complement format. Equation for computing mean and variance values respectively are given below:

- $$Mean = \bar{x} = \sum_{n=1}^{N} \frac{S(n)}{N}$$
- $$Variance = \sum_{n=1}^{N} \frac{|S(n) - \bar{x}|}{N}$$

Where S(n) is n^{th} sample, N is total number of samples used for computation, programmed by register bits SAMPLES FOR STATS[1:0].

Follow steps mentioned below to read the mean and variance:

1. Enable Statistical Module by setting bit EN STATS to ‘1’.
2. Select desired channel through bits STATS CH SEL[1:0].
3. Program number of samples, N, using register bits SAMPLES FOR STATS[1:0].
4. Wait for at least 4N samples for module to compute and update the results.
5. Disable Statistical Module by resetting EN STATS bit to ‘0’.
6. Read back mean and variance values from register bits MEAN[11:0] and VAR[11:0]. These values are in 2s complement format.

8.4.6.4 Temperature Sensor

The device is equipped with a temperature sensor to measure internal junction temperature.

The temperature sensor output is a 9-bit digital data available in 2s complement format directly representing temperature in degree Celsius units. Temperature data is internally updated every $1024 \times T_{CLK} \times 16$ seconds where T_{CLK} period of sampling clock in seconds. Follow the steps mentioned below to read temperature sensor’s output:

1. Enable temperature sensor by setting bits EN TEMP SENSE and EN TEMP SENSE CONV to ‘1’.
2. Wait for at least $1024 \times T_{CLK} \times 16$ seconds for temperature sensor to update the data.
3. Disable temperature sensor by resetting the bit EN TEMP SENSE to ‘0’.
4. Load temperature sensor's data to register bits TEMPDATA[8:0] by setting register bit EN TEMP DATA READOUT to '1'.
5. Readout 9-bit temperature data from register bits TEMPDATA[8:0] located in register addresses 10h and 11h.

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8.5 Programming

The ADC3421-Q1 can be configured using a serial programming interface, as described in this section.

8.5.1 Serial Interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock), SDATA (serial interface data), and SDOUT (serial interface data output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data SDATA are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to very low speeds (of a few hertz) and also with a non-50% SCLK duty cycle.

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Programming (continued)

8.5.1.1 Register Initialization

After power-up, the internal registers **must** be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin (of durations greater than 10 ns), as shown in Figure 47. If required, the serial interface registers can be cleared during operation either:

1. Through a hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

8.5.1.1.1 Serial Register Write

The device internal register can be programmed with these steps:

1. Drive the SEN pin low,
2. Set the R/W bit to 0 (bit A15 of the 16-bit address),
3. Set bit A14 in the address field to 1,
4. Initiate a serial interface cycle by specifying the address of the register (A13 to A0) whose content must be written, and
5. Write the 8-bit data that are latched in on the SCLK rising edge.

Figure 47 and Table 4 show the timing requirements for the serial register write operation.

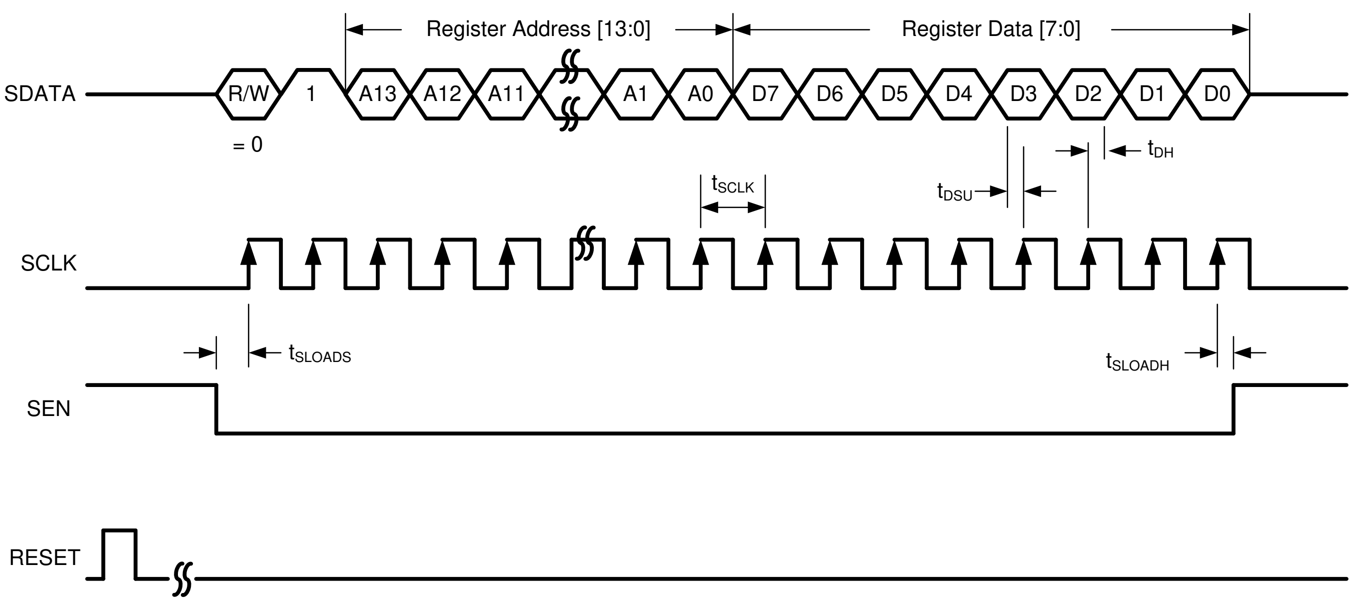

Figure 47. Serial Register Write Timing Diagram

Table 4. Serial Interface Timing(1)

		MIN	TYP	MAX	UNIT
f_{SCLK}	SCLK frequency (equal to 1 / t_{SCLK})	> dc		20	MHz
t_{SLOADS}	SEN to SCLK setup time	25			ns
t_{SLOADH}	SCLK to SEN hold time	25			ns
t_{DSU}	SDIO setup time	25			ns
t_{DH}	SDIO hold time	25			ns

(1) Typical values are at 25°C, full temperature range is from T_{MIN} = –40°C to T_{MAX} = 85°C, and AVDD = DVDD = 1.8 V, unless otherwise noted.

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8.5.1.1.2 Serial Register Readout

The device includes a mode where the contents of the internal registers can be read back using the SDOUT pin. This readback mode may be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low.
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers.
3. Set bit A14 in the address field to 1.
4. Initiate a serial interface cycle specifying the address of the register (A13 to A0) whose content must be read.
5. The device outputs the contents (D7 to D0) of the selected register on the SDOUT pin.
6. The external controller can latch the contents at the SCLK rising edge.
7. To enable register writes, reset the R/W register bit to 0.

When READOUT is disabled, the SDOUT pin is in a high-impedance mode. If serial readout is not used, the SDOUT pin must float. Figure 48 shows a timing diagram of the serial register read operation. Data appear on the SDOUT pin at the SCLK falling edge with an approximate delay (t_{SD_DELAY}) of 20 ns, as shown in Figure 49.

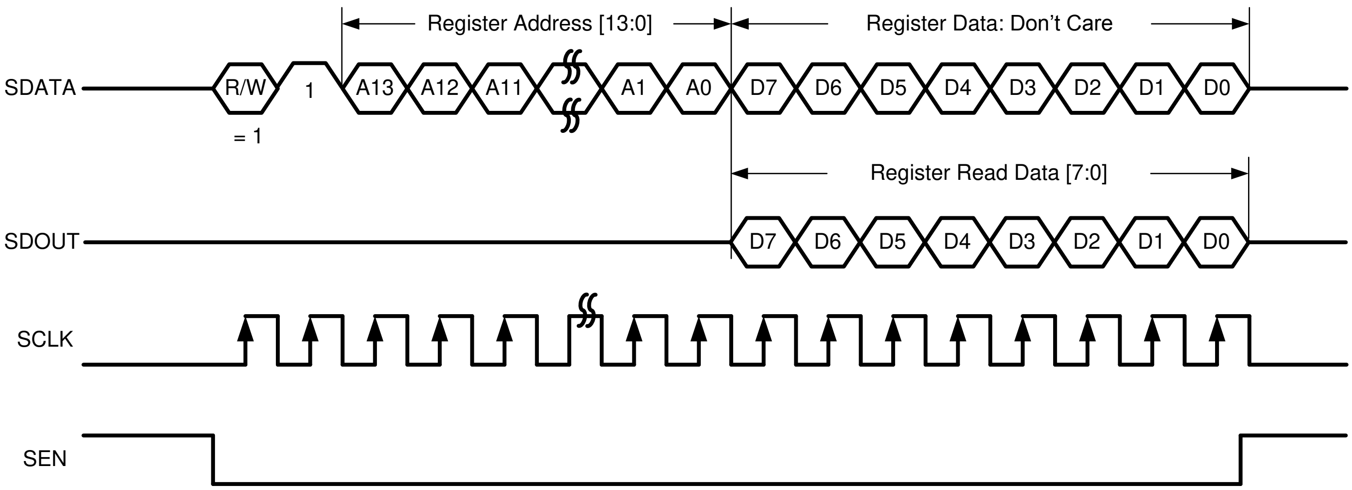

Figure 48. Serial Register Read Timing Diagram

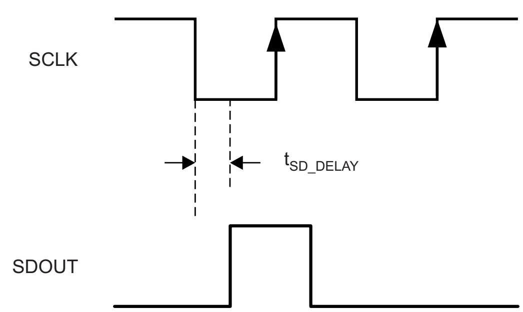

Figure 49. SDOUT Timing Diagram

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8.5.2 Register Initialization

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a high pulse on the RESET pin, as shown in Figure 50 and Table 5.

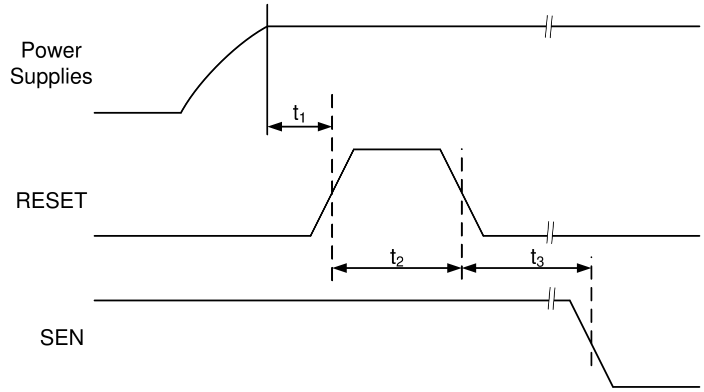

Figure 50. Initialization of Serial Registers after Power-Up

Table 5. Power-Up Timing

		MIN	TYP	MAX	UNIT
t_1	Power-on delay from power-up to active high RESET pulse	1			ms
t_2	Reset pulse duration: active high RESET pulse duration	10			ns
t_3	Register write delay from RESET disable to SEN active	100			ns

If required, the serial interface registers can be cleared during operation either:

1. Through hardware reset, or
2. By applying a software reset. When using the serial interface, set the RESET bit (D0 in register address 06h) high. This setting initializes the internal registers to the default values and then self-resets the RESET bit low. In this case, the RESET pin is kept low.

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8.6 Register Maps

Table 6. Register Map Summary

REGISTER ADDRESS, A[13:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
Register 01h	DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	
Register 02h	STATS CH SEL[1:0]		0	0	0	0	0	0
Register 03h	0	0	0	0	0	0	0	ODD EVEN
Register 04h	0	0	0	0	0	0	0	FLIP WIRE
Register 05h	0	0	0	0	0	0	0	1W-2W
Register 06h	0	0	0	0	0	0	TEST PATTERN EN	RESET
Register 07h	0	0	0	0	0	0	0	OVR ON LSB
Register 09h	0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
Register 0Ah	CHA TEST PATTERN				CHB TEST PATTERN			
Register 0Bh	CHC TEST PATTERN 0				CHD TEST PATTERN			
Register 0Eh	CUSTOM PATTERN[11:4]							
Register 0Fh	CUSTOM PATTERN[3:0]				0	0	0	0
Register 10h	REF STATUS CHB OR TEMPDATA [2]	REF STATUS CHD OR TEMPDATA [1]	REF STATUS CHA OR TEMPDATA [0]	CLK STATUS	TEMPDATA[6:4]			REF STATUS CHC OR TEMPDATA [3]
Register 11h	0	0	TEMPDATA [8:7]		0	0	0	0
Register 13h	0	EN REF STATUS CHECK	EN DC FORCE	EN STATS	0	0	LOW SPEED ENABLE	
Register 14h	0	EN TEMP SENS CONV	EN TEMP SENSE	0	0	EN TEMP DATA READOUT	0	0
Register 15h	CHA PDN	CHB PDN	CHC PDN	CHD PDN	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
Register 16h	MEAN[5:0]						0	0
Register 17h	0	0	MEAN[11:6]					
Register 18h	VAR[5:0]						0	0
Register 19h	0	0	VAR[11:6]					
Register 25h	LVDS SWING							
Register 27h	CLK DIV		0	0	0	0	0	0
Register 4Bh	0	0	0	0	0	0	SAMPLES FOR STATS[1:0]	
Register 11Dh	0	0	0	0	0	0	HIGH IF MODE0	0
Register 122h	0	0	0	0	0	0	DIS CHOP CHA	0
Register 134h	0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
Register 139h	0	0	0	0	SP1 CHA	0	0	0
Register 21Dh	0	0	0	0	0	0	HIGH IF MODE1	0
Register 222h	0	0	0	0	0	0	DIS CHOP CHD	0
Register 234h	0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0
Register 239h	0	0	0	0	SP1 CHD	0	0	0
Register 308h	HIGH IF MODE <5:4>		0	0	0	0	0	0
Register 31Dh	HIGH IF MODE4	0	0	0	0	0	HIGH IF MODE4	0
Register 41Dh	0	0	0	0	0	0	HIGH IF MODE2	0
Register 422h	0	0	0	0	0	0	DIS CHOP CHB	0
Register 434h	0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0

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Register Maps (continued)

Table 6. Register Map Summary (continued)

REGISTER ADDRESS, A[13:0] (Hex)	REGISTER DATA							
	7	6	5	4	3	2	1	0
Register 439h	0	0	0	0	SP1 CHB	0	0	0
Register 51Dh	0	0	0	0	0	0	HIGH IF MODE3	0
Register 522h	0	0	0	0	0	0	DIS CHOP CHC	0
Register 534h	0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0
Register 539h	0	0	0	0	SP1 CHC	0	0	0
Register 608h	HIGH IF MODE <7:6>		0	0	0	0	0	0
Register 61Dh	HIGH IF MODE5	0	0	0	0	0	HIGH IF MODE5	0
Register 70Ah	0	0	0	0	0	0	0	PDN SYSREF
Register 71Ah	0	0	0	0	DC FORCE[2:0]			0

8.6.1 Serial Register Description

8.6.1.1 Register 01h (address = 01h)

Figure 51. Register 01h

7	6	5	4	3	2	1	0
DIS DITH CHA		DIS DITH CHB		DIS DITH CHC		DIS DITH CHD	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

LEGEND: R/W = Read/Write; -n = value after reset

Table 7. Register 01h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DIS DITH CHA	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 134h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
5-4	DIS DITH CHB	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 434h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
3-2	DIS DITH CHC	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 534h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
1-0	DIS DITH CHD	R/W	0h	These bits enable or disable the on-chip dither. Control this bit along with bits 5 and 3 of register 234h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.

8.6.1.2 Register 02h (address = 02h)

Figure 52. Register 02h

7	6	5	4	3	2	1	0
STATS CH SEL[1:0]		0	0	0	0	0	0
R/W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 8. Register 02h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	STATS CH SEL[1:0]	R/W	0h	These bits select desired channel for statistical data computation 00 = Channel A, 01 = Channel B, 10 = Channel C, 11 = Channel D
5-0	0	W	0h	Must write 0.

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8.6.1.3 Register 03h (address = 03h)

Figure 53. Register 03h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	ODD EVEN
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 9. Register 03h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
0	ODD EVEN	R/W	0h	This bit selects the bit sequence on the output wires (in 2-wire mode only). 0 = Bits 0, 1, 2, and so forth appear on wire-0; bits 7, 8, 9, and so forth appear on wire-1. 1 = Bits 0, 2, 4, and so forth appear on wire-0; bits 1, 3, 5, and so forth appear on wire-1.

8.6.1.4 Register 04h (address = 04h)

Figure 54. Register 04h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	FLIP WIRE
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 10. Register 04h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	FLIP WIRE	R/W	0h	This bit flips the data on the output wires. Valid only in two wire configuration. 0 = Default 1 = Data on output wires is flipped. Pin D0x becomes D1x, and vice versa.

8.6.1.5 Register 05h (address = 05h)

Figure 55. Register 05h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	1W-2W
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 11. Register 05h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	1W-2W	R/W	0h	This bit transmits output data on either one or two wires. 0 = Output data are transmitted on two wires (Dx0P, Dx0M and Dx1P, Dx1M) 1 = Output data are transmitted on one wire (Dx0P, Dx0M).

8.6.1.6 Register 06h (address = 06h)

Figure 56. Register 06h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	TEST PATTERN EN	RESET
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 12. Register 06h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	TEST PATTERN EN	R/W	0h	This bit enables test pattern selection for the digital outputs. 0 = Normal output 1 = Test pattern output enabled
0	RESET	R/W	0h	This bit applies a software reset. This bit resets all internal registers to the default values and self-clears to 0.

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8.6.1.7 Register 07h (address = 07h)

Figure 57. Register 07h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	OVR ON LSB
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 13. Register 07h Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	OVR ON LSB	R/W	0h	This bit provides OVR information on the LSB bits. 0 = Output data bit 0 functions as the LSB of the 12-bit data 1 = Output data bit 0 carries the overrange (OVR) information

8.6.1.8 Register 09h (address = 09h)

Figure 58. Register 09h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	ALIGN TEST PATTERN	DATA FORMAT
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 14. Register 09h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	ALIGN TEST PATTERN	R/W	0h	This bit aligns the test patterns across the outputs of both channels. 0 = Test patterns of both channels are free running 1 = Test patterns of both channels are aligned
0	DATA FORMAT	R/W	0h	This bit selects th digital output data format. 0 = Twos complement 1 = Offset binary

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8.6.1.9 Register 0Ah (address = 0Ah)

Figure 59. Register 0Ah

7	6	5	4	3	2	1	0
CHA TEST PATTERN				CHB TEST PATTERN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 15. Register 0Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CHA TEST PATTERN	R/W	0h	These bits control the test pattern for channel A after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits 0110 = Deskew pattern: data are AAAh 1000 = PRBS pattern: data are a sequence of pseudo random numbers 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, and 599 Others = Do not use
3-0	CHB TEST PATTERN	R/W	0h	These bits control the test pattern for channel B after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095 0101 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits 0110 = Deskew pattern: data are AAAh 1000 = PRBS pattern: data are a sequence of pseudo random numbers 1001 = 8-point sine-wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, and 599 Others = Do not use

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8.6.1.10 Register 0Bh (address = 0Bh)

Figure 60. Register 0Bh

7	6	5	4	3	2	1	0
CHC TEST PATTERN				CHD TEST PATTERN			
R/W-0h				R/W-0h			

LEGEND: R/W = Read/Write; -n = value after reset

Table 16. Register 0Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CHC TEST PATTERN	R/W	0h	These bits control the test pattern for channel C after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095. 0110 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 1000 = Deskew pattern: data are AAAh. 1010 = PRBS pattern: data are a sequence of pseudo random numbers. 1011 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, 599. Others = Do not use
3-0	CHD TEST PATTERN	R/W	0h	These bits control the test pattern for channel D after the TEST PATTERN EN bit is set. 0000 = Normal operation 0001 = All 0's 0010 = All 1's 0011 = Toggle pattern: data alternate between 101010101010 and 010101010101. 0100 = Digital ramp: data increment by 1 LSB every clock cycle from code 0 to 4095. 0110 = Custom pattern: output data are the same as programmed by the CUSTOM PATTERN register bits. 1000 = Deskew pattern: data are AAAh. 1010 = PRBS pattern: data are a sequence of pseudo random numbers. 1011 = 8-point sine wave: data are a repetitive sequence of the following eight numbers that form a sine-wave: 0, 599, 2048, 3496, 4095, 3496, 2048, 599. Others = Do not use

8.6.1.11 Register 0Eh (address = 0Eh)

Figure 61. Register 0Eh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[11:4]							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 17. Register 0Eh Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CUSTOM PATTERN[11:4]	R/W	0h	These bits set the 12-bit custom pattern (bits 11-4) for all channels.

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8.6.1.12 Register 0Fh (address = 0Fh)

Figure 62. Register 0Fh

7	6	5	4	3	2	1	0
CUSTOM PATTERN[3:0]				0	0	0	0
R/W-0h				W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 18. Register 0Fh Field Descriptions

Bit	Field	Type	Reset	Description
7-4	CUSTOM PATTERN[3:0]	R/W	0h	These bits set the 12-bit custom pattern (bits 3-0) for all channels.
3-0	0	W	0h	Must write 0.

8.6.1.13 Register 10h (address = 10h)

Figure 63. Register 10h

7	6	5	4	3	2	1	0
REF STATUS CHB OR TEMPDATA [2]	REF STATUS CHD OR TEMPDATA [1]	REF STATUS CHA OR TEMPDATA [0]	CLK STATUS	TEMPDATA [6:4]			REF STATUS CHC OR TEMPDATA [3]
Read Only	Read Only	Read Only	Read Only	Read Only			Read Only

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 19. Register 10h Field Descriptions

Bit	Field	Type	Reset	Description
7-5, 0	REF STATUS CHB, REF STATUS CHD, REF STATUS CHA, REF STATUS CHC	Read Only	0h	When internal reference diagnostic is enabled by setting EN REF STATUS CHECK bit to ‘1’, these bits carry status of internal reference for corresponding channel. See Internal Reference and Clock Status Check for details. Note that these bits are multiplexed with temperature sensor’s data and carry TEMPDATA[3:0] if temperature sensor’s is enabled.
4	CLK STATUS	Read Only	0h	This bit indicates presence of input clock. By default, device sets this bit 0. If input clock is absent, this bit becomes '1'
7-5, 3-1, 0	TEMPDATA [6:0]	Read Only	0h	When temperature sensor’s data is being read, these bits carry seven MSBs of temperature sensor’s 9-bit data. Remaining two LSBs are available on address 11h bit 5:4. See Temperature Sensor for details of operation.

8.6.1.14 Register 11h (address = 11h)

Figure 64. Register 11h

7	6	5	4	3	2	1	0
0	0	TEMPDATA [8:7]		0	0	0	0
W-0h	W-0h	Read Only		W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 20. Register 11h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5-4	TEMPDATA [8:7]	Read Only	0h	These bits represent digital equivalent of temperature in 2s complement format.
3-0	0	W	0h	Must write 0.

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8.6.1.15 Register 13h (address = 13h)

Figure 65. Register 13h

7	6	5	4	3	2	1	0
0	EN REF STATUS CHECK	EN DC FORCE	EN STATS	0	0	LOW SPEED ENABLE	
W-0h	R/W-0h	R/W-0h	R/W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 21. Register 13h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0.
6	EN REF STATUS CHECK	R/W	0h	This Bit Enables reference diagnostic check. Must be set to '1' before reading reference status from REF STATUS CHECK CHx bits.
5	EN DC FORCE	R/W	0h	This Bit Enables internal DC voltage force diagnostic check together for all channels. Must be set to '1' before forcing internal DC voltage through DC FORCE[2:0] bits.
4	EN STATS	R/W	0h	This bit enables inter Statistics Module for mean and variance computation. After this bit is set to '1', statistical module for desired channel can be selected by using bits STATS CH SEL[1:0]
3-2	0	W	0h	Must write 0.
1-0	LOW SPEED ENABLE	R/W	0h	Enables low speed operation in 1-wire and 2-wire mode. Depending upon sampling frequency, write this bit as per Table 22

Table 22. LOW SPEED ENABLE Register Settings across f_S

f_S, MSPS		REGISTER BIT LOW SPEED ENABLE	
MIN	MAX	1- Wire Mode	2-Wire Mode
20	25	10	11
15	20	10	Not supported

8.6.1.16 Register 14h (address = 14h)

Figure 66. Register 14h

7	6	5	4	3	2	1	0
0	EN TEMP SENS CONV	EN TEMP SENSE	0	0	EN TEMP DATA READOUT	0	0
W-0h	R/W-0h	R/W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 23. Register 14h Field Descriptions

Bit	Field	Type	Reset	Description
7	0	W	0h	Must write 0.
6	EN TEMP SENS CONV	R/W	0h	This bit enables the temperature-to-digital conversion process of temperature sensor. This bit can be set to '1' after temperature sensor is enabled by setting EN TEMP SENSE bit to '1'.
5	EN TEMP SENSE	R/W	0h	This bit enables temperature sensor present inside device
4-3	0	W	0h	Must write 0.
2	EN TEMP DATA READOUT	R/W	0h	This bit places the 9-bit digital equivalent of temperature on register bits TEMPDATA[8:0].
1-0	0	W	0h	Must write 0.

8.6.1.17 Register 15h (address = 15h)

Figure 67. Register 15h

7	6	5	4	3	2	1	0
CHA PDN	CHB PDN	CHC PDN	CHD PDN	STANDBY	GLOBAL PDN	0	CONFIG PDN PIN
W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h	R/W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 24. Register 15h Field Descriptions

Bit	Field	Type	Reset	Description
7	CHA PDN	W	0h	0 = Normal operation 1 = Power-down channel A
6	CHB PDN	R/W	0h	0 = Normal operation 1 = Power-down channel B
5	CHC PDN	R/W	0h	0 = Normal operation 1 = Power-down channel C
4	CHD PDN	W	0h	0 = Normal operation 1 = Power-down channel D
3	STANDBY	R/W	0h	The ADCs of both channels enter standby. 0 = Normal operation 1 = Standby
2	GLOBAL PDN	R/W	0h	0 = Normal operation 1 = Global power-down
1	0	W	0h	Must write 0.
0	CONFIG PDN PIN	R/W	0h	This bit configures the PDN pin as either a global power-down or standby pin. 0 = Logic high voltage on the PDN pin sends the device into global power-down 1 = Logic high voltage on the PDN pin sends the device into standby

8.6.1.18 Register 16h (address = 16h)

Figure 68. Register 16h

7	6	5	4	3	2	1	0
MEAN[5:0]						0	0
Read Only						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 25. Register 16h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	MEAN[5:0]	Read Only	0h	These bits represent mean value in 2s complement format computed over programmed number of samples by statistical module.
1-0	0	W	0h	Must write 0.

8.6.1.19 Register 17h (address = 17h)

Figure 69. Register 17h

7	6	5	4	3	2	1	0
0	0	MEAN[11:6]					
W-0h	W-0h	Read Only					

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

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Table 26. Register 17h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5-0	MEAN[11:6]	Read Only	0h	These bits represent mean value in 2s complement format computed over programmed number of samples by statistical module.

8.6.1.20 Register 18h (address = 18h)

Figure 70. Register 18h

7	6	5	4	3	2	1	0
VAR[5:0]						0	0
Read Only						W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 27. Register 18h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	VAR[5:0]	Read Only	0h	These bits represent variance value in 2s complement format computed over programmed number of samples by statistical module
1-0	0	W	0h	Must write 0.

8.6.1.21 Register 19h (address = 19h)

Figure 71. Register 19h

7	6	5	4	3	2	1	0
0	0	VAR[11:6]					
W-0h	W-0h	Read Only					

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 28. Register 19h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5-0	VAR[11:6]	Read Only	0h	These bits represent variance value in 2s complement format computed over programmed number of samples by statistical module

8.6.1.22 Register 25h (address = 25h)

Figure 72. Register 25h

7	6	5	4	3	2	1	0
LVDS SWING							
R/W-0h							

LEGEND: R/W = Read/Write; -n = value after reset

Table 29. Register 25h Field Descriptions

Bit	Field	Type	Reset	Description
7-0	LVDS SWING	R/W	0h	These bits control the swing of the LVDS outputs (including the data output, bit clock, and frame clock).

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8.6.1.23 Register 27h (address = 27h)

Figure 73. Register 27h

7	6	5	4	3	2	1	0
CLK DIV		0	0	0	0	0	0
R/W-0h		W-0h	W-0h	W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 30. Register 27h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	CLK DIV	R/W	0h	These bits select the internal clock divider for the input sampling clock. 00 = Divide-by-1 01 = Divide-by-1 10 = Divide-by-2 11 = Divide-by-4
5-0	0	W	0h	Must write 0.

8.6.1.24 Register 4Bh (address = 4Bh)

Figure 74. Register 4Bh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	SAMPLES FOR STATS[1:0]	
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 31. Register 4Bh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1-0	SAMPLES FOR STATS[1:0]	R/W	0h	These bits program number of samples to be used by statistical module for computation of mean and variance. 00=256, 01=1024, 10=4096, 11=16384

8.6.1.25 Register 11Dh (address = 11Dh)

Figure 75. Register 11Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 32. Register 11Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE0			Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

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8.6.1.26 Register 122h (address = 122h)

Figure 76. Register 122h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHA	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 33. Register 122h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHA	R/W	0h	This bit disables the chopper. Set this bit to shift the 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

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8.6.1.27 Register 134h (address = 134h)

Figure 77. Register 134h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHA	0	DIS DITH CHA	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 34. Register 134h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHA	R/W	0h	Set this bit along with bits 7 and 6 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHA	R/W	0h	Set this bit along with bits 7 and 6 of register 01h. 00 = Default 11 = Dither is disabled for channel A. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

8.6.1.28 Register 139h (address = 139h)

Figure 78. Register 139h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHA	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 35. Register 139h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHA	R/W	0h	This bit sets the special mode for best performance on channel A. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

8.6.1.29 Register 21Dh (address = 21Dh)

Figure 79. Register 21Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE1	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 36. Register 21Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE1	R/W	0h	Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

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8.6.1.30 Register 222h (address = 222h)

Figure 80. Register 222h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHD	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 37. Register 222h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHD	R/W	0h	This bit disables the chopper. Set this bit to shift the 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

8.6.1.31 Register 234h (address = 234h)

Figure 81. Register 234h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHD	0	DIS DITH CHD	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 38. Register 234h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHD	R/W	0h	Set this bit with bits 1 and 0 of register 01h. 00 = Default 11 = Dither is disabled for channel D. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHD	R/W	0h	Set this bit with bits 1 and 0 of register 01h. 00 = Default 11 = Dither is disabled for channel D. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

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8.6.1.32 Register 239h (address = 239h)

Figure 82. Register 239h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHD	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 39. Register 239h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHD	R/W	0h	This bit sets the special mode for best performance on channel D. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

8.6.1.33 Register 308h (address = 308h)

Figure 83. Register 308h

7	6	5	4	3	2	1	0
HIGH IF MODE<5:4>		0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 40. Register 308h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HIGH IF MODE<5:4>	R/W	0h	Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
5-0	0	W	0h	Must write 0.

8.6.1.34 Register 31Dh (address = 31Dh)

Figure 84. Register 31Dh

7	6	5	4	3	2	1	0
HIGH IF MODE4	0	0	0	0	0	HIGH IF MODE4	0
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 41. Register 31Dh Field Descriptions

Bit	Field	Type	Reset	Description
7	HIGH IF MODE4	R/W	0h	Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
6-2	0	W	0h	Must write 0.
1	HIGH IF MODE4	R/W	0h	Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

8.6.1.35 Register 41Dh (address = 41Dh)

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Figure 85. Register 41Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE2	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 42. Register 41Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE2	R/W	0h	Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

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8.6.1.36 Register 422h (address = 422h)

Figure 86. Register 422h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHB	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 43. Register 422h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHB	R/W	0h	This bit disables the chopper. Set this bit to shift the 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

8.6.1.37 Register 434h (address = 434h)

Figure 87. Register 434h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHB	0	DIS DITH CHB	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 44. Register 434h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHB	R/W	0h	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHB	R/W	0h	Set this bit with bits 5 and 4 of register 01h. 00 = Default 11 = Dither is disabled for channel B. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

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8.6.1.38 Register 439h (address = 439h)

Figure 88. Register 439h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHB	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 45. Register 439h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHB	R/W	0h	This bit sets the special mode for best performance on channel B. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

8.6.1.39 Register 51Dh (address = 51Dh)

Figure 89. Register 51Dh

7	6	5	4	3	2	1	0
0	0	0	0	0	0	HIGH IF MODE3	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 46. Register 51Dh Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	HIGH IF MODE3	R/W	0h	Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

8.6.1.40 Register 522h (address = 522h)

Figure 90. Register 522h

7	6	5	4	3	2	1	0
0	0	0	0	0	0	DIS CHOP CHC	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 47. Register 522h Field Descriptions

Bit	Field	Type	Reset	Description
7-2	0	W	0h	Must write 0.
1	DIS CHOP CHC	R/W	0h	This bit disables the chopper. Set this bit to shift the 1/f noise floor at dc. 0 = 1/f noise floor is centered at f_S / 2 (default) 1 = Chopper mechanism is disabled; 1/f noise floor is centered at dc
0	0	W	0h	Must write 0.

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8.6.1.41 Register 534h (address = 534h)

Figure 91. Register 534h

7	6	5	4	3	2	1	0
0	0	DIS DITH CHC	0	DIS DITH CHC	0	0	0
W-0h	W-0h	R/W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 48. Register 534h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	0	W	0h	Must write 0.
5	DIS DITH CHC	R/W	0h	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel C. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
4	0	W	0h	Must write 0.
3	DIS DITH CHC	R/W	0h	Set this bit with bits 3 and 2 of register 01h. 00 = Default 11 = Dither is disabled for channel C. In this mode, SNR typically improves by 0.2 dB at 70 MHz.
2-0	0	W	0h	Must write 0.

8.6.1.42 Register 539h (address = 539h)

Figure 92. Register 539h

7	6	5	4	3	2	1	0
0	0	0	0	SP1 CHC	0	0	0
W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h	W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 49. Register 539h Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3	SP1 CHC	R/W	0h	This bit sets the special mode for best performance on channel C. Always write 1 after reset.
2-0	0	W	0h	Must write 0.

8.6.1.43 Register 608h (address = 608h)

Figure 93. Register 608h

7	6	5	4	3	2	1	0
HIGH IF MODE<7:6>		0	0	0	0	0	0
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 50. Register 608h Field Descriptions

Bit	Field	Type	Reset	Description
7-6	HIGH IF MODE<7:6>	R/W	0h	Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
5-0	0	W	0h	Must write 0.

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8.6.1.44 Register 61Dh (address = 61Dh)

Figure 94. Register 61Dh

7	6	5	4	3	2	1	0
HIGH IF MODE5	0	0	0	0	0	HIGH IF MODE5	PDN SYSREF
R/W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h	W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 51. Register 61Dh Field Descriptions

Bit	Field	Type	Reset	Description
7	HIGH IF MODE5	R/W	0h	Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
6-2	0	W	0h	Must write 0.
1	HIGH IF MODE5	R/W	0h	Set all register bits belonging to HIGH IF MODE as logic HIGH to improve HD3 by a couple of dB for IF > 100 MHz.
0	0	W	0h	Must write 0.

8.6.1.45 Register 70Ah (address = 70Ah)

Figure 95. Register 70Ah

7	6	5	4	3	2	1	0
0	0	0	0	0	0	0	PDN SYSREF
W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	W-0h	R/W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 52. Register 70Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-1	0	W	0h	Must write 0.
0	PDN SYSREF	R/W	0h	If the SYSREF pins are not used in the system, the SYSREF buffer must be powered down by setting this bit. 0 = Normal operation 1 = Powers down the SYSREF buffer

8.6.1.46 Register 71Ah (address = 71Ah)

Figure 96. Register 71Ah

7	6	5	4	3	2	1	0
0	0	0	0	DC FORCE[2:0]			0
W-0h	W-0h	W-0h	W-0h	R/W-0h			W-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

Table 53. Register 71Ah Field Descriptions

Bit	Field	Type	Reset	Description
7-4	0	W	0h	Must write 0.
3-1	DC FORCE[2:0]	R/W	0h	These Bits force internal DC voltage to ADC's analog inputs together for all channels. Minimum DC voltage corresponds to output code 745 and max DC voltage to output code 3332 typically following the equation: Output Code = 368 × DC FORCE[2:0] + 745
0	0	W	0h	Must write 0.

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9 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

Typical applications involving transformer-coupled circuits are discussed in this section. Transformers (such as ADT1-1WT or WBC1-1) can be used up to 250 MHz to achieve good phase and amplitude balances at ADC inputs. When designing the dc driving circuits, the ADC input impedance must be considered. Figure 97 and Figure 98 show the impedance (Z_{in} = R_{in} || C_{in}) across the ADC input pins.

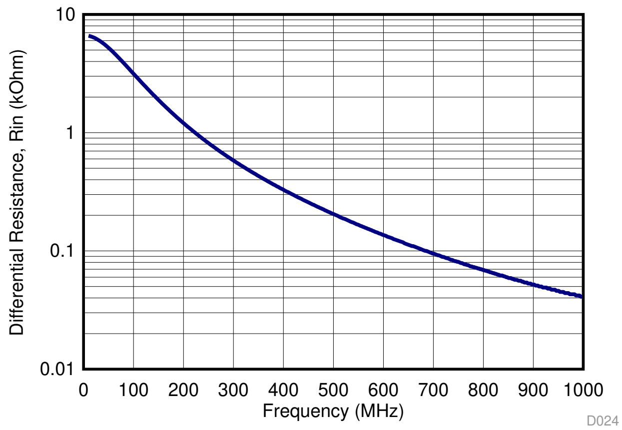

Figure 97. Differential Input Resistance, R_{IN}

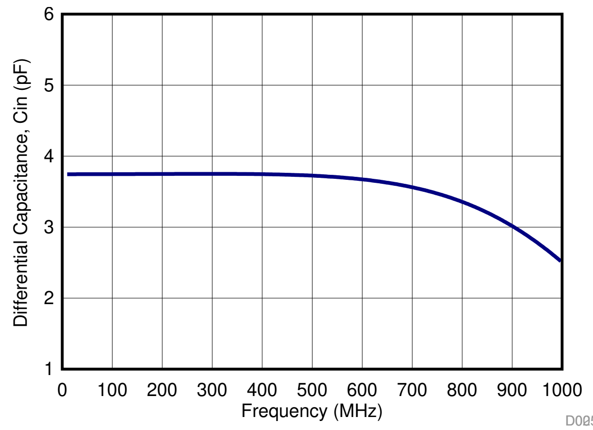

Figure 98. Differential Input Capacitance, C_{IN}

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9.2 Typical Applications

9.2.1 Driving Circuit Design: Low Input Frequencies

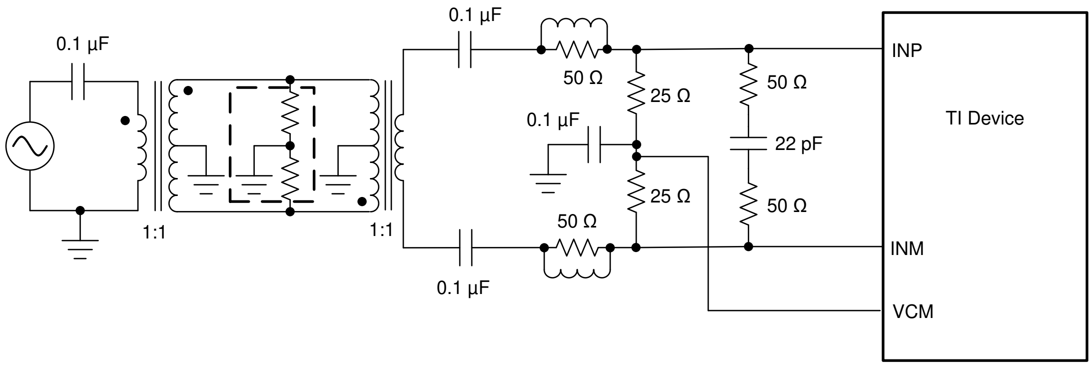


Figure 99. Driving Circuit for Low Input Frequencies

9.2.1.1 Design Requirements

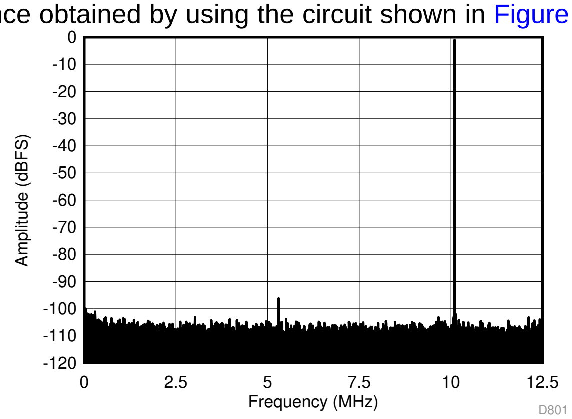
For optimum performance, the analog inputs must be driven differentially. An optional 5-Ω to 15-Ω resistor in series with each input pin can be kept to damp out ringing caused by package parasitic. The drive circuit may have to be designed to minimize the impact of kick-back noise generated by sampling switches opening and closing inside the ADC, as well as ensuring low insertion loss over the desired frequency range and matched impedance to the source.

9.2.1.2 Detailed Design Procedure

A typical application involving using two back-to-back coupled transformers is illustrated in Figure 99. The circuit is optimized for low input frequencies. An external R-C-R filter using 50-Ω resistors and a 22-pF capacitor is used with the series inductor (39 nH), this combination helps absorb the sampling glitches.

9.2.1.3 Application Curve

Figure 100 shows the performance obtained by using the circuit shown in Figure 99.



SFDR = 95 dBc, SNR = 71 dBFS, SINAD = 71 dBFS,
THD = 94 dBc, HD2 = 106 dBc, HD3 = 95 dBc

Figure 100. Performance FFT at 10 MHz (Low Input Frequency)

Typical Applications (continued)

9.2.2 Driving Circuit Design: Input Frequencies Between 100 MHz to 230 MHz

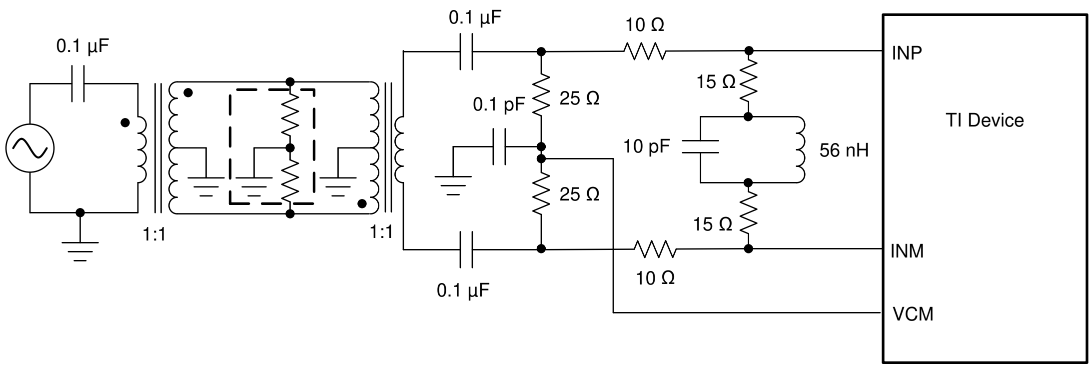


Figure 101. Driving Circuit for Mid-Range Input Frequencies (100 MHz < f_{IN} < 230 MHz)

9.2.2.1 Design Requirements

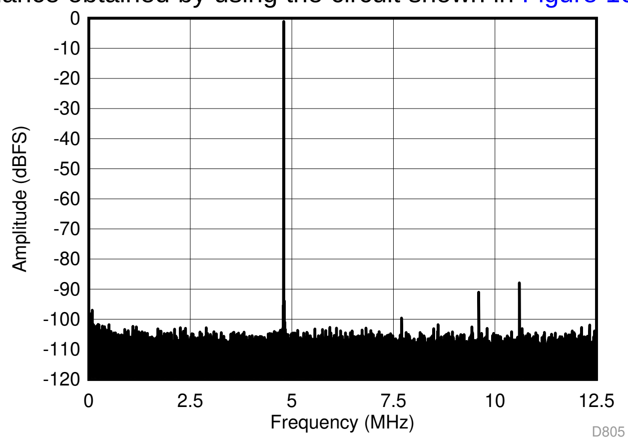
See the *Design Requirements* section for further details.

9.2.2.2 Detailed Design Procedure

When input frequencies are between 100 MHz to 230 MHz, an R-LC-R circuit can be used to optimize performance, as shown in Figure 101.

9.2.2.3 Application Curve

Figure 102 shows the performance obtained by using the circuit shown in Figure 101.



SFDR = 87 dBc, SNR = 69.8 dBFS, SINAD = 69.7 dBFS,
THD = 85 dBc, HD2 = 90 dBc, HD3 = 87 dBc

Figure 102. Performance FFT at 170 MHz (Mid Input Frequency)

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Typical Applications (continued)

9.2.3 Driving Circuit Design: Input Frequencies Greater than 230 MHz

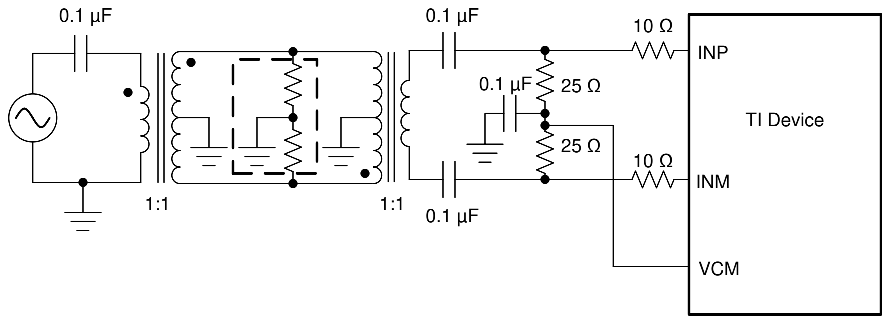


Figure 103. Driving Circuit for High Input Frequencies (f_{IN} > 230 MHz)

9.2.3.1 Design Requirements

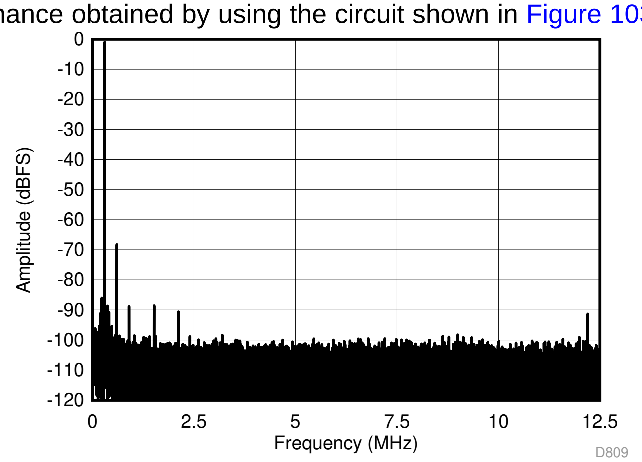
See the *Design Requirements* section for further details.

9.2.3.2 Detailed Design Procedure

For high input frequencies (> 230 MHz), using the R-C-R or R-LC-R circuit does not show significant improvement in performance. However, a series resistance of 10 Ω can be used as shown in Figure 103.

9.2.3.3 Application Curve

Figure 104 shows the performance obtained by using the circuit shown in Figure 103.



SFDR = 67 dBc, SNR = 66.4 dBFS, SINAD = 66.4 dBFS,
THD = 93 dBc, HD2 = 67 dBc, HD3 = 88 dBc

Figure 104. Performance FFT at 450 MHz (High Input Frequency)

10 Power Supply Recommendations

The device requires a 1.8-V nominal supply for AVDD and DVDD. There are no specific sequence power-supply requirements during device power-up. AVDD and DVDD can power up in any order.

11 Layout

11.1 Layout Guidelines

The ADC3421-Q1 EVM layout can be used as a reference layout to obtain the best performance. A layout diagram of the EVM top layer is provided in Figure 105. Some important points to remember during laying out the board are:

1. Analog inputs are located on opposite sides of the device pin out to ensure minimum crosstalk on the package level. To minimize crosstalk onboard, the analog inputs must exit the pin out in opposite directions, as shown in the reference layout of Figure 105 as much as possible.
2. In the device pin out, the sampling clock is located on a side perpendicular to the analog inputs in order to minimize coupling between them. This configuration is also maintained on the reference layout of Figure 105 as much as possible.
3. Keep digital outputs away from the analog inputs. When these digital outputs exit the pin out, the digital output traces must not be kept parallel to the analog input traces because this configuration can result in coupling from digital outputs to analog inputs and degrade performance. All digital output traces to the receiver [such as a field-programmable gate array (FPGA) or an application-specific integrated circuit (ASIC)] must be matched in length to avoid skew among outputs.
4. At each power-supply pin (AVDD and DVDD), keep a 0.1-µF decoupling capacitor close to the device. A separate decoupling capacitor group consisting of a parallel combination of 10-µF, 1-µF, and 0.1-µF capacitors can be kept close to the supply source.

11.2 Layout Example

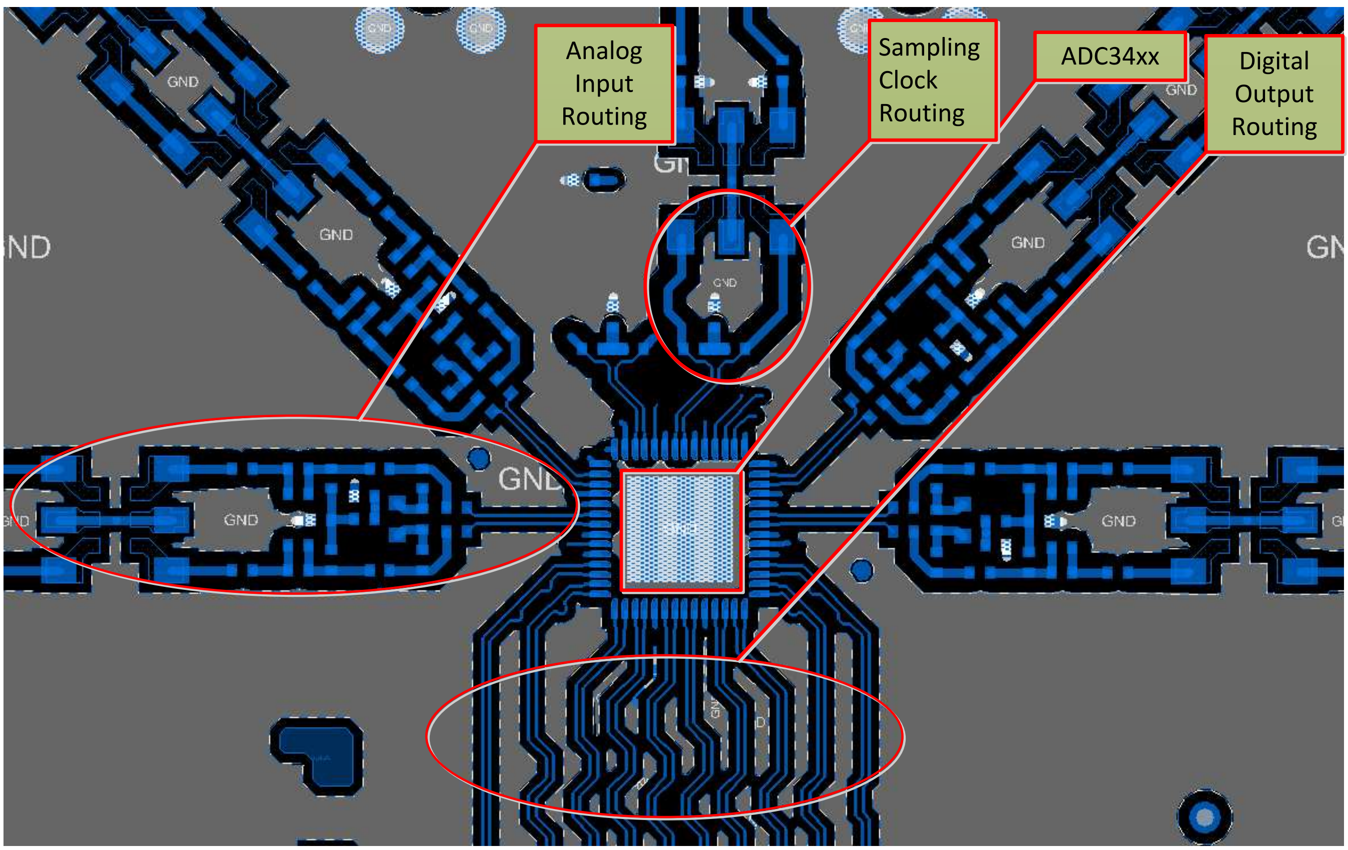


Figure 105. Typical Layout of the ADC3421-Q1 Board

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.3 Trademarks

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12.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

SLYZ022 — *TI Glossary*.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AD3421QRWERQ1	Active	Production	VQFNP (RWE) | 56	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	AZ3421Q
AD3421QRWERQ1.A	Active	Production	VQFNP (RWE) | 56	2000 | LARGE T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	AZ3421Q
AD3421QRWETQ1	Active	Production	VQFNP (RWE) | 56	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	AZ3421Q
AD3421QRWETQ1.A	Active	Production	VQFNP (RWE) | 56	250 | SMALL T&R	Yes	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	AZ3421Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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OTHER QUALIFIED VERSIONS OF ADC3421-Q1 :

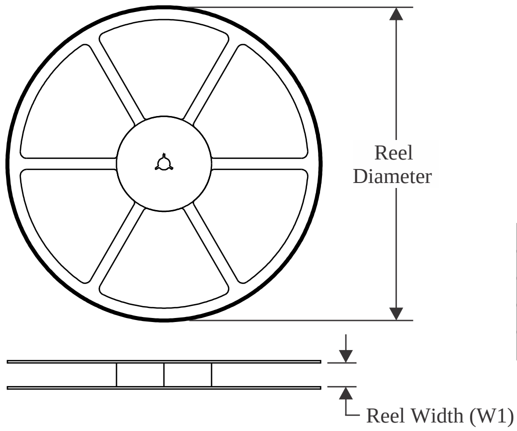
- Catalog : ADC3421

NOTE: Qualified Version Definitions:

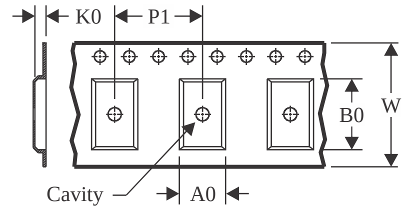
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

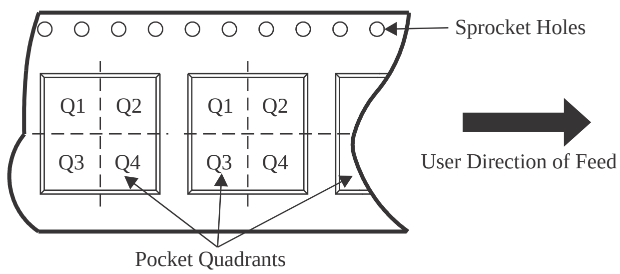


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

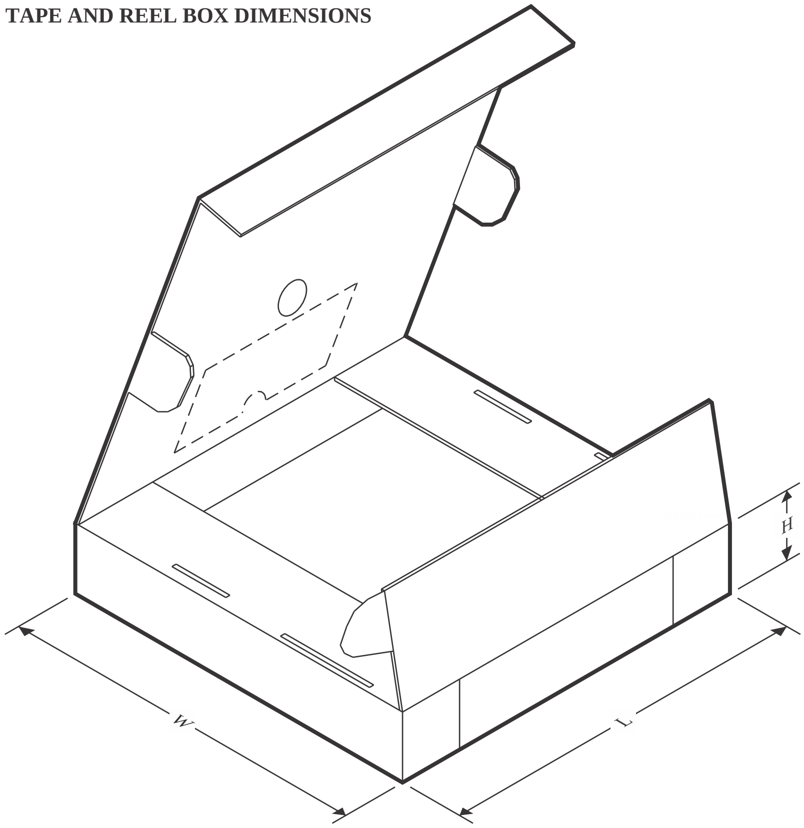
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AD3421QRWERQ1	VQFNP	RWE	56	2000	330.0	16.4	8.3	8.3	2.25	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AD3421QRWERQ1	VQFNP	RWE	56	2000	350.0	350.0	43.0

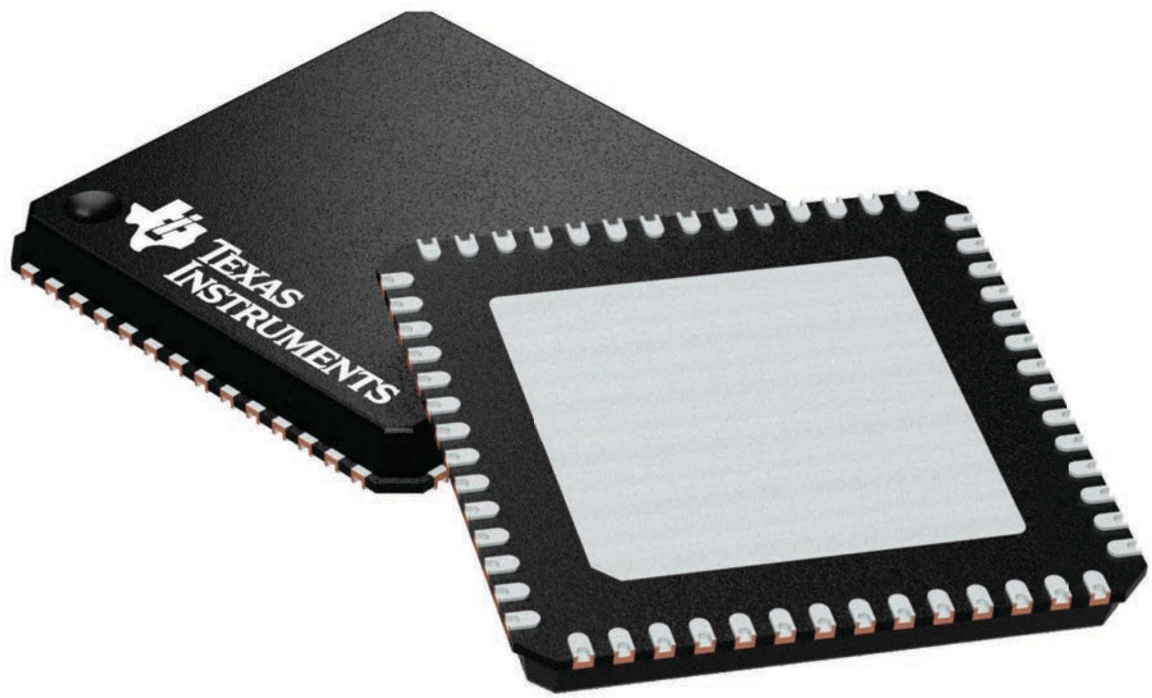
GENERIC PACKAGE VIEW

RWE 56

VQFNP - 0.9 mm max height

8 x 8, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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