TEXAS INSTRUMENTS

**ADC34RF52**
SBASAI7 – MARCH 2023

# ADC34RF52 Quad Channel 14-bit 1.5-GSPS RF Sampling Data Converter

## 1 Features

- 14-Bit, Quad channel 1.5-GSPS ADC
- Noise spectral density:
  - -153 dBFS/Hz without averaging
  - -156 dBFS/Hz with 2x averaging
- Single core (non-interleaved) ADC architecture
- Aperture jitter: 50 fs
- Low close-in residual phase noise:
  - -133 dBc/Hz at 10 kHz offset
- Spectral performance ($f_{IN}$ = 900 MHz, -4 dBFS):
  - 2x internal averaging
  - SNR: 65.2 dBFS
  - SFDR HD2,3: 74 dBc
  - SFDR worst spur: 90 dBFS
- Input fullscale: 1.0/1.1Vpp (1/1.8 dBm)
- Full power input bandwidth (-3 dB): 1.6 GHz
- JESD204B serial data interface
  - Maximum lane rate: 13 Gbps
  - Supports subclass 1 deterministic latency
- Digital down-converters
  - Up to two DDC per ADC channel
  - Complex output: 4x to 128x decimation
  - 48-bit NCO phase coherent frequency hopping
  - Fast frequency hopping: < 1 μs
- Power consumption: 0.73 W/channel (1x AVG)
- Power supplies: 1.8 V, 1.2 V

## 2 Applications

- Phased array radar
- Spectrum analyzer
- Software defined radio (SDR)
- Electronic warfare
- High-speed digitizer
- Cable infrastructure
- Communications infrastructure

## 3 Description

The ADC34RF52 is a single core 14-bit, 1.5-GSPS, quad channel analog to digital converter (ADC) that supports RF sampling with input frequencies up to 2.5 GHz. The design maximizes signal-to-noise ratio (SNR) and delivers a noise spectral density of -153 dBFS/Hz. Using additional internal ADCs along with on-chip signal averaging, the noise density improves to -156 dBFS/Hz.

Each ADC channel can be connected to a dual-band digital down-converter (DDC) using a 48-bit NCO which supports phase coherent frequency hopping. Using the GPIO pins for NCO frequency control, frequency hopping can be achieved in less than 1 μs.

The ADC34RF52 supports the JESD204B serial data interface with subclass 1 deterministic latency using data rates up to 13 Gbps. There are only 2 serdes lanes per ADC channel.

The power efficient ADC architecture consumes 0.73 W/ch at 1.5-GSPS and provides power scaling with lower sampling rates.

**Device Information**

| PART NUMBER | PACKAGE[1] | MAX SAMPLING RATE |
|---|---|---|
| ADC34RF52 | QFN (64) | 1.5 GSPS |

(1) For all available packages, see the package option addendum at the end of the data sheet.



**Block Diagram**

# Table of Contents

# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| DATE | REVISION | NOTES |
|---|---|---|
| March 2023 | * | Initial Release |

Product Folder Links: *ADC34RF52*

# 5 Pin Configuration and Functions
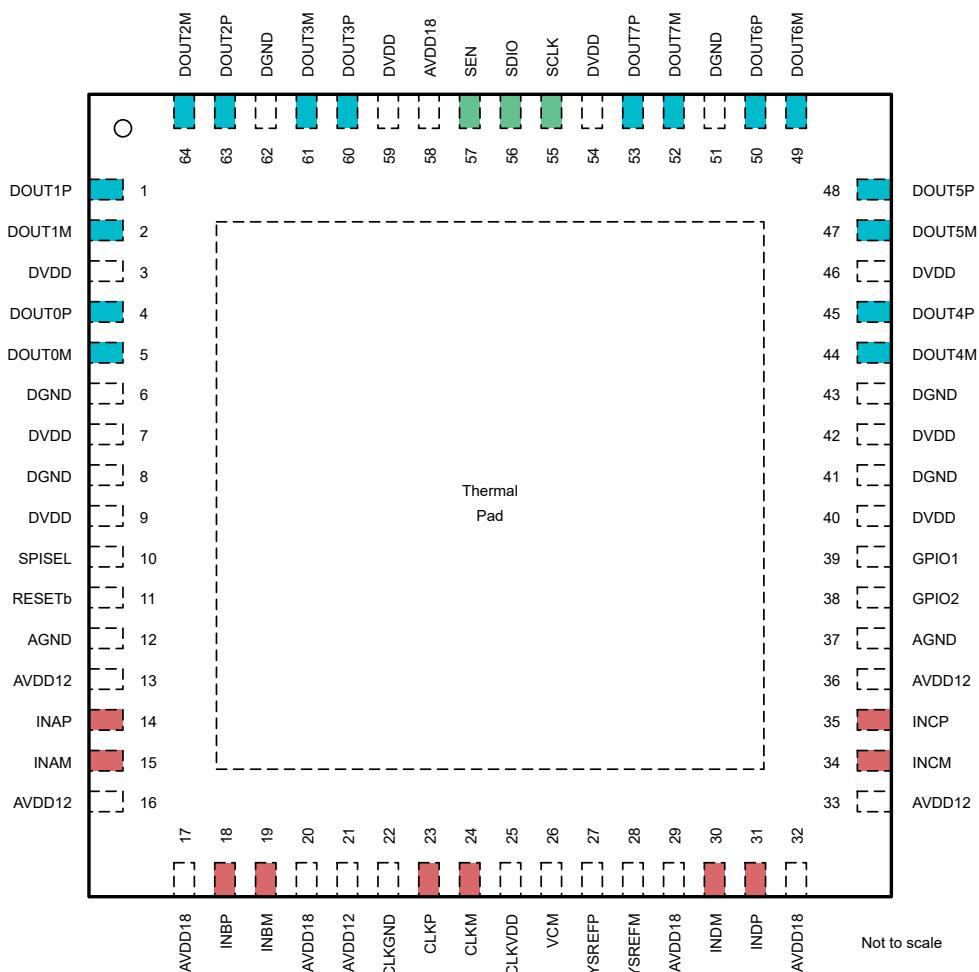


**Figure 5-1. RTD Package, 64 Pin QFN (Top View)**

**Table 5-1. Pin Functions**

| PIN | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| **ANALOG INPUTS** | | | |
| INAP | 14 | I | Differential analog input for channel A. 100 Ω differential internal termination. |
| INAM | 15 | | |
| INBP | 18 | I | Differential analog input for channel B. 100 Ω differential internal termination. |
| INBM | 19 | | |
| INCP | 35 | I | Differential analog input for channel C. 100 Ω differential internal termination. |
| INCM | 34 | | |
| INDP | 31 | I | Differential analog input for channel D. 100 Ω differential internal termination. |
| INDM | 30 | | |
| VCM | 26 | O | Common-mode voltage output for the analog inputs. |
| **CLOCK, SYNCHRONIZATION** | | | |
| CLKP | 23 | I | Differential sampling clock input. 100 Ω differential internal termination. |
| CLKM | 24 | | |

Product Folder Links: *ADC34RF52*

### Table 5-1. Pin Functions (continued)

| PIN NAME | PIN NO. | TYPE | DESCRIPTION |
|---|---|---|---|
| SYSREFP | 27 | I | Differential external synchronization input. |
| SYSREFM | 28 | | |
| **CONTROL** | | | |
| RESETb | 11 | I | Hardware reset. Active low. This pin has an internal 21 kΩ pull-up resistor to AVDD18. |
| SEN | 57 | I | Serial interface enable. Active low. This pin has an internal 21 kΩ pull-up resistor to AVDD18. |
| SCLK | 55 | I | Serial interface clock input. This pin has an internal 21 kΩ pull-down resistor. |
| SDIO | 56 | I/O | Serial interface data input and output. This pin has an internal 21 kΩ pull-down resistor. |
| GPIO1 | 39 | I/O | GPIO control pin. This pin is configured through SPI interface for power down or NCO control function. |
| GPIO2 | 38 | I/O | GPIO control pin. This pin is configured through SPI interface for power down or NCO control function. |
| SPISEL | 10 | I | Determines the functional of the SPI interface pins: either normal SPI for register programming or fast access to NCO selection only for fast frequency hopping. |
| **DIGITAL DATA INTERFACE** | | | |
| DOUT0P | 4 | O | JESD204B high-speed serial data output interface pins for channels A to D. Output lanes can be reordered using the output MUX. |
| DOUT0M | 5 | | |
| DOUT1P | 1 | O | |
| DOUT1M | 2 | | |
| DOUT2P | 63 | O | |
| DOUT2M | 64 | | |
| DOUT3P | 60 | O | |
| DOUT3M | 61 | | |
| DOUT4P | 45 | O | |
| DOUT4M | 44 | | |
| DOUT5P | 48 | O | |
| DOUT5M | 47 | | |
| DOUT6P | 50 | O | |
| DOUT6M | 49 | | |
| DOUT7P | 53 | O | |
| DOUT7M | 52 | | |
| **POWER SUPPLY** | | | |
| AVDD18 | 17,20,29,32, 58 | I | Analog 1.8-V power supply |
| AVDD12 | 13,16,21,33, 36 | I | Analog 1.2-V power supply |
| CLKVDD | 25 | I | Clock 1.2-V power supply. Very sensitive to power supply noise. Directly impacts close in aperture phase noise. |
| DVDD | 3,7,9,40,42, 46,54,59 | I | Digital 1.2-V power supply |
| AGND | 12,37 | I | Analog ground, shorted to thermal pad. |
| CLKGND | 22 | I | Clock ground. |
| DGND | 6,8,41,43,51,62 | I | Digital ground. |

Product Folder Links: *ADC34RF52*

# 6 Specifications

## 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

| PARAMETER | TEST CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage range, AVDD18 | | −0.3 | 2.1 | V |
| Supply voltage range, AVDD12, CLKVDD, DVDD | | −0.3 | 1.4 | V |
| Voltage applied to input pins | INAP/M, INBP/M, INCP/M, INDP/M | −0.6 | 1.2 | V |
| | CLKP/M | −0.3 | CLKVDD + 0.3 | V |
| | SYSREFP/M | −0.3 | AVDD12 + 0.6 | V |
| | GPIO1/2, PDN, RESET, SCLK, SEN, SDIO, SPISEL | −0.3 | AVDD18 + 0.2 | V |
| Peak RF input power (INAP/M, INBP/M, INCP/M, INDP/M) | Differential 100 Ω termination. | | 12 | dBm |
| Junction temperature, $T_J$ | Junction temperature, $T_J$ | | 115 | °C |
| Storage temperature, $T_{stg}$ | Storage temperature, $T_{stg}$ | −65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## 6.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1] | ± 1000 | V |
| | | Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002[2] | ± 500 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| AVDD18 | 1.8 V analog supply | 1.75 | 1.8 | 1.85 | V |
| AVDD12 | 1.2 V analog supply | 1.15 | 1.2 | 1.225 | V |
| CLKVDD | 1.2 V clock supply | 1.175 | 1.2 | 1.225 | V |
| DVDD | 1.2 V digital supply | 1.15 | 1.2 | 1.225 | V |
| $T_A$ | Operating free-air temperature | −40 | | 85 | °C |
| $T_J$ | Operating junction temperature | | | 105[1] | °C |
| | Maximum Operating Junction Temperature Range | 125 | | | |

(1) Prolonged use above this junction temperature may increase the device failure-in-time (FIT) rate.

Product Folder Links: *ADC34RF52*

## 6.4 Thermal Information

| THERMAL METRIC[1] | | ADC34RF5x | UNIT |
|---|---|---|---|
| | | RTD (QFN) | |
| | | 64 Pins | |
| $R_{\Theta JA}$ | Junction-to-ambient thermal resistance | 20.1 | °C/W |
| $R_{\Theta JC(top)}$ | Junction-to-case (top) thermal resistance | 6.8 | °C/W |
| $R_{\Theta JB}$ | Junction-to-board thermal resistance | 5.2 | °C/W |
| $\Psi_{JT}$ | Junction-to-top characterization parameter | 0.1 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 5.1 | °C/W |
| $R_{\Theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | 0.5 | °C/W |

(1)    For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 6.5 Electrical Characteristics - Power Consumption

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, Bypass mode, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **FS = 1.5 GSPS** | | | | | | |
| $I_{AVDD18}$ | Supply current, 1.8 V analog supply | Bypass mode, LMFS = 8-4-8-10 1x average | | 330 | | mA |
| $I_{AVDD12}$ | Supply current, 1.2 V analog supply | | | 740 | | |
| $I_{CLKVDD}$ | Supply current, 1.2 V clock supply | | | 80 | | |
| $I_{DVDD}$ | Supply current, 1.2 V digital supply | | | 1110 | | |
| $P_{DIS}$ | Power dissipation | | | 2.92 | | W |
| $I_{AVDD18}$ | Supply current, 1.8 V analog supply | Bypass mode, LMFS = 8-4-8-10 2x average | | 500 | | mA |
| $I_{AVDD12}$ | Supply current, 1.2 V analog supply | | | 1110 | | |
| $I_{CLKVDD}$ | Supply current, 1.2 V clock supply | | | 86 | | |
| $I_{DVDD}$ | Supply current, 1.2 V digital supply | | | 1410 | | |
| $P_{DIS}$ | Power dissipation | | | 4.05 | | W |
| **POWER DOWN MODES** | | | | | | |
| $P_{DIS}$ | Power down mode power consumption | Fast wake up time | | 210 | | mW |

Product Folder Links: *ADC34RF52*

## 6.6 Electrical Characteristics - DC Specifications

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, Bypass mode, 1x AVG, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and −1-dBFS differential input, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **DC ACCURACY** | | | | | | |
| | No missing codes | | 14 | | | bits |
| DNL | Differential nonlinearity | $F_{IN}$ = 10 MHz | | ±0.9 | | LSB |
| INL | Integral nonlinearity | $F_{IN}$ = 10 MHz | | ±4 | | LSB |
| $V_{OS\_ERR}$ | Offset error | | | ±0.2 | | %FSR |
| $GAIN_{ERR}$ | Gain error | | | ±0.2 | | %FSR |
| **ADC ANALOG INPUTS (INAP/M, INBP/M, INCP/M, INDP/M)** | | | | | | |
| FS | Input full scale (differential) | 1x or 2x AVG, RSW = 0 | | 0.95 | | Vpp |
| | | 1x AVG, RSW = 1 | | 1.0 | | |
| | | 2x AVG, RSW = 1 | | 1.1 | | |
| $V_{ICM}$ | Input common model voltage | | 250 | 350 | 450 | mV |
| $Z_{IN}$ | Differential input impedance | Differential at 100 MHz | | 100 | | Ω |
| $V_{OCM}$ | Output common mode voltage | | | 350 | | mV |
| BW | Analog Input Bandwidth (-3 dB) | No averaging, RSW=1 | | 1.6 | | GHz |
| | | 2x averaging, RSW=1 | | 1.5 | | |
| Phase imbalance, analog input | | | | ±2 | | deg |
| Amplitude imablance, analog input | | | | ±0.5 | | dB |
| **CLOCK INPUT (CLKP/M)** | | | | | | |
| Input clock frequency | | | 500 | | 1500 | MHz |
| $V_{ID}$ | Differential input voltage | | | 1 | 2.4 | Vpp |
| $V_{ICM}$ | Input common mode voltage | | 0.65 | 0.75 | 0.85 | V |
| $Z_{IN}$ | Differential input impedance | Differential at 1.5 GHz | | 100 | | Ω |
| Clock duty cycle | | | 45 | 50 | 55 | % |
| **SYSREF INPUT (SYSREFP/M)** | | | | | | |
| $V_{ID}$ | Differential input voltage | | 0.6 | 0.8 | 1 | Vpp |
| $V_{ICM}$ | Input common mode voltage | Input common mode voltage | 1.05 | 1.2 | 1.4 | V |
| $Z_{IN}$ | Differential input termination | | | 100 | | Ω |
| **DIGITAL INPUTS (RESET, PDN, SCLK, SEN, SDIO, GPIO1/2, SPISEL)** | | | | | | |
| $V_{IH}$ | High-level input voltage | | 0.8 | | | V |
| $V_{IL}$ | Low-level input voltage | | | | 0.4 | V |
| $C_I$ | Input capacitance | | | 0.6 | | pF |
| **DIGITAL OUTPUTS (SDIO)** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{LOAD}$ = -400 uA | AVDD18 − 0.1 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{LOAD}$ = 400 uA | | | 0.1 | V |
| **CML SERDES OUTPUTS: DOUT[0..7]P/M** | | | | | | |
| $V_{OD}$ | Serdes transmitter output amplitude | differential peak-peak | | 0.7 | | Vpp |
| $V_{OCM}$ | Serdes transmitter output common mode | | | 0.425 | | V |
| $Z_{TX}$ | Serdes transmitter single ended termination impedance | | | 50 | | Ω |
| | Transmitter short-circuit current | Transmitter pins shorted to any voltage between −0.25 V and 1.45 V | −100 | | 100 | mA |

www.ti.com

## 6.7 Electrical Characteristics - AC Specifications (Dither DISABLED)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, Bypass mode, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V, –1-dBFS differential input and dither DISABLED, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| NSD | Noise Spectral Density | $f_{IN}$ = 900 MHz, $A_{IN}$ = -20 dBFS no averaging | | -153.3 | | dBFS/Hz |
| | | $f_{IN}$ = 900 MHz, $A_{IN}$ = -20 dBFS 2x averaging | | -156.1 | | |
| NF | Noise Figure | $f_{IN}$ = 900 MHz, $A_{IN}$ = -20 dBFS no averaging | | 21.7 | | dB |
| | | $f_{IN}$ = 900 MHz, $A_{IN}$ = -20 dBFS 2x averaging | | 19.7 | | |
| SNR | Signal-to-noise ratio no averaging | $f_{IN}$ = 100 MHz | | 64.1 | | dBFS |
| | | $f_{IN}$ = 600 MHz | | 64.1 | | |
| | | $f_{IN}$ = 900 MHz | | 63.9 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 65.1 | | |
| | | $f_{IN}$ = 1.4 GHz | | 63.6 | | |
| | Signal-to-noise ratio 2x averaging | $f_{IN}$ = 100 MHz | | 66.5 | | |
| | | $f_{IN}$ = 600 MHz | | 66.6 | | |
| | | $f_{IN}$ = 900 MHz | | 66.3 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 67.9 | | |
| | | $f_{IN}$ = 1.4 GHz | | 65.9 | | |
| SINAD | Signal to noise and distortion ratio | $f_{IN}$ = 100 MHz | | 60.6 | | dBFS |
| | | $f_{IN}$ = 600 MHz | | 62.2 | | |
| | | $f_{IN}$ = 900 MHz | | 62.1 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 61.4 | | |
| | | $f_{IN}$ = 1.4 GHz | | 62.0 | | |
| ENOB | Effective number of bits | $f_{IN}$ = 100 MHz | | 10.4 | | Bits |
| | | $f_{IN}$ = 600 MHz | | 10.4 | | |
| | | $f_{IN}$ = 900 MHz | | 10.3 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 10.5 | | |
| | | $f_{IN}$ = 1.4 GHz | | 10.3 | | |
| THD | Total Harmonic Distortion (First five harmonics) | $f_{IN}$ = 100 MHz | | 64 | | dBc |
| | | $f_{IN}$ = 600 MHz | | 67 | | |
| | | $f_{IN}$ = 900 MHz | | 67 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 64 | | |
| | | $f_{IN}$ = 1.4 GHz | | 68 | | |
| HD2 | Second Harmonic Distortion | $f_{IN}$ = 100 MHz | | 72 | | dBc |
| | | $f_{IN}$ = 600 MHz | | 70 | | |
| | | $f_{IN}$ = 900 MHz | | 71 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 68 | | |
| | | $f_{IN}$ = 1.4 GHz | | 69 | | |
| HD3 | Third Harmonic Distortion | $f_{IN}$ = 100 MHz | | 65 | | dBc |
| | | $f_{IN}$ = 600 MHz | | 73 | | |
| | | $f_{IN}$ = 900 MHz | | 71 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 69 | | |
| | | $f_{IN}$ = 1.4 GHz | | 81 | | |

Product Folder Links: *ADC34RF52*

## 6.7 Electrical Characteristics - AC Specifications (Dither DISABLED) (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, Bypass mode, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V, –1-dBFS differential input and dither DISABLED, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Non HD2,3 | Spur free dynamic range (excluding HD2 and HD3) | $f_{IN}$ = 100 MHz | | 82 | | dBFS |
| | | $f_{IN}$ = 600 MHz | | 83 | | |
| | | $f_{IN}$ = 900 MHz | | 83 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 93 | | |
| | | $f_{IN}$ = 1.4 GHz | | 81 | | |
| IMD3 | Two tone inter-modulation distortion | $f_1$ = 900 MHz, $f_2$ = 1000 MHz, $A_{IN}$ = -7 dBFS/tone | | 81 | | dBFS |

## 6.8 Electrical Characteristics - AC Specifications (Dither ENABLED)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, Bypass mode, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V, –4-dBFS differential input and dither ENABLED, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN[2] | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| NSD[1] | Noise Spectral Density | $f_{IN}$ = 900 MHz, $A_{IN}$ = -20 dBFS no averaging | -151.0 | -153.3 | | dBFS/Hz |
| | | $f_{IN}$ = 900 MHz, $A_{IN}$ = -20 dBFS 2x averaging | -153.0 | -156.1 | | |
| NF[1] | Noise Figure | $f_{IN}$ = 900 MHz, $A_{IN}$ = -20 dBFS no averaging | | 21.6 | | dB |
| | | $f_{IN}$ = 900 MHz, $A_{IN}$ = -20 dBFS 2x averaging | | 19.7 | | |
| SNR[1] | Signal-to-noise ratio no averaging | $f_{IN}$ = 100 MHz | | 63.6 | | dBFS |
| | | $f_{IN}$ = 600 MHz | | 64.4 | | |
| | | $f_{IN}$ = 900 MHz | 61.3 | 64.4 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | 62.9 | 65.2 | | |
| | | $f_{IN}$ = 1.4 GHz | | 63.8 | | |
| | Signal-to-noise ratio 2x averaging | $f_{IN}$ = 100 MHz | | 66.3 | | |
| | | $f_{IN}$ = 600 MHz | | 66.9 | | |
| | | $f_{IN}$ = 900 MHz | 63.9 | 66.8 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | 64.9 | 68.0 | | |
| | | $f_{IN}$ = 1.4 GHz | | 66.1 | | |
| SINAD[1] | Signal to noise and distortion ratio | $f_{IN}$ = 100 MHz | | 62.2 | | dBFS |
| | | $f_{IN}$ = 600 MHz | | 63.4 | | |
| | | $f_{IN}$ = 900 MHz | | 63.6 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 64.4 | | |
| | | $f_{IN}$ = 1.4 GHz | | 62.8 | | |
| ENOB[1] | Effective number of bits | $f_{IN}$ = 100 MHz | | 10.3 | | Bits |
| | | $f_{IN}$ = 600 MHz | | 10.4 | | |
| | | $f_{IN}$ = 900 MHz | | 10.4 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 10.5 | | |
| | | $f_{IN}$ = 1.4 GHz | | 10.3 | | |
| THD | Total Harmonic Distortion (First five harmonics) | $f_{IN}$ = 100 MHz | | 68 | | dBc |
| | | $f_{IN}$ = 600 MHz | | 72 | | |
| | | $f_{IN}$ = 900 MHz | | 72 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 72 | | |
| | | $f_{IN}$ = 1.4 GHz | | 71 | | |
| HD2 | Second Harmonic Distortion | $f_{IN}$ = 100 MHz | | 75 | | dBc |
| | | $f_{IN}$ = 600 MHz | | 75 | | |
| | | $f_{IN}$ = 900 MHz | 70 | 74 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 87 | | |
| | | $f_{IN}$ = 1.4 GHz | | 72 | | |
| HD3 | Third Harmonic Distortion | $f_{IN}$ = 100 MHz | | 70 | | dBc |
| | | $f_{IN}$ = 600 MHz | | 77 | | |
| | | $f_{IN}$ = 900 MHz | 71 | 79 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 74 | | |
| | | $f_{IN}$ = 1.4 GHz | | 81 | | |

## 6.8 Electrical Characteristics - AC Specifications (Dither ENABLED) (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, Bypass mode, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V, –4-dBFS differential input and dither ENABLED, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN[2] | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| Non HD2,3 | Spur free dynamic range (excluding HD2 and HD3) | $f_{IN}$ = 100 MHz | | 92 | | dBFS |
| | | $f_{IN}$ = 600 MHz | | 89 | | |
| | | $f_{IN}$ = 900 MHz | 85 | 90 | | |
| | | $f_{IN}$ = 900 MHz, Ain = -20 dBFS | | 97 | | |
| | | $f_{IN}$ = 1.4 GHz | | 94 | | |
| IMD3 | Two tone inter-modulation distortion | $f_1$ = 900 MHz, $f_2$ = 1000 MHz, $A_{IN}$ = -10 dBFS/tone | 74 | 84 | | dBFS |

(1) Measured from 100 MHz to Nyquist ($F_S$/2) excluding dither
(2) SNR, IMD3 minimum values are specified by ATE, HD2, HD3 and Non HD23 are specified by bench characterization.

## 6.9 Timing Requirements

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, Bypass mode, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V, –1-dBFS differential input and dither DISABLED, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **ADC TIMING SPECIFICATIONS** | | | | | | |
| $T_{AD}$ | Aperture Delay | | | 0.17 | | ns |
| | Aperure Delay variation | | | 0.07 | | |
| $T_A$ | Aperture Jitter | | | 50 | | fs |
| Overload recovery time | | 3-dB overload condition | | 10 | | clock cycles |
| | | 6-dB overload condition | | 50 | | |
| $t_{ADC}$ | ADC latency from sampling instant to internal hand-off to digital | | | 68 | | ADC clock cycles |
| | Internal propagation delay | | | 5 | | ns |
| | Latency adder for 2x averaging | | | 4 | | ADC clock cycles |
| | Deterministic delay from digital block (DDC (if used) and JESD interface) | LMFS = 8-4-8-10 | | 163 | | ADC clock cycles |
| | | LMFS = 8-4-2-2 | | 131 | | |
| | | 4x real decimation, LMFS = 8-4-2-2 | | 456 | | |
| | | 4x decimation, F (number of octets) = 2 | | 394 | | |
| | | 4x decimation, F = 4 | | 374 | | |
| | | 4x decimation, F = 8 | | 367 | | |
| | | 8x decimation, F = 2 | | 560 | | |
| | | 8x decimation, F = 4 | | 520 | | |
| | | 8x decimation, F = 8 | | 506 | | |
| | | 8x decimation, F = 16 | | 491 | | |
| | | 16x decimation, F = 2 | | 900 | | |
| | | 16x decimation, F = 4 | | 820 | | |
| | | 16x decimation, F = 8 | | 792 | | |
| | | 16x decimation, F = 16 | | 762 | | |
| | | 16x decimation, F = 32 | | 748 | | |
| | | 32x decimation, F = 2 | | 1596 | | |
| | | 32x decimation, F = 4 | | 1436 | | |
| | | 32x decimation, F = 8 | | 1380 | | |
| | | 32x decimation, F = 16 | | 1320 | | |
| | | 32x decimation, F = 32 | | 1292 | | |
| | | 64x decimation, F = 2 | | 2940 | | |
| | | 64x decimation, F = 4 | | 2620 | | |
| | | 64x decimation, F = 8 | | 2508 | | |
| | | 64x decimation, F = 16 | | 2388 | | |
| | | 64x decimation, F = 32 | | 2332 | | |
| | | 128x decimation, F = 2 | | 5668 | | |
| | | 128x decimation, F = 4 | | 5028 | | |
| | | 128x decimation, F = 8 | | 4804 | | |
| | | 128x decimation, F = 16 | | 4564 | | |
| | | 128x decimation, F = 32 | | 4452 | | |

Product Folder Links: *ADC34RF52*

## 6.9 Timing Requirements (continued)

Maximum and minimum values are specified over the operating free-air temperature range and nominal supply voltages. Typical values are specified at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, Bypass mode, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V, –1-dBFS differential input and dither DISABLED, unless otherwise noted

| PARAMETER | | TEST CONDITIONS | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SERIAL PROGRAMMING INTERFACE (SCLK, SEN, SDIO) - Input** | | | | | | |
| $f_{CLK(SCLK)}$ | Serial clock frequency | | 1 | | 20 | MHz |
| $t_{SU(SEN)}$ | SEN to rising edge of SCLK | | 10 | | | ns |
| $t_{H(SEN)}$ | SEN from rising edge of SCLK | | 10 | | | ns |
| $t_{SU(SDIO)}$ | SDIO to rising edge of SCLK | | 10 | | | ns |
| $t_{H(SDIO)}$ | SDIO from rising edge of SCLK | | 10 | | | ns |
| **SERIAL PROGRAMMING INTERFACE (SDIO) - Output** | | | | | | |
| $t_{(OZD)}$ | SDIO tri-state to driven | | | | 10 | ns |
| $t_{(ODZ)}$ | SDIO data to tri-state | | | | 14 | ns |
| $t_{(OD)}$ | SDIO valid from falling edge of SCLK | | | | 10 | ns |
| **TIMING: SYSREFP/M** | | | | | | |
| $t_{s(SYSREF)}$ | Setup time, SYSREFP/M valid to rising edge of CLKP/M | | 50 | | | ps |
| $t_{h(SYSREF)}$ | Hold time, SYSREFP/M valid to rising edge of CLKP/M | | 50 | | | ps |
| **CML SERDES OUTPUTS: DOUT[0..7]P/M** | | | | | | |
| $f_{Serdes}$ | Serdes bit rate | | 0.5 | 12.8 | 13.0 | Gbps |
| $R_J$ | Random jitter, RMS | RPAT, 6.4 Gbps | | 0.7 | | ps |
| $R_J$ | Random jitter, RMS | RPAT, 12.8 Gbps | | 0.6 | | ps |
| $D_J$ | Deterministic jitter, peak to peak | RPAT, 6.4 Gbps | | 8.9 | | ps |
| $D_J$ | Deterministic jitter, peak to peak | RPAT, 12.8 Gbps | | 14.7 | | ps |
| $T_J$ | Total jitter, peak to peak | RPAT, 6.4 Gbps | | 19.5 | | ps |
| $T_J$ | Total jitter, peak to peak | RPAT, 12.8 Gbps | | 24 | | |

## 6.10 Typical Characteristics

Typical values are at $T_A$ = 25°C, ADC sampling rate = 1.5 GSPS, 50% clock duty cycle, AVDD18 = 1.8 V, AVDD12, CLKVDD, DVDD = 1.2 V and –1-dBFS differential input, Dither = DIS, unless otherwise noted
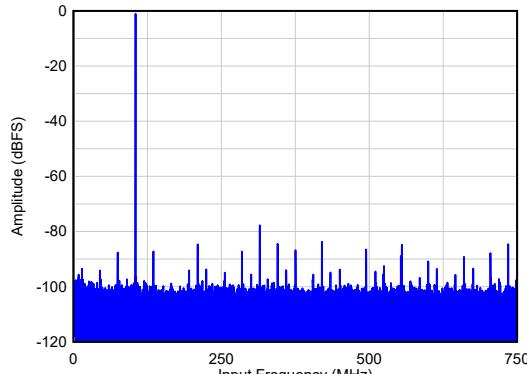


SNR = 64.5 dBFS, HD23 = 77 dBc, Non HD23 = 84 dBFS

$A_{IN}$ = -1 dBFS, 1x AVG, Dither = DIS

**Figure 6-1. Single Tone FFT at $F_{IN}$ = 100 MHz**
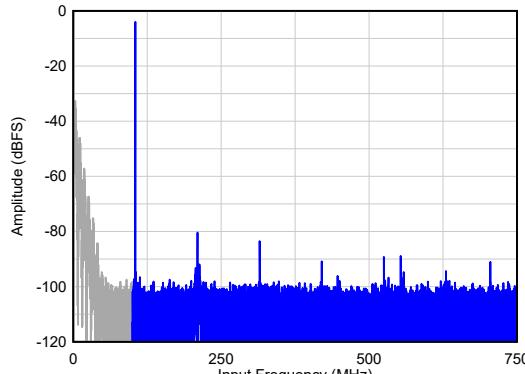


SNR = 64.3 dBFS[1], HD23 = 76 dBc, Non HD23 = 89 dBFS

$A_{IN}$ = -4 dBFS, 1x AVG, Dither = EN

**Figure 6-2. Single Tone FFT at $F_{IN}$ = 100 MHz**
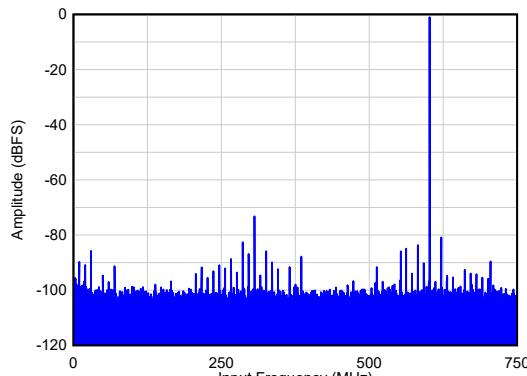


SNR = 64.4 dBFS, HD23 = 72 dBc, Non HD23 = 81 dBFS

$A_{IN}$ = -1 dBFS, 1x AVG, Dither = DIS

**Figure 6-3. Single Tone FFT at $F_{IN}$ = 600 MHz**
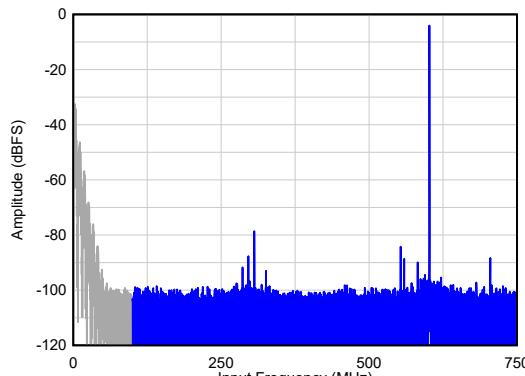


SNR = 64.4 dBFS[1], HD23 = 75 dBc, Non HD23 = 84 dBFS

$A_{IN}$ = -4 dBFS, 1x AVG, Dither = EN

**Figure 6-4. Single Tone FFT at $F_{IN}$ = 600 MHz**
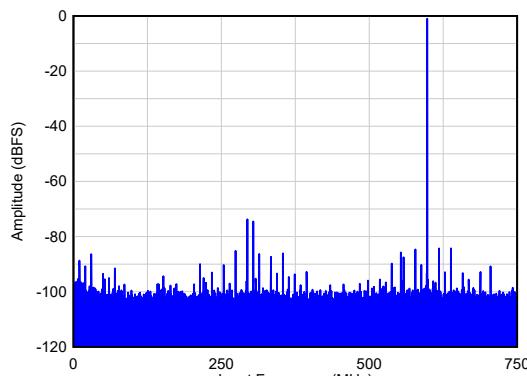


SNR = 64.3 dBFS, HD23 = 72 dBc, Non HD23 = 84 dBFS

$A_{IN}$ = -1 dBFS, 1x AVG, Dither = DIS

**Figure 6-5. Single Tone FFT at $F_{IN}$ = 900 MHz**
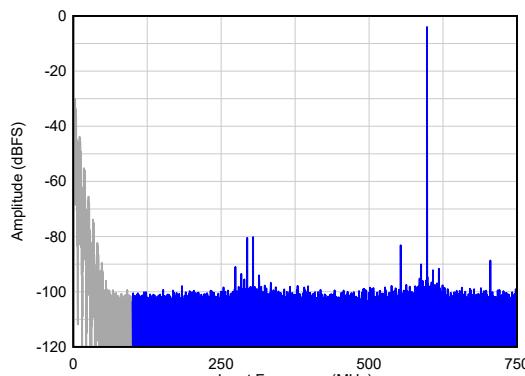


SNR = 64.4 dBFS[1], HD23 = 76 dBc, Non HD23 = 83 dBFS

$A_{IN}$ = -4 dBFS, 1x AVG, Dither = EN

**Figure 6-6. Single Tone FFT at $F_{IN}$ = 900 MHz**

---

[1]  Measured from 100 MHz to $F_S$/2

Product Folder Links: *ADC34RF52*

SNR = 63.8 dBFS, HD23 = 69 dBc, Non HD23 = 80 dBFS

$A_{IN}$ = -1 dBFS, 1x AVG, Dither = DIS
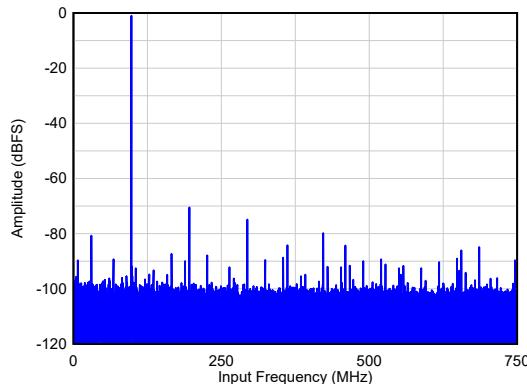
**Figure 6-7. Single Tone FFT at $F_{IN}$ = 1400 MHz**



SNR = 64.1 dBFS[1], HD23 = 71 dBc, Non HD23 = 86 dBFS

$A_{IN}$ = -4 dBFS, 1x AVG, Dither = EN
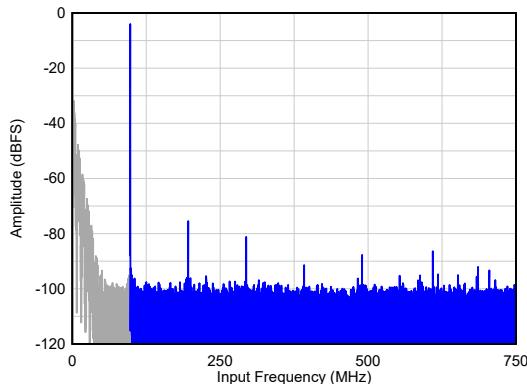
**Figure 6-8. Single Tone FFT at $F_{IN}$ = 1400 MHz**



SNR = 62.6 dBFS, HD23 = 60 dBc, Non HD23 = 79 dBFS

$A_{IN}$ = -1 dBFS, 1x AVG, Dither = DIS
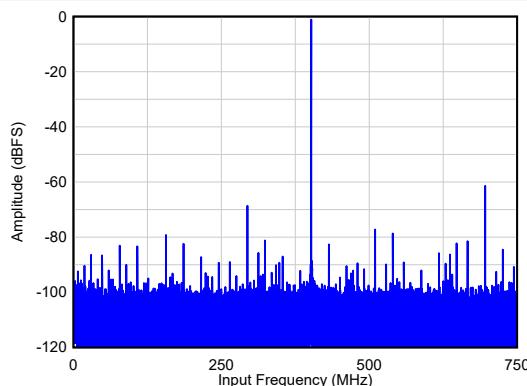
**Figure 6-9. Single Tone FFT at $F_{IN}$ = 1900 MHz**



SNR = 63.4 dBFS[1], HD23 = 63 dBc, Non HD23 = 89 dBFS

$A_{IN}$ = -4 dBFS, 1x AVG, Dither = EN
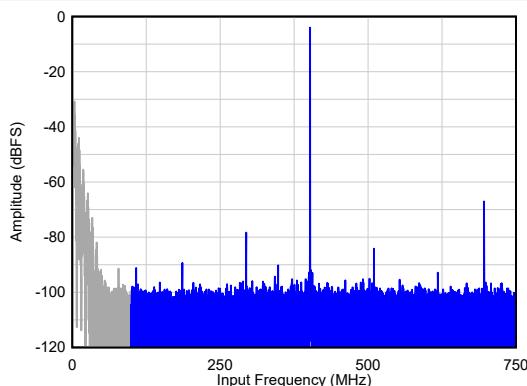
**Figure 6-10. Single Tone FFT at $F_{IN}$ = 1900 MHz**



SNR = 66.8 dBFS, HD23 = 67 dBc, Non HD23 = 82 dBFS

$A_{IN}$ = -1 dBFS, 2x AVG, Dither = DIS
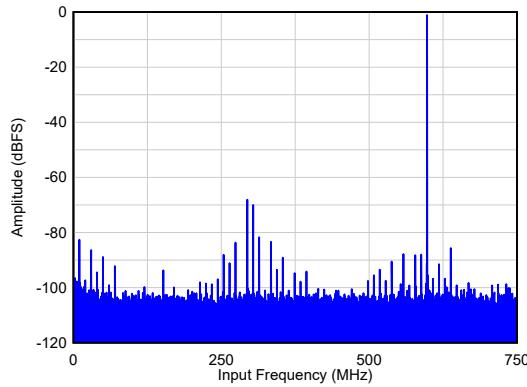
**Figure 6-11. Single Tone FFT at $F_{IN}$ = 900 MHz**



SNR = 67.0 dBFS[1], HD23 = 72 dBc, Non HD23 = 89 dBFS

$A_{IN}$ = -4 dBFS, 2x AVG, Dither = EN
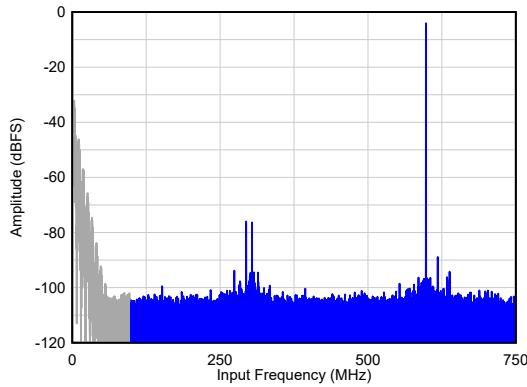
**Figure 6-12. Single Tone FFT at $F_{IN}$ = 900 MHz**
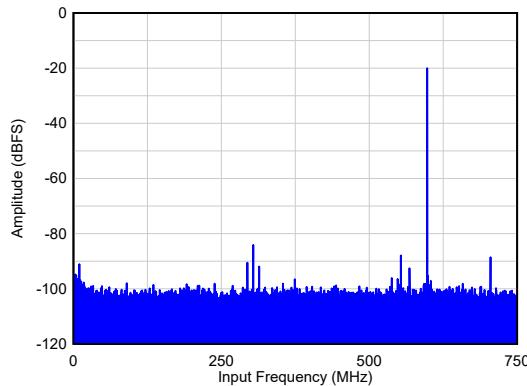
SNR = 65.2 dBFS, HD23 = 64 dBc, Non HD23 = 88 dBFS
$A_{IN}$ = -20 dBFS, 1x AVG, Dither = DIS

**Figure 6-13. Single Tone FFT at $F_{IN}$ = 900 MHz**
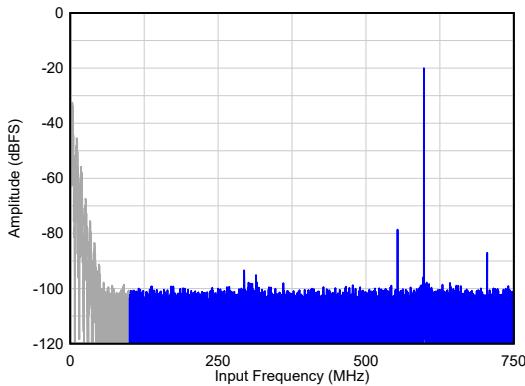


SNR = 64.8 dBFS[1], HD23 = 59 dBc, Non HD23 = 79 dBFS
$A_{IN}$ = -20 dBFS, 1x AVG, Dither = EN

**Figure 6-14. Single Tone FFT at $F_{IN}$ = 900 MHz**
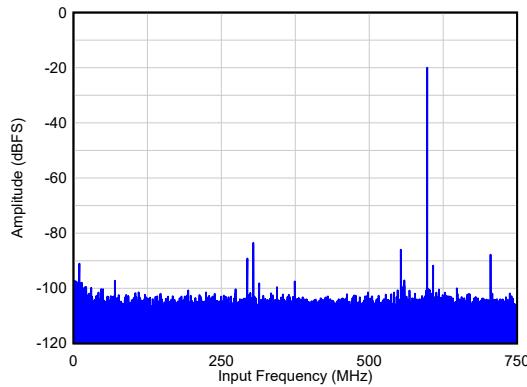


SNR = 67.9 dBFS, HD23 = 64 dBc, Non HD23 = 86 dBFS
$A_{IN}$ = -20 dBFS, 2x AVG, Dither = DIS

**Figure 6-15. Single Tone FFT at $F_{IN}$ = 900 MHz**
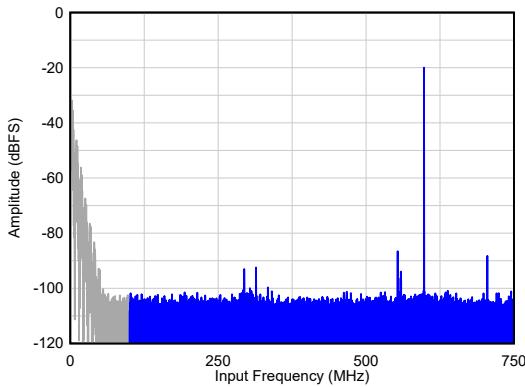


SNR = 67.6 dBFS[1], HD23 = 67 dBc, Non HD23 = 87 dBFS
$A_{IN}$ = -20 dBFS, 2x AVG, Dither = EN

**Figure 6-16. Single Tone FFT at $F_{IN}$ = 900 MHz**
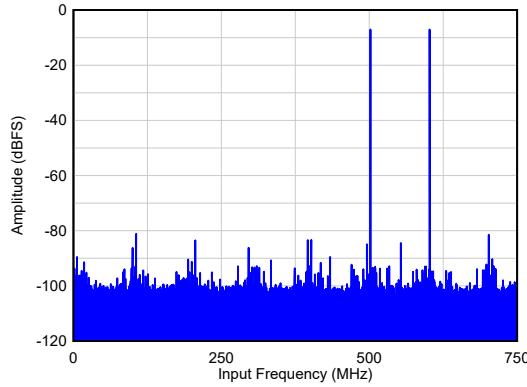


IMD3 = 73 dBc
$A_{IN}$ = -7 dBFS/tone, 1x AVG, Dither = DIS

**Figure 6-17. Two Tone FFT at $F_{IN}$ = 900, 1000 MHz**
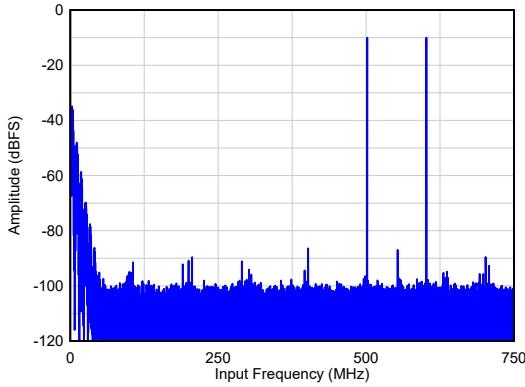


IMD3 = 75 dBc
$A_{IN}$ = -10 dBFS/tone, 1x AVG, Dither = EN

**Figure 6-18. Two Tone FFT at $F_{IN}$ = 900, 1000 MHz**

Product Folder Links: *ADC34RF52*
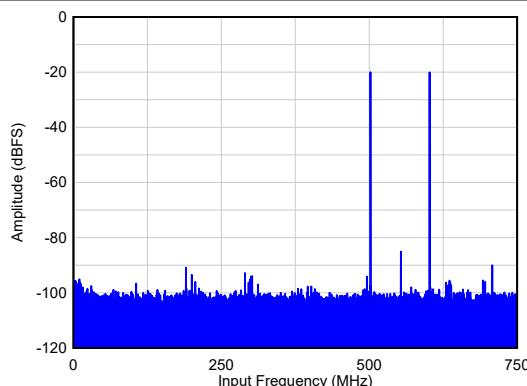
IMD3 = 70 dBc

A$_{IN}$ = -20 dBFS/tone, 1x AVG, Dither = DIS

**Figure 6-19. Two Tone FFT at F$_{IN}$ = 900, 1000 MHz**
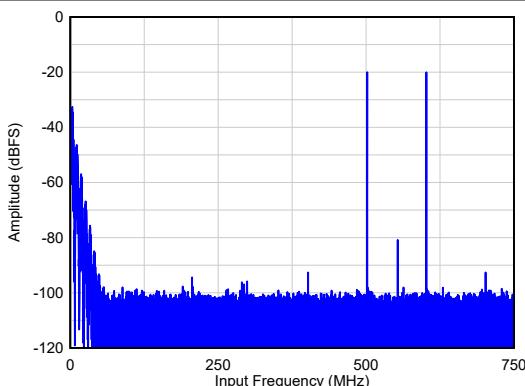


IMD3 = 72 dBc

A$_{IN}$ = -20 dBFS/tone, 1x AVG, Dither = EN

**Figure 6-20. Two Tone FFT at F$_{IN}$ = 900, 1000 MHz**
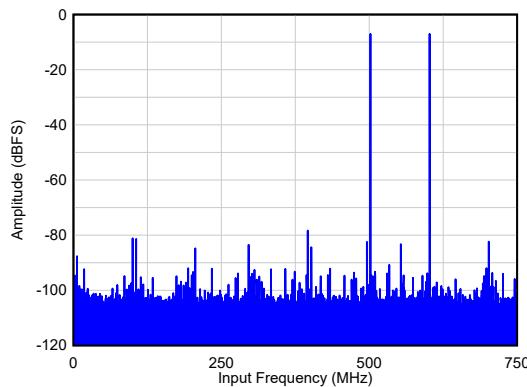


IMD3 = 72 dBc

A$_{IN}$ = -7 dBFS/tone, 2x AVG, Dither = DIS

**Figure 6-21. Two Tone FFT at F$_{IN}$ = 900, 1000 MHz**
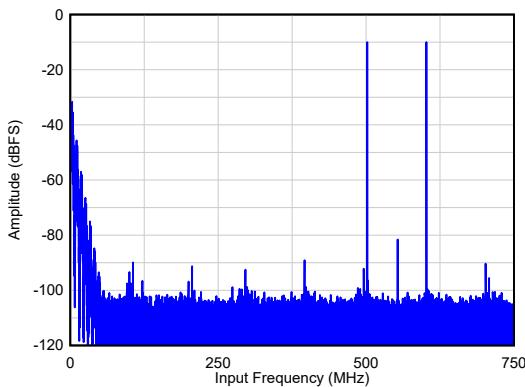


IMD3 = 79 dBc

A$_{IN}$ = -10 dBFS/tone, 2x AVG, Dither = EN

**Figure 6-22. Two Tone FFT at F$_{IN}$ = 900, 1000 MHz**
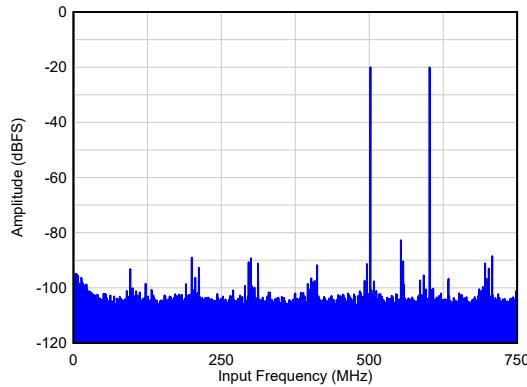


IMD3 = 63 dBc

A$_{IN}$ = -20 dBFS/tone, 2x AVG, Dither = DIS

**Figure 6-23. Two Tone FFT at F$_{IN}$ = 900, 1000 MHz**
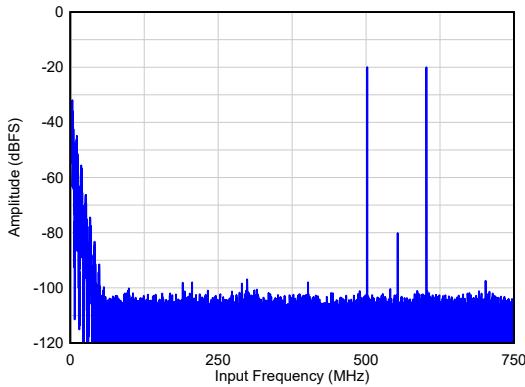


IMD3 = 77 dBc

A$_{IN}$ = -20 dBFS/tone, 2x AVG, Dither = EN

**Figure 6-24. Two Tone FFT at F$_{IN}$ = 900, 1000 MHz**

A_IN = -1 dBFS, Dither = DIS
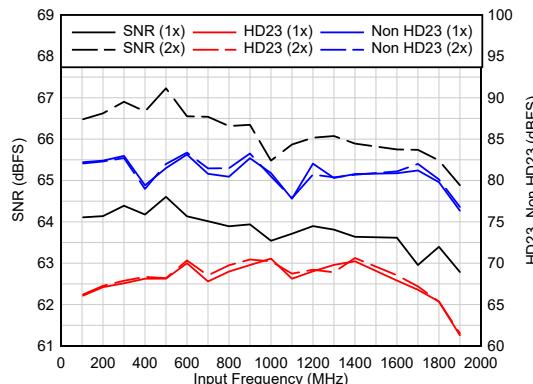
**Figure 6-25. AC Performance vs F_IN**



A_IN = -4 dBFS, Dither = EN
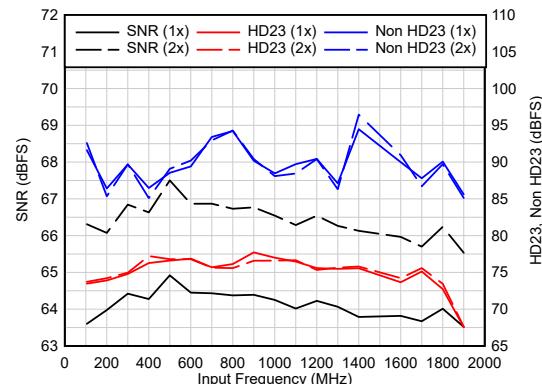
**Figure 6-26. AC Performance vs F_IN**
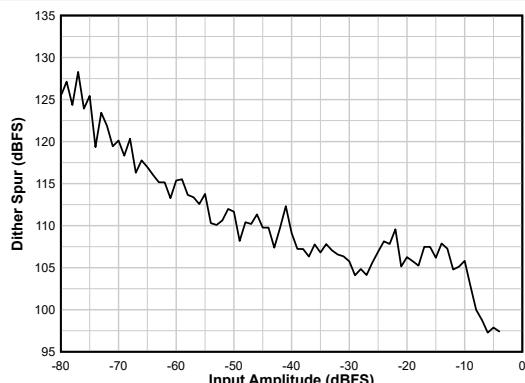


F_IN = 900 MHz

**Figure 6-27. Dither Spur vs A_IN**



A_IN = -20 dBFS
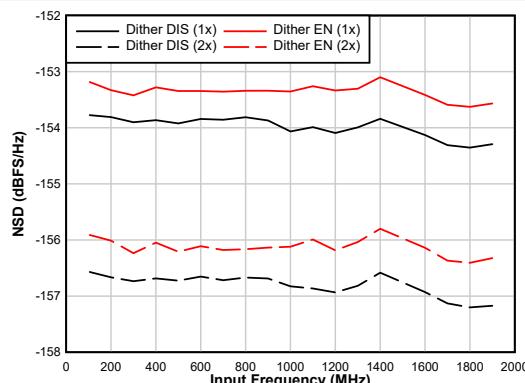
**Figure 6-28. NSD Performance vs F_IN**
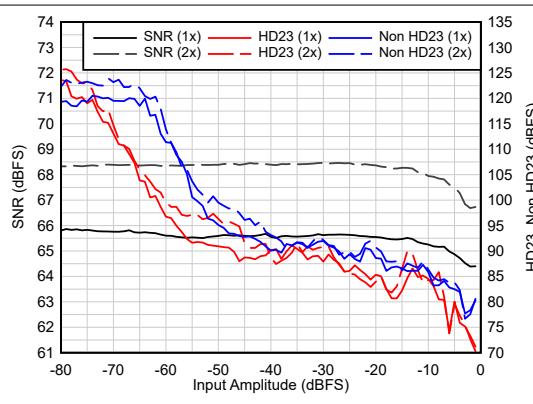


Dither = DIS

**Figure 6-29. AC Performance vs A_IN**
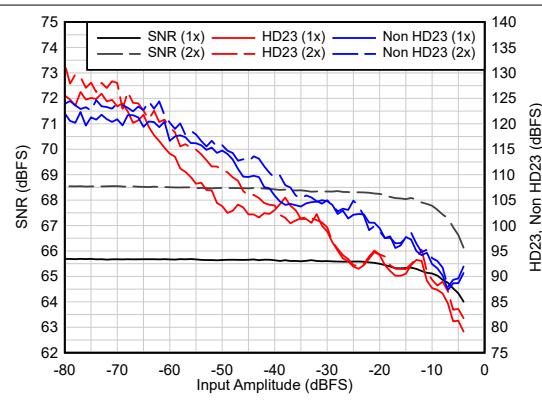


Dither = EN

**Figure 6-30. AC Performance vs A_IN**

Product Folder Links: *ADC34RF52*
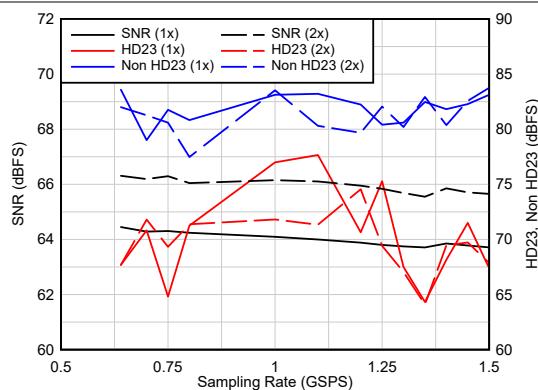
$F_{IN}$ = 900 MHz, $A_{IN}$ = -1 dBFS, Dither = DIS

**Figure 6-31. AC Performance vs $F_S$**
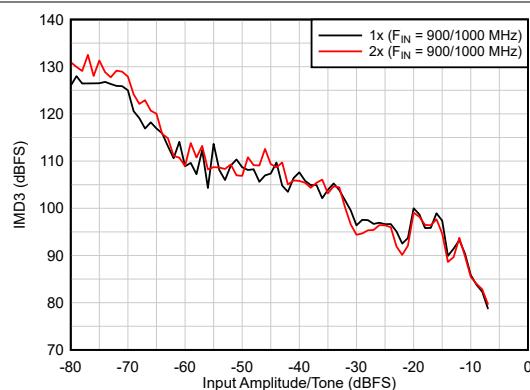


Dither = DIS

**Figure 6-32. IMD3 Performance vs $A_{IN}$**
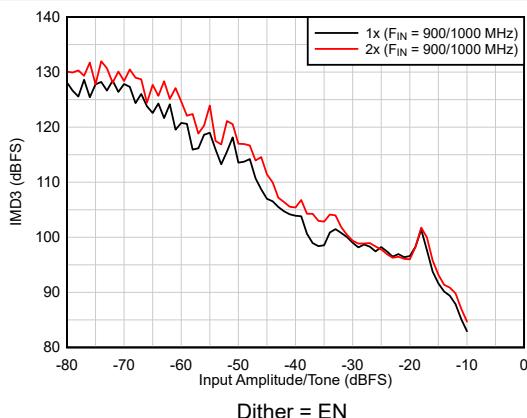


Dither = EN

**Figure 6-33. IMD3 Performance vs $A_{IN}$**
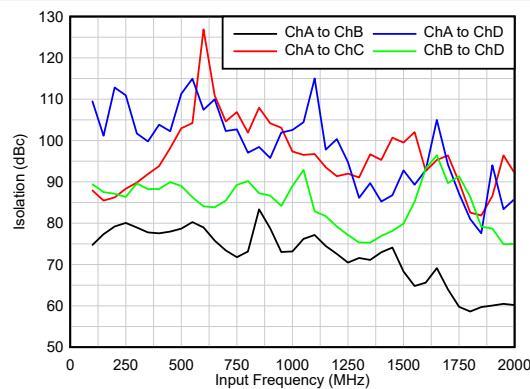


**Figure 6-34. Isolation vs Input Frequency**
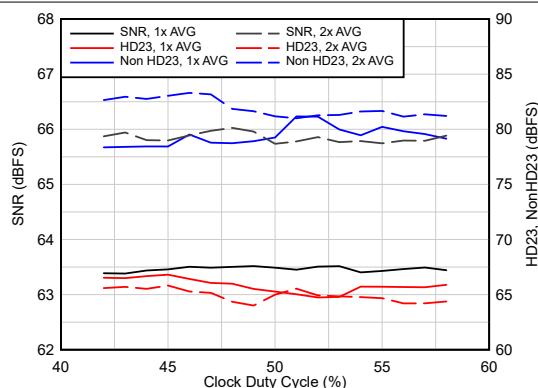


$F_{IN}$ = 900 MHz, $A_{IN}$ = -1 dBFS, 1x AVG, Dither = DIS

**Figure 6-35. AC Performance vs Clock Duty Cycle**
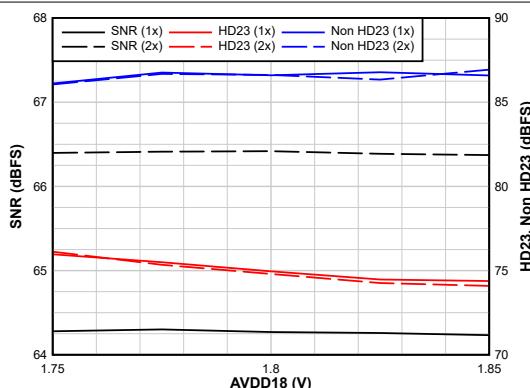


$F_{IN}$ = 900 MHz, $A_{IN}$ = -1 dBFS, Dither = DIS

**Figure 6-36. AC Performance vs AVDD18**

Product Folder Links: *ADC34RF52*

F$_{IN}$ = 900 MHz, A$_{IN}$ = -1 dBFS, Dither = DIS
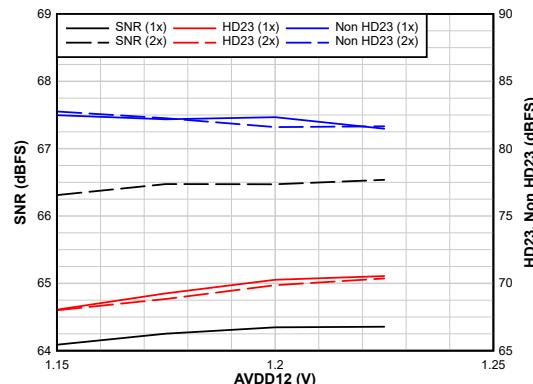
**Figure 6-37. AC Performance vs AVDD12**



F$_{IN}$ = 900 MHz, A$_{IN}$ = -1 dBFS, Dither = DIS
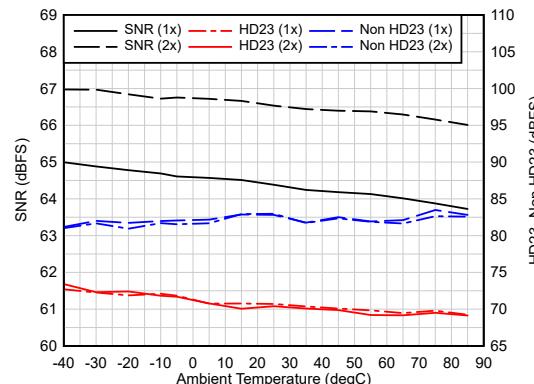
**Figure 6-38. AC Performance vs Temperature**



F$_{IN}$ = 900 MHz, A$_{IN}$ = -1 dBFS, Dither = EN
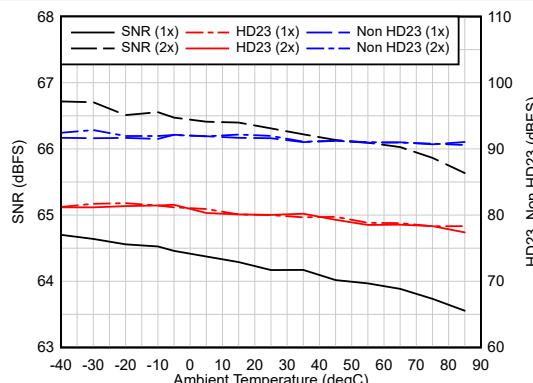
**Figure 6-39. AC Performance vs Temperature**



F$_{IN}$ = 900 MHz, Dither = DIS
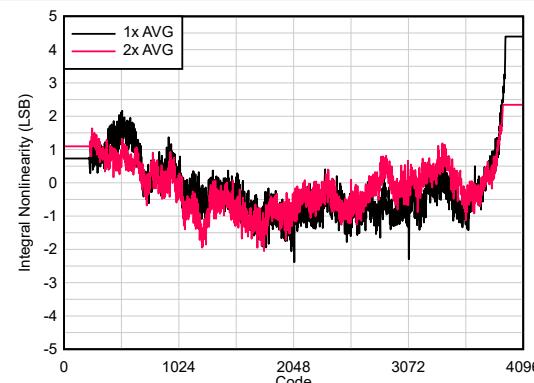
**Figure 6-40. INL vs Code**



F$_{IN}$ = 900 MHz, Dither = DIS
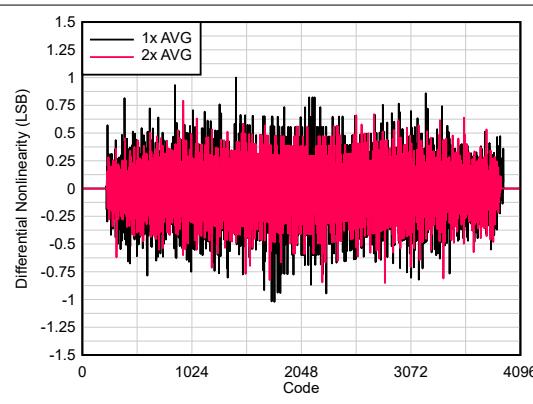
**Figure 6-41. DNL vs Code**
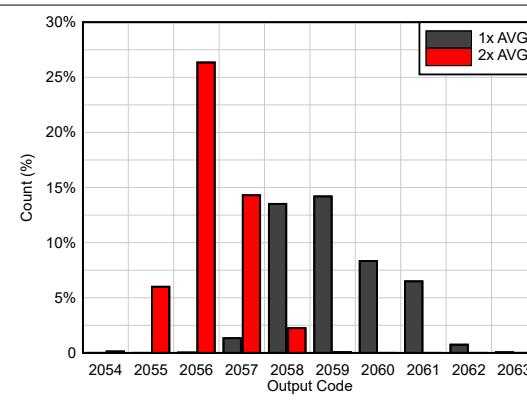


Dither = DIS

**Figure 6-42. DC Offset Histogram**
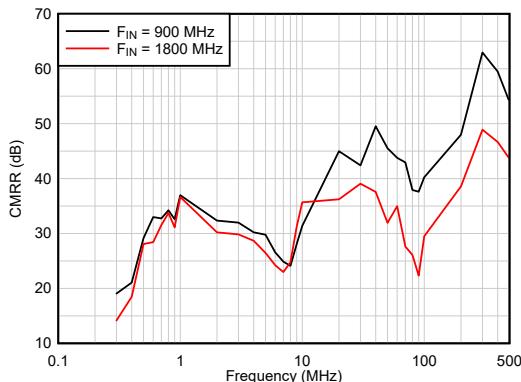
A_IN = -1 dBFS, 1x AVG, Dither = DIS

**Figure 6-43. CMRR**



DDC Bypass
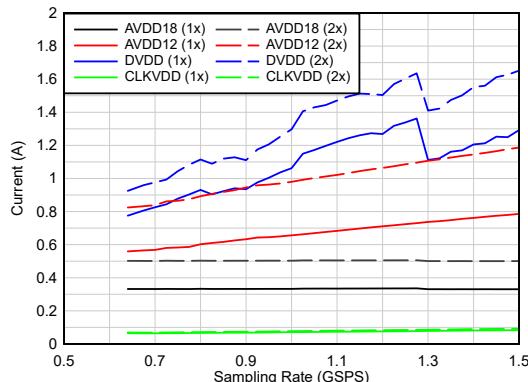
**Figure 6-44. Current vs Sampling Rate vs Averaging**
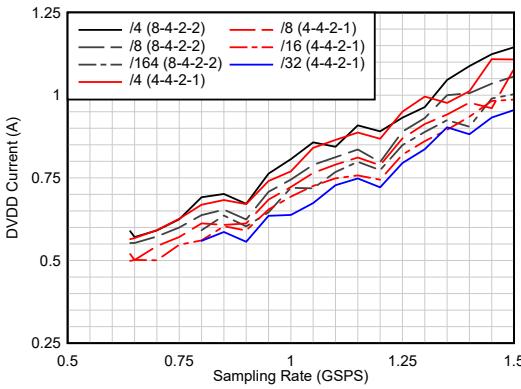


A_IN = -1 dBFS, 1x AVG

**Figure 6-45. Current vs Sampling Rate vs Real Decimation**
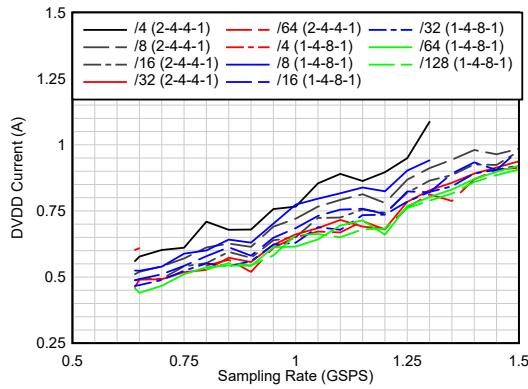


A_IN = -1 dBFS, 1x AVG

**Figure 6-46. Current vs Sampling Rate vs Real Decimation**
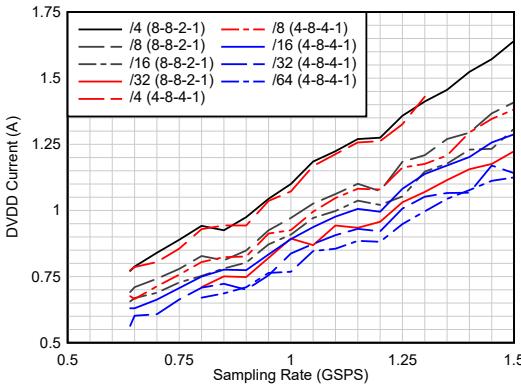


A_IN = -1 dBFS, 1x AVG

Single Band Decimation

**Figure 6-47. Current vs Sampling Rate vs Complex Decimation**
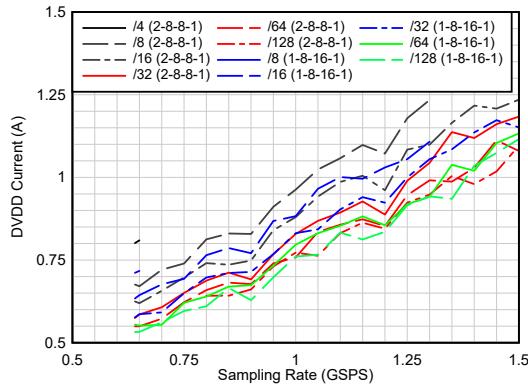


A_IN = -1 dBFS, 1x AVG

Single Band Decimation

**Figure 6-48. Current vs Sampling Rate vs Complex Decimation**
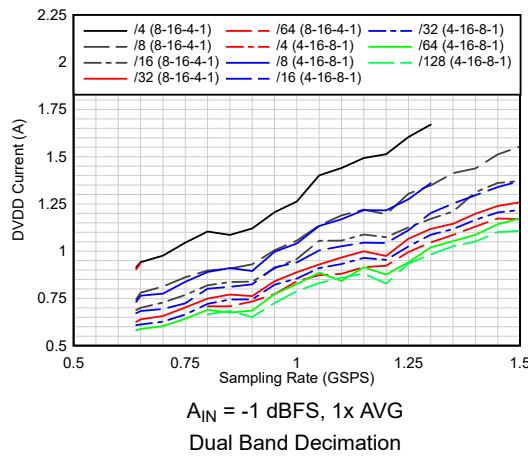
**Figure 6-49. Current vs Sampling Rate vs Complex Decimation**
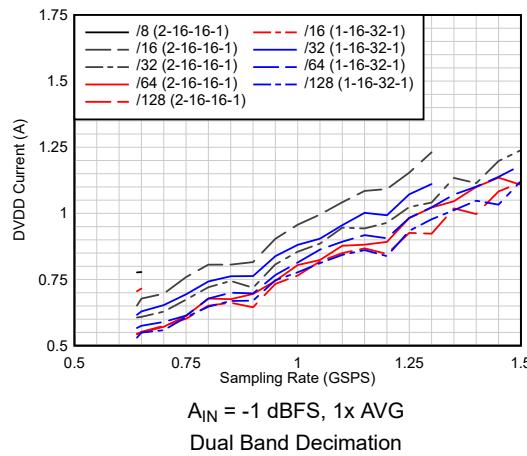


**Figure 6-50. Current vs Sampling Rate vs Complex Decimation**
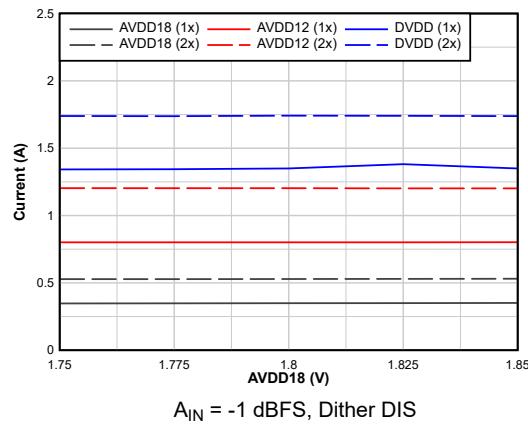


**Figure 6-51. Current vs AVDD18**
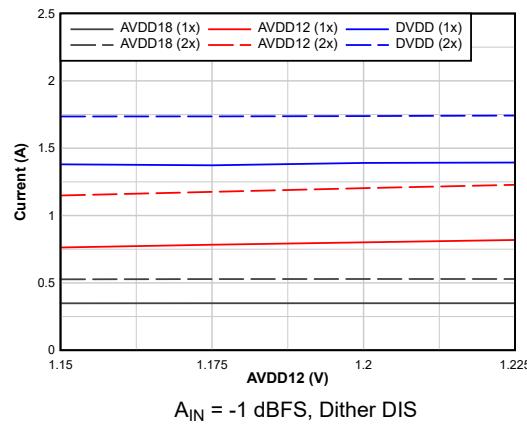


**Figure 6-52. Current vs AVDD12**
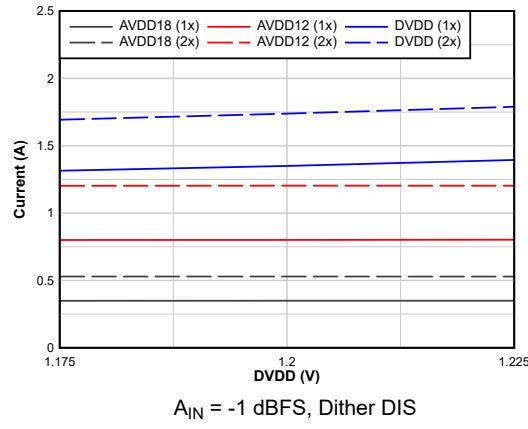


**Figure 6-53. Current vs DVDD**
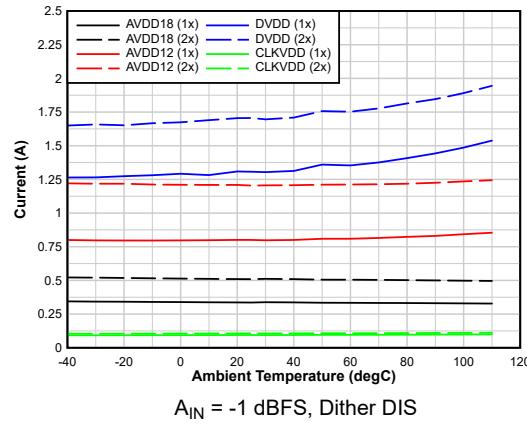


**Figure 6-54. Current vs Temperature**

A$_{IN}$ = -1 dBFS
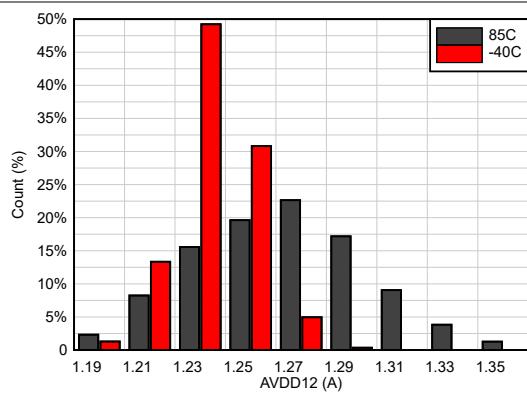
**Figure 6-55. AVDD12 Distribution**



A$_{IN}$ = -1 dBFS
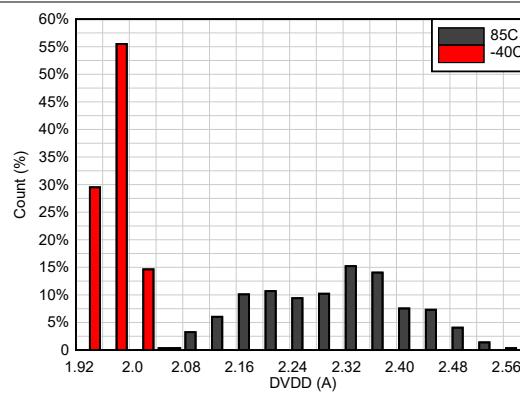
**Figure 6-56. DVDD Distribution**

Product Folder Links: *ADC34RF52*

## 7 Detailed Description

### 7.1 Overview

The ADC34RF52 is a single core (non-interleaved) 14-bit, 1.5 GSPS, quad channel analog to digital converter (ADC).The design maximizes signal-to-noise ratio (SNR) and delivers a noise spectral density of -153 dBFS/Hz. Additional internal ADCs can be used for on-chip averaging to further improve the noise density to as low as -156 dBFS/Hz.

The analog signal input is non-buffered to save power consumption with a nominal differential input impedance of 100 Ω. The full power input bandwidth is 1.6 GHz (-3dB) and the device supports direct RF sampling with input frequencies through the L-band. The device is designed for low residual phase noise to support high performance radar applications. The sampling clock input has a dedicated power supply input which requires a clean power supply.

Each ADC channel can be connected to a dual-band digital down-converter (DDC) using a 48-bit NCO which supports phase coherent frequency hopping. Using the GPIO pins for NCO frequency control, frequency hopping is achieved in less than 1 µs. The digital down converters support a wide range of instantaneous bandwidth (IBW) coverage. A single wide band mode with 4x complex decimation up to two narrow bandwidth channels with as high as 128x complex decimation.

The ADC34RF52 supports the JESD204B serial data interface with subclass 1 deterministic latency using data rates up to 13.0 GBPS. The device is pin-pin compatible with the ADC34RF54 (2.6 GSPS) and ADC34RF55 (3 GSPS).

The power efficient ADC architecture consumes 0.73 W/ch at 1.5 GSPS at maximum sampling rate and provides power scaling with lower sampling rates (0.55 W/ch at 0.6 GSPS).

### 7.2 Functional Block Diagram
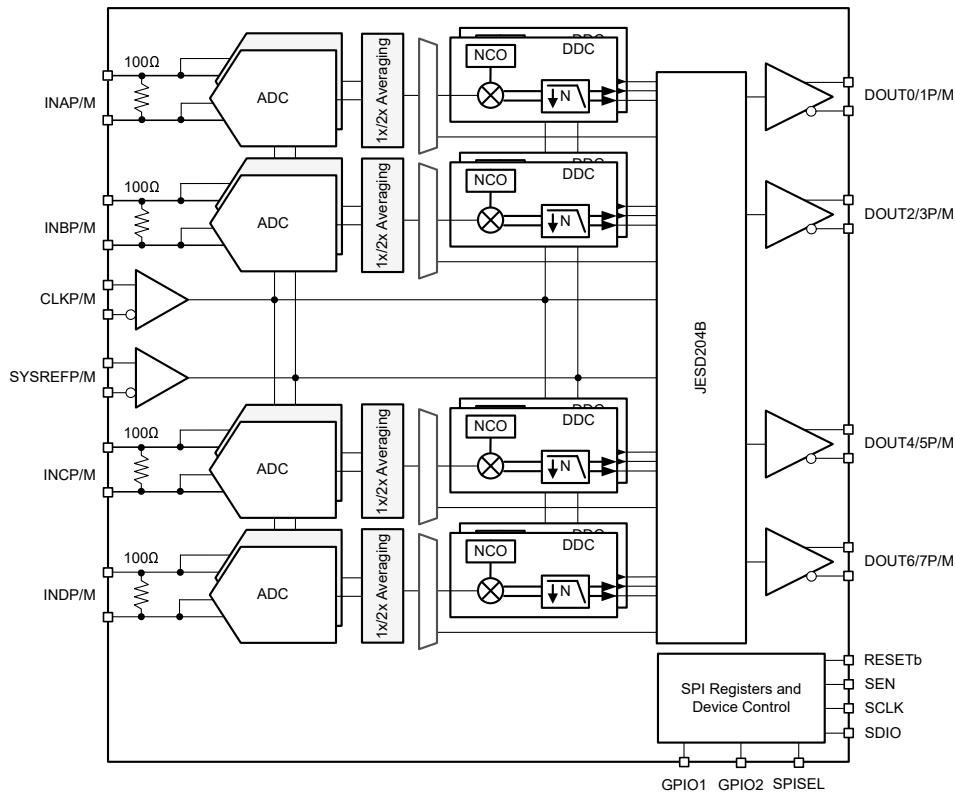
## 7.3 Feature Description

### 7.3.1 Analog Inputs

The ADC34RF52 provides up to two internal ADCs per channel for purpose of averaging to improve the noise performance. Two ADCs are connected internally to the same differential input pins as shown in the equivalent input schematic (see Figure 7-1). The analog inputs have a differential 100 Ω split termination with internal biasing. When only a single ADC is used, there is a minor parasitic capacitance remaining from the unused ADC.
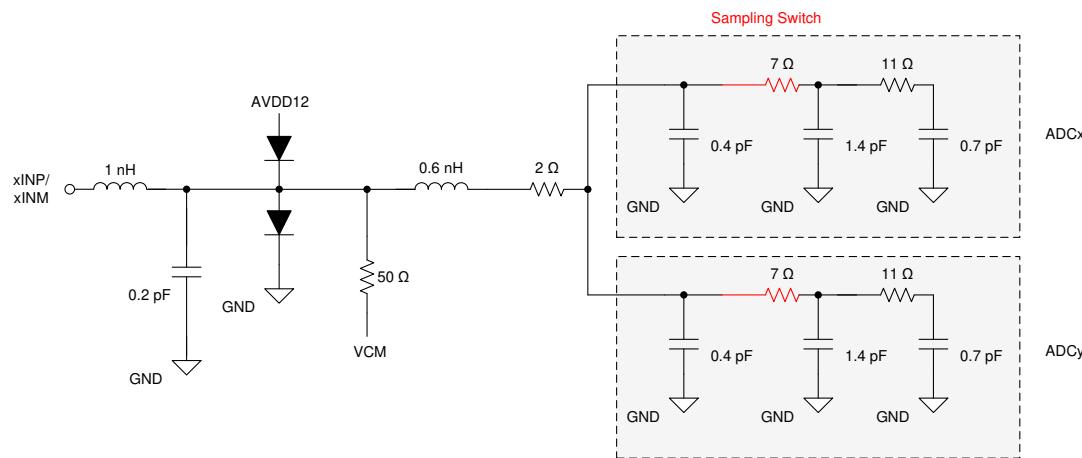


**Figure 7-1. Equivalent input schematic**

### 7.3.1.1 Input Bandwidth and Full-Scale

The input bandwidth (-3 dB) and input fullscale are dependent on what input termination and averaging mode are chosen as shown in the summary in Table 7-1. With averaging enabled the -3 dB bandwidth reduces to ~ 1.5 GHz and 100 Ω differential termination; the bandwidth can be increased by changing the input termination to 50 Ω differential.

**Table 7-1. Digital averaging vs full power input bandwidth (–3 dB)**

| # of ADCs averaged | Input Bandwidth (-3 dB) | Reset Switch | Selected differential input termination | Input Full-scale |
|---|---|---|---|---|
| 1 (Default) | 1.6 GHz | 1 | | + 1 dBm |
| 2 | 1.5 GHz | 1 | 100 Ω | + 1.8 dBm |
| 1 | 1.5 GHz | 0 | | + 0.5 dBm |
| 2 | 0.8 GHz | 0 | | |

There is an internal RESET switch which resets the sampling capacitor to VCM in between samples when enabled. The full power input bandwidth plots with input RESET switch disabled (RSW0) and enabled (RSW1) are shown in Figure 7-2.
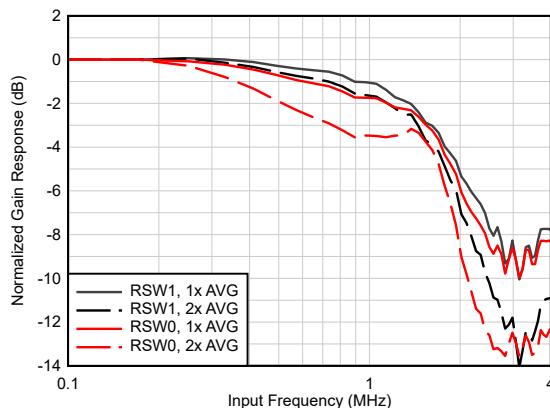


**Figure 7-2. Full power input bandwidth (100 Ω)**

The RESET switch is enabled by default and can be disabled with the following register writes:

**Table 7-2. Register Write Example for Configuring the RESET Switch**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x40 | Select ANALOG page |
| 0x6D | 0xC0 | Disable RESET Switch (to enable: 0x00) |
| 0x6E | 0x08 | Disable RESET Switch (to enable: 0x00) |

### 7.3.1.2 Input Imbalance

The AC performance is sensitive to amplitude and phase imbalance of the analog inputs, as shown in Figure 7-3 and Figure 7-4 for 1x and 2x internal averaging ($F_S$ = 1.5 GSPS, $F_{IN}$ = 0.9 GHz, $A_{IN}$ = -1 dBFS, dither = DIS).
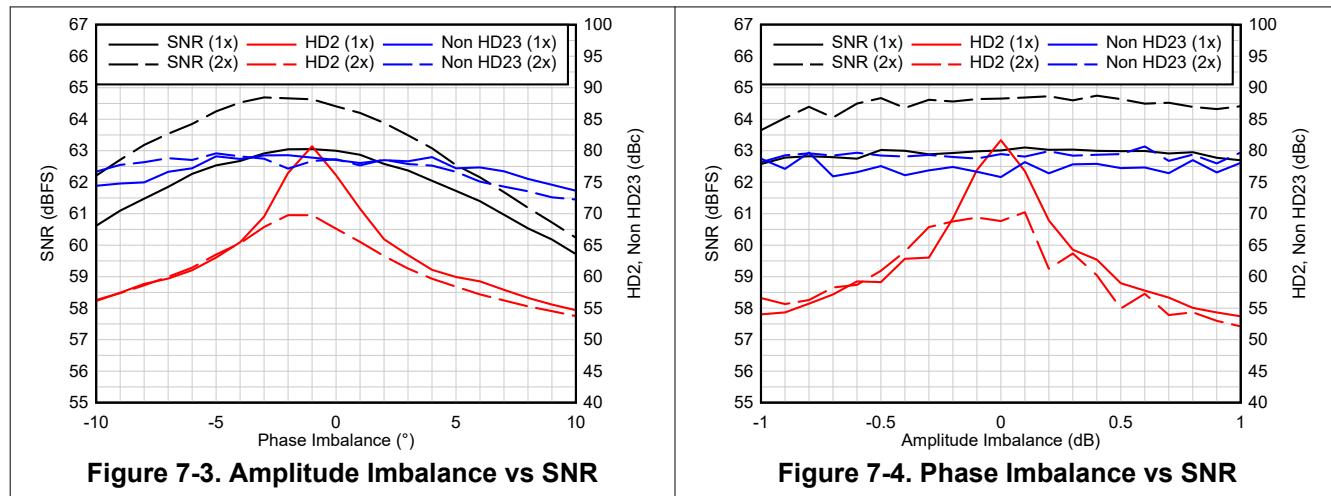


**Figure 7-3. Amplitude Imbalance vs SNR**



**Figure 7-4. Phase Imbalance vs SNR**

### 7.3.1.3 Overrange Indication

The ADC provides two options (configured using SPI) to indicate if input fullscale overrange occurred:
- Fast Overrange on GPIO1/2 pins: indication is available after ~ 6 clock cycles and the overrange indication flag stays high (sticky) until it is cleared via SPI register writes. Note: OVRA and OVRB are OR-ed together and OVRC and OVRD are OR-ed together and given on GPIO1/2.
- Overrange embedded in JESD stream: in this configuration the overrange indicator replaces the LSB of the output data of the corresponding channel. The indicator is output ahead of the data and is updated every clock cycle.

**Table 7-3. JESD OVR Latency**

| Decimation | # of Bands | OVR Latency (incl JESD, in sampling clock cycles) |
|---|---|---|
| DDC Bypass | - | 140-144 |
| 8 | Single (real and complex) | 44 |
| 8 | Dual | 33 |
| 16 | Single (real and complex) | 80 |
| 16 | Dual | 58 |
| 32 | Single (real and complex) | 152 |
| 32 | Dual | 108 |
| 64 | Single (real and complex) | 296 |
| 64 | Dual | 208 |
| 128 | Single (real and complex) | 584 |
| 128 | Dual | 408 |

The overrange output flag (GPIO or JESD) is the output of individual overrange flags of all ADCs per channel being used. For example, in non-averaged mode the overrange indication per channel is for a single ADC while in 2x average mode the overrange flag of all 2 ADCs are OR-ed together. Table 7-4 shows how to configure the OVR using SPI registers.

**Table 7-4. Programming example to configure the OVR to GPIO or JESD**

| ADDR | DATA | DESCRIPTION | ADDR | DATA | DESCRIPTION |
|---|---|---|---|---|---|
| OVR on GPIO1 and GPIO2, OVR sticky | | | OVR on JESD | | |
| 0x05 | 0x02 | Select DIGITAL page | 0x05 | 0x02 | Select DIGITAL page |
| 0x238 | 0xF0 | | 0x2E | D0 | Set D0 = 1 to enable OVR on JESD |
| 0x383 | 0x02 | | 0x05 | 0x00 | |
| Clear OVR | | | These extra writes are only needed using decimation | | |
| 0x05 | 0x40 | Select ANALOG page | 0x05 | 0x18 | Select DDCAB/ DDCCD page |
| 0x74 | 0x04 | Clear OVR flag chA | 0x20 | 0x06 | Enable OVR on JESD |
| 0x74 | 0x00 | Clear OVR flag chA | | | |
| 0x84 | 0x04 | Clear OVR flag chB | | | |
| 0x84 | 0x00 | Clear OVR flag chB | | | |
| Change OVR from sticky to non sticky (self clear) | | | | | |
| 0x05 | 0x40 | Select ANALOG page | | | |
| 0x31 | 0x06 | Set OVR to non-sticky | | | |

### 7.3.1.4 Analog out-of-band dither

The ADC34RF52 provides optional (enabled via SPI writes) analog out-of-band, large amplitude dither. It has a bandwidth of ~ 20 MHz located at DC and an adjustable amplitude with a maximum dither power of approximately ~ -20 dBFS (PAR ~ 9 dB). The dither is completely rolled-off into the noise floor within ~ 100 MHz as illustrated in Figure 7-5. Since the dither is large, the amplitude is recommended for the signal input not to exceed -2.5 dBFS to avoid input saturation. The dither signal also couples to the input signal and, depending on input frequency, can degrade the close in phase noise for offsets > 1 MHz.
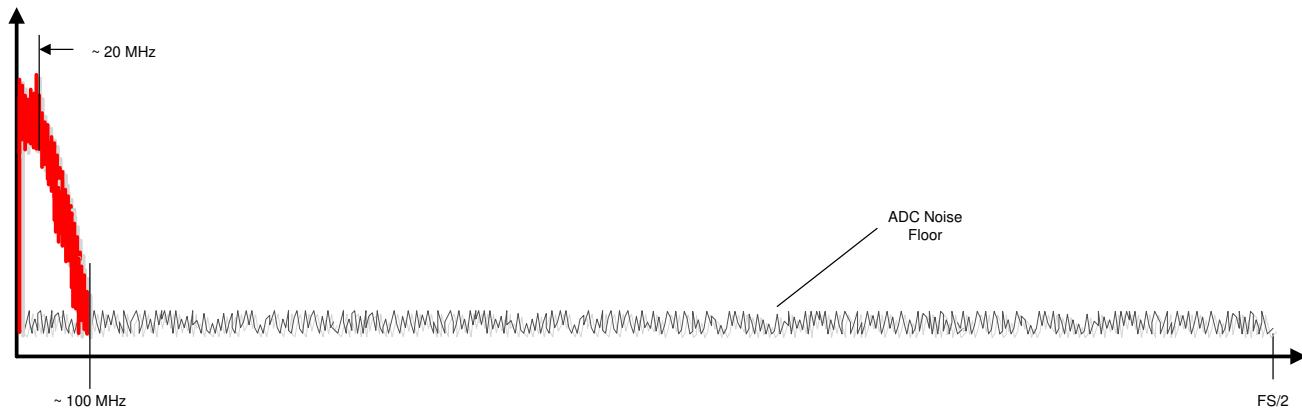


**Figure 7-5. Analog out-of-band dither**

In the frequency domain, the dither signal shows up in individual tones as shown in Figure 7-6. The dither update frequency can be adjusted with the dither divider setting. The dither update frequency is: $F_S$ / 4 / 2047 / 'Dither Divider'. In the frequency spectrum, there is a 2 larger dither spurs at $F_{IN}$ +/- $F_S$ / 4 / 'Dither Divider'.

By default, the divider is set to 50, which translates to a dither spur spacing of ~ 7 kHz. A divider setting of 32 translates to a dither spacing of ~ 11 kHz as shown in Figure 7-7. The lower the divider setting, the higher the dither tone frequency. Figure 7-7 also shows that the dither energy reduces as the offset frequency increases. Less dither energy reduces the higher harmonic spur improvement.
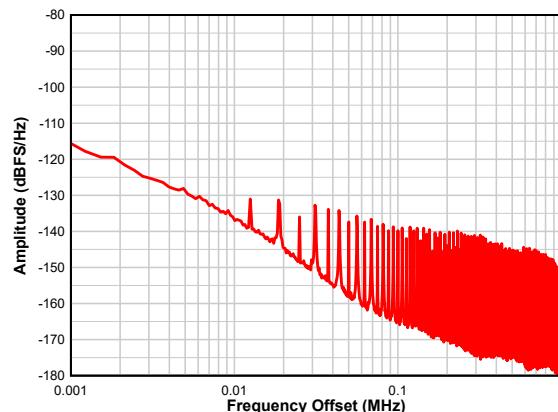


**Figure 7-6. Dither Close-Up**
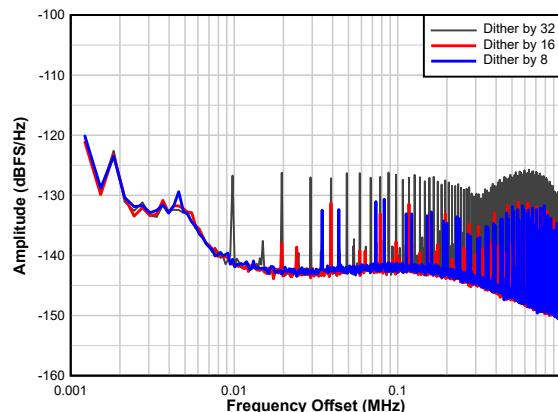


**Figure 7-7. Dither vs Dither Divider Setting**

Product Folder Links: *ADC34RF52*

The analog dither must be enabled in multiple locations. The different dither amplitudes must be used based on the internal averaging as shown in Table 7-5.

**Table 7-5. Recommended dither amplitude settings**

| Mode | Amplitude | Dither Amp1 | Dither Amp2 |
|---|---|---|---|
| 1x AVG | ±1024 codes | 0 | 0 |
| 1x AVG | ±768 codes | 0 | -4 |
| 2x AVG | ±1024 codes | 3 | 0 |
| 2x AVG | ±768 codes | 0 | 0 |

The internal analog dither can be enabled via the following register writes. After enabling the dither (or changing the dither amplitude) another calibration needs to be performed. See Table 7-6.

**Table 7-6. Register write example for configuring the internal dither**

| ADDR | DATA | DESCRIPTION | ADDR | DATA | DESCRIPTION |
|---|---|---|---|---|---|
| 0x05 | 0x40 | Select ANALOG page | 0xB1 | 0x00 | Sets dither divider. 0x00 = /50 |
| 0xA8 | 0x00 | DITHER AMP1: 3 = 0x80, 0 = 0x00 | 0xB2 | 0x00 | |
| 0xCD | 0x00 | DITHER AMP2: -4 = 0x40, 0 = 0x00 | 0xAF | 0x18 | |
| 0x04 | 0x01 | | 0xAF | 0x10 | 0x10 = dither ENABLED, 0x90 = dither DISABLED |
| 0x20 | 0x04 | | 0x04 | 0x01 | |
| 0x91 | 0x40 | | 0x20 | 0x00 | |
| 0xAF | 0x10 | | 0x04 | 0x00 | |

Product Folder Links: ADC34RF52

### 7.3.2 Sampling Clock Input

The internal sampling clock path was designed for lowest residual phase noise contribution. The sampling clock circuitry requires a dedicated low noise power supply for best performance. The internal residual clock phase noise is also sensitive to clock amplitude and for best performance the clock amplitude should be larger than 1 $V_{PP}$.

**Table 7-7. Internal Aperture Clock Phase Noise**
**($F_S$ = 1.5 Gsps, $V_{IN}$ = 1 $V_{PP}$)**

| Frequency Offset (MHz) | Amplitude (dBc/Hz) |
|---|---|
| 0.001 | -123 |
| 0.01 | -133 |
| 0.1 | -143 |
| 1 | -152 |
| 10 | -157 |
| 250 | -160 |

The clock input and ADC sampling circuitry also have an amplitude noise component which modulates on to the sampled input signal. Unlike phase noise, the amplitude noise does not scale with input frequency as shown in Figure 7-8. This noise component can dominate the close in noise performance at lower input frequencies.
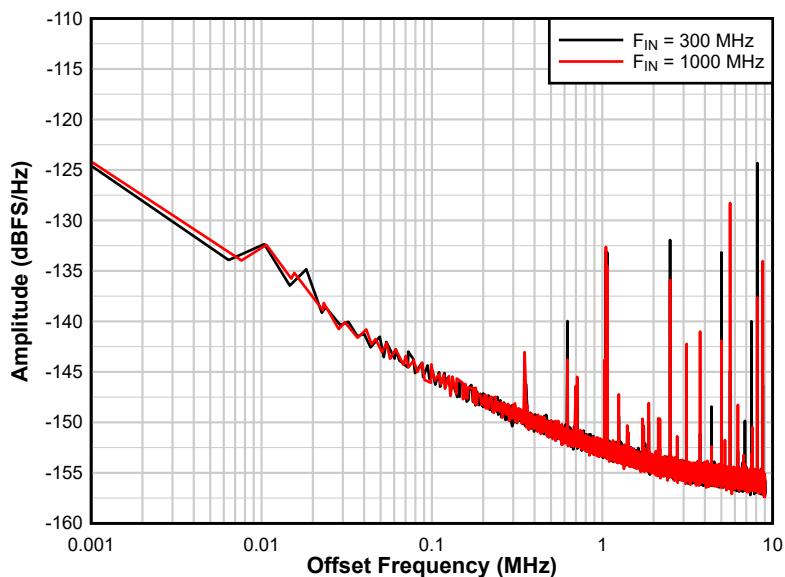


**Figure 7-8. Amplitude Noise**

Product Folder Links: *ADC34RF52*

The internal aperture jitter is also dependent on the amplitude of the external clock input signal. Figure 7-9 and Figure 7-10 show the expected SNR performance with dither on/off across clock amplitude.
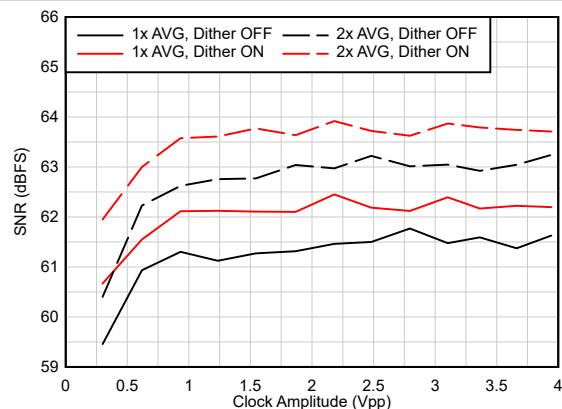


**Figure 7-9. SNR vs Clock Amplitude (F$_{IN}$ = 900 MHz)**
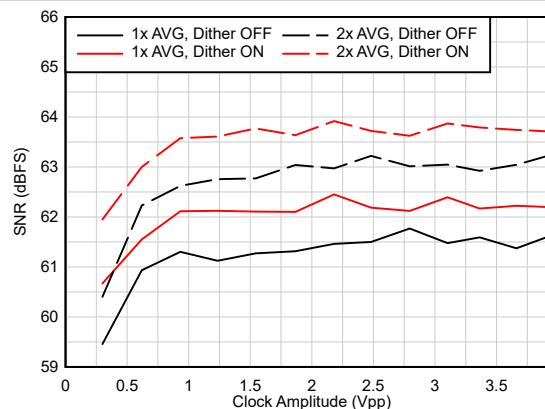


**Figure 7-10. SNR vs Clock Amplitude (F$_{IN}$ = 1800 MHz)**

The sampling clock input is internally terminated to 100 Ω differentially and provides a return loss better than 10 dB (see Figure 7-11). The clock input consists of a single clock input buffer followed by a dedicated clock buffer for ADCA/B as well as ADCC/D. When averaging two ADCs internally, there is some decrease in clock buffer noise which is correlated and does not improve with averaging.
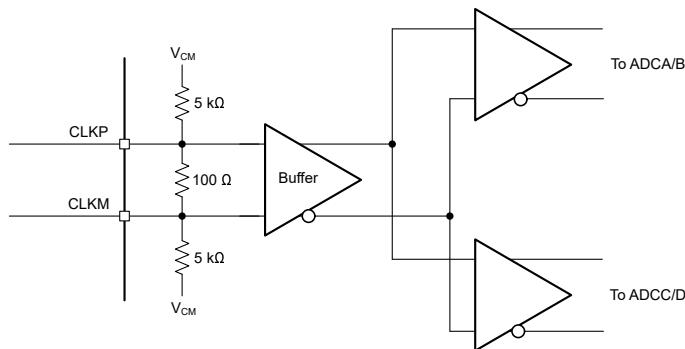


**Figure 7-11. Clock Input Internal Circuitry**

### 7.3.3 SYSREF

The SYSREF input signal is used to reset internal digital blocks and align them to the internal multi-frame clock to achieve deterministic latency subclass 1. The SYSREF input signal can be AC or DC coupled (selected via SPI register option) as shown in Figure 7-12. The ADC34RF52 has internal 100-Ω termination for DC coupling and internal biasing when using AC coupling.

A register mask can be used to only give SYSREF to the NCO (see NCO section) in the decimation filter block. Leave all other blocks such as JESD interface unaffected.

When giving a periodic SYSREF signal, the frequency must be a sub-harmonic of the internal local multi-frame clock (LMFC). The LMFC frequency is determined by the selected decimation: frames per multi-frame setting (K), samples per frame (S), and the device sampling frequency (FS).

**Table 7-8. LMFC and SYSREF settings for different operating modes**

| Operating Mode | LMFS Mode | LMFC Clock Frequency | SYSREF Frequency |
|---|---|---|---|
| DDC Bypass Mode | 84810 | FS / (20 x K) | FS / (N x 20 x K) |
| | 8422 | FS / (4 x K) | FS / (N x 4 x K) |
| Decimation | Various | FS / (D x S x K) | FS / (N x D x S x K) |

Where N is an integer value (1, 2, 3...).

After enabling SYSREF input, the internal SYSREF input ignores any incoming SYSREF pulse after the first 16 pulses.
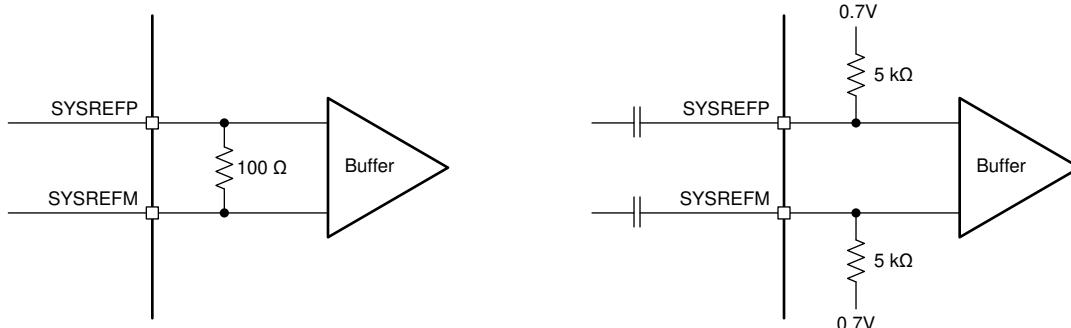


**Figure 7-12. SYSREF Input Circuitry and Edge Alignment**

The internal synchronization using the external SYSREF signal can be enabled with the following register writes.

**Table 7-9. Register Write Example for Enabling SYSREF Synchronization**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x02 | Select DIGITAL page |
| 0x236 | 0x02 | Enable internal SYSREF input and clear SYSREF pulse counter |
| 0x236 | 0x03 | Starts internal SYSREF counter |

AC coupling with internal biasing of the SYSREF input can be enabled with the following SPI register writes.

**Table 7-10. Register Write Example for Enabling SYSREF AC Coupling**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x40 | Select ANALOG page |
| 0xB4 | 0x01 | Enable external AC coupling with internal biasing on SYSREF |

### 7.3.3.1 SYSREF Capture Detection

The SYSREF input signal rising edge should be edge aligned with the rising edge of the sampling clock to maximize the setup and hold times. The ADC34RF52 includes an internal SYSREF monitoring circuitry to detect possible metastability resulting in a clock cycle slip, and thus, misalignment across devices.

The sampling clock gets delayed by ~ 160 ps and then captures the SYSREF signal. The SYSREF monitoring circuitry captures the SYSREF signal ±50 ps (-50, -25, +16, +32, +48 ps) around the main SYSREF capture. Ideally no SYSREF transition happens within the 100 ps SYSREF capture window and all XOR flags show "0". If a SYSREF/clock misalignment happens and the SYSREF transition falls within the SYSREF monitoring window, then one of the XOR flags (which monitor adjacent SYSREF captures within the window) will show a "1" and the SYSREF can be adjusted externally.

The SYSREF monitor registers are not 'sticky' registers and they are updated at every rising edge of SYSREF.
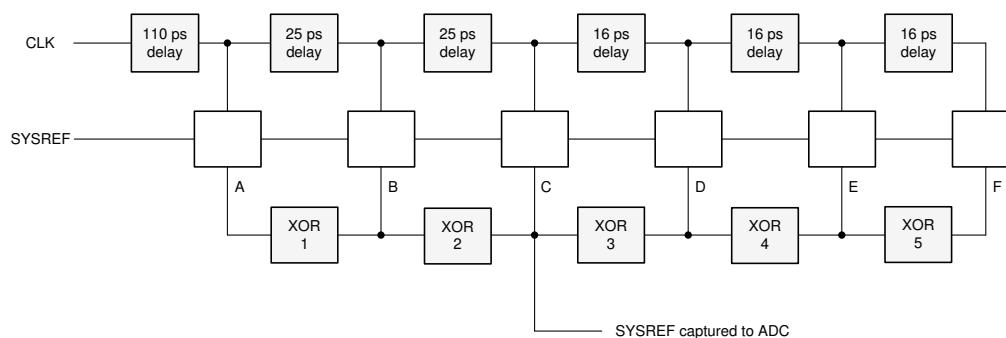


**Figure 7-13. SYSREF Detection Circuitry**

The example in Figure 7-14 shows a misaligned SYSREF signal where the SYSREF signal arrives much later than the sampling clock rising edge. The SYSREF window feature checks if the SYSREF transition is within ±50 ps of the instant when the SYSREF signal gets captured by the sampling clock.

In this example, the delayed SYSREF signal transitions between the "B" and "C" flip flop which raises the XOR2 flag. The XOR flags is reported in register 0x22F in the digital page. Register 0x22F in this example would read back 0x8B, as shown in Table 7-11.
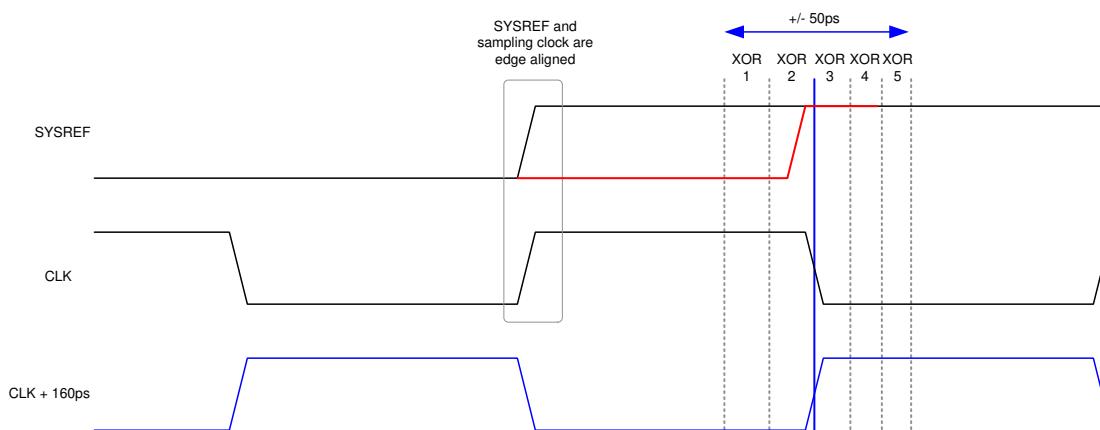


**Figure 7-14. Detection of SYSREF Transition within Capture Window**

**Table 7-11. SYSREF Window Register Example (0x22F)**

| ADDR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----|----|----|----|----|
| 0x22F | 1 | SYSREF X5 | SYSREF X4 | SYSREF X3 | SYSREF X2 | SYSREF X1 | SYSREF OR | 1 |
| | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 |

### 7.3.4 ADC Foreground Calibration

The internal ADC architecture is sensitive to temperature changes. The ADC34RF52 contains two additional internal ADC cores (one for channel A/B and one for channel C/D) which are used whenever one of the ADCs is in calibration. ADCs are calibrated as pairs where one ADC at a time is connected to the internal calibration DAC. The calibration is configured via SPI register writes and can be executed using SPI register writes or using the GPIO1 pin. When executed the calibration takes ~ 27 ms/ADC pair (~13.5 ms/ADC). The example in Figure 7-15 shows 2x internal averaging where 4 ADC cores (#1,2,3,4 for chA/B and #6,7,8,9 for chC/D) are used in operation and ADCs #5 and #10 for calibration.
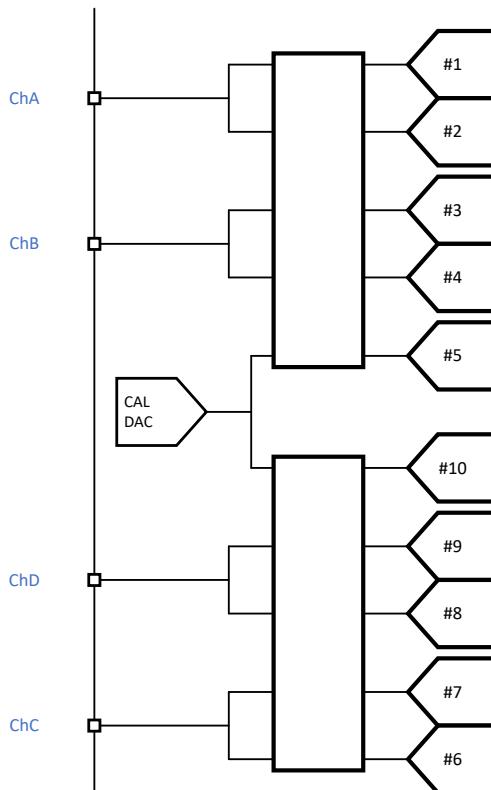


**Figure 7-15. Internal ADC setup for 2x averaging mode**

### 7.3.4.1 Calibration Control

Figure 7-16 shows a timing diagram of the calibration control using GPIO1 pin.

When GPIO1 transitions to LOW logic state:
- an ADC pair gets swapped out within approximately 120 ns
- a new calibration gets triggered immediately

If GPIO1 is being held low when the calibration of an ADC pair is completed, the next ADC pair is switched and a new calibration is triggered. The order in which ADC pair gets calibrated can be configured via SPI to serial or random.

When using 2x averaging for example, the calibration must be executed for 5 ADC pairs to make sure all ADCs in use have been calibrated recently.
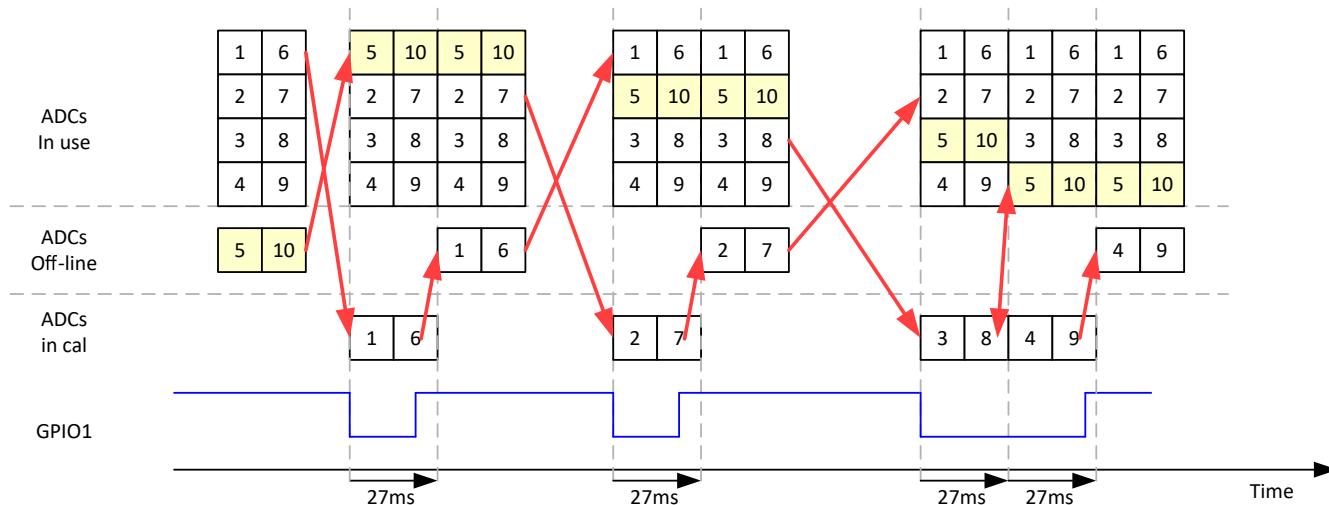


**Figure 7-16. Timing diagram - calibration (2x AVG example)**

Figure 7-17 shows the ADC switch happens approximately 120 ns after the logic level change on GPIO1 is detected.
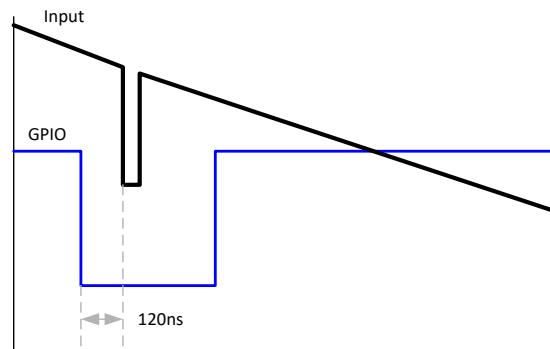


**Figure 7-17. Timing diagram shows the ADC switch**

### 7.3.4.2 ADC Switch

During the ADC transition, the amplitude may drop less 1% for 1-2 samples as shown in Figure 7-18. The gain variation from one ADC to the next is ~ < 0.05 dB while the phase change is less 0.01 deg as shown in Figure 7-19.
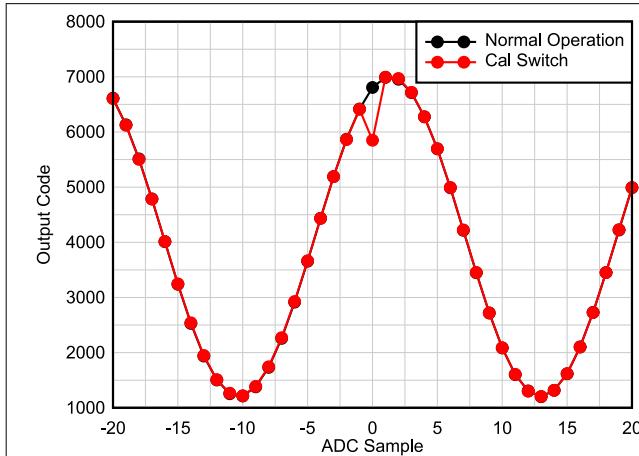


**Figure 7-18. Output Code vs ADC Sample**
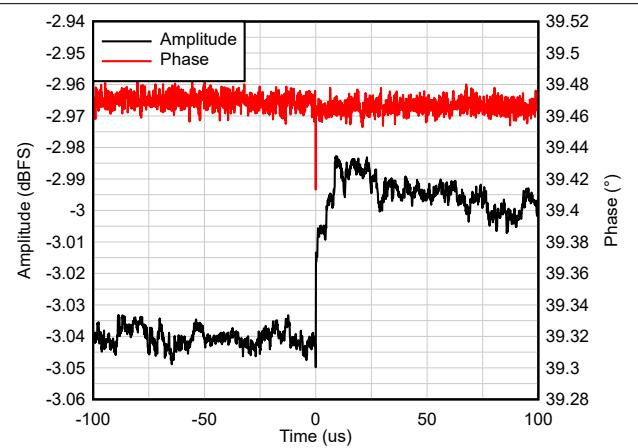


**Figure 7-19. Amplitude and Phase vs Time**

### 7.3.4.3 Calibration Configuration

The ADC34RF52 provides 3 different options to configure the internal foreground calibration:

- Continous calibration - see Table 7-12
- Calibrate all ADCs one time using SPI trigger - see Table 7-13
- Calibrate 2 ADC pairs at a time using GPIO trigger - see Table 7-14

The status of the calibration can be read back from register 0x298 (CALIBRATION page). Successful calibration reads back 0x0E.

**Table 7-12. Register writes to trigger CONTINOUS calibration of all ADCs using SPI**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x20 | Select CALIBRATION page |
| 0x46 | 0x03 | |

**Table 7-13. Register writes to trigger SINGLE calibration of all ADCs using SPI**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x20 | Select CALIBRATION page |
| 0x48 | 0x15 | |
| 0x45 | 0x8A | Toggle calibration start |
| 0x45 | 0x0A | |
| | | wait 2 s |

**Table 7-14. Register writes to trigger ADC pair calibration using the GPIO pin**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x20 | Select CALIBRATION page |
| 0x46 | 0x02 | |
| 0x45 | 0x4A | |
| 0x05 | 0x02 | Select DIGITAL page |
| 0x234 | 0x04 | Use GPIO1 pin to freeze calibration switch |

### 7.3.5 Decimation Filter

The ADC34RF52 provides up to two digital down converters per ADC channel (see Figure 7-20). The decimation filters provide a flexible option to cover a wide range of instantaneous bandwidths (IBW) as shown in Table 7-15. Single band decimation supports a wide bandwidth up to complex decimation by 4x. In dual band decimation mode the widest bandwidth supported is complex decimation by 8.
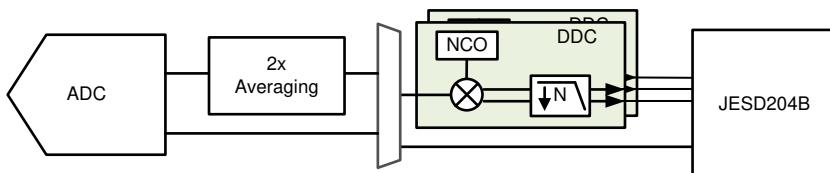


**Figure 7-20. Digital Decimation Filter Options**

**Table 7-15. Summary of Different Decimation Filter Band Options**

| # of DDCs | Minimum Complex Decimation | Maximum Complex Decimation |
|---|---|---|
| 1 | 4 | 128 |
| 2 | 8 | 128 |

The decimation filter can be configured to two different operating modes:

- Complex Decimation: This mode provides complex output with ~ 80% passband bandwidth using a 48-bit phase coherent NCO.
  During the complex mixing operation the digital output is reduced by 6-dB. This reduces the fullscale from 0-dBFS to -6-dBFS. This 6-dB change applies to signals and noise and thus no dynamic range is lost.
- Real Decimation: In real decimation mode the complex mixer is bypassed (NCO should be set to 0 for lowest power consumption) and the digital filter acts as a low pass filter. There is no frequency shifting and the output passband bandwidth is ~ 40%.

Since the JESD204B interface is common across all ADC channels, the decimation ratio as well as the # of DDCs/ADC has to be the same across all ADC channels.

By default, the output of values of the decimation filter are rounded to 16-bit resolution. To avoid quantization noise limitation when using high order of decimation (that is, /64 or /128), a special 32-bit output mode can be enabled (see 32-bit mode).

Table 7-16 provides an overview of the available complex decimation settings and resulting complex and real output bandwidths.

**Table 7-16. Decimation Setting vs Output Bandwidth**

| Decimation Factor N (complex) | Complex Output Bandwidth per DDC | $F_S$ = 1.5 Gsps | | Real Output Bandwidth per DDC | $F_S$ = 1.5 Gsps | |
|---|---|---|---|---|---|---|
| | | Complex Output Rate per DDC | Complex Output Bandwidth per DDC | | Real Output Rate per DDC | Real Output Bandwidth per DDC |
| 4 | $0.8 \times F_S / 4$ | 375 Msps | 300 MHz | $0.4 \times F_S / 4$ | 375 Msps | 150 MHz |
| 8 | $0.8 \times F_S / 8$ | 187.5 Msps | 150 MHz | $0.4 \times F_S / 8$ | 187.5 Msps | 75 MHz |
| 16 | $0.8 \times F_S / 16$ | 93.75 Msps | 75 MHz | $0.4 \times F_S / 16$ | 93.75 Msps | 37.5 MHz |
| 32 | $0.8 \times F_S / 32$ | 46.875 Msps | 37.5 MHz | $0.4 \times F_S / 32$ | 46.875 Msps | 18.75 MHz |
| 64 | $0.8 \times F_S / 64$ | 23.4375 Msps | 18.75 MHz | $0.4 \times F_S / 64$ | 23.4375 Msps | 9.375 MHz |
| 128 | $0.8 \times F_S / 128$ | 11.71875 Msps | 9.375 MHz | $0.4 \times F_S / 128$ | 11.71875 Msps | 4.6875 MHz |

### 7.3.5.1 Decimation Filter Response

This section provides the different decimation filter responses with a normalized ADC sampling rate. The complex filter pass band is ~ 80% (-1 dB) with a minimum of 85 dB stop band rejection.
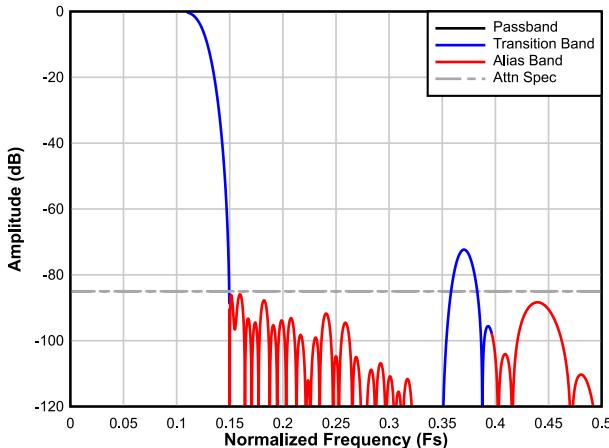


**Figure 7-21. Complex Decimation by 4 Filter Response**
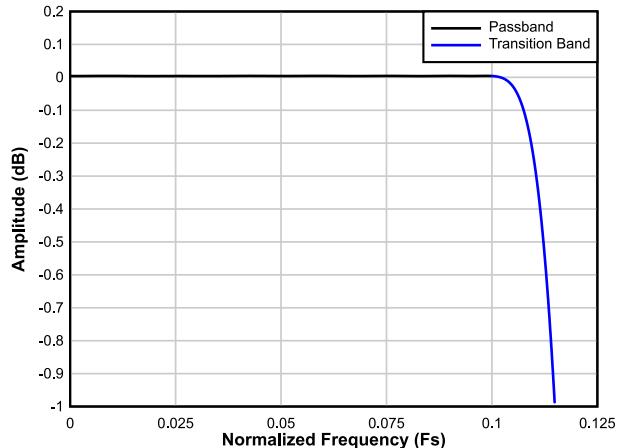


**Figure 7-22. Decimation by 4 Passband Ripple Response**
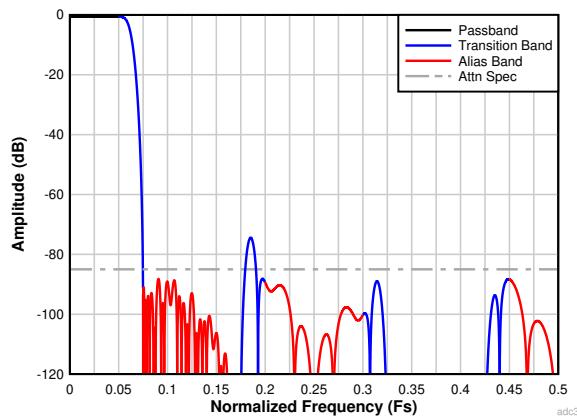


**Figure 7-23. Complex Decimation by 8 Filter Response**
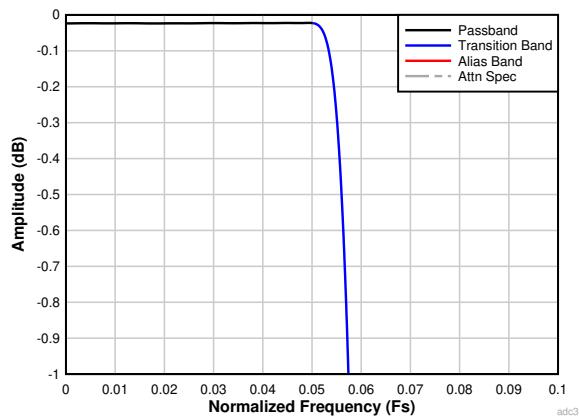


**Figure 7-24. Decimation by 8 Passband Ripple Response**
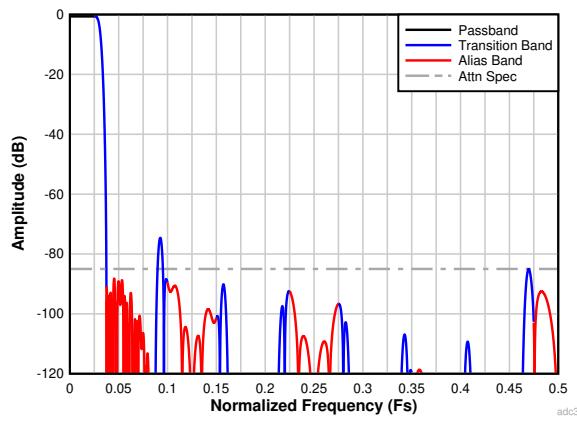


**Figure 7-25. Complex Decimation by 16 Filter Response**
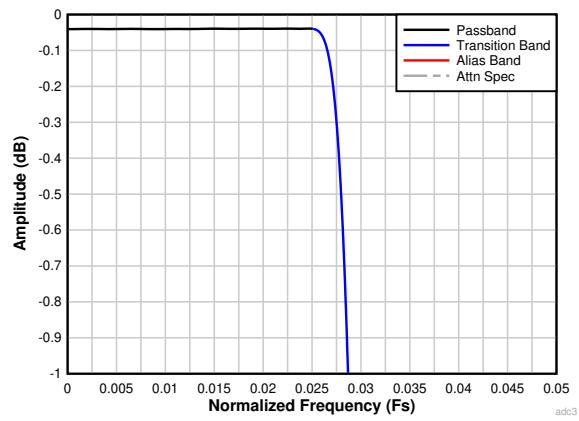


**Figure 7-26. Decimation by 16 Passband Ripple Response**

Product Folder Links: *ADC34RF52*
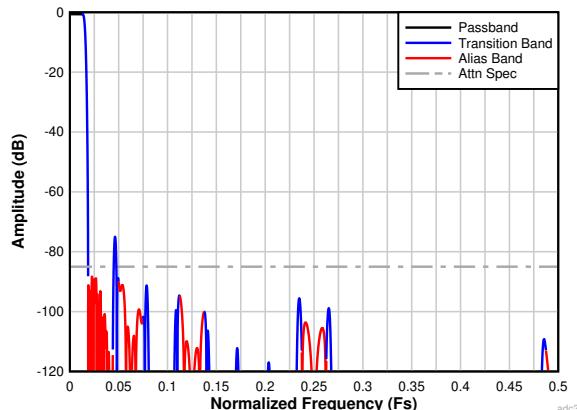
Figure 7-27. Complex Decimation by 32 Filter Response
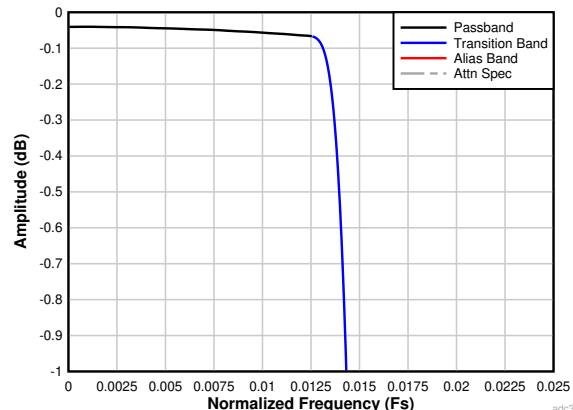


Figure 7-28. Decimation by 32 Passband Ripple Response
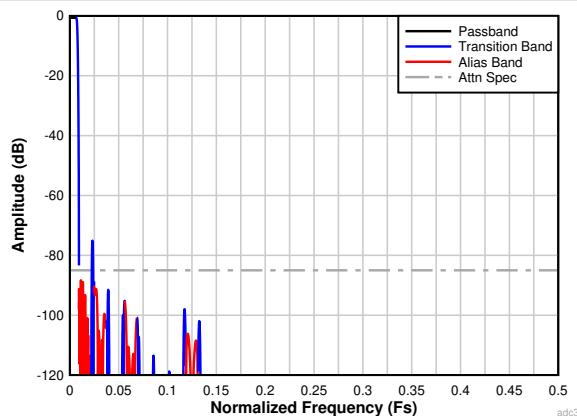


Figure 7-29. Complex Decimation by 64 Filter Response
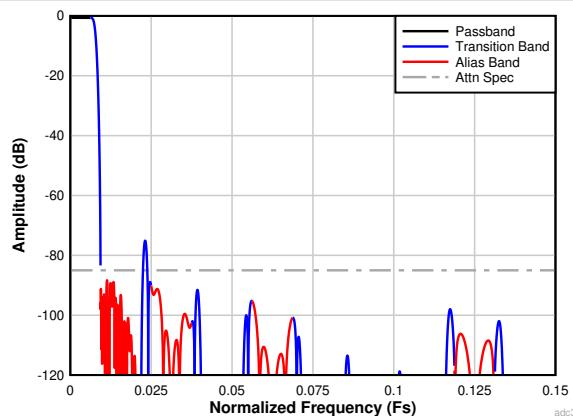


Figure 7-30. Complex Decimation by 64 Filter Response
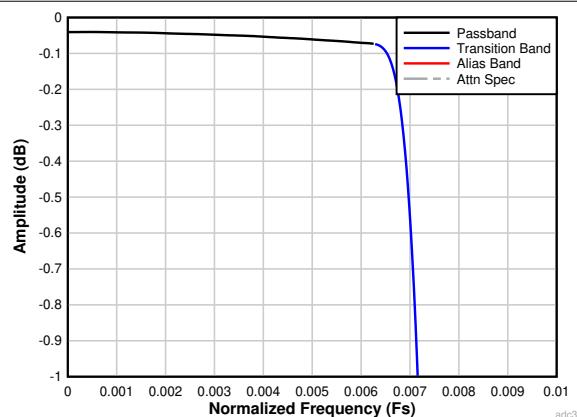


Figure 7-31. Decimation by 64 Passband Ripple Response
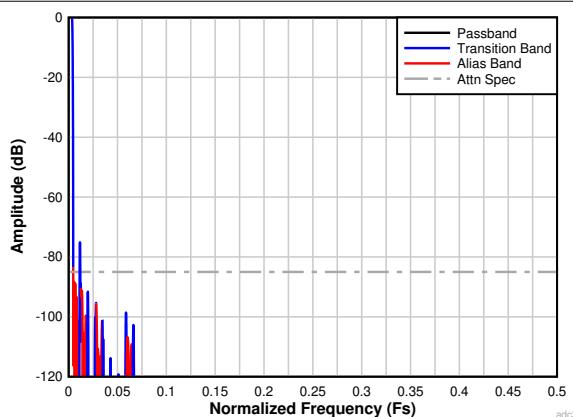


Figure 7-32. Complex Decimation by 128 Filter Response

Product Folder Links: ADC34RF52
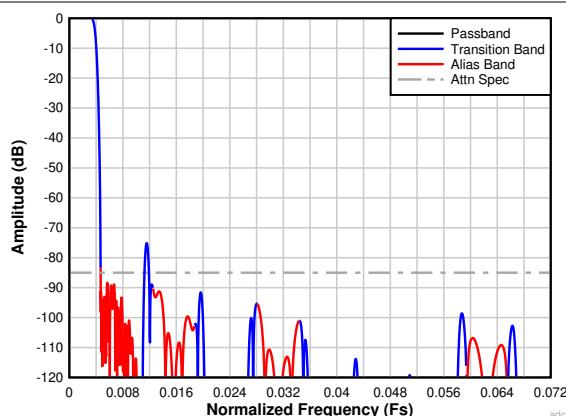
**Figure 7-33. Complex Decimation by 128 Filter Response**
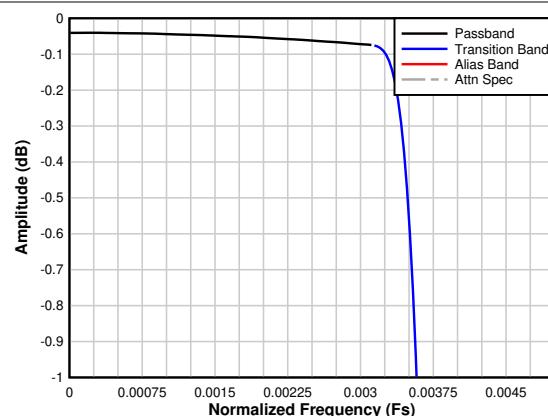


**Figure 7-34. Decimation by 128 Passband Ripple Response**

### 7.3.5.2 Decimation Filter Configuration

The decimation filter is configured with these register writes.

**Table 7-17. Register writes to enable the internal decimation filter**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x02 | Select DIGITAL page |
| 0x2C | | Select single/dual band |
| 0x2D | | Select decimation |
| 0x05 | 0x04 | Select JESD page |
| 0x22 | | Select LMFS mode |
| 0x24 | | Select DDC CLK setting |
| 0x25 | | Select JESD TX CLK DIV setting |
| 0x9F | | Select JESD PLL1/2 settings |
| 0xA0 | | Select JESD PLL INPUT1 setting |
| 0xA1 | | Select JESD PLL INPUT2 settings |

### 7.3.5.3 20-bit Output Mode

The device includes a 20-bit output resolution mode which can be used for high order decimation (such as: 64x, 128x) to avoid SNR degradation due to quantization noise limitation. In this mode, no additional JESD204B output lanes are added but the output data is transmitted at 2x the output rate and two consecutive 16-bit samples are filled with one 20-bit sample. So for example, a single band complex decimation would go from LMFS = 4841 (16-bit output mode) to LMFS = 4881 (20-bit output mode) as illustrated in Table 7-18.

**Table 7-18. JESD Frame Assembly Comparison between 16-bit and 20-bit Output Mode**

| LMFS = 4841 | | | | | LMFS = 4881 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| $xI_0[15:8]$ | $xI_0[7:0]$ | $xQ_0[15:8]$ | $xQ_0[7:0]$ | | $xI_0[31:24]$ | $xI_0[23:16]$ | $xI_0[15:8]$ | $xI_0[7:0]$ | $xQ_0[31:24]$ | $xQ_0[23:16]$ | $xQ_0[15:8]$ | $xQ_0[7:0]$ |
| | | | | | 20-bit sample I | | 0000 00000000 | | 20-bit sample Q | | 0000 00000000 | |

The 20-bit output mode is enabled by setting D7 in 0x2C (DIGITAL page) and selecting viable decimation and LMFS mode.

Product Folder Links: *ADC34RF52*

### 7.3.5.4 Numerically Controlled Oscillator (NCO)

Each digital down-converter (DDC) uses a 48-bit numerically controlled oscillator (NCO) to fine tune the frequency placement prior to the digital filtering. Different NCO frequencies for each DDC are programmed using SPI register writes and the desired NCO frequency can be selected using SPI or the GPIO pins. When using the GPIO pins for NCO frequency control, frequency hopping can be achieved in less than 1 µs. The digital NCO is designed to have a SFDR of at least 100 dB. The number of available, programmable NCO frequencies depends on # of DDC bands used as illustrated in Table 7-19.
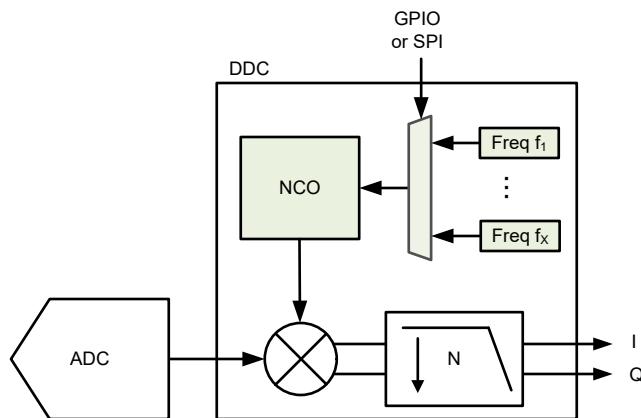


**Figure 7-35. NCO Block Diagram**

**Table 7-19. Available # of Frequencies per NCO depending on # of DDCs used**

| # of DDCs used | # of Frequencies per NCO |
|---|---|
| 1 | 4 |
| 2 | 4 |

There are two different NCO operating modes available - phase continuous and infinite phase coherent.

**Phase Continuous NCO**: During a NCO frequency change, the NCO phase gradually adjusts to the new frequency as shown in Figure 7-36. The 'dashed' line shows the phase of original $f_1$ frequency.

**Infinite Phase Coherent NCO**: With a phase coherent NCO, all frequencies are synchronized to a single event using SYSREF. This enables an infinite amount of frequency hops without the need to reset the NCO as phase coherency is maintained between frequency hops. This is illustrated in Figure 7-36 (right). When returning to the original frequency $f_1$, the NCO phase appears as if the NCO have never changed frequencies.
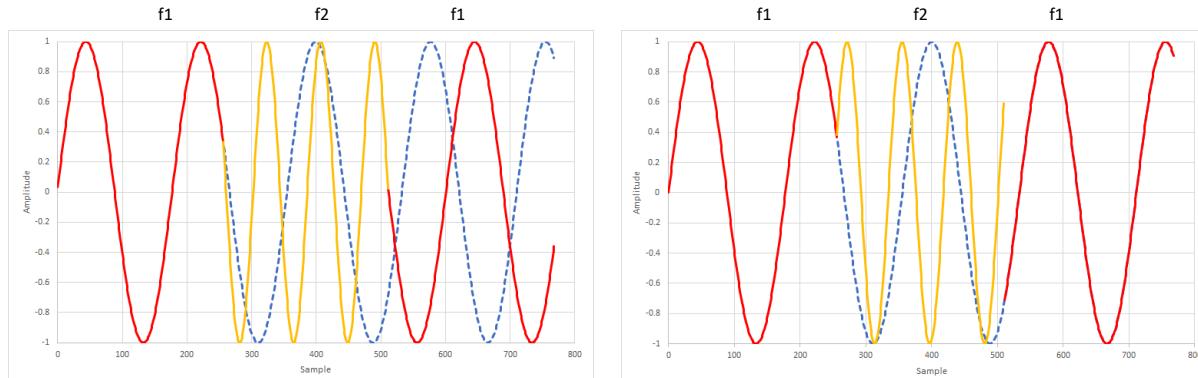


**Figure 7-36. Phase Continuous (left) and Infinite Phase Coherent (right) NCO Frequency Switching**

The oscillator generates a complex exponential sequence of:

$$e^{j\omega n} \text{ (default) or } e^{-j\omega n} \tag{1}$$

where: frequency ($\omega$) is specified as a signed number by the 48-bit register setting

The complex exponential sequence is multiplied with the real input from the ADC to mix the desired carrier to a frequency equal to $f_{IN} + f_{NCO}$. The NCO frequency can be tuned from $-F_S/2$ to $+F_S/2$ and is processed as a signed, 2s complement number.

The NCO frequency setting is set by the 48-bit register value given and calculated as:

$$\text{NCO frequency (0 to } + F_S/2\text{): NCO} = f_{NCO} \times 2^{48} / F_S \tag{2}$$

$$\text{NCO frequency (-}F_S/2 \text{ to 0): NCO} = (f_{NCO} + F_S) \times 2^{48} / F_S \tag{3}$$

where:
- NCO = NCO register setting (decimal value)
- $f_{NCO}$ = Desired NCO frequency (MHz)
- $F_S$ = ADC sampling rate (MSPS)

The NCO programming is illustrated with this example:
- ADC sampling rate $F_S$ = 1300 MSPS
- Desired NCO frequency = 460 MHz

$$\text{NCO frequency setting} = f_{NCO} \times 2^{48} / F_S = 460 \text{ MHz x } 2^{48} / 1300 \text{ MSPS} = 99,598,837,913,001 \tag{4}$$

Table 7-20 shows the register writes to set frequency 1 of NCO1 of DDCA to that frequency:

**Table 7-20. Example register writes to change NCO frequency**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x08 | Select DDCA page |
| 0x105 | 0x5A | Frequency = 460 MHz with $F_S$ = 1.3 GSPS 99,598,837,913,001 = 0x5A95A95A95A9 where the MSB goes to address 0x105 and the LSB to 0x100. |
| 0x104 | 0x95 | |
| 0x103 | 0xA9 | |
| 0x102 | 0x5A | |
| 0x101 | 0x95 | |
| 0x100 | 0xA9 | |
| 0x181 | 0x00 | Load and update NCO1 with the new frequency. |
| 0x181 | 0x30 | |

### 7.3.5.5 NCO Frequency programming using the SPI interface

There are 2 separate NCOs per channel - one for each band (that is, NCO1 = band 1) and 4 different frequencies can be programmed per NCO as shown in Figure 7-37. The NCO frequencies are located in the DDCAB/CD pages (0x05 0x08 for channel A/B and 0x05 0x10 for channel C/D) in registers 0x100 to 0x17D. Depending on # of bands used, the frequencies for each NCO are selected in registers 0x3B and 0x41 (DIGITAL page) as shown in Table 7-21. If the NCO frequencies are the same for channel A/B and channel C/D, the frequencies can be written to both DDCAB and DDCCD pages simultaneously by selecting both pages (0x05 0x18).

| | Channel A | Channel B | Channel C | Channel D |
|---|---|---|---|---|
| **NCO1** | 1: 0x100..0x105<br>2: 0x108..0x10D<br>3: 0x110..0x115<br>4: 0x118..0x11D | 1: 0x140..0x145<br>2: 0x148..0x14D<br>3: 0x150..0x155<br>4: 0x158..0x15D | 1: 0x100..0x105<br>2: 0x108..0x10D<br>3: 0x110..0x115<br>4: 0x118..0x11D | 1: 0x140..0x145<br>2: 0x148..0x14D<br>3: 0x150..0x155<br>4: 0x158..0x15D |
| **NCO2** | 1: 0x120..0x125<br>2: 0x128..0x12D<br>3: 0x130..0x135<br>4: 0x138..0x13D | 1: 0x160..0x165<br>2: 0x168..0x16D<br>3: 0x170..0x175<br>4: 0x178..0x17D | 1: 0x120..0x125<br>2: 0x128..0x12D<br>3: 0x130..0x135<br>4: 0x138..0x13D | 1: 0x160..0x165<br>2: 0x168..0x16D<br>3: 0x170..0x175<br>4: 0x178..0x17D |

**Figure 7-37. Multi-Band NCO**

Single band DDC uses the frequencies of both NCO1 and NCO2 for a combined 8 different frequencies for NCO1 using 3 bit control (NCO2 CHx [1] and NCO1 CHx [1:0]). The NCO2 selection bit (D3) decides if frequencies from NCO1 or NCO2 are being used. In dual and quad band DDC operating mode, there are 4 frequencies per NCO available and selected using 2 register bits (NCOx CHx [1:0]).

.
**Table 7-21. NCO Frequency Selection SPI Interface Registers**

| # OF BANDS | ADDR | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|
| SINGLE | 0x3B | NCO2 CHB [1] | 0 | NCO1 CHB [1:0] | | NCO2 CHA [1] | 0 | NCO1 CHA [1:0] | |
| | 0x41 | NCO2 CHD [1] | 0 | NCO1 CHD [1:0] | | NCO2 CHC [1] | 0 | NCO1 CHC [1:0] | |
| DUAL | 0x3B | NCO2 CHB [1:0] | | NCO1 CHB [1:0] | | NCO2 CHA [1:0] | | NCO1 CHA [1:0] | |
| | 0x41 | NCO2 CHD [1:0] | | NCO1 CHD [1:0] | | NCO2 CHC [1:0] | | NCO1 CHC [1:0] | |

To select a different frequency for the NCO, two registers (0x3B and 0x41) in the DIGITAL page must be updated. Assuming a SPI clock frequency of 10 MHz (100 ns period), programming two registers (2x (16 bit address and 8 bit data) = 48 bit) means that the NCO frequency would be updated in ~ 5 us.

When updating the currently being used NCO frequency to a new frequency, the following command has to be written to load the new frequency into the NCO - 0x181 0x00/0x30 in each of the DDCAB/CD pages.

**Table 7-22. Example Register Writes**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x02 | Select DIGITAL page |
| 0x3B | 0x01 | Select frequency 2 for NCO1 of channel A. |
| 0x235 | 0xFF | Select NCO using SPI |
| 0x05 | 0x08 | Select DDCAB page |
| 0x10D...0x108 | 0x.. | Write new frequency in frequency 2 of NCO1 of channel A |
| 0x181 | 0x00 | Update NCO with current frequencies from the register map. |
| 0x181 | 0x30 | |

The NCO phase accumulators can be reset using the external SYSREF signal. A SYSREF mask can be setup such the SYSREF signal only goes to the NCO and the remaining device remains unaffected. The following register writes configure the SYSREF mask to only affect the NCO. After completion, the SYSREF mask should be set back to default.

**Table 7-23. Example Register Writes to configure the SYSREF MASK**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x18 | Select DDCAB/CD page |
| 0x181 | 0x40 | Reset NCO phases with SYSREF toggle |
| 0x05 | 0x02 | Select DIGITAL page |
| 0x357 | 0xA2 | SYSREF mask settings (0x00 is mask default) |
| 0x358 | 0x02 | SYSREF mask settings (0x00 is mask default) |

### 7.3.5.6 Fast Frequency Hopping

The ADC34RF52 supports several different options to update the NCO frequencies. Fast frequency hopping can be achieved in one of the following ways:

- Using the GPIO1/2 pins to select the NCO frequency
- Using the GPIO1/2, SPISEL and SCLK/SDIO pins to select the NCO frequency
- Using the GPIO1/2 pins to program the NCO frequency selection (Fast SPI)

| NCO CONTROL | SCLK | SDATA | SPISEL | GPIO1 | GPIO2 | NCO SEL MODE |
|---|---|---|---|---|---|---|
| Regular SPI (default) | SPI Interface | | 0 | used for other purpose | | 00 |
| GPIO1/2 | SPI Interface | | 0 | used for NCO control | | 00 |
| GPIO1/2, SPISEL, SCLK/SDATA | NCO CONTROL | | 1 | used for NCO control | | 00 |
| FAST SPI | SPI Interface | | 1 | SDATA | SCLK | 10 |

The internal NCO is switched quickly; however, the switching time depends primarily on the time it takes to flush out the decimation filter as shown in Table 7-24.

**Table 7-24. NCO Switching Time ($F_S$ = 1.5 GSPS) vs Decimation Setting**

| Decimation Setting | NCO Switching Time |
|---|---|
| /4 | ~ 500 ns |
| /8 | ~ 700 ns |
| /16 | ~ 1.2 us |
| /32 | ~ 2 us |
| /64 | ~ 4 us |
| /128 | ~ 8 us |

#### 7.3.5.6.1 Fast frequency hopping using the GPIO1/2 pins

The NCO frequency is selected as shown in Table 7-25. This mode is enabled with the following register writes:

1. Set 0x234 to 0x03 (NCO SEL MODE = 0, GPIO MODE = 3)

*** selection common to all NCOs. there is option to only update single nco??

**Table 7-25. NCO Frequency Selection using GPIO1/2 Pins**

| # OF BANDS | GPIO2 | GPIO1 | GPIO2 | GPIO1 | GPIO2 | GPIO1 | GPIO2 | GPIO1 |
|---|---|---|---|---|---|---|---|---|
| SINGLE | 0 | 0 | NCO1 CHB [1:0] | | 0 | 0 | NCO1 CHA [1:0] | |
| | 0 | 0 | NCO1 CHD [1:0] | | 0 | 0 | NCO1 CHC [1:0] | |
| DUAL | NCO2 CHB [1:0] | | NCO1 CHB [1:0] | | NCO2 CHA [1:0] | | NCO1 CHA [1:0] | |
| | NCO2 CHD [1:0] | | NCO1 CHD [1:0] | | NCO2 CHC [1:0] | | NCO1 CHC [1:0] | |

#### 7.3.5.6.2 Fast frequency hopping using GPIO1/2, SEN and SDATA pins

This mode is enabled by setting the SPISEL to logic high and using the following register writes:

1. NCO SEL MODE in address 0x234 needs to be set to 3

**Table 7-26. NCO Frequency Selection SPI Interface Registers**

| # OF BANDS | SDATA | SEN | GPIO2 | GPIO1 | SDATA | SEN | GPIO2 | GPIO1 |
|---|---|---|---|---|---|---|---|---|
| SINGLE | NCO1 CHB [2] | 0 | NCO1 CHB [1:0] | | NCO1 CHA [2] | 0 | NCO1 CHA [1:0] | |
| | NCO1 CHD [2] | 0 | NCO1 CHD [1:0] | | NCO1 CHC [2] | 0 | NCO1 CHC [1:0] | |
| DUAL | NCO2 CHB [1:0] | | NCO1 CHB [1:0] | | NCO2 CHA [1:0] | | NCO1 CHA [1:0] | |
| | NCO2 CHD [1:0] | | NCO1 CHD [1:0] | | NCO2 CHC [1:0] | | NCO1 CHC [1:0] | |

#### 7.3.5.6.3 Fast frequency hopping using the fast SPI

In this mode the GPIO1/2 pins are used as a "fast SPI" input which only updates the NCO selection registers. No register address information needs to be sent. GPIO1 pin is SDATA and GPIO2 pin is SCLK.

This mode is enabled by setting the SPISEL to logic high and using the following register writes:

1. Set 0x234 to 0x43 (NCO SEL MODE = 2, GPIO MODE = 3)

The NCO frequencies are selected as shown in Table 7-27.

**Table 7-27. NCO Frequency Programming using FAST SPI**

| # OF BANDS | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SINGLE | NCO1 CHD [2] | 0 | NCO1 CHD [1:0] | | NCO1 CHC [2] | 0 | NCO1 CHC [1:0] | | NCO1 CHB [2] | 0 | NCO1 CHB [1:0] | | NCO1 CHA [2] | 0 | NCO1 CHA [1:0] | |
| DUAL | NCO2 CHD [1:0] | | NCO1 CHD [1:0] | | NCO2 CHC [1:0] | | NCO1 CHC [1:0] | | NCO2 CHB [1:0] | | NCO1 CHB [1:0] | | NCO2 CHA [1:0] | | NCO1 CHA [1:0] | |

### 7.3.6 JESD204B Interface

The ADC34RF52 uses the JESD204B high-speed serial interface to transfer data from the ADC to the receiving logic device. ADC34RF52 serialized lanes are capable of operating up to 13 Gbps, slightly above the JESD204B max lane rate. A maximum of 8 lanes can be used to allow lower lane rates for interfacing with speed limited logic devices. Figure 7-38 shows a simplified block diagram of the JESD204B interface.
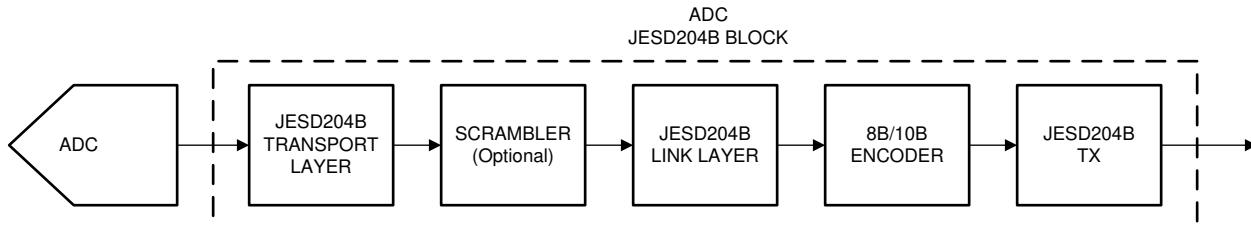


**Figure 7-38. JESD204B Block Diagram**

#### 7.3.6.1 JESD204B Initial Lane Alignment (ILA)

The receiving device starts the initial lane alignment process by deasserting the $\overline{\text{SYNC}}$ signal. When a logic low state is detected on the $\overline{\text{SYNC}}$ input, the ADC starts transmitting comma characters (K28.5) to establish the code group synchronization, as shown in Figure 7-39. When synchronization is completed, the receiving device reasserts the $\overline{\text{SYNC}}$ signal and the ADC starts the initial lane alignment sequence with the next local multi-frame clock (LMFC) boundary. The ADC transmits four multi-frames, each containing K frame (K is SPI programmable). EAch of the multi-frames contains the frame start and frame end symbols. The second multi-frame also contains the JESD204B link configuration data.
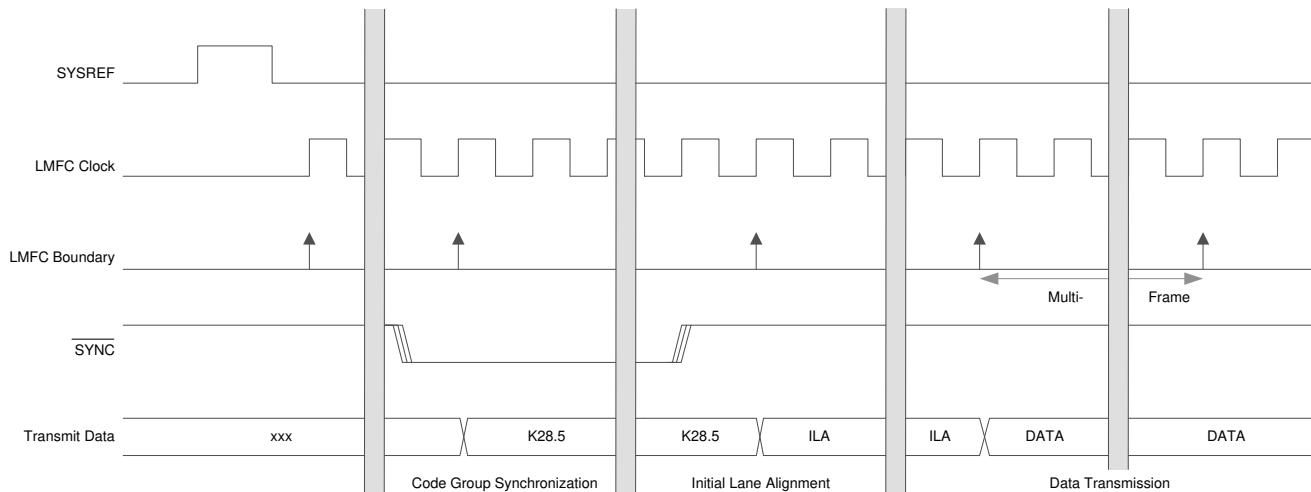


**Figure 7-39. JESD204B Internal Timing Diagram**

#### 7.3.6.1.1 $\overline{\text{SYNC}}$ Signal

The $\overline{\text{SYNC}}$ signal can be issued using one of two different methods:
- One of the GPIO1/2 pins can be configured via SPI to become the $\overline{\text{SYNC}}$ input pin (address 0x234 in the digital page)
- The synchronization command can be issued via SPI register write (address 0x21 in the JESD page)

When using the GPIO1/2 pins for the $\overline{\text{SYNC}}$ signal input, the device also supports the option to invert the signal polarity (address 0x236 in the digital page).

### 7.3.6.2 JESD204B Frame Assembly

The JESD204B standard defines the following parameters:

- L: number of lanes per link
- M: number of converters per device
- F: number of octets per frame clock period
- S: number of samples per frame

#### 7.3.6.2.1 JESD204B Frame Assembly in Bypass Mode

Table 7-28 lists the available JESD204B formats and corresponding valid sampling rate ranges for the ADC34RF52. The sampling rates are limited by the minimum and maximum SERDES line rate as well as ADC sampling clock frequencies. The JESD204B frame assembly for the different lanes is shown in Table 7-29.

**Table 7-28. JESD Mode Options: Bypass Mode**

| DECIMATION SETTING D (complex) | OUTPUT RESOLUTION (Bits) | L | M | F | S | MIN $F_S$ (Gsps) | MAX $F_S$ (Gsps) | RATIO [$f_{SERDES}/F_S$] |
|---|---|---|---|---|---|---|---|---|
| Bypass | 12[1] | 8 | 4 | 8 | 10 | 0.5 | 1.5 | 8 |
| | 14/16[2] | 8 | 4 | 2 | 2 | 0.5 | 1.3 | 10 |
| | | 4 | 4 | 2 | 1 | 0.5 | 0.65 | 20 |

(1) In full rate output, two LSBs are truncated to a 12-bit output.
(2) When using digital averaging the output resolution changes to 16-bit.

**Table 7-29. JESD Sample Frame Assembly: Bypass Mode**

| OUTPUT LANE | LMFS = 84810 | | | | | | | | LMFS = 8422 | | LMFS = 4421 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DOUT0 | $A_0$[11:4] | $A_0$[3:0], $A_1$[11:8] | $A_1$[7:0] | $A_2$[11:4] | $A_2$[3:0], $A_3$[11:8] | $A_3$[7:0] | $A_4$[11:4] | $A_4$[3:0], 0000 | $A_0$[13:6] | $A_0$[5:0], 00 | $A_0$[13:6] | $A_0$[5:0], 00 |
| DOUT1 | $A_5$[11:4] | $A_5$[3:0], $A_6$[11:8] | $A_6$[7:0] | $A_7$[11:4] | $A_7$[3:0], $A_8$[11:8] | $A_8$[7:0] | $A_9$[11:4] | $A_9$[3:0], 0000 | $A_1$[13:6] | $A_1$[5:0], 00 | $B_0$[13:6] | $B_0$[5:0], 00 |
| DOUT2 | $B_0$[11:4] | $B_0$[3:0], $B_1$[11:8] | $B_1$[7:0] | $B_2$[11:4] | $B_2$[3:0], $B_3$[11:8] | $B_3$[7:0] | $B_4$[11:4] | $B_4$[3:0], 0000 | $B_0$[13:6] | $B_0$[5:0], 00 | $C_0$[13:6] | $C_0$[5:0], 00 |
| DOUT3 | $B_5$[11:4] | $B_5$[3:0], $B_6$[11:8] | $B_6$[7:0] | $B_7$[11:4] | $B_7$[3:0], $B_8$[11:8] | $B_8$[7:0] | $B_9$[11:4] | $B_9$[3:0], 0000 | $B_1$[13:6] | $B_1$[5:0], 00 | $D_0$[13:6] | $D_0$[5:0], 00 |
| DOUT4 | $C_0$[11:4] | $C_0$[3:0], $C_1$[11:8] | $C_1$[7:0] | $C_2$[11:4] | $C_2$[3:0], $C_3$[11:8] | $C_3$[7:0] | $C_4$[11:4] | $C_4$[3:0], 0000 | $C_0$[13:6] | $C_0$[5:0], 00 | | |
| DOUT5 | $C_5$[11:4] | $C_5$[3:0], $C_6$[11:8] | $C_6$[7:0] | $C_7$[11:4] | $C_7$[3:0], $C_8$[11:8] | $C_8$[7:0] | $C_9$[11:4] | $C_9$[3:0], 0000 | $C_1$[13:6] | $C_1$[5:0], 00 | | |
| DOUT6 | $D_0$[11:4] | $D_0$[3:0], $D_1$[11:8] | $D_1$[7:0] | $D_2$[11:4] | $D_2$[3:0], $D_3$[11:8] | $D_3$[7:0] | $D_4$[11:4] | $D_4$[3:0], 0000 | $D_0$[13:6] | $D_0$[5:0], 00 | | |
| DOUT7 | $D_5$[11:4] | $D_5$[3:0], $D_6$[11:8] | $D_6$[7:0] | $D_7$[11:4] | $D_7$[3:0], $D_8$[11:8] | $D_8$[7:0] | $D_9$[11:4] | $D_9$[3:0], 0000 | $D_1$[13:6] | $D_1$[5:0], 00 | | |

Product Folder Links: ADC34RF52

### 7.3.6.2.2 JESD204B Frame Assembly with Real Decimation - Single Band

Table 7-30 lists the available JESD204B formats and corresponding valid sampling rate ranges for the ADC34RF52. The sampling rates are limited by the minimum and maximum SERDES line rate as well as ADC sampling clock frequencies. The JESD204B frame assembly for the different lanes is shown in Table 7-31.

**Table 7-30. JESD Mode Options: Real Decimation**

| DECIMATION SETTING D (complex) | L | M | F | S | MIN $F_S$ (Gsps) | MAX $F_S$ (Gsps) | RATIO [$f_{SERDES}$/($F_S$/D)] |
|---|---|---|---|---|---|---|---|
| /4 | 8 | 4 | 2 | 2 | 0.5 | 1.5 | 10 |
| /8 | | | | | | | |
| /16 | | | | | 0.8 | | |
| /4 | 4 | 4 | 2 | 1 | 0.5 | 1.5 | 20 |
| /8 | | | | | | | |
| /16 | | | | | | | |
| /32 | | | | | 0.8 | | |
| /4 | 2 | 4 | 4 | 1 | 0.5 | 1.3 | 40 |
| /8 | | | | | | | |
| /16 | | | | | | 1.5 | |
| /32 | | | | | | | |
| /64 | | | | | 0.8 | | |
| /8 | 1 | 4 | 8 | 1 | 0.5 | 1.3 | 80 |
| /16 | | | | | | | |
| /32 | | | | | | 1.5 | |
| /64 | | | | | | | |
| /128 | | | | | 0.8 | | |

**Table 7-31. JESD Sample Frame Assembly: Real Decimation - Single Band**

| OUTPUT LANE | LMFS = 8422 | | LMFS = 4421 | | LMFS = 2441 | | | | LMFS = 1481 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DOUT0 | $A_0$ [15:8] | $A_0$ [7:0] | $A_0$ [15:8] | $A_0$ [7:0] | $A_0$ [15:8] | $A_0$ [7:0] | $B_0$ [15:8] | $B_0$ [7:0] | $A_0$ [15:8] | $A_0$ [7:0] | $B_0$ [15:8] | $B_0$ [7:0] | $C_0$ [15:8] | $C_0$ [7:0] | $D_0$ [15:8] | $D_0$ [7:0] |
| DOUT1 | $A_1$ [15:8] | $A_1$ [7:0] | $B_0$ [15:8] | $B_0$ [7:0] | $C_0$ [15:8] | $C_0$ [7:0] | $D_0$ [15:8] | $D_0$ [7:0] | | | | | | | | |
| DOUT2 | $B_0$ [15:8] | $B_0$ [7:0] | $C_0$ [15:8] | $C_0$ [7:0] | | | | | | | | | | | | |
| DOUT3 | $B_1$ [15:8] | $B_1$ [7:0] | $D_0$ [15:8] | $D_0$ [7:0] | | | | | | | | | | | | |
| DOUT4 | $C_0$ [15:8] | $C_0$ [7:0] | | | | | | | | | | | | | | |
| DOUT5 | $C_1$ [15:8] | $C_1$ [7:0] | | | | | | | | | | | | | | |
| DOUT6 | $D_0$ [15:8] | $D_0$ [7:0] | | | | | | | | | | | | | | |
| DOUT7 | $D_1$ [15:8] | $D_1$ [7:0] | | | | | | | | | | | | | | |

Product Folder Links: ADC34RF52

#### 7.3.6.2.3 JESD204B Frame Assembly with Decimation - Single Band

Table 7-32 lists the available JESD204B interface formats and corresponding valid sampling rate ranges for the ADC34RF52 with complex decimation (single band). The sampling rates are limited by the minimum and maximum SERDES line rate as well as ADC sampling clock frequencies. The JESD204B frame assembly for the different lanes are shown in Table 7-33 and Table 7-34.

**Table 7-32. JESD Mode Options: Decimation - Single Band**

| DECIMATION SETTING D (complex) | L | M | F | S | MIN $F_S$ (Gsps) | MAX $F_S$ (Gsps) | RATIO [$f_{SERDES}/(F_S/D)$] |
|---|---|---|---|---|---|---|---|
| /4 | 8 | 8 | 2 | 1 | 0.5 | 1.5 | 20 |
| /8 | | | | | 0.5 | 1.5 | 20 |
| /16 | | | | | 0.5 | 1.5 | 20 |
| /32 | | | | | 0.8 | 1.5 | 20 |
| /4 | 4 | 8 | 4 | 1 | 0.5 | 1.3 | 40 |
| /8 | | | | | 0.5 | 1.5 | 40 |
| /16 | | | | | 0.5 | 1.5 | 40 |
| /32 | | | | | 0.5 | 1.5 | 40 |
| /64 | | | | | 0.8 | 1.5 | 40 |
| /4 | 2 | 8 | 8 | 1 | 0.5 | 0.65 | 80 |
| /8 | | | | | 0.5 | 1.3 | 80 |
| /16 | | | | | 0.5 | 1.5 | 80 |
| /32 | | | | | 0.5 | 1.5 | 80 |
| /64 | | | | | 0.5 | 1.5 | 80 |
| /128 | | | | | 0.8 | 1.5 | 80 |
| /8 | 1 | 8 | 16 | 1 | 0.5 | 0.65 | 160 |
| /16 | | | | | 0.5 | 1.3 | 160 |
| /32 | | | | | 0.5 | 1.5 | 160 |
| /64 | | | | | 0.5 | 1.5 | 160 |
| /128 | | | | | 0.5 | 1.5 | 160 |

**Table 7-33. JESD Sample Frame Assembly: Decimation - Single Band**

| OUTPUT LANE | LMFS = 8821 | | LMFS = 4841 | | | | LMFS = 2881 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DOUT0 | $AI_0$[15:8] | $AI_0$[7:0] | $AI_0$[15:8] | $AI_0$[7:0] | $AQ_0$[15:8] | $AQ_0$[7:0] | $AI_0$[15:8] | $AI_0$[7:0] | $AQ_0$[15:8] | $AQ_0$[7:0] | $BI_0$[15:8] | $BI_0$[7:0] | $BQ_0$[15:8] | $BQ_0$[7:0] |
| DOUT1 | $AQ_0$[15:8] | $AQ_0$[7:0] | $BI_0$[15:8] | $BI_0$[7:0] | $BQ_0$[15:8] | $BQ_0$[7:0] | $CI_0$[15:8] | $CI_0$[7:0] | $CQ_0$[15:8] | $CQ_0$[7:0] | $DI_0$[15:8] | $DI_0$[7:0] | $DQ_0$[15:8] | $DQ_0$[7:0] |
| DOUT2 | $BI_0$[15:8] | $BI_0$[7:0] | $CI_0$[15:8] | $CI_0$[7:0] | $CQ_0$[15:8] | $CQ_0$[7:0] | | | | | | | | |
| DOUT3 | $BQ_0$[15:8] | $BQ_0$[7:0] | $DI_0$[15:8] | $DI_0$[7:0] | $DQ_0$[15:8] | $DQ_0$[7:0] | | | | | | | | |
| DOUT4 | $CI_0$[15:8] | $CI_0$[7:0] | | | | | | | | | | | | |
| DOUT5 | $CQ_0$[15:8] | $CQ_0$[7:0] | | | | | | | | | | | | |
| DOUT6 | $DI_0$[15:8] | $DI_0$[7:0] | | | | | | | | | | | | |
| DOUT7 | $DQ_0$[15:8] | $DQ_0$[7:0] | | | | | | | | | | | | |

Product Folder Links: ADC34RF52

**Table 7-34. JESD Sample Frame Assembly: Decimation - Single Band**

| OUTPUT LANE | LMFS = 1-8-16-1 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DOUT 0 | $AI_0$ [15:8] | $AI_0$ [7:0] | $AQ_0$ [15:8] | $AQ_0$ [7:0] | $CI_0$ [15:8] | $CI_0$ [7:0] | $CQ_0$ [15:8] | $CQ_0$ [7:0] | $BI_0$ [15:8] | $BI_0$ [7:0] | $BQ_0$ [15:8] | $BQ_0$ [7:0] | $DI_0$ [15:8] | $DI_0$ [7:0] | $DQ_0$ [15:8] | $DQ_0$ [7:0] |
| DOUT 1 | | | | | | | | | | | | | | | | |
| DOUT 2 | | | | | | | | | | | | | | | | |
| DOUT 3 | | | | | | | | | | | | | | | | |
| DOUT 4 | | | | | | | | | | | | | | | | |
| DOUT 5 | | | | | | | | | | | | | | | | |
| DOUT 6 | | | | | | | | | | | | | | | | |
| DOUT 7 | | | | | | | | | | | | | | | | |

Product Folder Links: *ADC34RF52*

**7.3.6.2.4 JESD204B Frame Assembly with Decimation - Dual Band**

Table 7-35 lists the available JESD204B interface formats and corresponding valid sampling rate ranges for the ADC34RF52 with complex decimation (dual band). The sampling rates are limited by the minimum and maximum SERDES line rate as well as ADC sampling clock frequencies. The JESD204B frame assembly for the different lanes are shown in Table 7-36, Table 7-37 and Table 7-38.

**Table 7-35. JESD Mode Options: Decimation - Dual Band**

| DECIMATION SETTING D (complex) | L | M | F | S | MIN $F_S$ (Gsps) | MAX $F_S$ (Gsps) | RATIO [$f_{SERDES}/(F_S/D)$] |
|---|---|---|---|---|---|---|---|
| /8 | 8 | 16 | 4 | 1 | 0.5 | 1.5 | 40 |
| /16 | | | | | | | |
| /32 | | | | | | | |
| /64 | | | | | 0.8 | | |
| /8 | 4 | 16 | 8 | 1 | 0.5 | 1.5 | 80 |
| /16 | | | | | | | |
| /32 | | | | | | | |
| /64 | | | | | | | |
| /128 | | | | | 0.8 | | |
| /8 | 2 | 16 | 16 | 1 | 0.5 | 0.65 | 160 |
| /16 | | | | | | 1.3 | |
| /32 | | | | | | | |
| /64 | | | | | | 1.5 | |
| /128 | | | | | | | |
| /16 | 1 | 16 | 32 | 1 | 0.5 | 0.65 | 320 |
| /32 | | | | | | 1.3 | |
| /64 | | | | | | | |
| /128 | | | | | | 1.5 | |

**Table 7-36. JESD Sample Frame Assembly: Decimation - Dual Band**

| OUTPUT LANE | LMFS = 8-16-4-1 | | | | LMFS = 4-16-8-1 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DOUT0 | $A1I_0$ [15:8] | $A1I_0$ [7:0] | $A1Q_0$ [15:8] | $A1Q_0$ [7:0] | $A1I_0$ [15:8] | $A1I_0$ [7:0] | $A1Q_0$ [15:8] | $A1Q_0$ [7:0] | $A2I_0$ [15:8] | $A2I_0$ [7:0] | $A2Q_0$ [15:8] | $A2Q_0$ [7:0] |
| DOUT1 | $A2I_0$ [15:8] | $A2I_0$ [7:0] | $A2Q_0$ [15:8] | $A2Q_0$ [7:0] | $B1I_0$ [15:8] | $B1I_0$ [7:0] | $B1Q_0$ [15:8] | $B1Q_0$ [7:0] | $B2I_0$ [15:8] | $B2I_0$ [7:0] | $B2Q_0$ [15:8] | $B2Q_0$ [7:0] |
| DOUT2 | $B1I_0$ [15:8] | $B1I_0$ [7:0] | $B1Q_0$ [15:8] | $B1Q_0$ [7:0] | $C1I_0$ [15:8] | $C1I_0$ [7:0] | $C1Q_0$ [15:8] | $C1Q_0$ [7:0] | $C2I_0$ [15:8] | $C2I_0$ [7:0] | $C2Q_0$ [15:8] | $C2Q_0$ [7:0] |
| DOUT3 | $B2I_0$ [15:8] | $B2I_0$ [7:0] | $B2Q_0$ [15:8] | $B2Q_0$ [7:0] | $D1I_0$ [15:8] | $D1I_0$ [7:0] | $D1Q_0$ [15:8] | $D1Q_0$ [7:0] | $D2I_0$ [15:8] | $D2I_0$ [7:0] | $D2Q_0$ [15:8] | $D2Q_0$ [7:0] |
| DOUT4 | $CI_0$ [15:8] | $C1I_0$ [7:0] | $C1Q_0$ [15:8] | $C1Q_0$ [7:0] | | | | | | | | |
| DOUT5 | $C2I_0$ [15:8] | $C2I_0$ [7:0] | $C2Q_0$ [15:8] | $C2Q_0$ [7:0] | | | | | | | | |
| DOUT6 | $D1I_0$ [15:8] | $D1I_0$ [7:0] | $D1Q_0$ [15:8] | $D1Q_0$ [7:0] | | | | | | | | |
| DOUT7 | $D2I_0$ [15:8] | $D2I_0$ [7:0] | $D2Q_0$ [15:8] | $D2Q_0$ [7:0] | | | | | | | | |

**Table 7-37. JESD Sample Frame Assembly: Decimation - Dual Band**

| OUTPUT LANE | LMFS = 2-16-16-1 | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DOUT 0 | A1I$_0$ [15:8] | A1I$_0$ [7:0] | A1Q$_0$ [15:8] | A1Q$_0$ [7:0] | A2I$_0$ [15:8] | A2I$_0$ [7:0] | A2Q$_0$ [15:8] | A2Q$_0$ [7:0] | B1I$_0$ [15:8] | B1I$_0$ [7:0] | B1Q$_0$ [15:8] | B1Q$_0$ [7:0] | B2I$_0$ [15:8] | B2I$_0$ [7:0] | B2Q$_0$ [15:8] | B2Q$_0$ [7:0] |
| DOUT 1 | C1I$_0$ [15:8] | C1I$_0$ [7:0] | C1Q$_0$ [15:8] | C1Q$_0$ [7:0] | C2I$_0$ [15:8] | C2I$_0$ [7:0] | C2Q$_0$ [15:8] | C2Q$_0$ [7:0] | D1I$_0$ [15:8] | D1I$_0$ [7:0] | D1Q$_0$ [15:8] | D1Q$_0$ [7:0] | D2I$_0$ [15:8] | D2I$_0$ [7:0] | D2Q$_0$ [15:8] | D2Q$_0$ [7:0] |
| DOUT 2 | | | | | | | | | | | | | | | | |
| DOUT 3 | | | | | | | | | | | | | | | | |
| DOUT 4 | | | | | | | | | | | | | | | | |
| DOUT 5 | | | | | | | | | | | | | | | | |
| DOUT 6 | | | | | | | | | | | | | | | | |
| DOUT 7 | | | | | | | | | | | | | | | | |

**Table 7-38. JESD Sample Frame Assembly: Decimation - Dual Band**

| OUTPUT LANE | LMFS = 1-16-32-1 | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| DOUT 0 | A1I$_0$ [15:8] | A1I$_0$ [7:0] | A1Q$_0$ [15:8] | A1Q$_0$ [7:0] | A2I$_0$ [15:8] | A2I$_0$ [7:0] | A2Q$_0$ [15:8] | A2Q$_0$ [7:0] | B1I$_0$ [15:8] | B1I$_0$ [7:0] | B1Q$_0$ [15:8] | B1Q$_0$ [7:0] | B2I$_0$ [15:8] | B2I$_0$ [7:0] | B2Q$_0$ [15:8] | B2Q$_0$ [7:0] | ... |
| | ... | C1I$_0$ [15:8] | C1I$_0$ [7:0] | C1Q$_0$ [15:8] | C1Q$_0$ [7:0] | C2I$_0$ [15:8] | C2I$_0$ [7:0] | C2Q$_0$ [15:8] | C2Q$_0$ [7:0] | D1I$_0$ [15:8] | D1I$_0$ [7:0] | D1Q$_0$ [15:8] | D1Q$_0$ [7:0] | D2I$_0$ [15:8] | D2I$_0$ [7:0] | D2Q$_0$ [15:8] | D2Q$_0$ [7:0] |
| DOUT 1 | | | | | | | | | | | | | | | | | |
| DOUT 2 | | | | | | | | | | | | | | | | | |
| DOUT 3 | | | | | | | | | | | | | | | | | |
| DOUT 4 | | | | | | | | | | | | | | | | | |
| DOUT 5 | | | | | | | | | | | | | | | | | |
| DOUT 6 | | | | | | | | | | | | | | | | | |
| DOUT 7 | | | | | | | | | | | | | | | | | |

Product Folder Links: *ADC34RF52*

### 7.3.6.3 SERDES Output MUX

The SERDES output block contains one digital mux per SERDES output lane with a 3-bit register. This allows routing any of the 8 digital lanes to any output serdes transmitter as shown in the example for output lane DOUT0 in Figure 7-40.
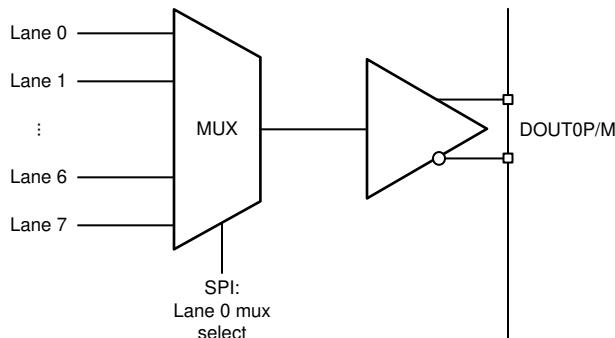


**Figure 7-40. SERDES Output Mux for DOUT0**

By default after power the active SERDES lanes start on lane DOUT0 as shown for the complex decimation single band example in Table 7-39. After power up the output is transmitted on lanes DOUT0..3. Using the digital output muxes, the output data for channel B is shifted from lanes DOUT2,3 to DOUT4,5. All SERDES transmitters are powered up and enabled by default. After configuring the output mux unused lanes can be powered down to save power consumption.

**Table 7-39. JESD Sample Frame Assembly: Complex Decimation - Single Band with LMFS = 4841**

| OUTPUT LANE | Default | | | | Using MUX | | | |
|---|---|---|---|---|---|---|---|---|
| DOUT0 | $AI_0$ [15:8] | $AI_0$ [7:0] | $AQ_0$ [15:8] | $AQ_0$ [7:0] | $AI_0$ [15:8] | $AI_0$ [7:0] | $AQ_0$ [15:8] | $AQ_0$ [7:0] |
| DOUT1 | $BI_0$ [15:8] | $BI_0$ [7:0] | $BQ_0$ [15:8] | $BQ_0$ [7:0] | $BI_0$ [15:8] | $BI_0$ [7:0] | $BQ_0$ [15:8] | $BQ_0$ [7:0] |
| DOUT2 | $CI_0$ [15:8] | $CI_0$ [7:0] | $CQ_0$ [15:8] | $CQ_0$ [7:0] | | | | |
| DOUT3 | $DI_0$ [15:8] | $DI_0$ [7:0] | $DQ_0$ [15:8] | $DQ_0$ [7:0] | | | | |
| DOUT4 | | | | | $CI_0$ [15:8] | $CI_0$ [7:0] | $CQ_0$ [15:8] | $CQ_0$ [7:0] |
| DOUT5 | | | | | $DI_0$ [15:8] | $DI_0$ [7:0] | $DQ_0$ [15:8] | $DQ_0$ [7:0] |
| DOUT6 | | | | | | | | |
| DOUT7 | | | | | | | | |

Table 7-40 shows the register writes to shift the output lanes from default as illustrated in Table 7-39.

**Table 7-40. Example register writes to shift the output serdes lanes using the SERDES Output MUX**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x04 | Select JESD page |
| 0x81 | 0x54 | Select internal JESD streams 4 and 5 to lanes DOUT2 and DOUT3 |
| 0x82 | 0x32 | Select internal JESD streams 2 and 3 to lanes DOUT4 and DOUT5 |

### 7.3.7 Test Pattern

The ADC34RF52 provides several different options to output test patterns instead of the actual output data of the ADC to simplify the serial interface and system debug of the JESD204B digital interface link. The output data path is shown in Figure 7-41.
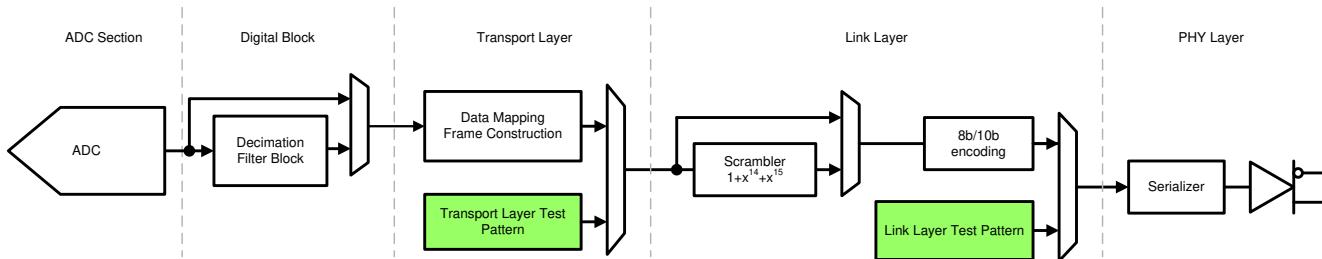


**Figure 7-41. Test Pattern Options**

The available test patterns in each block are described in Table 7-41. Both test pattern blocks replace output data from the digital block (and not from the ADC); therefore, are available in decimation or decimation bypass mode.

**Table 7-41. Test Pattern Overview**

| TEST PATTERN LOCATION | TYPE | 8b/10b encoded | REGISTER PAGE | REGISTER |
|---|---|---|---|---|
| TRANSPORT LAYER | CUSTOM PATTERN | Yes | JESD 0x05 0x04 | 0x2E, D0 |
| | TOGGLE 1010 PATTERN | Yes | | 0x2E, D1 |
| | RAMP PATTERN | Yes | | 0x2E, D2 |
| | PRBS PATTERN ($2^7$.. $2^{31}$) | Yes | | 0x2F, D0 |
| LINK LAYER | JESD204B TEST PATTERNS | Depends | | 0x2D, D2-D0 |
| | PRBS PATTERN ($2^7$.. $2^{31}$) | No | | 0x2F, D4 |

The RAMP pattern provides two different output options. Internally each ADC data bus consists of 4 parallel data streams (1 stream per serdes lane). The RAMP pattern is generated for each stream and a different starting value can be set for each stream. By default the starting values are 0. For example a LMFS mode using 2 lanes/ADC would show a *slow* ramp which increments once every 2 clock cycles with starting values set to 0 and ramp increment = 1. Also, a RAMP pattern which increments every clock cycle can be set using different starting values (that is, 0/1) for the 2 streams/lanes and setting the RAMP increment to 2. Table 7-42 shows how to enable the RAMP test pattern.

**Table 7-42. Example Register Writes to Enable RAMP Test Pattern**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x04 | Select JESD page |
| 0x32 | 0x01 | Set lane DOUT1 starting value = 1 |
| 0x36 | 0x03 | Set lane DOUT3 starting value = 1 |
| 0x42 | 0x01 | Set lane DOUT5 starting value = 1 |
| 0x46 | 0x03 | Set lane DOUT7 starting value = 1 |
| 0x2E | 0x14 | Enable RAMP pattern, RAMP increment = 2 |

#### 7.3.7.1 Transport Layer

The transport layer maps the ADC output data into 8-bit octets and constructs the JESD204B frames using the LMFS parameters. Tail bits or 0's are added when needed. Alternatively, test patterns can be substituted instead of the ADC data with the JESD frame, as shown in Table 7-41.

### 7.3.7.2 Link Layer

The link layer contains the scrambler and the 8b/10b encoding of any data passed on from the transport layer. Additionally, the link layer also handles the initial lane alignment sequence that can be manually restarted. The link layer test patterns are intended for testing the quality of the link (jitter testing and so forth). The test patterns do not pass through the 8b/10b encoder and contain the options listed in Table 7-41.

### 7.3.7.3 Internal Capture Memory Buffer

The ADC includes a small internal capture memory buffer which can store up to 64 samples. Once a strobe is given to the memory using SPI register write, the memory will store the next continuous 64 samples of one ADC channel (selected via SPI register write) and stop. The samples are captured from the ADC cores (prior to averaging or decimation). These samples can be read back using the SPI interface without involving the JESD204B interface at all.

This mode allows debug of the analog front end during the initial bring-up phase even if the JESD204B interface is not operational yet.

**Table 7-43. Register writes to enable the internal sample capture buffer**

| ADDR | DATA | DESCRIPTION |
|------|------|-------------|
| 0x05 | 0x02 | Select DIGITAL page |
| 0x34 |      | Select ADC channel (D5/D4) and give strobe (D6). The 64 samples are stored in 0x800 to 0x87F in the digital page |

## 7.4 Device Functional Modes

The device offers two different operating modes: bypass mode and digital averaging. Both operating modes use the same digital back end and JESD204B output configurations.

### 7.4.1 Bypass Mode

This default operating mode provides the lowest power consumption.

### 7.4.2 Digital Averaging

The ADC34RF52 provides a total of eight internal single core 1.5 Gsps ADCs. The normal operating mode uses only four ADC cores (one ADC per channel). The four additional ADC cores can be enabled to trade off additional noise density improvement against a small power increase. Figure 7-42 shows the internal block diagram in digital averaging mode where one external input is connected to 2 ADC cores internally.
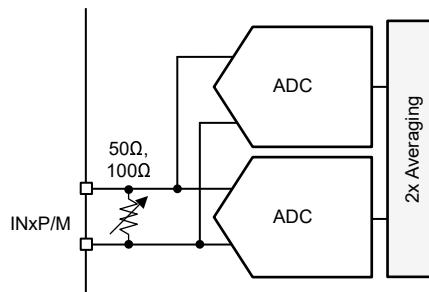


**Figure 7-42. Internal Digital Averaging**

Table 7-44 provides a trade-off comparison of digital averaging mode vs the non-averaged mode (default).

**Table 7-44. Digital averaging vs full power input bandwidth (–3 dB)**

| # of ADCs averaged | Input Bandwidth (-3 dB) | Effective input termination | Noise density | Power/ch (W) |
|---|---|---|---|---|
| Default | 1.6 GHz | 100 Ω | -153 dBFS/Hz | 0.7 |
| 2 | 1.5 GHz | 100 Ω | -156 dBFS/Hz | 1.0 |

Digital averaging improves decorrelated noise contributions by 3 dB per 2x AVG (ideal) while correlated noise does not improve with averaging. Some of the dominant noise sources are correlated (that is, clock jitter (external or first clock input buffer) or power supply noise) while others (that is, ADC thermal noise, clock distribution buffers) are decorrelated.

SNR: When operating close to ADC full scale, some of the SNR limitation is due to jitter and hence the SNR improvement won't reach 3 dB (2x AVG). As the input full scale is reduced, the clock jitter contribution to SNR becomes less and the SNR improvement is approaching the ideal 3 dB per 2x AVG. The same phenomenon can be observed when using digital decimation. As the decimation factor increases, the close-in (correlated noise) becomes the more dominating noise unless the input signal amplitude is reduced.

SFDR: The amplitude of low order harmonics (HD2-HD5) and IMD3 typically is similar across ADCs, and thus, the improvement with averaging is small.

## 7.5 Programming

The device is primarily configured and controlled using the serial programming interface (SPI); however, the device can operate in a default configuration without requiring the SPI interface. Furthermore, the power down function as well as internal/external reference configuration is possible via pin control (PDN/SYNC pin).

### 7.5.1 GPIO Pin Control

There are several commands which can be executed using SPI programming or GPIO pins. Table 7-45 provides an overview of the commands available using GPIO pins.

**Table 7-45. GPIO Pin Command Options**

| FEATURE | DESCRIPTION |
|---|---|
| JESD SYNC | Support for single ended CMOS or differential LVDS |
| NCO Control | Fast frequency hopping with 3 different control options |
| Fast Overrange | GPIO1 indicates overrange for channel A and B and GPIO2 for channel C and D. In this mode the overrange indication can be made 'sticky' where flag needs to be cleared using SPI commands. |
| Calibration Freeze | Freezes swapping of calibration ADC |

### 7.5.2 Configuration using the SPI interface

The device has a set of internal registers that can be accessed by the serial interface formed by the SEN (serial interface enable), SCLK (serial interface clock) and SDIO (serial interface data input/output) pins. Serially shifting bits into the device is enabled when SEN is low. Serial data input are latched at every SCLK rising edge when SEN is active (low). The serial data are loaded into the register at every 24th SCLK rising edge when SEN is low. When the word length exceeds a multiple of 24 bits, the excess bits are ignored. Data can be loaded in multiples of 24-bit words within a single active SEN pulse. The interface can function with SCLK frequencies from 20 MHz down to ~ 1 MHz and also with a non-50% SCLK duty cycle.

*Submit Document Feedback*      57

Product Folder Links: *ADC34RF52*

### 7.5.2.1 Register Write

The internal registers can be programmed following these steps:

1. Drive the SEN pin low
2. Set the R/W bit to 0 (bit A15 of the 16-bit address) and bits A[14:12] in address field to 0.
3. Initiate a serial interface cycle by specifying the address of the register (A[11:0]) whose content is written and
4. Write the 8-bit data that are latched in on the SCLK rising edges

Figure 7-43 shows the timing requirements for the serial register write operation.
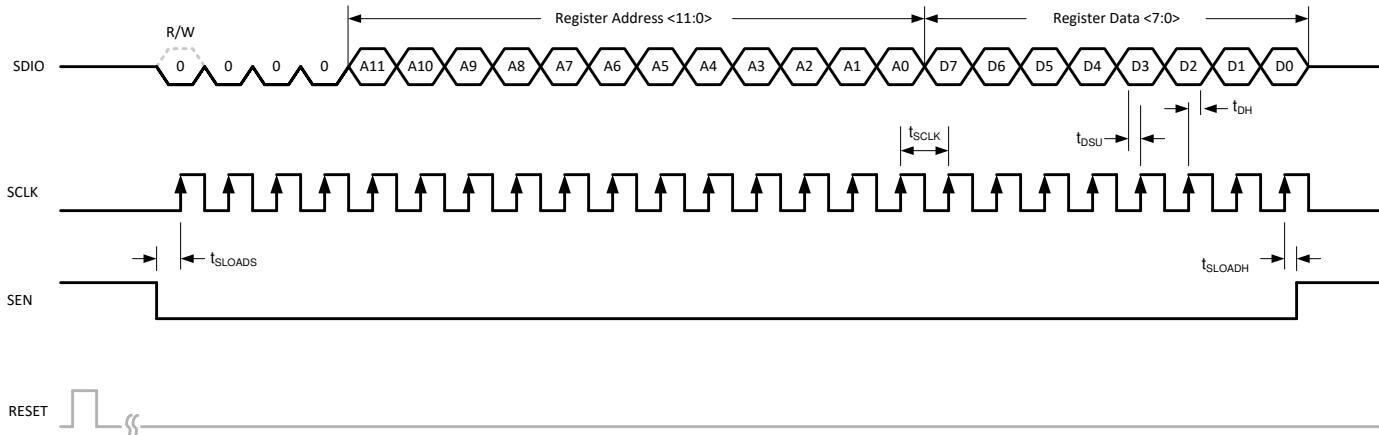


**Figure 7-43. Serial Register Write Timing Diagram**

### 7.5.2.2 Register Read

The device includes a mode where the contents of the internal registers can be read back using the SDIO pin. This readback mode can be useful as a diagnostic check to verify the serial interface communication between the external controller and the ADC. The procedure to read the contents of the serial registers is as follows:

1. Drive the SEN pin low
2. Set the R/W bit (A15) to 1. This setting disables any further writes to the registers. Set A[14:12] in address field to 0.
3. Initiate a serial interface cycle specifying the address of the register (A[11:0]) whose content must be read
4. The device outputs the contents (D[7:0]) of the selected register on the SDIO pin
5. The external controller can latch the contents at the SCLK falling edge
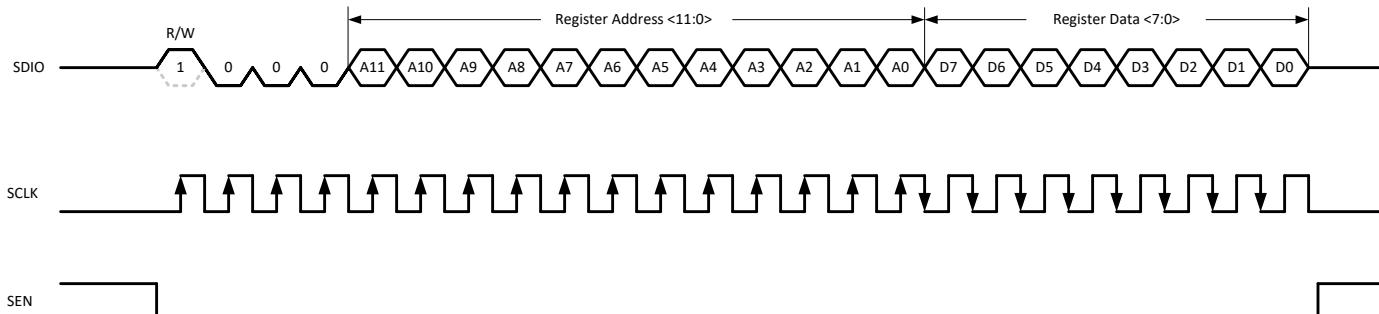


**Figure 7-44. Serial Register Read Timing Diagram**

## 7.6 Register Maps

**Table 7-46. Register Map Summary**

| PAGE | REGISTER ADDRESS | REGISTER DATA | | | | | | | |
|------|------------------|---------------|---|---|---|---|---|---|---|
| | A[11:0] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| **GLOBAL** | 0x00 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | RESET |
| | 0x05 | 0 | ANALOG PAGE | CALIB PAGE | DDCCD PAGE | DDCAB PAGE | JESD PAGE | DIGITAL PAGE | 0 |
| **DIGITAL** | 0x2C | 20-BIT OUT | DDC BAND SEL | | 0 | 0 | 0 | DDC REAL | BYP EN |
| | 0x2D | 0 | DECIMATION | | | 0 | 0 | 0 | 0 |
| | 0x2E | 0 | 0 | 0 | 0 | AVG EN | AVG SEL(1) | | 0 |
| | 0x33 | 0 | 0 | 0 | 1 | FORMAT | 0 | GBL PDN | 0 |
| | 0x34 | 0 | MEM STROBE | MEM CH SEL | | 0 | 0 | 0 | 0 |
| | 0x3B | NCO2 CHB [1:0] | | NCO1 CHB [1:0] | | NCO2 CHA [1:0] | | NCO1 CHA [1:0] | |
| | 0x41 | NCO2 CHD [1:0] | | NCO1 CHD [1:0] | | NCO2 CHC [1:0] | | NCO1 CHC [1:0] | |
| | 0x22F | 1 | SYSREF X5 | SYSREF X4 | SYSREF X3 | SYSREF X2 | SYSREF X1 | SYSREF OR | 1 |
| | 0x234 | 0 | NCO SEL MODE | | 0 | 0 | GPIO MODE | | |
| | 0X235 | NCO SEL SOURCE | | | | | | | |
| | 0x236 | 0 | GPIO2 INV | GPIO1 INV | GPIO SWAP | 0 | 0 | SYSREF RESET | SYSREF EN |
| | 0x238 | OVR OUTPUT CFG | | | | 0 | 0 | 0 | 0 |
| **JESD** | 0x20 | K | | | | | | | |
| | 0x21 | 0 | SYNC SPI EN | SYNC SPI | 0 | 0 | SYSREF MODE | | |
| | 0x22 | LMFS MODE | | | | | | | |
| | 0x24 | DDC CLK DIV | | | | | | | |
| | 0x25 | JESD TX CLK DIV | | | | | | | |
| | 0x27 | 0 | 0 | DROP LSB | 0 | 0 | 0 | CLK BAL EN | 0 |
| | 0x28 | JESD TX LANE EN | | | | | | | |
| | 0x2B | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SYNC INV |
| | 0x2D | 0 | 0 | 0 | 0 | 0 | TEST SEQ SEL | | |
| | 0x2E | RAMP INCR | | | 0 | RAMP EN | ALT PAT | 0 | |
| | 0x2F | 0 | PRBS PAT | | PRBS EN | 0 | JESD PRBS PAT | | JESD PRBS EN |
| | 0x30 | START VALUE JESD RAMP DOUT0 | | | | | | | |
| | 0x32 | START VALUE JESD RAMP DOUT1 | | | | | | | |
| | 0x34 | START VALUE JESD RAMP DOUT2 | | | | | | | |
| | 0x36 | START VALUE JESD RAMP DOUT3 | | | | | | | |
| | 0x40 | START VALUE JESD RAMP DOUT4 | | | | | | | |
| | 0x42 | START VALUE JESD RAMP DOUT5 | | | | | | | |
| | 0x44 | START VALUE JESD RAMP DOUT6 | | | | | | | |
| | 0x46 | START VALUE JESD RAMP DOUT7 | | | | | | | |
| | 0x53 | SCR EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0x5C | F in ILA | | | | | | | |
| | 0x5D | K in ILA | | | | | | | |

## Table 7-46. Register Map Summary (continued)

| PAGE | REGISTER ADDRESS | REGISTER DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | A[11:0] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| JESD | 0x7A | JESD LANE POL INV | | | | | | | |
| | 0x80 | 0 | LANE DOUT1 SEL | | | 0 | LANE DOUT0 SEL | | |
| | 0x81 | 0 | LANE DOUT3 SEL | | | 0 | LANE DOUT2 SEL | | |
| | 0x82 | 0 | LANE DOUT5 SEL | | | 0 | LANE DOUT4 SEL | | |
| | 0x83 | 0 | LANE DOUT7 SEL | | | 0 | LANE DOUT6 SEL | | |
| | 0x84 | 0 | 0 | 0 | 0 | 0 | 0 | JESD PLL FACTOR | |
| | 0x89 | TX EMPH DOUT1 [0] | TX EMPH DOUT0 [5:0] | | | | | | 0 |
| | 0x8A | 0 | 0 | 0 | TX EMPH DOUT1 [5:1] | | | | |
| | 0x8B | TX EMPH DOUT3 [0] | TX EMPH DOUT2 [5:0] | | | | | | 0 |
| | 0x8C | 0 | 0 | 0 | TX EMPH DOUT3 [5:1] | | | | |
| | 0x8D | TX EMPH DOUT5 [0] | TX EMPH DOUT4 [5:0] | | | | | | 0 |
| | 0x8E | 0 | 0 | 0 | TX EMPH DOUT5 [5:1] | | | | |
| | 0x8F | TX EMPH DOUT7 [0] | TX EMPH DOUT6 [5:0] | | | | | | 0 |
| | 0x90 | 0 | 0 | 0 | TX EMPH DOUT7 [5:1] | | | | |
| | 0x9D | PD DOUT7 [0] | PD DOUT6 [0] | PD DOUT5 [0] | PD DOUT4 [0] | PD DOUT3 [0] | PD DOUT2 [0] | PD DOUT1 [0] | PD DOUT0 [0] |
| | 0x9E | PD DOUT7 [1] | PD DOUT6 [1] | PD DOUT5 [1] | PD DOUT4 [1] | PD DOUT3 [1] | PD DOUT2 [1] | PD DOUT1 [1] | PD DOUT0 [1] |
| | 0x9F | 0 | JESD PLL1 | | | 0 | JESD PLL2 | | |
| | 0xA0 | 0 | JESD PLL INPUT1 | | | 0 | 0 | 0 | 0 |
| | 0xA1 | 0 | JESD PLL INPUT2 | | | 0 | 0 | 0 | 0 |
| | 0xA2 | 0 | 0 | 0 | 0 | JESD PLL INPUT3 | | | 0 |
| | 0xED | 0 | 0 | JESD DDC BYP | | 0 | 0 | 0 | 0 |
| DDCAB/CD | 0x100..0x105 | NCO1 CHA/C FREQUENCY1 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x108..0x10D | NCO1 CHA/C FREQUENCY2 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x110..0x115 | NCO1 CHA/C FREQUENCY3 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x118..0x11D | NCO1 CHA/C FREQUENCY4 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x120..0x125 | NCO2 CHA/C FREQUENCY1 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x128..0x12D | NCO2 CHA/C FREQUENCY2 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x130..0x135 | NCO2 CHA/C FREQUENCY3 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x138..0x13D | NCO2 CHA/C FREQUENCY4 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x140..0x145 | NCO1 CHB/D FREQUENCY1 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x148..0x14D | NCO1 CHB/DFREQUENCY2 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x150..0x155 | NCO1 CHB/DFREQUENCY3 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x158..0x15D | NCO1 CHB/DFREQUENCY4 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x160..0x165 | NCO2 CHB/DFREQUENCY1 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x168..0x16D | NCO2 CHB/DFREQUENCY2 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x170..0x175 | NCO2 CHB/DFREQUENCY3 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x178..0x17D | NCO2 CHB/DFREQUENCY4 [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| | 0x181 | 0 | 0 | LOAD NCO | | 0 | 0 | 0 | 0 |

Copyright © 2023 Texas Instruments Incorporated

Product Folder Links: ADC34RF52

**Table 7-46. Register Map Summary (continued)**

| PAGE | REGISTER ADDRESS | REGISTER DATA | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | A[11:0] | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| CALIBRATION | 0x34 | 0 | 0 | 0 | 0 | 0 | AVG SEL(2) | | 1 |
| | 0x45 | CAL SPI | CAL GPIO | 0 | 0 | 1 | 0 | 1 | 0 |
| | 0x298 | 0 | 0 | 0 | 0 | CAL STATUS | | | |
| ANALOG | 0x7B | 0 | 0 | TERM AB | 0 | 0 | 0 | 0 | TERM AB |
| | 0x8B | 0 | 0 | TERM CD | 0 | 0 | 0 | 0 | TERM CD |
| | 0xA8 | 0 | DITHER AMP1 | | | 0 | 0 | 0 | 0 |
| | 0xAF | DITHER DIS | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| | 0xB1 | DITHER DIVIDER | | | | | | | |
| | 0xB4 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | SYSREF AC EN |
| | 0xCD | 0 | DITH AMP2 | | | 0 | 0 | 0 | 0 |
| | 0xE6 | TX SWING [0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | 0xE7 | 0 | 0 | 0 | 0 | 0 | 0 | TX SWING [2:1] | |

Product Folder Links: ADC34RF52

## 7.6.1 Detailed Register Description

**Figure 7-45. Register 0x00**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | RESET |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-47. Register 0x00 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R/W | 0 | Must write 0 |
| 0 | RESET | R/W | 0 | This bit resets all internal registers to the default values. Does not self clear to 0. |

**Figure 7-46. Register 0x05**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | ANALOG PAGE | CALIB PAGE | DDCCD PAGE | DDCAB PAGE | JESD PAGE | DIGITAL PAGE | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-48. Register 0x05 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6 | ANALOG PAGE | R/W | 0 | This bit enables access to the ANALOG page<br>0: ANALOG page access disabled<br>1: ANALOG page access enabled |
| 5 | CALIB PAGE | R/W | 0 | This bit enables access to the CALIBRATION page<br>0: CALIBRATION page access disabled<br>1: CALIBRATION page access enabled |
| 4 | DDCCD PAGE | R/W | 0 | This bit enables access to the DDCCD page. Contents can be written to DDCAB and DDCCD page simultaneously if it is identical.<br>0: DDCCD page access disabled<br>1: DDCCD page access enabled. |
| 3 | DDCAB PAGE | R/W | 0 | This bit enables access to the DDCAB page. Contents can be written to DDCAB and DDCCD page simultaneously if it is identical.<br>0: DDCAB page access disabled<br>1: DDCAB page access enabled |
| 2 | JESD PAGE | R/W | 0 | This bit enables access to the JESD page<br>0: JESD page access disabled<br>1: JESD page access enabled |
| 1 | DIGITAL PAGE | R/W | 0 | This bit enables access to the DIGITAL page<br>0: DIGITAL page access disabled<br>1: DIGITAL page access enabled |
| 0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-47. Register 0x2C (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 20-BIT OUT | DDC BAND SEL | | 0 | 0 | 0 | DDC REAL | BYP EN |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-49. Register 0x2C Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 20-BIT OUT | R/W | 0 | This bit enables the 20-bit output mode. It carries the output sample with 20-bit output resolution from the DDC and the sample is filled to 32-bit with 12 trailing 0s.<br>0: Normal operation<br>1: 20-bit output mode |
| 6-5 | DDC BAND SEL | R/W | 00 | Selects 1 or DDC per ADC when complex decimation is enabled<br>0: Single band<br>1: Dual band<br>2,3: not used |
| 4-2 | 0 | R | 0 | Must write 0 |
| 1 | DDC REAL | R/W | 0 | This bit enables real decimation filter (NCO = 0). BYP EN (D0) must be set to 0.<br>0: Complex decimation<br>1: Real decimation |
| 0 | BYP EN | R/W | 0 | This bit enables DDC bypass mode<br>0: Decimation filter enabled. Complex decimation by default unless D1 is set<br>1: Decimation filter bypass |

**Figure 7-48. Register 0x2D (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DECIMATION | | | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-50. Register 0x2D Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6-4 | DECIMATION | R/W | 0 | Selects decimation.<br>0,1: not used<br>2: Decimation by 4<br>3: Decimation by 8<br>4: Decimation by 16<br>5: Decimation by 32<br>6: Decimation by 64<br>7: Decimation by 128 |
| 3-0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-49. Register 0x2E (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | AVG EN | AVG SEL (1) | | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-51. Register 0x2E Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R/W | 0 | Must write 0 |
| 3 | AVG EN | R/W | 0 | This bit enables averaging<br>0: no average<br>1: ADC averaging enabled |
| 2-1 | AVG SEL (1) | R/W | 00 | Selects ADC averaging. Also AVG SEL (2) in CALIBRATION page needs to be set.<br>0: no average<br>1: 2 ADC average |
| 0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-50. Register 0x33 (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | FORMAT | 0 | GBL PDN | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-52. Register 0x33 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5 | 0 | R/W | 0 | Must write 0 |
| 4 | 1 | R/W | 0 | Must write 1 |
| 3 | FORMAT | R/W | 0 | This register bit determines the output data format in DDC bypass mode only.<br>0: Offset Binary<br>1: 2s Complement<br>DDC mode only supports 2s complement output format. |
| 2 | 0 | R/W | 0 | Must write 0 |
| 1 | GBL PDN | R/W | 0 | This register bit enables global power down mode<br>0: normal operation<br>1: global power down mode enabled |
| 0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-51. Register 0x34 (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | MEM STROBE | MEM CH SEL | | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-53. Register 0x34 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6 | MEM STROBE | R/W | 0 | This register enables fast power down mode<br>0: normal operation<br>1: fast power down mode enabled |
| 5-4 | MEM CH SEL | R/W | 0 | This register selects which ADC channel is used to fill up the capture sample buffer. Only 1 channel can be selected at a time and the samples are captured from the ADC core without averaging or decimation.<br>00: capture memory is filled from chA input<br>01: capture memory is filled from chB input<br>10: capture memory is filled from chC input<br>11: capture memory is filled from chD input |

**Table 7-53. Register 0x34 Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-52. Register 0x3B (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NCO2 CHB [1:0] | | NCO1 CHB [1:0] | | NCO2 CHA [1:0] | | NCO1 CHA [1:0] | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-54. Register 0x3B Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | NCO2 CHB [1:0] | R/W | 00 | This register is used when selecting the NCO frequency for channel B, band 2 with the SPI interface in dual band DDC mode. |
| 5-4 | NCO1 CHB [1:0] | R/W | 00 | This register is used when selecting the NCO1 of channel B with the SPI interface. |
| 3-2 | NCO2 CHA [1:0] | R/W | 00 | This register is used when selecting the NCO frequency for channel A, band 2 with the SPI interface in dual band DDC mode. |
| 1-0 | NCO1 CHA [1:0] | R/W | 00 | This register is used when selecting the NCO1 of channel A with the SPI interface. |

**Figure 7-53. Register 0x41 (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NCO2 CHD [1:0] | | NCO1 CHD [1:0] | | NCO2 CHC [1:0] | | NCO1 CHC [1:0] | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-55. Register 0x41 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-6 | NCO2 CHD [1:0] | R/W | 00 | This register is used when selecting the NCO frequency for channel D, band 2 with the SPI interface in dual band DDC mode. |
| 5-4 | NCO1 CHD [1:0] | R/W | 00 | This register is used when selecting the NCO1 of channel D with the SPI interface. |
| 3-2 | NCO2 CHC [1:0] | R/W | 00 | This register is used when selecting the NCO frequency for channel C, band 2 with the SPI interface in dual band DDC mode. |
| 1-0 | NCO1 CHC [1:0] | R/W | 00 | This register is used when selecting the NCO1 of channel C with the SPI interface. |

**Figure 7-54. Register 0x22F (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 1 | SYSREF X5 | SYSREF X4 | SYSREF X3 | SYSREF X2 | SYSREF X1 | SYSREF OR | 1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-56. Register 0x22F Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 1 | R/W | 1 | Must write 1 |
| 6-2 | SYSREF X1..5 | R/W | 0 | These bits are the XOR flags from the SYSREF window monitoring circuitry. The sampling clock gets delayed internally by ~ 160 ps and used to capture the SYSREF signal. If a SYSREF signal transition happens within +/- 50 ps of the SYSREF capture the appropriate XOR flag gets raised. These bits are not sticky - they get overwritten with the next SYSREF rising edge.<br>X1: Window from 110 ps to 135 ps after the rising sampling clock edge<br>X2: Window from 135 ps to 160 ps after the rising sampling clock edge<br>X3: Window from 160 ps to 176 ps after the rising sampling clock edge<br>X4: Window from 176 ps to 192 ps after the rising sampling clock edge<br>X5: Window from 192 ps to 208 ps after the rising sampling clock edge<br>0: No SYSREF transition detected<br>1: SYSREF transition detected within given window |
| 1 | SYSREF OR | R/W | 0 | This bit is the output of the five SYSREF XOR flags logically OR'ed together.<br>0: no SYSREF flag raised<br>1: one of the five SYSREF XOR flags is raised. |
| 0 | 1 | R/W | 1 | Must write 1 |

**Figure 7-55. Register 0x234 (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | NCO SEL MODE | | 0 | 0 | GPIO MODE | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-57. Register 0x234 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6-5 | NCO SEL MODE | R/W | 00 | These bits select control of the NCO selection in complex decimation.<br>0: NCO selection using GPIO pins (GPIO MODE (D2-D0) needs to be set accordingly)<br>2: GPIO1/2 pins are used as a fast serial interface to only up NCO selection for each digital mixer<br>others: not used |
| 4-3 | 0 | R/W | 0 | Must write 0 |
| 2-0 | GPIO MODE | R/W | 000 | This register sets the functionality of the two GPIO pins<br>0: GPIO pins are used as SYNC input (LVDS), GPIO1 = SYNCP, GPIO2 = SYNCM<br>1: GPIO1 is used as SYNC input (CMOS)<br>3: Both GPIO pins are used to select NCOs for the decimation filters<br>4: GPIO1 is used to disable the calibration<br>5: GPIO1 is used as start of SYSREF counter<br>others: not used |

**Figure 7-56. Register 0x235 (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | NCO SEL SOURCE | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-58. Register 0x235 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | NCO SEL SOURCE | R/W | 0 | This register works in conjuction with NCO SEL MODE (0x234). 0x00: NCO selection other than regular SPI (GPIO, Fast SPI etc) 0xFF: NCO selection using regular SPI with addresses 0x3B/41. |

**Figure 7-57. Register 0x236 (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | GPIO2 INV | GPIO1 INV | GPIO SWAP | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-59. Register 0x236 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6 | GPIO2 INV | R/W | 0 | This bit inverts polarity of the GPIO2 pin 0: Polarity as is 1: Polarity inverted |
| 5 | GPIO1 INV | R/W | 0 | This bit inverts polarity of the GPIO1 pin 0: Polarity as is 1: Polarity inverted |
| 4 | GPIO SWAP | R/W | 0 | This bit swaps GPIO1 and GPIO2 pins internally. 0: Normal operation 1: GPIO1 and GPIO2 are swapped |
| 3-0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-58. Register 0x238 (DIGITAL page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | OVR OUTPUT CFG | | | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-60. Register 0x238 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | OVR OUTPUT CFG | R/W | 0000 | This bit configures if the overrange indication (OVR) is output on JESD output stream or on GPIO pins 0000: OVR on JESD 1111: OVR on GPIO |
| 3-0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-59. Register 0x20 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | K | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-61. Register 0x20 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | K | R/W | 00000000 | This is JESD204B parameter K which sets number of frames in a multi-frame. Bit value is set as K minus 1. |

**Figure 7-60. Register 0x21 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SYNC SPI EN | SYNC SPI | 0 | 0 | SYSREF MODE | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-62. Register 0x21 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6 | SYNC SPI EN | R/W | 0 | This bit enables JESD SYNC control using SPI (ignoring SYNC using GPIO1/2 pins) using bit D5 (SYNC SPI).<br>0: SPI SYNC disabled<br>1: SPI SYNC (using register bit D5) enabled |
| 5 | SYNC SPI | R/W | 0 | This bit enables JESD SYNC. SYNC control via SPI must be enabled also (D6).<br>0: ADC outputs data (SYNC disabled)<br>1: SYNC enabled (ADC outputs K28.5 characters for JESD interface synchronization) |
| 4-3 | 0 | R/W | 0 | Must write 0 |
| 2-0 | SYSREF MODE | R/W | 000 | This register controls how the ADC processes incoming SYSREF pulses.<br>0: Ignore all SYSREF pulses<br>1: Use all SYSREF pulses<br>2: Don't use SYSREF pulses<br>3: Skip one SYSREF pulse then use only the next one<br>4: Skip one SYSREF pulse then use all pulses<br>5: Skip two SYSREF pulses and then use one<br>6: Skip two SYSREF pulses and then use all |

**Figure 7-61. Register 0x22 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| JESD MODE | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-63. Register 0x22 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7:0 | JESD MODE | R/W | 00000000 | This register sets the LMFS configuration<br>1: LMFS = 8-2-2-4<br>2: LMFS = 8-4-8-10 (also bit DROP LSB in 0x27 needs to be set)<br>3: LMFS = 8-4-2-2<br>4: LMFS = 8-16-4-1<br>5: LMFS = 4-16-8-1<br>6: LMFS = 2-16-16-1<br>7: LMFS = 1-16-32-1<br>8: LMFS = 8-8-2-1<br>9: LMFS = 4-8-4-1<br>10: LMFS = 2-8-8-1<br>11: LMFS = 1-8-16-1<br>12: LMFS = 4-4-2-1<br>13: LMFS = 2-4-4-1<br>14: LMFS = 1-4-8-1<br>others: not used |

**Figure 7-62. Register 0x24 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | DDC CLK DIV | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-64. Register 0x24 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DDC CLK DIV | R/W | 00000000 | This register sets the internal clock divider when using the decimation filter. See Table 7-66 |

**Figure 7-63. Register 0x25 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | JESD TX CLK DIV | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-65. Register 0x25 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | JESD TX CLK DIV | R/W | 0000000 | This register sets the internal clock divider for the selected LMFS output mode. See Table 7-66 |

**Table 7-66. Register settings for 0x24/0x25 based on bypass/decimation and LMFS mode**

| LMFS | 0x24 (DDC CLK DIV) | | | | | | | 0x25 (JESD TX CLK DIV) | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | BYP | /4 | /8 | /16 | /32 | /64 | /128 | BYP | /4 | /8 | /16 | /32 | /64 | /128 |
| 8-4-8-10 | 1 | | | | | | | 4 | | | | | | |
| 8-4-2-2 | 1 | | | | | | | 0 | | | | | | |
| 4-4-2-1 | 3 | | | | | | | 0 | | | | | | |
| 8-8-2-1 | | 0 | 0 | 0 | 0 | 0 | 0 | | 0 | 0 | 0 | 0 | 0 | 0 |
| 8-16-4-1 | | | 1 | 1 | 1 | 1 | 1 | | | 0 | 0 | 0 | 0 | 0 |
| 4-8-4-1 | | 1 | 1 | 1 | 1 | 1 | 1 | 0 | | 0 | 0 | 0 | 0 | 0 |
| 4-16-8-1 | | | 3 | 3 | 3 | 3 | 3 | | | 0 | 0 | 0 | 0 | 0 |
| 2-8-8-1 | | 3 | 3 | 3 | 3 | 3 | 3 | 0 | | 0 | 0 | 0 | 0 | 0 |
| 2-16-16-1 | | | 7 | 7 | 7 | 7 | 7 | | | 0 | 0 | 0 | 0 | 0 |
| 1-8-16-1 | | | 7 | 7 | 7 | 7 | 7 | | | 0 | 0 | 0 | 0 | 0 |
| 1-16-32-1 | | | 15 | 15 | 15 | 15 | 15 | | | 0 | 0 | 0 | 0 | 0 |

**Figure 7-64. Register 0x27 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | DROP LSB | 0 | 0 | 0 | CLK BAL EN | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-67. Register 0x27 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | R/W | 0 | Must write 0 |
| 5 | DROP LSB | R/W | 0 | This register needs to be set when using the 12-bit output LMFS mode.<br>0: Drop LSB disabled<br>1: Drop LSB enabled when using LMFS = 8-4-8-10 |
| 4-2 | 0 | R/W | 0 | Must write 0 |
| 1 | CLK BAL EN | R/W | 0 | This register bit needs to be enabled in bypass mode LMFS = 8-4-2-2 only in order to improve some internal clock balancing.<br>0: CLK BAL disabled<br>1: CLK BAL EN. Set for LMFS = 8-4-2-2 |

**Table 7-67. Register 0x27 Field Descriptions (continued)**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-65. Register 0x28 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | JESD LANE EN | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-68. Register 0x28 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-0 | JESD LANE EN | R/W | 11111111 | This register turns on individual output lanes<br>0: Lane powered down<br>1: Serdes lane enabled<br>D0: Lane DOUT0<br>D1: Lane DOUT1<br>...<br>D7: Lane DOUT7 |

**Figure 7-66. Register 0x2B (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SYNC INV |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-69. Register 0x2B Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-1 | 0 | R/W | 0 | Must write 0 |
| 0 | SYNC INV | R/W | 0 | This register inverts the polarity from external SYNC pin<br>0: Polarity as is<br>1: Polarity inverted |

**Figure 7-67. Register 0x2D (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | | JESD SEQ SEL | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-70. Register 0x2D Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-3 | 0 | R/W | 0 | Must write 0 |
| 2-0 | JESD SEQ SEL | R/W | 000 | This register selects the JESD test pattern sequence<br>0: Test sequence disabled<br>1: Repeat D21.5 high frequency pattern for random jitter (RJ)<br>2: Repeat K28.5 mixed frequency pattern for deterministic jitter (DJ)<br>3: Repeat initial lane alignment (ILA) sequence<br>4: Modified random pattern<br>5: Scrambled jitter pattern<br>6: Repeat K28.7 low frequency pattern<br>7: Short test pattern |

Product Folder Links: *ADC34RF52*

**Figure 7-68. Register 0x2E (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| RAMP INCR | | | | 0 | RAMP EN | ALT PAT | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-71. Register 0x2E Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7-4 | RAMP INCR | R/W | 0000 | This register value sets the increment step size for the ramp pattern on 16-bit output. The step size is RAMP INCR plus 1. |
| 3 | 0 | R/W | 0 | Must write 0 |
| 2 | RAMP EN | R/W | 0 | Enables RAMP output pattern in the TRANSPORT LAYER. |
| 1 | ALT PAT | R/W | 0 | Enables a toggle pattern switching between 0x0000 and 0xFFFF in the TRANSPORT LAYER |
| 0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-69. Register 0x2F (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | SERDES PRBS | | SERDES PRBS EN | 0 | JESD PRBS | | JESD PRBS EN |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-72. Register 0x2F Field Descriptions**

| Bit | Field | Type | Reset | Description |
|-----|-------|------|-------|-------------|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6-5 | SERDES PRBS | R/W | 0 | This register selects the PRBS pattern in the LINK LAYER (no 8b/10b encoding). PRBS pattern must be enabled (D4).<br>0: PRBS $2^7$-1<br>1: PRBS $2^{15}$-1<br>2: PRBS $2^{23}$-1<br>3: PRBS $2^{31}$-1 |
| 4 | SERDES PRBS EN | R/W | 0 | This register enables PRBS test pattern in the LINK LAYER<br>0: Test pattern mode disabled<br>1: PRBS test pattern mode enabled |
| 3 | 0 | R/W | 0 | Must write 0 |
| 2-1 | JESD PRBS | R/W | 0 | This register selects the PRBS pattern in the TRANSPORT LAYER (test pattern will be 8b/10b encoded). PRBS pattern must be enabled (D0).<br>0: PRBS $2^7$-1<br>1: PRBS $2^{15}$-1<br>2: PRBS $2^{23}$-1<br>3: PRBS $2^{31}$-1 |
| 0 | JESD PRBS EN | R/W | 0 | This register enables PRBS test pattern in the TRANSPORT LAYER<br>0: Test pattern mode disabled<br>1: PRBS test pattern mode enabled |

Product Folder Links: *ADC34RF52*

**Figure 7-70. Register 0x30/32/34/36/40/42/44/46 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| START VALUE JESD RAMP DOUT0/1/2/3/4/5/6/7 | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-73. Register 0x30/32/34/36/40/42/44/46 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | START VALUE JESD RAMP DOUT0/1/2/3/4/5/6/7 | R/W | 00000000 | The JESD RAMP test pattern is designed to act as an individual RAMP pattern on each output lane. If the starting value on each lane is set to 0 (default) each output lane shows the same RAMP code at any given time. The RAMP pattern can be configured such that the RAMP pattern is constructed across JESD output lanes using the start value registers. DOUT1=1, DOUT2=2, DOUT3=3, DOUT4=0, DOUT5=1, DOUT6=2 and DOUT7=3 as well as the RAMP increment to 4 (RAMP INCR (0x2E) = 0x30) results in a RAMP pattern across lanes for each channel in bypass mode. |

**Figure 7-71. Register 0x53 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| SCR EN | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-74. Register 0x53 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | SCR EN | R/W | 0 | Enables scrambling of the JESD output data<br>0: Output scrambling disabled<br>1: Output scrambling enabled |
| 6-0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-72. Register 0x5C (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| F in ILA | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-75. Register 0x53 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | F in ILA | R/W | 0 | These bits set F in the ILA sequence. Register value is actual F value -1 (0x01 = F(2)). |

Product Folder Links: *ADC34RF52*

**Figure 7-73. Register 0x5D (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | K in ILA | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-76. Register 0x5D Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | K in ILA | R/W | 0 | These bits set K in the ILA sequence. Register value is actual K value -1 (0x0F = K(15)) |

**Figure 7-74. Register 0x7A (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| | | | JESD LANE POL INV | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-77. Register 0x7A Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | JESD LANE POL INV | R/W | 00000000 | This register inverts the polarity of the individual SERDES output lanes. Register bit D0 corresponds to SERDES lane DOUT0, D1 to DOUT1 etc<br>0: Output polarity as is<br>1: Output polarity inverted |

**Figure 7-75. Register 0x80/81/82/83 (JESD page)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0x80 | 0 | | LANE DOUT1 SEL | | 0 | | LANE DOUT0 SEL | |
| 0x81 | 0 | | LANE DOUT3 SEL | | 0 | | LANE DOUT2 SEL | |
| 0x82 | 0 | | LANE DOUT5 SEL | | 0 | | LANE DOUT4 SEL | |
| 0x83 | 0 | | LANE DOUT7 SEL | | 0 | | LANE DOUT6 SEL | |
| | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-78. Register 0x80/81/82/83 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7,3 | 0 | R/W | 0 | Must write 0 |
| 6-4 | LANE DOUT1/3/5/7 SEL | R/W | 000 | These register bits control the output mux. Any physical serdes output lane (DOUTx) can be connected to any JESD digital stream. By default lane DOUT0 is connected to JESD stream 0, lane DOUT1 to JESD stream 1 etc.<br>0: JESD stream 0<br>1: JESD stream 1<br>...<br>7: JESD stream 7 |
| 2-0 | LANE DOUT0/2/4/6 SEL | R/W | 000 | |

**Figure 7-76. Register 0x84 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | JESD PLL FACTOR | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-79. Register 0x84 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-2 | 0 | R/W | 0 | Must write 0 |
| 1-0 | JESD PLL FACTOR | R/W | 00 | This register bit must be set for 12-bit output LMFS = 8-4-8-10 only.<br>0: all other JESD LMFS modes<br>1: Set for LMFS = 8-4-8-10 |

**Figure 7-77. Register 0x89/8A/8B/8C/8D/8E/8F/90 (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| TX EMPH DOUT1 [0] | TX EMPH DOUT0 [5:0] | | | | | | 0 |
| 0 | 0 | 0 | TX EMPH DOUT1 [5:1] | | | | |
| TX EMPH DOUT3 [0] | TX EMPH DOUT2 [5:0] | | | | | | 0 |
| 0 | 0 | 0 | TX EMPH DOUT3 [5:1] | | | | |
| TX EMPH DOUT5 [0] | TX EMPH DOUT4 [5:0] | | | | | | 0 |
| 0 | 0 | 0 | TX EMPH DOUT5 [5:1] | | | | |
| TX EMPH DOUT7 [0] | TX EMPH DOUT6 [5:0] | | | | | | 0 |
| 0 | 0 | 0 | TX EMPH DOUT7 [5:1] | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-80. Register 0x89/8A/8B/8C/8D/8E/8F/90 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-5,0 | 0 | R/W | 0 | Must write 0 |
| 6-1 | TX EMPH DOUT0/2/4/6 [5:0] | R/W | 000000 | These bits select the amount of de-emphasis for the JESD output transmitter. The de-emphasis value in dB is measured as the ratio between the peak value after the signal transition to the settled value of the voltage in one bit period.<br>0: 0 dB<br>1: –1 dB<br>3: –2 dB<br>7: –4.1 dB<br>15: –6.2 dB<br>31: –8.2 dB<br>63: –11.5 dB |
| 4-0,7 | TX EMPH DOUT1/3/5/7 [5:0] | R/W | 000000 | |

**Figure 7-78. Register 0x9D/9E (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| PD DOUT7 [0,1] | PD DOUT6 [0,1] | PD DOUT5 [0,1] | PD DOUT4 [0,1] | PD DOUT3 [0,1] | PD DOUT2 [0,1] | PD DOUT1 [0,1] | PD DOUT0 [0,1] |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-81. Register 0x9D/9E Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | PD DOUTx [0,1] | R/W | 0 | Register 0x9D and 0x9E allow power down of individual serdes output lanes. Register 0x9D (PD DOUTx [0]) covers the output driver, 0x9E (PD DOUTx [1]) covers the associated internal high-speed data clock.<br>0: Output lane enabled<br>1: Output lane powered down |

Product Folder Links: *ADC34RF52*

**Figure 7-79. Register 0x9F (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | JESD PLL1 | | | 0 | JESD PLL2 | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-82. Register 0x9F Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6-4 | JESD PLL1 | R/W | 000 | Internal JESD PLL input divider setting. See Table 7-84 how to configure it for the different decimation and LMFS settings. |
| 3 | 0 | R/W | 0 | Must write 0 |
| 2-0 | JESD PLL2 | R/W | 000 | Internal JESD PLL input divider setting. See Table 7-84 how to configure it for the different decimation and LMFS settings. |

**Figure 7-80. Register 0xA0/A1/A2 (JESD page)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0xA0 | 0 | JESD PLL INPUT1 | | | 0 | 0 | 0 | 0 |
| 0xA1 | 0 | JESD PLL INPUT2 | | | 0 | 0 | 0 | 0 |
| 0xA2 | 0 | 0 | 0 | 0 | JESD PLL INPUT3 | | | 0 |
| | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-83. Register 0xA0/A1/A2 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | 0 | R/W | 0 | Must write 0 |
| 6-4 | JESD PLL INPUT1/2 | R/W | 000 | Internal JESD PLL input divider setting. See Table 7-84 how to configure it for the different decimation and LMFS settings. |
| 3-1 | JESD PLL INPUT3 | R/W | 000 | Internal JESD PLL input divider setting. See Table 7-84 how to configure it for the different decimation and LMFS settings. |

**Table 7-84. Register settings for 0x9F/A0/A1/A2 based on bypass/decimation and LMFS mode**

| | JESD PLL1/2, JESD PLL INPUT 2 | | | | | | | JESD PLL INPUT 1 | | | | | | | JESD PLL INPUT 3 | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LMFS | BYP | /4 | /8 | /16 | /32 | /64 | /128 | BYP | /4 | /8 | /16 | /32 | /64 | /128 | BYP | /4 | /8 | /16 | /32 | /64 | /128 |
| 8-4-8-10 | 0 | | | | | | | 0 | | | | | | | 1 | | | | | | |
| 8-4-2-2 | 0 | | | | | | | 0 | | | | | | | 1 | | | | | | |
| 4-4-2-1 | 0 | | | | | | | 0 | | | | | | | 3 | | | | | | |
| 8-8-2-1 | | 0 | 1 | 2 | 3 | 4 | 5 | | 0 | 1 | 2 | 3 | 4 | 5 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| 8-16-4-1 | | | 0 | 1 | 2 | 3 | 4 | | 0 | 0 | 1 | 2 | 3 | 4 | | | 0 | 0 | 0 | 0 | 0 |
| 4-4-2-1 | | 0 | 1 | 2 | 3 | 4 | 5 | | 0 | 1 | 2 | 3 | 4 | 5 | | 0 | 0 | 0 | 0 | 0 | 0 |
| 4-8-4-1 | | 0 | 0 | 1 | 2 | 3 | 4 | | 0 | 0 | 1 | 2 | 3 | 4 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 4-16-8-1 | | | 0 | 0 | 1 | 2 | 3 | | 0 | 0 | 0 | 1 | 2 | 3 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| 2-8-8-1 | | 0 | 0 | 0 | 1 | 2 | 3 | | 0 | 0 | 0 | 1 | 2 | 3 | 3 | 1 | 0 | 0 | 0 | 0 | 0 |
| 2-16-16-1 | | | 0 | 0 | 0 | 1 | 2 | | 0 | 0 | 0 | 0 | 1 | 2 | | 3 | 1 | 0 | 0 | 0 | 0 |
| 1-8-16-1 | | | 0 | 0 | 0 | 1 | 2 | | | 0 | 0 | 0 | 1 | 2 | | 3 | 1 | 0 | 0 | 0 | 0 |
| 1-16-32-1 | | | | 0 | 0 | 0 | 1 | | | 0 | 0 | 0 | 1 | | | | 3 | 1 | 0 | 0 | 0 |

Product Folder Links: ADC34RF52

**Figure 7-81. Register 0xED (JESD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | JESD DDC BYP | | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-85. Register 0xED Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | R/W | 0 | Must write 0 |
| 5-4 | JESD DDC BYP | R/W | 00 | This register needs to be set for the internal JESD frame assembly in DDC bypass output mode:<br>0: Any DDC mode<br>1: LMFS = 8-4-2-2 or 8-4-8-10<br>2: LMFS = 4-4-2-1 |
| 3-0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-82. Register 0x100..0x17D (DDCAB/CD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| NCOx FREQUENCYx [7:0],[15:8],[23:16],[31:24],[39:32],[47:40] | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-86. Register 0x100..0x17D Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 47:0 | NCOx CHAB/CD FREQUENCYx | R/W | 0 | The frequencies for NCOs are located in addresses 0x100 to 0x17D. Each frequency is 48-bit and the MSB starts on the highest address. |

**Figure 7-83. Register 0x181 (DDCAB/CD page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | LOAD NCO | | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-87. Register 0x181 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | R/W | 0 | Must write 0 |
| 5-4 | LOAD NCO | R/W | 00 | This register loads all the NCO frequencies from the memory to the NCOs. To update the NCO this register has to be set to 3 and back to 0 as shown in Table 7-88 |
| 3-0 | 0 | R/W | 0 | Must write 0 |

**Table 7-88. NCO frequency programming example**

| ADDR | DATA | DESCRIPTION |
|---|---|---|
| 0x105 | 0x4E | Frequency = 460 MHz with $F_S$ = 1.3 GSPS<br>99,598,837,913,001 = 0x5A95A95A95A9 where the MSB goes to address 0x105 and the LSB to 0x100. |
| 0x104 | 0x81 | |
| 0x103 | 0xB4 | |
| 0x102 | 0xE8 | |
| 0x101 | 0x1B | |
| 0x100 | 0x4E | |
| 0x181 | 0x00 | Load and update all NCO frequencies |
| 0x181 | 0x30 | |

**Figure 7-84. Register 0x34 (CALIBRATION page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | AVG SEL (2) | | 1 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-89. Register 0x34 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-3 | 0 | R/W | 0 | Must write 0 |
| 2-1 | AVG SEL (2) | R/W | 00 | Selects ADC averaging. Also AVG SEL (1) in DIGITAL page needs to be set.<br>0: no average<br>01: 2 ADC average<br>10/11: not used |
| 0 | 1 | R/W | 1 | Must write 1 |

**Figure 7-85. Register 0x45 (CALIBRATION page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| CAL SPI | CAL GPIO | 0 | 0 | 1 | 0 | 1 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-90. Register 0x45 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | CAL SPI | R/W | 0 | This register triggers the calibration using SPI write. It needs to be toggled (0=>1=>0). |
| 6 | CAL GPIO | R/W | 0 | This register triggers the calibration using the GPIO1 pin. |
| 5-4 | 0 | R/W | 0 | Must write 0 |
| 3 | 1 | R/W | 1 | Must write 1 |
| 2 | 0 | R/W | 0 | Must write 0 |
| 1 | 1 | R/W | 1 | Must write 1 |
| 0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-86. Register 0x298 (CALIBRATION page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | CAL STATUS | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-91. Register 0x298 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-4 | 0 | R/W | 0 | Must write 0 |
| 3-0 | CAL STATUS | R/W | 0000 | This register can be used to check if calibration state machine has finished without any errors. A value of 0xE indicates successful calibration. |

Product Folder Links: *ADC34RF52*

**Figure 7-87. Register 0x7B (ANALOG page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | TERM AB | 0 | 0 | 0 | 0 | TERM AB |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-92. Register 0x7B Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | R/W | 0 | Must write 0 |
| 5,0 | TERM AB | R/W | 00 | This register sets the internal termination resistor at the analog inputs for channel A and B.<br>0: 100 ohm differential termination<br>1: 50 ohm differential termination |
| 4-1 | 0 | R/W | 0 | Must write 0 |

**Figure 7-88. Register 0x8B (ANALOG page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | TERM CD | 0 | 0 | 0 | 0 | TERM CD |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-93. Register 0x8B Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-6 | 0 | R/W | 0 | Must write 0 |
| 5,0 | TERM CD | R/W | 00 | This register sets the internal termination resistor at the analog inputs for channel C and D.<br>0: 100 ohm differential termination<br>1: 50 ohm differential termination |
| 4-1 | 0 | R/W | 0 | Must write 0 |

**Figure 7-89. Register 0xA8 (ANALOG page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DITH AMP1 | | | | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-94. Register 0xA8 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6-3 | DITH AMP1 | R/W | 0000 | This register sets dither amplitude coarse gain. There are two recommended settings:<br>0000: Amplitude = 0<br>0011: Amplitude = 3<br>Here is a list of all the settings:<br>0000: Amplitude = 0 (smallest)<br>0001: Amplitude = 1<br>...<br>1110: Amplitude = 14<br>1111: Amplitude = 15 (largest) |
| 2-0 | 0 | R/W | 0 | Must write 0 |

Product Folder Links: *ADC34RF52*

**Figure 7-90. Register 0xAF (ANALOG page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DITHER DIS | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-95. Register 0xAF Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | DITHER DIS | R/W | 0 | This register disables internal dither.<br>0: Dither enabled<br>1: Dither disabled |
| 6-5 | 0 | R/W | 0 | Must write 0 |
| 4 | 1 | R/W | 0 | Must write 1 |
| 3-0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-91. Register 0xB1 (ANALOG page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| DITHER DIVIDER | | | | | | | |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-96. Register 0xB1 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | DITHER DIVIDER | R/W | 0 | This register sets the dither divider frequency. SPI write is actual -1. For example a divider of 48 is 47 (0x2F).<br>0x00 (default) is a divide /50 |

**Figure 7-92. Register 0xB4 (ANALOG page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 | 0 | SYSREF AC |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-97. Register 0xB4 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-1 | 0 | R/W | 0 | Must write 0 |
| 0 | SYSREF AC | R/W | 0 | This register enables external AC coupling of the SYSREF input with internal biasing.<br>0: External DC coupling with internal 100 Ω termination<br>1: External AC coupling with internal biasing |

Product Folder Links: *ADC34RF52*

**Figure 7-93. Register 0xCD (ANALOG page)**

| 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|
| 0 | DITH AMP2 | | | 0 | 0 | 0 | 0 |
| R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-98. Register 0xCD Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7 | 0 | R/W | 0 | Must write 0 |
| 6-4 | DITH AMP2 | R/W | 0 | This register sets dither amplitude fine gain. There are two recommended settings:<br>000: Amplitude = 0<br>100: Amplitude = -4<br>Here is a list of all the settings:<br>000: Amplitude = 0<br>001: Amplitude = 1<br>010: Amplitude = 2<br>011: Amplitude = 3 (largest)<br>100: Amplitude = -4 (smallest)<br>101: Amplitude = -3<br>110: Amplitude = -2<br>111: Amplitude = -1 |
| 5-0 | 0 | R/W | 0 | Must write 0 |

**Figure 7-94. Register 0xE6/E7 (ANALOG page)**

| ADDR | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---|---|---|---|---|---|---|---|---|
| 0xE6 | TX SWING [0] | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 0xE7 | 0 | 0 | 0 | 0 | 0 | 0 | TX SWING [2:1] | |
| | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |

**Table 7-99. Register 0xE6/E7 Field Descriptions**

| Bit | Field | Type | Reset | Description |
|---|---|---|---|---|
| 7-0 | 0 | R/W | 0 | Must write 0 |
| 1,0,7 | TX SWING [2:0] | R/W | 000 | This register adjusts the output amplitude on all 8 serdes lanes.<br>0: 850 mVpp<br>1: 825 mVpp<br>2: 800 mVpp<br>3: 775 mVpp<br>4: 950 mVpp<br>5: 925 mVpp<br>6: 900 mVpp<br>7: 875 mVpp |

# 8 Application Information Disclaimer

> **Note**
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

## 8.1 Application Information

The ADC34RF52 can be used in a wide range of applications including radar, frequency domain digitizer and spectrum analyzer, test and communications equipment and software-defined radios (SDRs). The Typical Applications section describe one configuration that meets the needs of a number of these applications.

## 8.2 Typical Application

### 8.2.1 Wideband RF Sampling Receiver
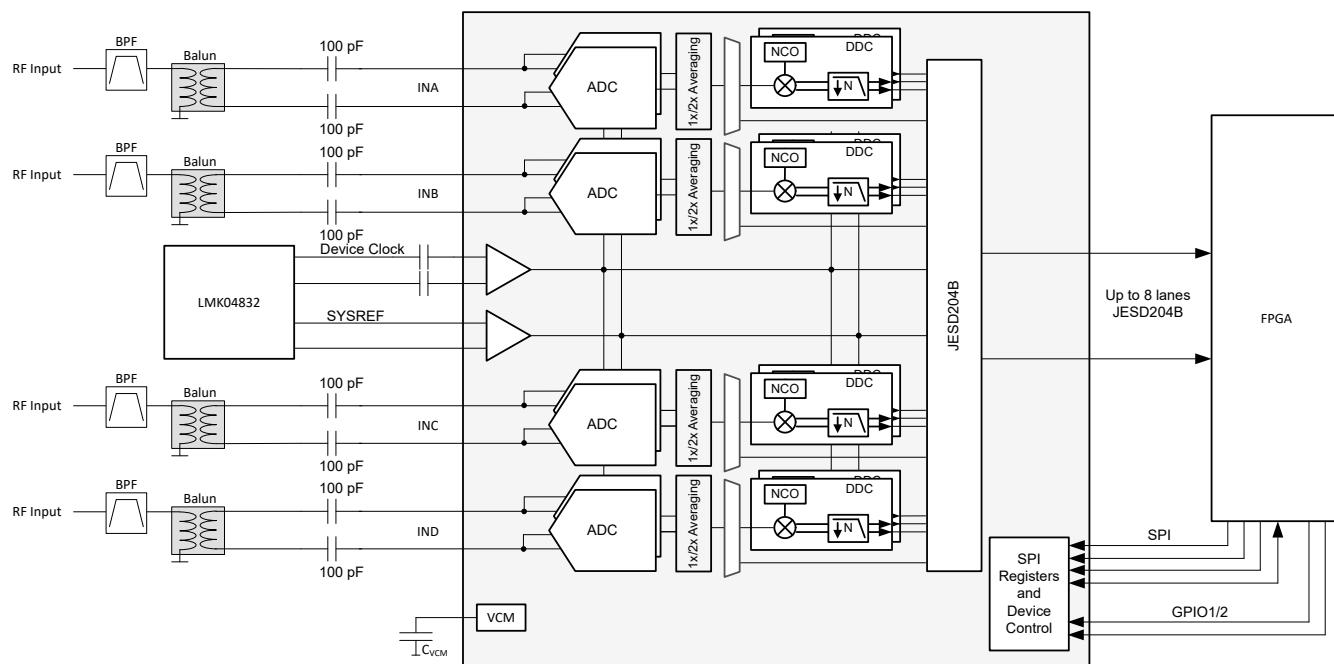


**Figure 8-1. Typical Configuration for Wideband RF Sampling**

### 8.2.2 Design Requirements

#### 8.2.2.1 Input Signal Path

Appropriate band limiting filters are be used to reject unwanted frequencies in the receive signal path.

A 1:2 (for 100 Ω effective termination impedance) or a 1:1 (for 50 Ω effective termination impedance) balun transformer is needed to convert the single ended RF input to differential for input to the ADC. The balun outputs can be AC coupled with 100 pF capacitors. The balun must have good amplitude (< 2 dB) and phase balance (less than 2 deg) within the frequency range of interest. A back-to-back balun configuration often times gives better SFDR performance. Table 8-1 lists a number of recommended baluns for different impedance ratios and frequency ranges.

The S-parameters of the ADC input can be used to design the front end matching network.

**Table 8-1. Recommended Baluns**

| PART NUMBER | MANURACTURER | IMPEDANCE RATIO | AMPLITUDE BALANCE (dB) | PHASE BALANCE (°) | FREQUENCY RANGE |
|---|---|---|---|---|---|
| BAL-0009SMG | Marki Microwave | 1:2 | 0.6 | 5 | 0.5 MHz to 9 GHz |
| TCM2-43X+ | Minicircuits | 1:2 | 0.5 | 7 | 10 MHz to 4 GHz |
| TCM2-33WX+ | Minicircuits | 1:2 | 0.7 | 4 | 10 MHz to 3 GHz |
| TC1-1-13M+ | Minicircuits | 1:1 | 0.5 | 2-3 | 10 MHz to 3 GHz |

### 8.2.2.2 Clocking

The ADC34RF52 clock inputs must be AC-coupled to the device to provide the rated performance. The clock source must have low jitter (integrated phase noise) for the ADC to meet the stated SNR performance, especially when operating at higher input frequencies. The clock signal needs to be filtered with a band pass filter to remove some of the broad band clock noise.

The JESD204B data converter system (ADC and FPGA) requires additional SYSREF and device clocks. The LMK04828 or LMK04832 devices are designed to generate these clocks. Depending on the ADC clock frequency and jitter requirements, the device can also be used as a system clock synthesizer or as a device clock and SYSREF distribution device when using multiple ADC34RF52 devices in a system.

### 8.2.3 Detailed Design Procedure

#### 8.2.3.1 Sampling Clock

To maximize the SNR performance of the ADC a low jitter (< 50 fs) sampling clock is required. Figure 8-2 shows the estimated SNR performance vs input frequency vs external clock jitter. The internal ADC aperture jitter also has some dependency to the clock amplitude (gets more sensitive with higher input frequency) as shown in Figure 8-3.

When using averaging and/or decimation, the SNR for a single ADC core is estimated before adding the SNR improvement from internal averaging and/or decimation.
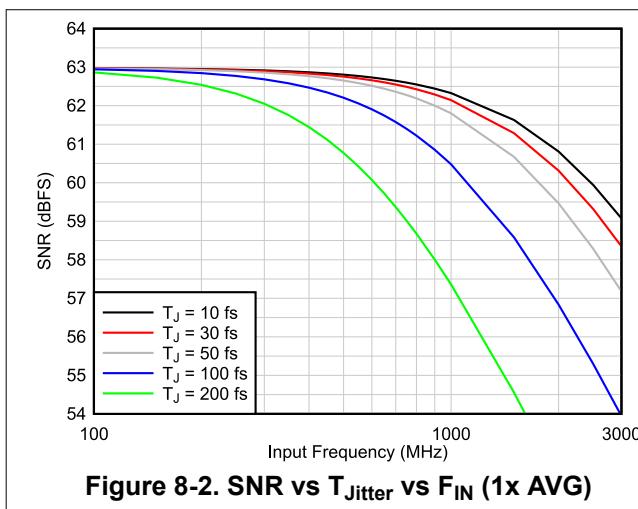


**Figure 8-2. SNR vs T$_{Jitter}$ vs F$_{IN}$ (1x AVG)**
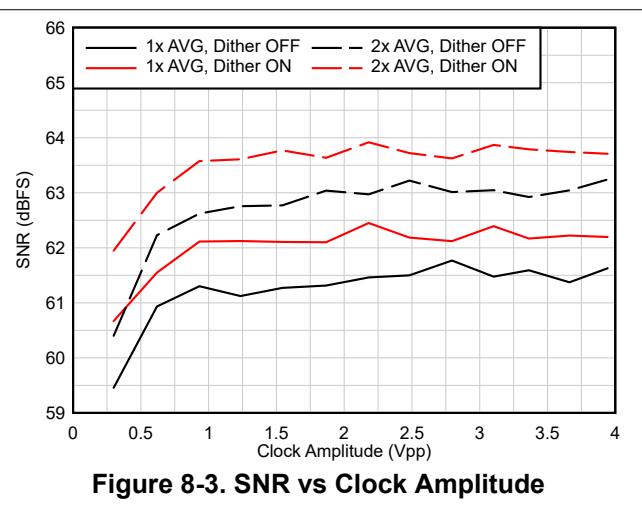


**Figure 8-3. SNR vs Clock Amplitude**

Product Folder Links: *ADC34RF52*

## 8.2.4 Application Curves

The following application curves demonstrate performance and results only of the ADC using a balun front end and configured to 2x internal averaging. The input frequency is 900 MHz ($F_S$ = 1.5 GSPS) and input amplitudes of -1/-4 and -20 dBFS are shown with dither enabled/disabled.
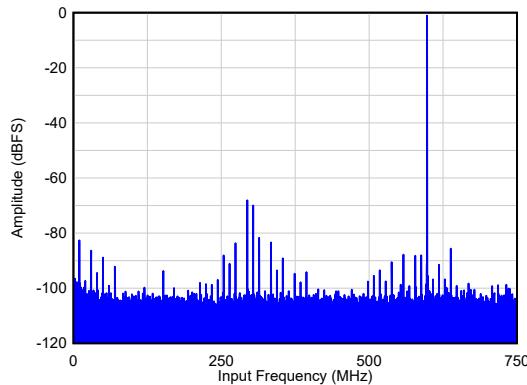


$A_{IN}$ = -1 dBFS, 2x AVG, Dither = DIS
SNR = 66.8 dBFS, HD23 = 67 dBc, Non HD23 = 82 dBFS

**Figure 8-4. Single Tone FFT at $F_{IN}$ = 900 MHz**
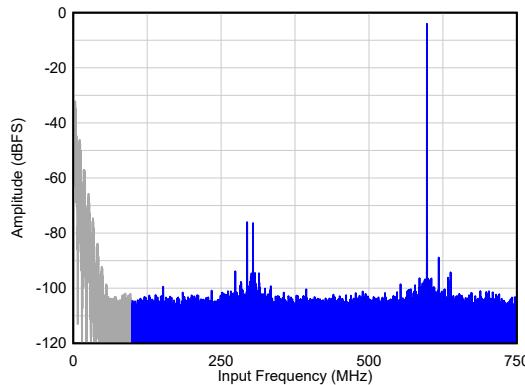


$A_{IN}$ = -4 dBFS, 2x AVG, Dither = EN
SNR = 67.0 dBFS[2], HD23 = 72 dBc, Non HD23 = 89 dBFS

**Figure 8-5. Single Tone FFT at $F_{IN}$ = 900 MHz**
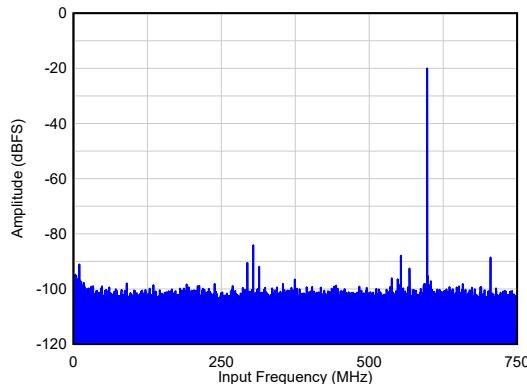


$A_{IN}$ = -20 dBFS, 1x AVG, Dither = DIS
SNR = 65.2 dBFS, HD23 = 64 dBc, Non HD23 = 88 dBFS

**Figure 8-6. Single Tone FFT at $F_{IN}$ = 900 MHz**
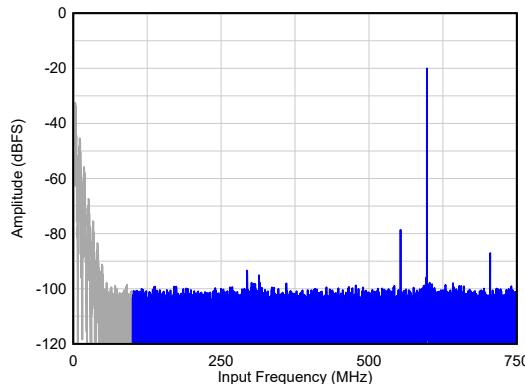


$A_{IN}$ = -20 dBFS, 1x AVG, Dither = EN
SNR = 64.8 dBFS[1], HD23 = 59 dBc, Non HD23 = 79 dBFS

**Figure 8-7. Single Tone FFT at $F_{IN}$ = 900 MHz**

[2] Measured from 100 MHz to $F_S$/2

## 8.3 Initialization Set Up

After power-up, the internal registers must be initialized to their default values through a hardware reset by applying a low pulse on the RESET pin, as shown in Figure 8-8.

1. Apply 1.2 V DVDD digital power supply
2. Apply remaining 1.2 V power supplies (AVDD12, CLKVDD), in no specific order
3. Apply 1.8 V AVDD18 power supply
4. Apply hardware reset. After hardware reset is released, the default registers are loaded from internal fuses.
5. Begin programming the internal registers using the SPI interface.
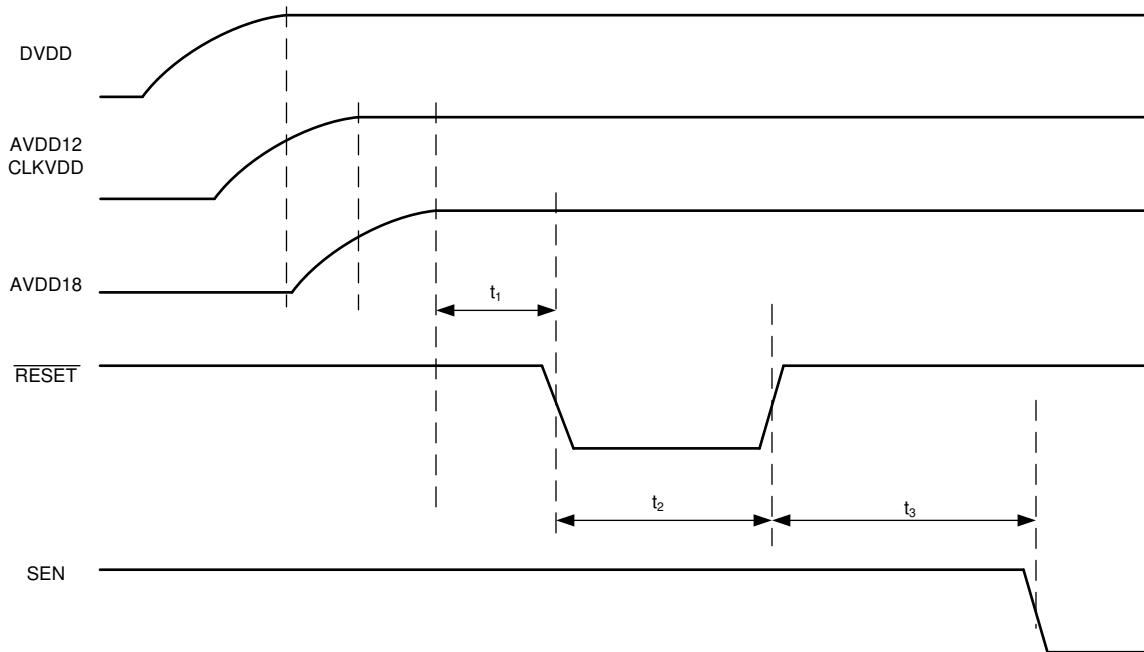


**Figure 8-8. Initialization of serial registers after power up**

**Table 8-2. Power-up timing**

|  |  | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $t_1$ | Power-on delay: delay from power up to active high RESET pulse | 1 |  |  | ms |
| $t_2$ | Reset pulse width: active low RESET pulse width | 100 |  |  | ns |
| $t_3$ | Register write delay: delay from RESET disable to SEN active | 45k |  |  | Clock cycles |

### 8.3.1 Initial Device Configuration After Power-Up

The following section outlines the sequence of register writes for the device configuration after initial power up.

**Table 8-3. Summary of programming steps after initial power up**

| Step | Section | Description |
|---|---|---|
| 1 | RESET | Hardware and software RESET to reset all registers to known state |
| 2 | DEVICE CONFIG | Configures the digital operating modes like averaging, test pattern output, input termination, internal dither and decimation. |
| 3 | JESD | Configures the JESD204B interface |
| 4 | SYSREF | Enables SYSREF input and resets internal circuits based on external SYSREF signal. |
| 5 | JESD | Clears and configures some of the JESD registers |
| 6 | TRIM | Set trim settings for best analog performance |
| 7 | CALIB CONFIG | Configure the calibration settings |
| 8 | SYSREF | Issue SYSREF for trim settings to go into effect |
| 9 | RUN CALIB | Run power up calibration |
| 10 | JESD | Synchronize the JESD interface with the receiver |

The following section outlines the detailed register writes for the device configuration after initial power up. This includes all the register writes (fields in gray) which are not documented in the register summary table. The register examples are given for 2x internal averaging, DDC bypass mode (LMFS = 8422).

### 8.3.1.1 STEP 1: RESET

After the initial power up both hardware and software reset are required.

**Table 8-4. Register programming sequence for software RESET**

| ADDRESS | DATA | DESCRIPTION |
|---|---|---|
| 0x00 | 0x01 | Software set and reset |
| 0x00 | 0x00 | |
| 0x01 | 0x00 | |
| 0x09 | 0x20 | These two resets are staggered to minimize strain on external power supply. |
| 0x09 | 0x80 | |
| 0x09 | 0x00 | |
| 0x08 | 0x01 | Internal memory reset (set and reset) |
| 0x08 | 0x00 | |
| 0x05 | 0x40 | Select ANALOG page |
| 0x47 | 0x80 | Analog reset (set and reset) |
| 0x47 | 0x00 | |

### 8.3.1.2 STEP 2: Device Configuration

In this step, the operating mode and digital features (DDC, test pattern) are configured.

**Table 8-5. Register programming sequence for device configuration**

| ADDRESS | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x20 | Select CALIBRATION page |
| 0x34 | 0x03 | Select 2x averaging (1x AVG: 0x01) |
| 0x05 | 0x02 | Select DIGITAL page |
| 0x2C | 0x01 | Select DDC Bypass mode |
| 0x2D | 0x00 | No decimation, step can be skipped |
| 0x2E | 0x0B | Select 2x averaging (1x: 0x09) |
| 0x23C | 0x07 | |
| 0x33 | 0x10 | |
| 0x2F | 0xE1 | Select 2x averaging (1x: 0x99, 2x: 0xE1) |
| 0x30 | 0xE1 | Select 2x averaging (1x: 0x99, 2x: 0xE1) |
| 0x05 | 0x40 | Select ANALOG page |
| 0x7B/8B | 0x00 | Select internal input termination (0x00 = 100 ohm) |
| 0xA8 | 0x00 | DITHER AMP1: 3 = 0x80, 0 = 0x00 |
| 0xCD | 0x00 | DITHER AMP2: -4 = 0x40, 0 = 0x00 |
| 0x04 | 0x01 | |
| 0x20 | 0x04 | |
| 0x91 | 0x40 | |
| 0xAF | 0x10 | |
| 0xB1 | 0x00 | Sets dither divider. 0x00 = /50 |
| 0xB2 | 0x00 | |
| 0xAF | 0x18 | |
| 0xAF | 0x10 | 0x10 = dither ENABLED, 0x90 = dither DISABLED |
| 0x04 | 0x01 | |
| 0x20 | 0x00 | |
| 0x04 | 0x00 | |
| 0x05 | 0x02 | |
| 0x363 | 0x01 | |
| 0x05 | 0x08 | Select DDCAB page, load non linearity correction (NLC) trims |
| 0x224 | 0x00 | |
| 0x223 | 0x00 | |
| 0x21D | 0x14 | |
| 0x21E | 0x11 | |
| 0x205 | 0x03 | |
| 0x204 | 0xFF | |
| 0x21A | 0x3C | |
| 0x31C | 0x3E | |
| 0x325 | 0x00 | |
| 0x325 | 0x01 | |
| 0x325 | 0x00 | |
| 0x21C | 0x00 | Nyquist zone 1: 0x00, other Nyquist zone 0x02 |
| 0x225 | 0x00 | |
| 0x225 | 0x01 | |

**Table 8-5. Register programming sequence for device configuration (continued)**

| ADDRESS | DATA | DESCRIPTION |
|---|---|---|
| 0x225 | 0x00 | |
| 0x05 | 0x10 | Select DDCCD page, load non linearity correction (NLC) trims |
| 0x224 | 0x00 | |
| 0x223 | 0x00 | |
| 0x21D | 0x14 | |
| 0x21E | 0x11 | |
| 0x205 | 0x03 | |
| 0x204 | 0xFF | |
| 0x21A | 0x3C | |
| 0x21C | 0x00 | Nyquist zone 1: 0x00, other Nyquist zone 0x02 |
| 0x31C | 0x3E | |
| 0x325 | 0x00 | |
| 0x325 | 0x01 | |
| 0x325 | 0x00 | |
| 0x225 | 0x00 | |
| 0x225 | 0x01 | |
| 0x225 | 0x00 | |
| 0x05 | 0x08 | |
| 0x20 | 0x02 | OVR MUX EN |
| 0x203 | 0x30 | |
| 0x303 | 0x30 | |
| 0x180 | 0x30 | |

### 8.3.1.3 STEP 3: JESD Interface Configuration (1)

In this step, the JESD204B digital interface and parameters are configured.

**Table 8-6. Register programming sequence for JESD204B interface configuration**

| ADDRESS | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x02 | Select DIGITAL page |
| 0x81 | 0x00 | |
| 0x80 | 0xFF | |
| 0x7F | 0xFF | |
| 0x7E | 0xFF | |
| 0x7D | 0xFF | |
| 0x7C | 0xFF | |
| 0x7B | 0x3B | |
| 0x7A | 0x28 | |
| 0x79 | 0x51 | |
| 0x78 | 0x40 | |
| 0x05 | 0x04 | Select JESD page |
| 0x23 | 0x03 | Set register to 0x03 |
| 0x29 | 0xFF | Set register to 0xFF |
| 0x20 | 0x0F | Select K (0x0F: K=15) |
| 0x21 | 0x01 | SYSREF mode |
| 0x22 | 0x03 | Select LMFS configuration (LMFS = 8-4-2-2) |
| 0x24 | 0x01 | Select DDC CLK DIV |
| 0x25 | 0x00 | Select JESD TX CLK DIV |
| 0x53 | 0x80 | Output scrambler EN/DIS (SCR EN) |
| 0x5C | 0x01 | F-1 in ILA (F=2) |
| 0x5D | 0x0F | K-1 in ILA (K=15) |
| 0x6E | 0x11 | |
| 0xA0 | 0x00 | Set JESD PLL INPUT1 = 0 Set JESD PLL INPUT2 = 0 Set JESD PLL INPUT3 = 1 |
| 0xA1 | 0x00 | |
| 0xA2 | 0x02 | |
| 0xED | 0x10 | Set JESD DDC BYP to 1 |
| 0x9F | 0x00 | Select JESD PLL setting |
| 0x2A | 0x0C | |
| 0x23 | 0x02 | JESD INIT toggle |
| 0x23 | 0x00 | |

Product Folder Links: *ADC34RF52*

### 8.3.1.4 STEP 4: SYSREF Synchronization

After device and JESD204B interface configuration, a synchronization using external SYSREF is necessary.

**Table 8-7. Device synchronization using external SYSREF**

| ADDRESS | DATA | DESCRIPTION |
|---------|------|-------------|
| 0x05 | 0x02 | Select DIGITAL page |
| 0x236 | 0x02 | Enable internal SYSREF input and clear SYSREF pulse counter |
| 0x236 | 0x03 | Starts SYSREF counter |

### 8.3.1.5 STEP 5: JESD Interface Configuration (2)

Some registers of the JESD204B interface must be set after the first SYSREF.

**Table 8-8. Register programming sequence for JESD204B interface configuration**

| ADDRESS | DATA | DESCRIPTION |
|---------|------|-------------|
| 0x05 | 0x04 | Select JESD page |
| 0x29 | 0x00 | |
| 0x84 | 0x00 | JESD PLL factor |

### 8.3.1.6 STEP 6: Analog Trim Settings

The following registers must be set for best analog performance. The register write order is all writes in first 2 columns before moving to the next set of address/data in middle columns and so on.

**Table 8-9. Analog Trim Setting Registers**

| ADDR | DATA | ADDR | DATA | COMMENT | ADDR | DATA | COMMENT |
|------|------|------|------|---------|------|------|---------|
| 0x05 | 0x40 | 0x3B | 0x0C | | 0x56 | 0x03 | |
| 0xE8 | 0xF0 | 0xA8 | 0x18 | Only for 1x AVG | 0x56 | 0x07 | |
| 0xE9 | 0x01 | 0xA8 | 0x00 | Only for 2x AVG, $F_S$<1.1 GSPS | 0x56 | 0x0F | |
| 0x4B | 0x1F | 0xA8 | 0x08 | Only for 2x AVG, $F_S$=1.1-1.5 GSPS | 0x6E | 0x08 | |
| 0x5B | 0x01 | 0xCD | 0x00 | | 0x102 | 0x02 | |
| 0xEA | 0x00 | 0xCE | 0x00 | | 0x103 | 0xD9 | |
| 0xEB | 0x03 | 0x100 | | See Table 8-10 for sample rate dependent trim registers | 0xA7 | 0x00 | |
| 0x95 | 0x00 | 0x101 | | | 0xA6 | 0x08 | |
| 0xFC | 0x28 | 0x104 | | | 0x05 | 0x20 | |
| 0xE0 | 0x8E | 0x105 | | | 0xC9 | 0x09 | |
| 0xE1 | 0x03 | 0x107 | 0x10 | | 0x102 | 0xFE | |
| 0x4C | 0x40 | 0x05 | 0x20 | | 0x103 | 0x03 | |
| 0x4E | 0x01 | 0x30 | 0xE8 | | 0x104 | 0xD4 | |
| 0x4E | 0x00 | 0x31 | 0xFF | | 0x105 | 0x03 | |
| 0xA1 | 0x01 | 0x30 | 0x08 | | 0x106 | 0xFE | |
| 0xF8 | 0x00 | 0x31 | 0x80 | | 0x107 | 0x03 | |
| 0x31 | 0x20 | 0x32 | 0x03 | | 0x108 | 0xBC | |
| 0xFD | 0x1C | 0x05 | 0x02 | | 0x109 | 0x1A | |
| 0xAA | 0x02 | 0x243 | 0x02 | | 0x101 | 0x01 | |
| 0x4D | 0x80 | 0x05 | 0x20 | | 0x159 | 0x63 | |
| 0xB3 | 0x30 | 0x36 | 0x04 | | 0x05 | 0x40 | |
| 0x64 | 0x10 | 0x1F8 | 0x01 | | 0x31 | 0x00 | |
| 0x62 | 0x12 | 0x1FC | 0x0A | | 0x4D | 0x00 | |
| 0xFE | 0x80 | 0x1F0 | 0x20 | | 0x62 | 0x10 | |

**Table 8-9. Analog Trim Setting Registers (continued)**

| ADDR | DATA | ADDR | DATA | COMMENT | ADDR | DATA | COMMENT |
|---|---|---|---|---|---|---|---|
| 0xFC | 0x28 | 0x1F1 | 0x0C | | 0x56 | 0x0E | |
| 0xFF | 0x14 | 0x05 | 0x40 | | 0x56 | 0x0C | |
| 0x106 | 0x00 | 0x39 | 0x40 | | 0x56 | 0x08 | |
| 0x107 | 0x00 | 0x56 | 0x01 | | 0x56 | 0x00 | |
| | | | | | 0x6E | 0x00 | |
| | | | | | 0xF8 | 0x06 | |

**Table 8-10. Sample rate dependent trim registers**

| $F_S$ (GSPS) | 0x100 | 0x101 | 0x104 | 0x105 |
|---|---|---|---|---|
| 0.6-0.7 | 0x48 | 0x00 | 0x01 | 0x01 |
| 0.7-0.9 | 0xC8 | 0x01 | 0x81 | 0x00 |
| 0.9-1.1 | 0x48 | 0x01 | 0x81 | 0x00 |
| 1.1-1.3 | 0xC8 | 0x00 | 0x81 | 0x00 |
| 1.3-1.5 | 0x48 | 0x00 | 0x81 | 0x00 |

### 8.3.1.7 STEP 7: Calibration Configuration

The following registers configure the internal foreground calibration. The register write order is all writes in first 2 columns before moving to the next set of address/data in middle columns and so on.

**Table 8-11. Calibration Register Settings**

| ADDRESS | DATA | ADDRESS | DATA | ADDRESS | DATA |
|---|---|---|---|---|---|
| 0x05 | 0x40 | 0xFC | 0x13 | 0x47 | 0xC7 |
| 0x68 | 0xC0 | 0xFD | 0x08 | 0x46 | 0x13 |
| 0x69 | 0xFF | 0x36 | 0x04 | 0xFC | 0x13 |
| 0x05 | 0x20 | 0x36 | 0x05 | 0xFD | 0x00 |
| 0x46 | 0x03 | 0x36 | 0x04 | 0x36 | 0x04 |
| 0x47 | 0xC2 | 0xFC | 0x13 | 0x36 | 0x05 |
| 0x46 | 0x13 | 0xFD | 0x0A | 0x36 | 0x04 |
| 0x1AE | 0x00 | 0x36 | 0x04 | 0xFC | 0x13 |
| 0x1E6 | 0x1C | 0x36 | 0x05 | 0xFD | 0x02 |
| 0x1AE | 0x00 | 0x36 | 0x04 | 0x36 | 0x04 |
| 0x1E6 | 0x1C | 0xFC | 0x13 | 0x36 | 0x05 |
| 0x1E9 | 0x08 | 0xFD | 0x0C | 0x36 | 0x04 |
| 0x1E9 | 0xA8 | 0x36 | 0x04 | 0xFC | 0x13 |
| 0x1E8 | 0x02 | 0x36 | 0x05 | 0xFD | 0x04 |
| 0x1E8 | 0x06 | 0x36 | 0x04 | 0x36 | 0x04 |
| 0x1E8 | 0x04 | 0xFC | 0x13 | 0x36 | 0x05 |
| 0x1E8 | 0x00 | 0xFD | 0x0E | 0x36 | 0x04 |
| 0x1E9 | 0xA0 | 0x36 | 0x04 | 0xFC | 0x13 |
| 0x1F0 | 0x28 | 0x36 | 0x05 | 0xFD | 0x06 |
| 0x1F1 | 0x0C | 0x36 | 0x04 | 0x36 | 0x04 |
| 0x1F0 | 0x2A | 0xFC | 0x03 | 0x36 | 0x05 |
| 0x1F0 | 0x2E | 0x36 | 0x04 | 0x36 | 0x04 |
| 0x1F0 | 0x2C | 0x46 | 0x03 | 0xFC | 0x13 |
| 0x1F0 | 0x28 | 0x47 | 0xC0 | 0xFD | 0x08 |
| 0x1F0 | 0x08 | 0x46 | 0x13 | 0x36 | 0x04 |
| 0x1F0 | 0x18 | 0x46 | 0x03 | 0x36 | 0x05 |

Product Folder Links: *ADC34RF52*

#### Table 8-11. Calibration Register Settings (continued)

| ADDRESS | DATA | ADDRESS | DATA | ADDRESS | DATA |
|---|---|---|---|---|---|
| 0x1F0 | 0x38 | 0x47 | 0xC7 | 0x36 | 0x04 |
| 0x1F1 | 0x0C | 0x46 | 0x13 | 0xFC | 0x13 |
| 0x1F0 | 0x3A | 0x1AE | 0x00 | 0xFD | 0x0A |
| 0x1F0 | 0x3E | 0x1E6 | 0x1C | 0x36 | 0x04 |
| 0x1F0 | 0x3C | 0x1AE | 0x00 | 0x36 | 0x05 |
| 0x1F0 | 0x38 | 0x1E6 | 0x1C | 0x36 | 0x04 |
| 0x1F0 | 0x18 | 0x1E9 | 0xA8 | 0xFC | 0x13 |
| 0x1F0 | 0x10 | 0x1E8 | 0x02 | 0xFD | 0x0C |
| 0x1AE | 0x00 | 0x1E8 | 0x06 | 0x36 | 0x04 |
| 0x1E6 | 0x1C | 0x1E8 | 0x04 | 0x36 | 0x05 |
| 0x1AE | 0x00 | 0x1E8 | 0x00 | 0x36 | 0x04 |
| 0x1E6 | 0x1C | 0x1E9 | 0xA0 | 0xFC | 0x13 |
| 0x47 | 0xC0 | 0x1F0 | 0x18 | 0xFD | 0x0E |
| 0x46 | 0x03 | 0x1F0 | 0x08 | 0x36 | 0x04 |
| 0x47 | 0xC2 | 0x1F0 | 0x28 | 0x36 | 0x05 |
| 0x46 | 0x13 | 0x1F1 | 0x0C | 0x36 | 0x04 |
| 0xFC | 0x13 | 0x1F0 | 0x2A | 0xFC | 0x03 |
| 0xFD | 0x00 | 0x1F0 | 0x2E | 0x36 | 0x04 |
| 0x36 | 0x04 | 0x1F0 | 0x2C | 0x46 | 0x03 |
| 0x36 | 0x05 | 0x1F0 | 0x28 | 0x47 | 0xC0 |
| 0x36 | 0x04 | 0x1F0 | 0x08 | 0x46 | 0x13 |
| 0xFC | 0x13 | 0x1F0 | 0x18 | 0x05 | 0x40 |
| 0xFD | 0x02 | 0x1F0 | 0x38 | 0x68 | 0x40 |
| 0x36 | 0x04 | 0x1F1 | 0x0C | 0x69 | 0xFD |
| 0x36 | 0x05 | 0x1F0 | 0x3A | 0x69 | 0xF5 |
| 0x36 | 0x04 | 0x1F0 | 0x3E | 0x69 | 0xD5 |
| 0xFC | 0x13 | 0x1F0 | 0x3C | 0x69 | 0x55 |
| 0xFD | 0x04 | 0x1F0 | 0x38 | 0x68 | 0x00 |
| 0x36 | 0x04 | 0x1F0 | 0x18 | 0x69 | 0x54 |
| 0x36 | 0x05 | 0x1F0 | 0x10 | 0x69 | 0x50 |
| 0x36 | 0x04 | 0x1AE | 0x00 | 0x69 | 0x40 |
| 0xFC | 0x13 | 0x1E6 | 0x1C | 0x69 | 0x00 |
| 0xFD | 0x06 | 0x1AE | 0x00 | 0x93 | 0x0E |
| 0x36 | 0x04 | 0x1E6 | 0x1C | 0x94 | 0x70 |
| 0x36 | 0x05 | 0x47 | 0xC0 | 0x94 | 0x77 |
| 0x36 | 0x04 | 0x46 | 0x03 | | |

### 8.3.1.8 STEP 8: SYSREF Synchronization

After setting the analog trim registers, a synchronization using external SYSREF is necessary.

#### Table 8-12. Device synchronization using external SYSREF

| ADDRESS | DATA | DESCRIPTION |
|---|---|---|
| 0x05 | 0x02 | Select DIGITAL page |
| 0x236 | 0x02 | Enable internal SYSREF input and clear SYSREF pulse counter |
| 0x236 | 0x03 | Starts SYSREF counter |

### 8.3.1.9 STEP 9: Run Power up Calibration

The following registers start the power up foreground calibration. The register write order is all writes in first 2 columns before moving to the next set of address/data in middle columns and so on.

#### Table 8-13. Calibration Register Settings

| ADDRESS | DATA | ADDRESS | DATA | ADDRESS | DATA |
|---------|------|---------|------|---------|------|
| 0x05 | 0x20 | 0x93 | 0x20 | 0x58 | 0x30 |
| 0xE7 | 0x01 | 0x20 | 0x00 | 0x58 | 0x20 |
| 0x174 | 0x02 | 0x05 | 0x00 | 0x58 | 0x00 |
| 0x178 | 0x00 | 0x04 | 0x01 | 0x89 | x020 |
| 0x17C | 0x22 | 0x20 | 0x1F | 0x95 | 0x00 |
| 0x3C | 0x00 | 0x93 | 0x20 | 0x96 | 0x00 |
| 0xFC | 0x03 | 0x04 | 0x01 | 0x97 | 0x10 |
| 0xFD | 0x00 | 0x20 | 0x00 | 0x9C | 0x00 |
| 0x154 | 0x1C | 0x04 | 0x00 | 0x57 | 0x1E |
| 0x155 | 0x03 | 0x05 | 0x20 | 0x46 | 0x02 |
| 0xFC | 0x03 | 0xC0 | 0x7C | 0x45 | 0x8A |
| 0xEE | 0x26 | 0xBC | 0x3C | 0x45 | 0x0A |
| 0xEF | 0x02 | 0xC9 | 0x01 | Delay 3 seconds | |
| 0x18C | 0x88 | 0xC9 | 0x00 | 0x89 | 0x00 |
| 0xAE | 0xC8 | 0xC9 | 0x06 | 0x95 | 0x00 |
| 0xAF | 0x00 | 0x38 | 0x01 | 0x96 | 0x00 |
| 0xB0 | 0x4C | 0x110 | 0x10 | 0x97 | 0x00 |
| 0xB1 | 0x3F | 0x111 | 0x42 | 0x9C | 0x00 |
| 0x4F | 0x46 | 0x112 | 0xA6 | 0x57 | 0x1A |
| 0x50 | 0x2C | 0x112 | 0xD6 | 0x57 | 0x3A |
| 0x51 | 0x05 | 0x113 | 0xBB | 0x57 | 0x7A |
| 0x154 | 0x7C | 0x113 | 0xDB | 0x57 | 0xFA |
| 0x158 | 0x7C | 0x114 | 0xF4 | 0x58 | 0x01 |
| 0x159 | 0x6F | 0x114 | 0x64 | 0x58 | 0x03 |
| 0x15C | 0x7C | 0x115 | 0x0E | 0x58 | 0x07 |
| 0x15D | 0x3F | 0x115 | 0xFE | 0x58 | 0x0F |
| 0x160 | 0x7C | 0x116 | 0x0D | 0x58 | 0x1F |
| 0x161 | 0x3F | 0x116 | 0xDD | 0x58 | 0x3F |
| 0x164 | 0x7C | 0x117 | 0x0D | 0x45 | 0x8A |
| 0x165 | 0x4F | 0x117 | 0xDD | 0x45 | 0x0A |
| 0x16C | 0x7C | 0x46 | 0x03 | Delay 3 seconds | |
| 0x1B0 | 0x1C | 0x3D | 0x00 | 0x47 | 0xC0 |
| 0x1B1 | 0x5F | 0x45 | 0x0A | 0x46 | 0x03 |
| 0x1D8 | 0x1C | 0x46 | 0x02 | 0x47 | 0xC0 |
| 0x1D9 | 0xAF | 0x64 | 0x4A | 0x05 | 0x80 |
| 0xB2 | 0x1F | 0x65 | 0x05 | 0x20 | 0x1F |
| 0xB5 | 0x7F | 0x68 | 0x28 | 0x9D | 0x05 |
| 0x165 | 0xFF | 0x69 | 0x5E | 0x9E | 0x08 |
| 0x38 | 0x01 | 0x6A | 03D | 0x8B | 0x40 |
| 0xA4 | 0x30 | 0x6B | 0x8F | 0x20 | 0x00 |
| 0xC5 | 0x7F | 0x6C | 0x44 | 0x05 | 0x00 |
| 0xA8 | 0x00 | 0x57 | 0xDA | 0x04 | 0x01 |

**Table 8-13. Calibration Register Settings (continued)**

| ADDRESS | DATA | ADDRESS | DATA | ADDRESS | DATA |
|---------|------|---------|------|---------|------|
| 0xA2 | 0x63 | 0x57 | 0x9A | 0x20 | 0x1F |
| 0xA3 | 0x00 | 0x57 | 0x1A | 0x9D | 0x05 |
| 0xAD | 0x02 | 0x58 | 0x3E | 0x9E | 0x08 |
| 0x05 | 0x80 | 0x58 | 0x3C | 0x8B | 0x40 |
| 0x20 | 0x1F | 0x58 | 0x38 | | |

### 8.3.1.10 Step 10: JESD Interface Synchronization

The JESD interface can be synchronized using SPI writes or the GPIO1 pin (needs additional config).

**Table 8-14. JESD interface synchronization using SPI writes**

| ADDRESS | DATA | DESCRIPTION |
|---------|------|-------------|
| 0x05 | 0x04 | Select JESD page |
| 0x21 | 0x41 | Configure ADC to control SYNC using SPI writes |
| 0x21 | 0x61 | Configure JESD interface to send K28.5 characters for receiver synchronization |
| 0x21 | 0x41 | Configure JESD interface to send normal ADC data |

Product Folder Links: ADC34RF52

## 8.4 Power Supply Recommendations

The ADC34RF52 requires four different power-supplies. The AVDD18, AVDD12 and CLKVDD rail provides power for the internal analog and clocking circuits of the ADC while the DVDD rail powers the digital logic (including averaging and decimation filter) and the JESD204B digital interface.

Power sequencing is required as shown in Initialization Set Up. The AVDD18, AVDD12 and especially the CLKVDD power supply must be low noise to achieve data sheet performance. For applications operating near DC, the 1/f noise contribution of the power supply needs to be considered as well.

Power supply decoupling capacitors (0.1 µF) as close to the pins as possible on the top layer are recommended.
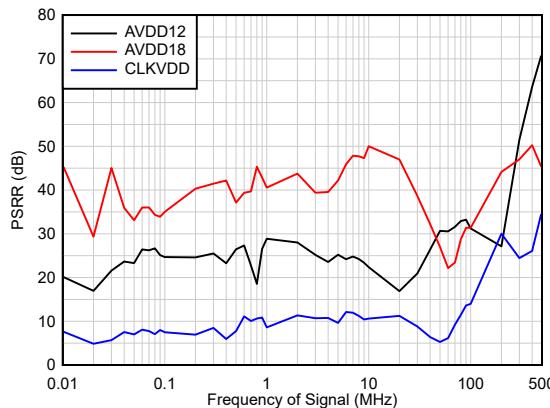


**Figure 8-9. Power supply rejection ratio (PSRR) vs frequency**

The recommended power supply architecture for a low noise design is to first use a high-efficiency step down switching regular, followed by a second stage of regulation using a low noise LDO for each power rail as shown in Figure 8-10. This provides additional switching noise reduction and improved voltage accuracy.

TI WEBENCH® Power Designer can be used to select and design the individual power-supply elements. Recommended switching regulators for the first stage include the LMS3635, and similar devices. Recommended low dropout (LDO) linear regulators include the TPS7A8400, and similar devices.
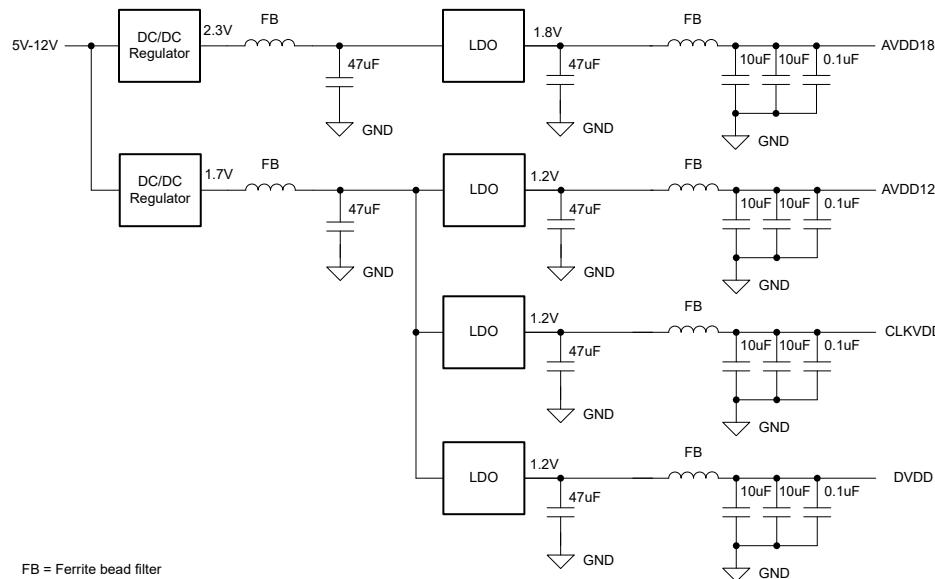


**Figure 8-10. Power supply design example**

AVDD12 or CLKVDD should not be shared with the DVDD to prevent digital switching noise from coupling into the analog domain.

## 8.5 Layout

### 8.5.1 Layout Guidelines

There are several critical signals which require specific care during board design:

1. Analog input and clock signals
   - Traces should be as short as possible and vias should be avoided where possible to minimize impedance discontinuities.
   - Traces should be routed using loosely coupled 100-Ω differential traces.
   - Differential trace lengths should be matched as close as possible to minimize phase imbalance and HD2 degradation.
2. Digital JESD204B output interface
   - Traces should be routed using tightly coupled 100-Ω differential traces.
3. Power and ground connections
   - Provide low resistance connection paths to all power and ground pins.
   - Use power and ground planes instead of traces.
   - Avoid narrow, isolated paths which increase the connection resistance.
   - Use a signal/ground/power circuit board stackup to maximize coupling between the ground and power plane.

### 8.5.2 Layout Example

The following screen shot shows the top layer of the ADC34RF52 EVM.

- The input signal traces are routed as differential signals on the top layer avoiding vias. Care is taken to maintain symmetry between positive and negative input with matched trace length to minimize phase imbalance.
  Figure 8-11 shows the layout example for 1x and 2x averaging configuration
- JESD204B output interface lanes are routed differential and length matched
- Bypass caps are close to the power pins on the top layer avoiding vias.
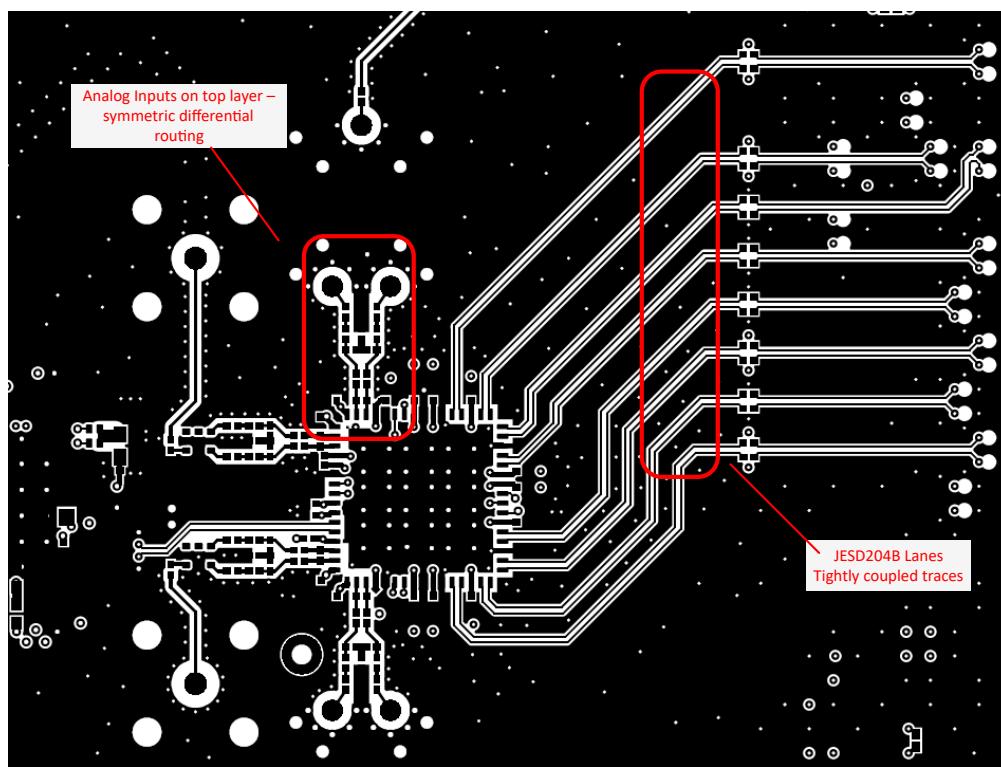


**Figure 8-11. Layout example: top layer of the EVM**

Product Folder Links: *ADC34RF52*

# 9 Device and Documentation Support

## 9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 9.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

## 9.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.
TI WEBENCH® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

## 9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 9.5 Glossary

TI Glossary        This glossary lists and explains terms, acronyms, and definitions.

# 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

# PACKAGE OPTION ADDENDUM

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| ADC34RF52IRTD | ACTIVE | VQFN | RTD | 64 | 260 | RoHS & Green | Call TI \| NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ34RF52 | Samples |
| ADC34RF52IRTDT | ACTIVE | VQFN | RTD | 64 | 250 | RoHS & Green | Call TI \| NIPDAU | Level-3-260C-168 HR | -40 to 85 | AZ34RF52 | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:**  TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4205146/D

B

9.1
8.9

A

PIN 1 ID

9.1
8.9

(□ 8.71)

0.975
0.875

C

(0.2)

SEATING PLANE

⌒ 0.08 C

4X (45° X0.42)

5.566±0.1

17

32

16

33

4X
7.5

SYMM
₵

65

6.866±0.1

1

48

64X 0.5

64

49

64X 0.3
0.2

PIN 1 ID

SYMM
₵

64X 0.5
0.3

⊕ 0.1 Ⓜ C B A
0.05 Ⓜ C

4226371/A   11/2020
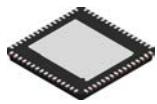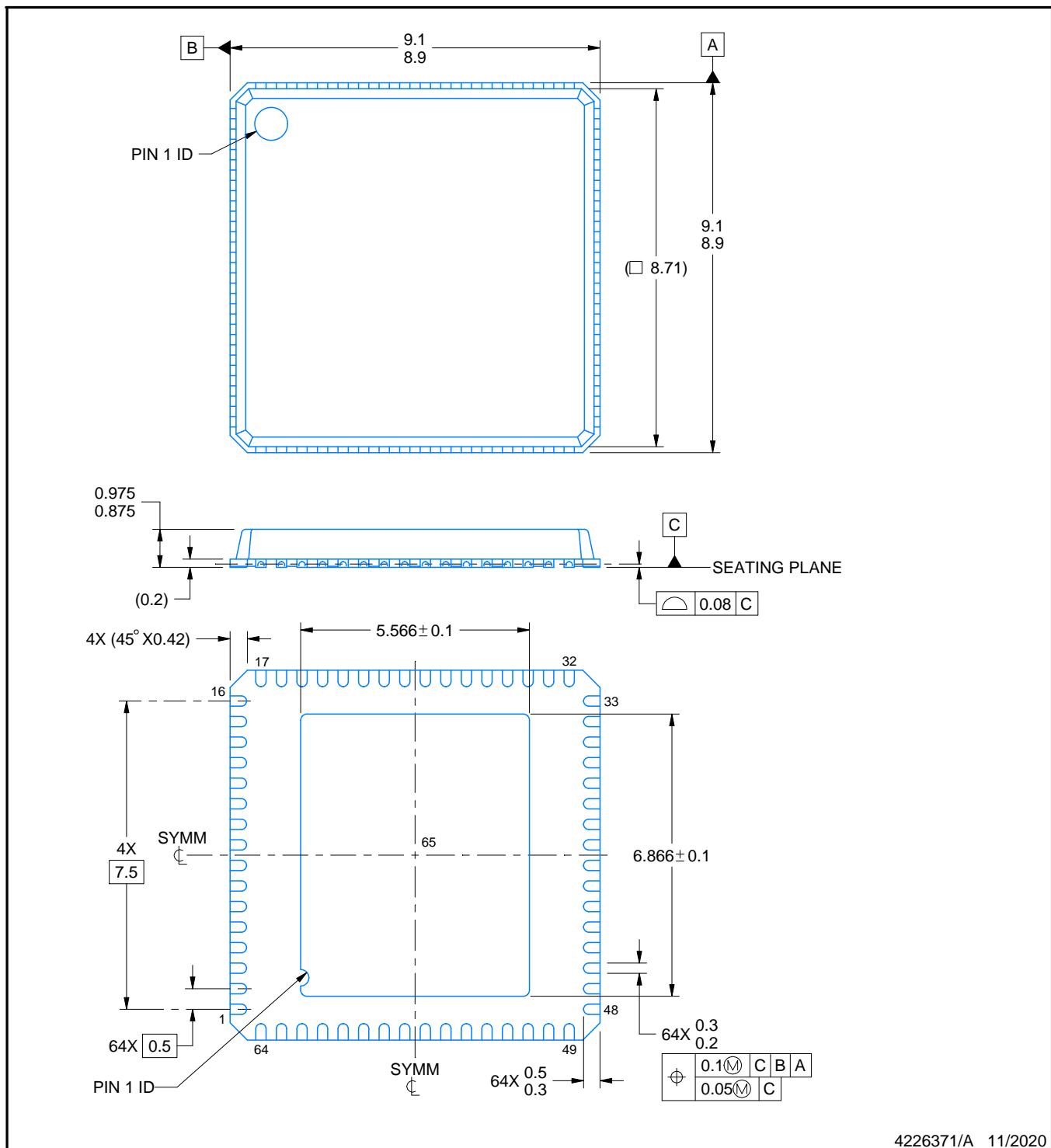
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

LAND PATTERN EXAMPLE
SCALE:8X

(5.566)

(1.17) TYP

(1.33) TYP

64X (0.6)

64X (0.25)

1

64    49

48

60X (0.5)

(1.26) TYP

SYMM ℄

65

6.866

(0.63)

(8.8)

(R0.05) TYP

16

33

(R0.1) TYP VIA

17    32

SYMM ℄

(8.8)

SOLDER MASK DETAILS

0.07 MAX ALL AROUND

METAL

SOLDER MASK OPENING

NON SOLDER MASK DEFINED (PREFERRED)

0.07 MIN ALL AROUND

SOLDER MASK OPENING

METAL UNDER SOLDER MASK
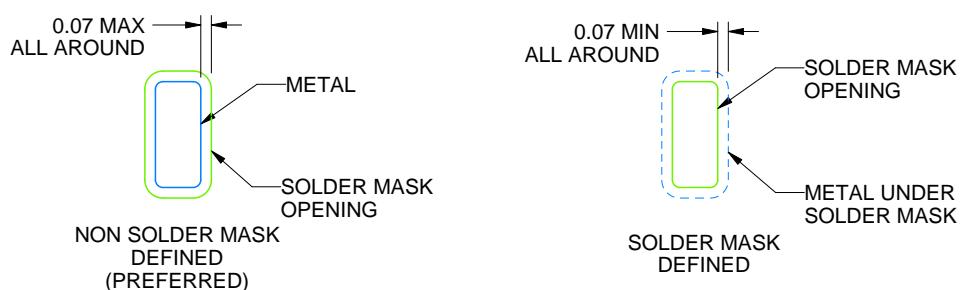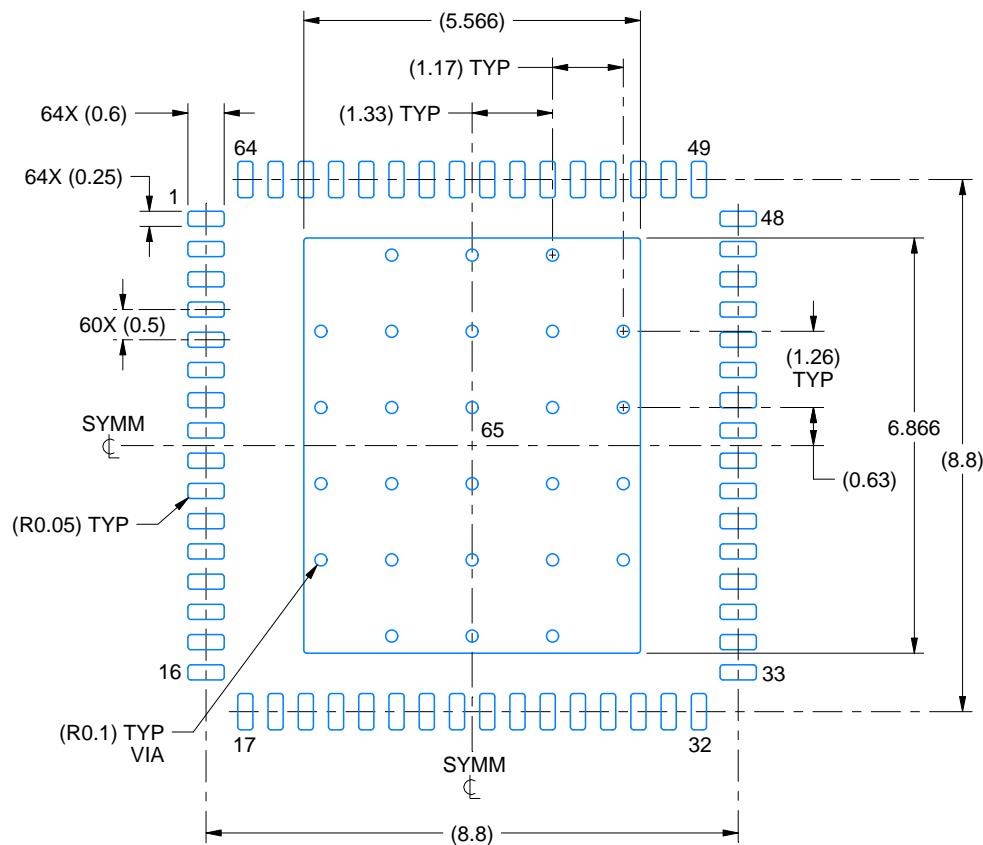
SOLDER MASK DEFINED

4226371/A   11/2020

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

64X (0.6)

64X (0.25)

60X (0.5)

SYMM

METAL
TYP

(0.665)

(1.33) TYP

(1.26) TYP

(1.26) TYP

(8.8)

20X (1.06)

20X (1.13)

(8.8)

SYMM

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 65:
63% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:10X

4226371/A   11/2020
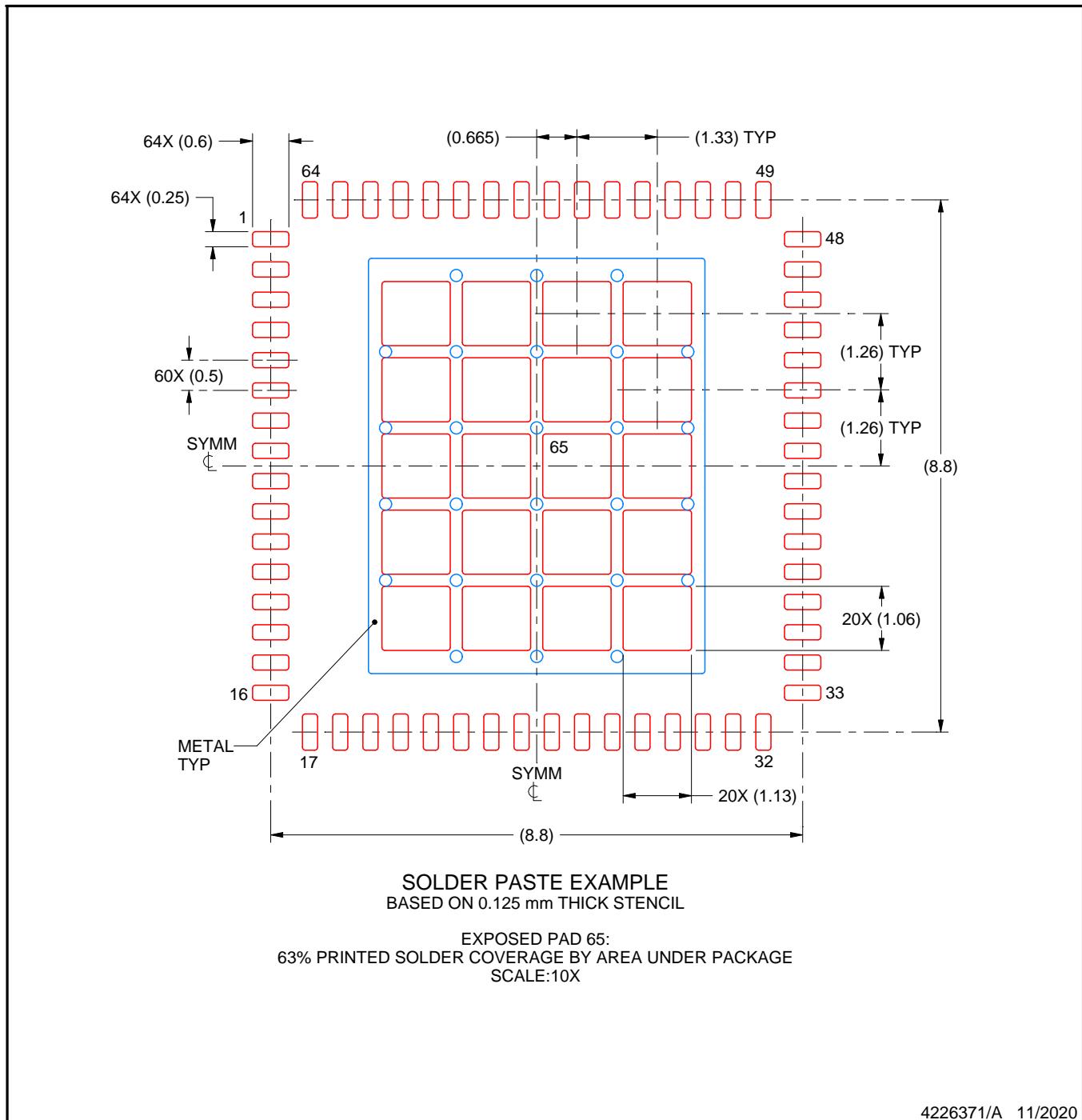
NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

# IMPORTANT NOTICE AND DISCLAIMER