BURR-BROWN®

ADS1201

High Dynamic Range DELTA-SIGMA MODULATOR

FEATURES

- 130dB DYNAMIC RANGE
- FULLY DIFFERENTIAL INPUT
- TWO-WIRE INTERFACE
- INTERNAL/EXTERNAL REFERENCE
- ON-CHIP SWITCHES FOR CALIBRATION

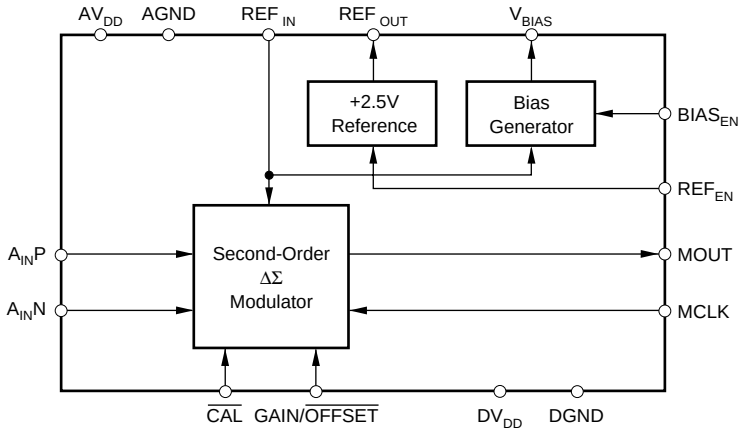
APPLICATIONS

- INDUSTRIAL PROCESS CONTROL
- INSTRUMENTATION
- SMART TRANSMITTERS
- PORTABLE INSTRUMENTS
- WEIGH SCALES
- PRESSURE TRANSDUCERS

DESCRIPTION

The ADS1201 is a precision, 130dB dynamic range, delta-sigma (ΔΣ) modulator operating from a single +5V supply. The differential inputs are ideal for direct connection to transducers or low level signals. With the appropriate digital filter and modulator rate, the device can be used to achieve 24-bit analog-to-digital (A/D) conversion with no missing codes. Effective resolution of 20 bits can be maintained with a digital filter bandwidth of 1kHz at a modulator rate of 320kHz.

The ADS1201 is designed for use in high resolution measurement applications including smart transmitters, industrial process control, weigh scales, chromatography, and portable instrumentation. It is available in a 16-lead SOIC package.



International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS

At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, MCLK = 320kHz, REF_{EN} LOW, $BIAS_{EN}$ LOW, and external +2.5V reference, unless otherwise specified.

PARAMETER	CONDITIONS	ADS1201U MIN	ADS1201U TYP	ADS1201U MAX	UNITS
ANALOG INPUT					
Absolute Input Voltage Range		0		+5	V
	With V_{BIAS}[1]	–10		+10	V
Differential Input Voltage Range		–5		+5	V
	With V_{BIAS}[1]	–20	See Note 2	+20	V
Input Impedance			250[4]		kΩ
Input Capacitance			8		pF
Input Leakage Current			5	50	pA
	At T_{MIN} to T_{MAX}			1	nA
SYSTEM PERFORMANCE					
Dynamic Range	10Hz Bandwidth[5]		130[6]		dB
	60Hz Bandwidth[5]	115[6]	120[6]		dB
	1kHz Bandwidth[5]		115[6]		dB
Integral Linearity Error	60Hz Bandwidth[5]			±0.0015	%FSR
	1kHz Bandwidth[5]			±0.0015	%FSR
Offset Error[2]			See Note 7		µV
Offset Drift[3]			1		µV/°C
Gain Error[2]			See Note 7		ppm
Gain Error Drift[3]			1		µV/°C
Common-Mode Rejection	At DC	80	100		dB
Power Supply Rejection			80		dB
REFERENCE					
Internal Reference (REF_{OUT})		2.4	2.5	2.6	V
Drift			25		ppm/°C
Noise			50		µVp-p
Load Current	Source or Sink	–1		1	mA
Output Impedance			2		Ω
External Reference (REF_{IN})		2.0		3.0	V
Load Current				2.5	µA
V_{BIAS} Output	Using Internal Reference	3.15	3.3	3.45	V
Drift			50		ppm/°C
Load Current				10	mA
DIGITAL INPUT/OUTPUT					
Logic Family			TTL Compatible CMOS		
Logic Levels:					
V_{IH} (MCLK)	I_{IH} = +5µA	2.0		DV_{DD} +0.3	V
V_{IL} (MCLK)	I_{IL} = +5µA	–0.3		0.8	V
V_{OH} (MOUT)	I_{OH} = 2 TTL Loads	2.4			V
V_{OL} (MOUT)	I_{OL} = 2 TTL Loads			0.4	V
MCLK Frequency		0.02		1	MHz
POWER SUPPLY REQUIREMENTS					
Power Supply Voltage	Specified Performance	4.75		5.25	V
Supply Current					
Analog Current			4.6		mA
Digital Current			0.4		mA
Additional Analog Current					
REF_{OUT} Enabled	No Load		1.6		mA
V_{BIAS} Enabled	No Load		1		mA
Total Power Dissipation	REF_{OUT}, V_{BIAS} Disabled		25	40	mW
TEMPERATURE RANGE					
Specified Performance		–40		+85	°C

NOTES: (1) This range is set with external resistors and V_{BIAS} (as described in the text). Other ranges are possible. (2) After the on-chip offset and gain calibration functions have been employed. (3) Re-calibration can reduce these errors. (4) Input impedance changes with MCLK. (5) Assume brick wall digital filter is used. (6) 20 Log (full scale/rms noise). (7) After calibration, these errors will be of the order of the effective resolution.

ABSOLUTE MAXIMUM RATINGS

Analog Input: Current	±100mA, Momentary
	±10mA, Continuous
Voltage	AGND –0.3V to AV_{DD} +0.3V
AV_{DD} to DV_{DD}	–0.3V to 6V
AV_{DD} to AGND	–0.3V to 6V
DV_{DD} to DGND	–0.3V to 6V
AGND to DGND	±0.3V
REF_{IN} Voltage to AGND	–0.3V to AV_{DD} +0.3V
Digital Input Voltage to DGND	–0.3V to DV_{DD} +0.3V
Digital Output Voltage to DGND	–0.3V to DV_{DD} +0.3V
Lead Temperature (soldering, 10s)	+300°C
Internal Power Dissipation	500mW

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

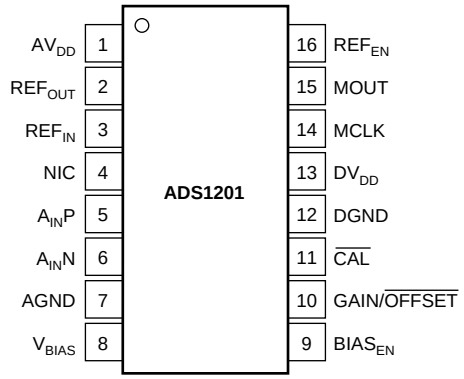
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATION

Top View **SOIC**



PIN DESCRIPTIONS

PIN NO	NAME	DESCRIPTION
1	AV_{DD}	Analog Input: Analog Supply, +5V nominal.
2	REF_{OUT}	Analog Output: Internal Reference Voltage Output: +2.5V nominal.
3	REF_{IN}	Analog Input: Reference Voltage Input.
4	NIC	Not Internally Connected.
5	$A_{IN}P$	Analog Input: Noninverting Input.
6	$A_{IN}N$	Analog Input: Inverting Input.
7	AGND	Analog Input: Analog Ground.
8	V_{BIAS}	Analog Output: Bias Voltage Output, nominally +3.3V (with +2.5V reference).
9	$BIAS_{EN}$	Digital Input: Bias Voltage Enable Input (HIGH = enabled, LOW = disabled).
10	GAIN/$\overline{OFFSET}$	Digital Input: Gain/Offset Calibration Select Input (with CAL LOW; HIGH = gain configuration, LOW = offset configuration).
11	$\overline{CAL}$	Digital Input: Calibration Control Input (HIGH = normal operation, LOW = gain or offset calibration configuration).
12	DGND	Digital Input: Digital Ground.
13	DV_{DD}	Digital Input: Digital Supply, +5V nominal.
14	MCLK	Digital Input: Modulator Clock Input. CMOS compatible.
15	MOUT	Digital Output: Modulator Output.
16	REF_{EN}	Digital Input: REF_{OUT} Voltage Enable Input (HIGH = enabled, LOW = disabled).

PACKAGE/ORDERING INFORMATION

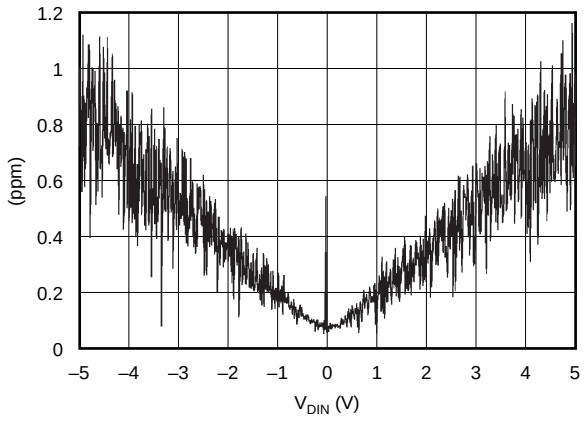
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(1)	TRANSPORT MEDIA
ADS1201U	SOL-16	211	–40°C to +85°C	ADS1201U	ADS1201U	Rails
"	"	"	"	"	ADS1201U/1K	Tape and Reel

NOTE: (1) Models with a slash (/) are available only in Tape and Reel in the quantities indicated (e.g., /1K indicates 1000 devices per reel). Ordering 1000 pieces of "ADS1201U/1K" will get a single 1000-piece Tape and Reel.

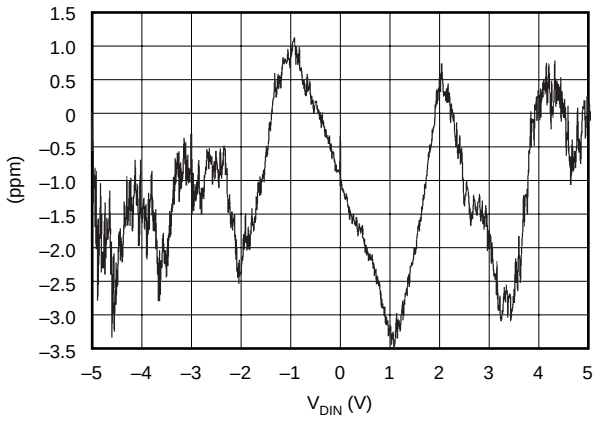
TYPICAL PERFORMANCE CURVES

At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, MCLK = 320kHz, REF_{EN} LOW, $BIAS_{EN}$ LOW, and external +2.5V reference, unless otherwise specified.

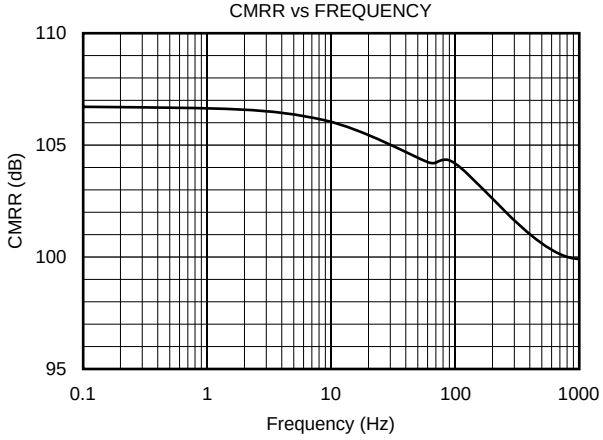
rms NOISE



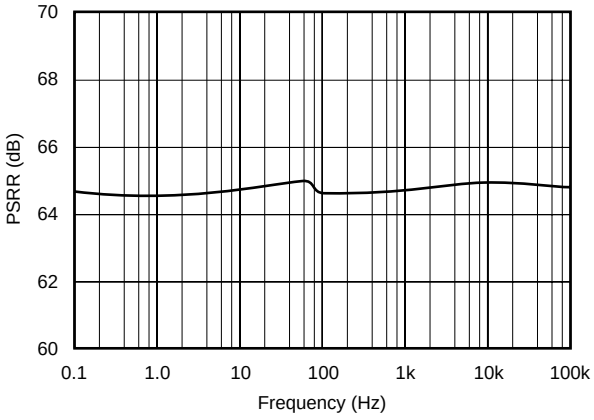
LINEARITY



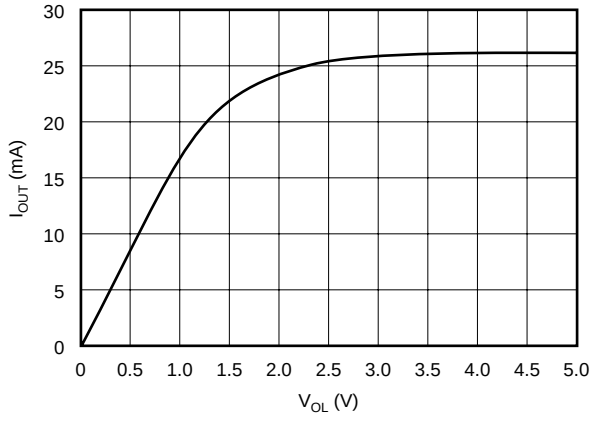
CMRR vs FREQUENCY



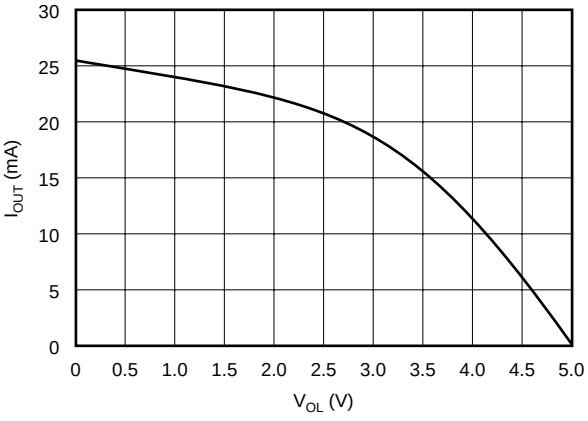
PSRR vs FREQUENCY



TYPICAL SINK CURRENT

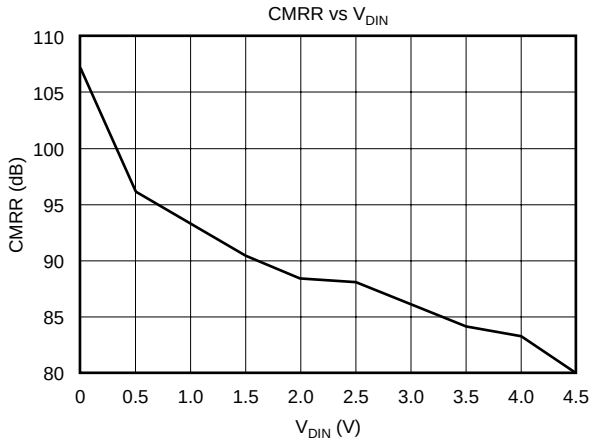


TYPICAL SOURCE CURRENT



TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = +25°C, AV_{DD} = DV_{DD} = +5V, MCLK = 320kHz, REF_{EN} LOW, $BIAS_{EN}$ LOW, and external +2.5V reference, unless otherwise specified.



GENERAL DESCRIPTION

The ADS1201 is a single channel, second-order, CMOS analog modulator designed for high resolution conversions from dc to 1000Hz. The output of the converter (MOUT) provides a stream of digital ones and zeros. The time average of this serial output is proportional to the analog input voltage. The combination of an ADS1201 and a processor that is programmed to implement a digital filter results in a high resolution A/D converter system. This system allows flexibility with the digital filter design and is capable of A/D conversion results that have a dynamic range that exceeds 130dB (see Figure 1).

THEORY OF OPERATION

The differential analog input of the ADS1201 is implemented with a switched capacitor circuit. This switched capacitor circuit implements a 2nd-order modulator stage which digitizes the input signal into a binary output stream. The input stage of the converter can be configured to sample an analog signal or to perform a calibration which quantifies offset and gain errors. The sample clock (MCLK) provides the switched capacitor network and modulator clock signal for the A/D conversion process, as well as the output data framing clock. Different frequencies for this clock allows for a variety of performance solutions in resolution and signal bandwidth. The analog input signal is continuously sampled by the A/D converter and compared to an internal or external voltage reference. A digital stream appears at the output of the converter. This digital stream accurately represents the analog input voltage over time.

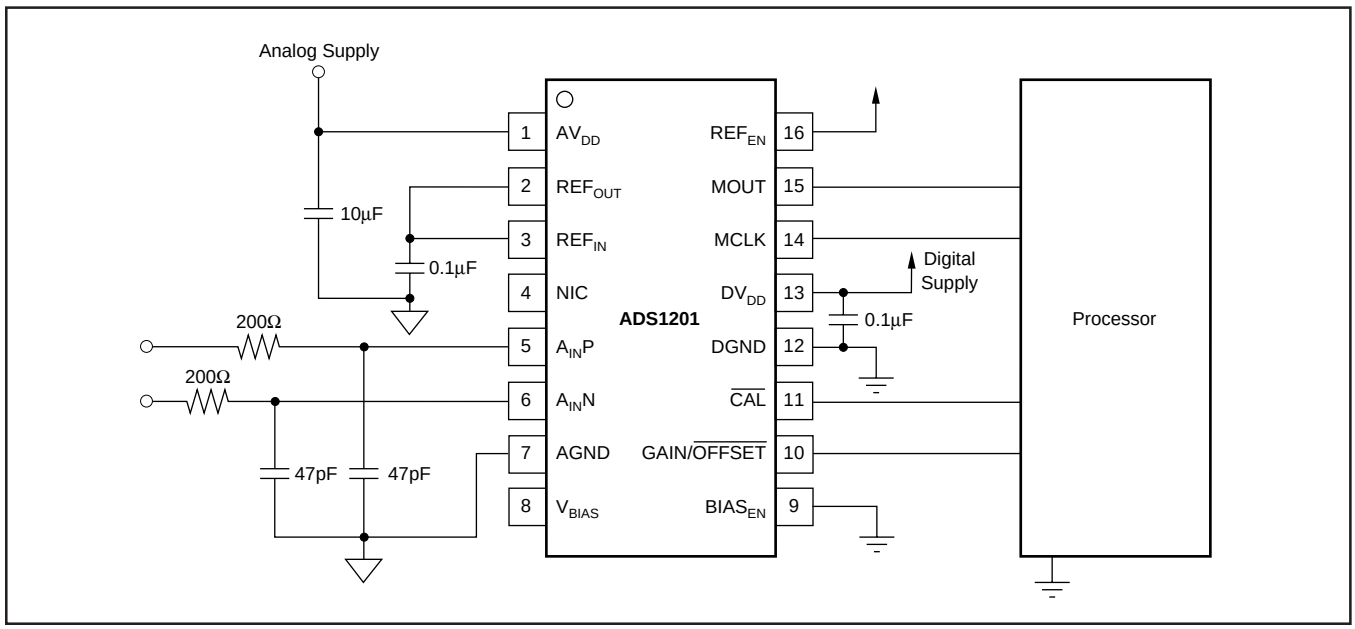


FIGURE 1. Connection Diagram for the ADS1201 Delta-Sigma Modulator Including External Processor.

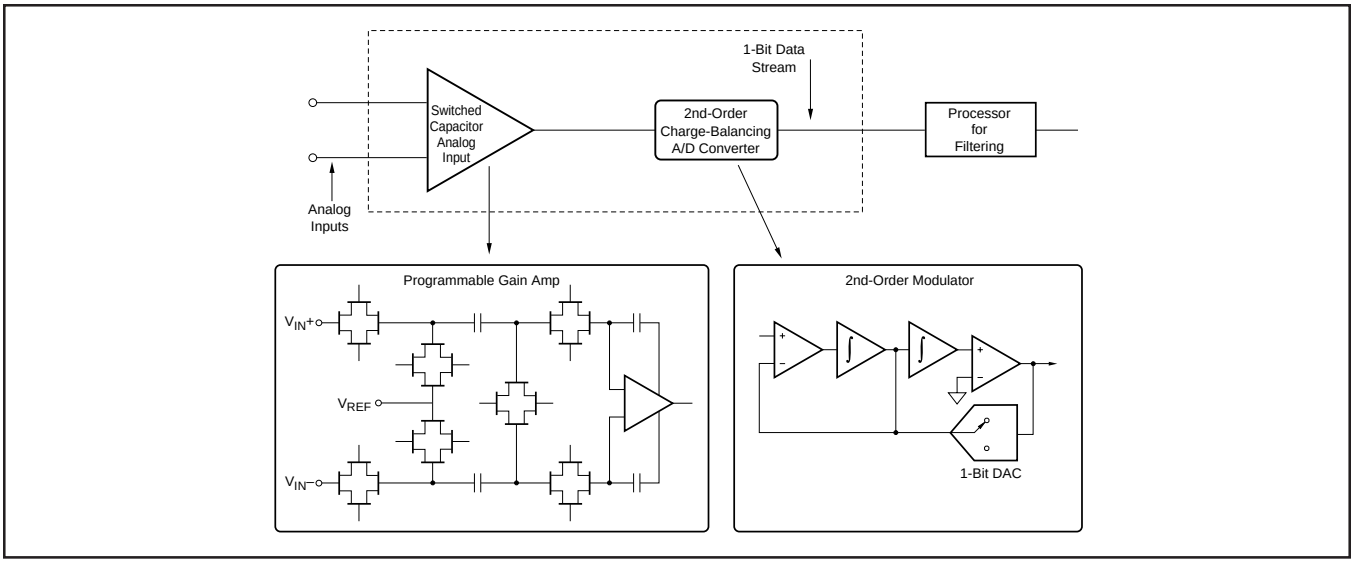


FIGURE 2. Block Diagram of the ADS1201.

ANALOG INPUT STAGE

Analog Input

The input design topology of the ADS1201 is based on a fully differential switched capacitor architecture. This input stage provides the mechanism to achieve low system noise, high common-mode rejection (100dB) and excellent power supply rejection. The input impedance of the analog input is dependent on the input capacitor and modulator clock frequency (MCLK), which is also the sampling frequency of the converter. Figure 3 shows the basic input structure of the ADS1201. The relationship between the input impedance of the ADS1201 and the modulator clock frequency is:

$$A_{IN}\ \text{Input Impedance}(\Omega) = \frac{1E12}{12 \bullet f_{MCLK}}$$

The input impedance becomes a consideration in designs where the source impedance of the input signal is significant. In this case, it is possible for a portion of the signal to be lost across this external source impedance. The importance of this effect depends on the desired system performance.

There are two restrictions on the analog input signal to the ADS1201. Under no conditions should the current into or out of the analog inputs exceed 10mA. In addition, the linearity of the device is guaranteed only when the analog voltage applied to either input resides within the range defined by AGND = > –30mV and < = AV_{DD} + 30mV. If either of the inputs exceed these limits, the input protection diodes on the front end of the converter will begin to turn on. This will induce leakage paths resulting in nonlinearities in the conversion process.

For this reason, the 0V to 5V input range must be used with caution. Should AV_{DD} be 4.75V, the analog input signal would swing outside the guaranteed specifications of the device. Designs utilizing this mode of operation should consider limiting the span to a slightly smaller range. Common-mode voltages are also a significant concern and must be carefully analyzed.

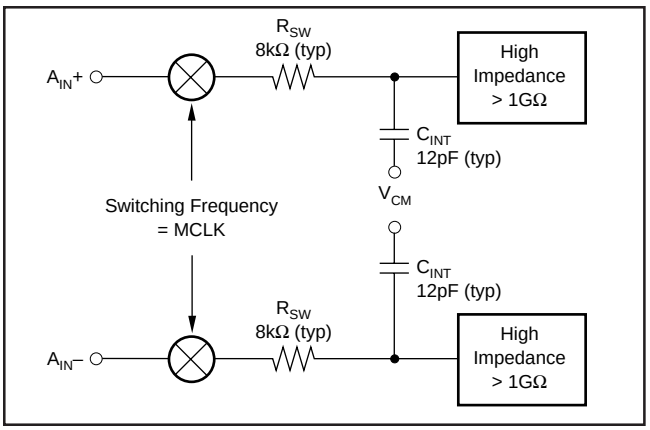


FIGURE 3. Input Impedance of the ADS1201.

Modulator

The modulator sampling frequency (MCLK) can be operated over a range of 20kHz to 1MHz. The frequency of MCLK can be increased to improve the performance of the converter or adjusted to comply with the clock requirements of the application.

The modulator topology is fundamentally a 2nd-order, charge-balancing A/D converter, as the one conceptualized in Figure 4. The analog input voltage and the output of the 1-bit DAC is differentiated, providing an analog voltage at X_2 and X_3. The voltage at X_2 and X_3 are presented to their individual integrators. The output of these integrators progress in a negative or positive direction. When the value of the signal at X_4 equals the comparator reference voltage, the output of the comparator switches from negative to positive or positive to negative, depending on its original state. When the output value of the comparator switches from a HIGH to LOW or vise versa, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage at X_6, causing the integrators to progress in the opposite direction. The feedback of the modulator to the front end of the integrators force the value of the integrator output to track the average of the input.

REFERENCE CIRCUIT

There are two reference circuits included in the ADS1201 converter: V_{REF} (REF_{IN}, REF_{OUT}) and V_{BIAS}. The circuitry for V_{REF} is configured to allow the user to utilize the internal reference on the chip or provide an external reference to the converter (see Figure 5). The second reference, V_{BIAS}, is derived from V_{REF}, whether it is internal or external. V_{BIAS} is exclusively an output reference. This ratiometric relationship between V_{REF} and V_{BIAS} reduces system errors when two separate bias voltages are required in the application.

REFERENCE INPUT (REF_{IN})

The reference input (REF_{IN}) of the ADS1201 can be configured so that the 2.5V (nominal) internal or external reference can be used in the conversion process. If the internal reference is used, the correct connection configuration is shown in Figure 5a. The capacitor in this circuit is absolutely required if low noise performance is desired.

An external reference can be used to reduce the noise in the conversion process. If an external reference is used, care should be taken to insure that the selected reference has low noise performance. The appropriate connection circuit of an external reference is shown in Figure 5b. The reference must be configured with appropriate capacitors to reduce the high frequency noise that may be contributed by the reference. The input impedance of REF_{IN} changes with the modulator clock frequency. The relationship is:

$$\text{Typical } REF_{IN} \text{ Input Impedance} = \frac{1E12}{50 \bullet f_{MCLK}}$$

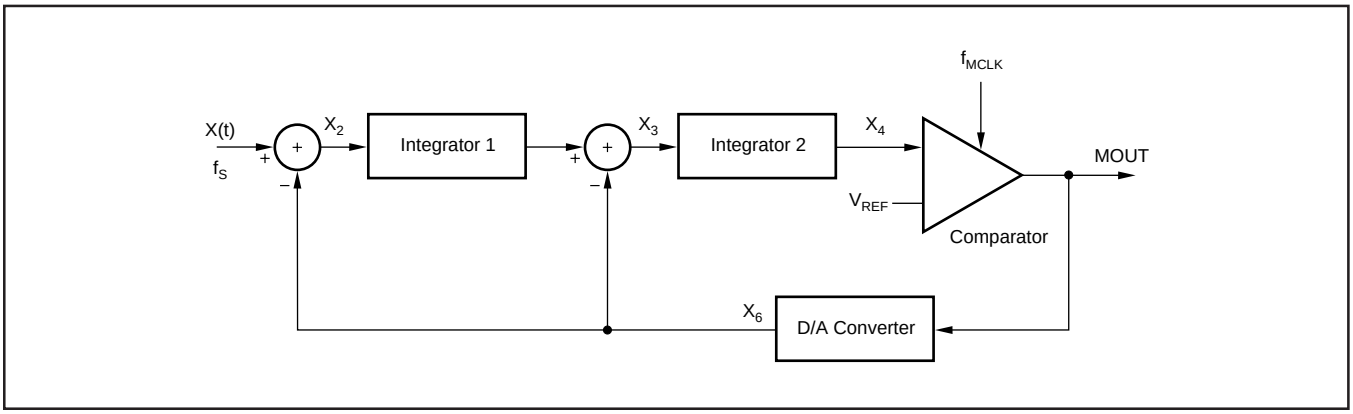


FIGURE 4. Block Diagram of a Second-Order Modulator.

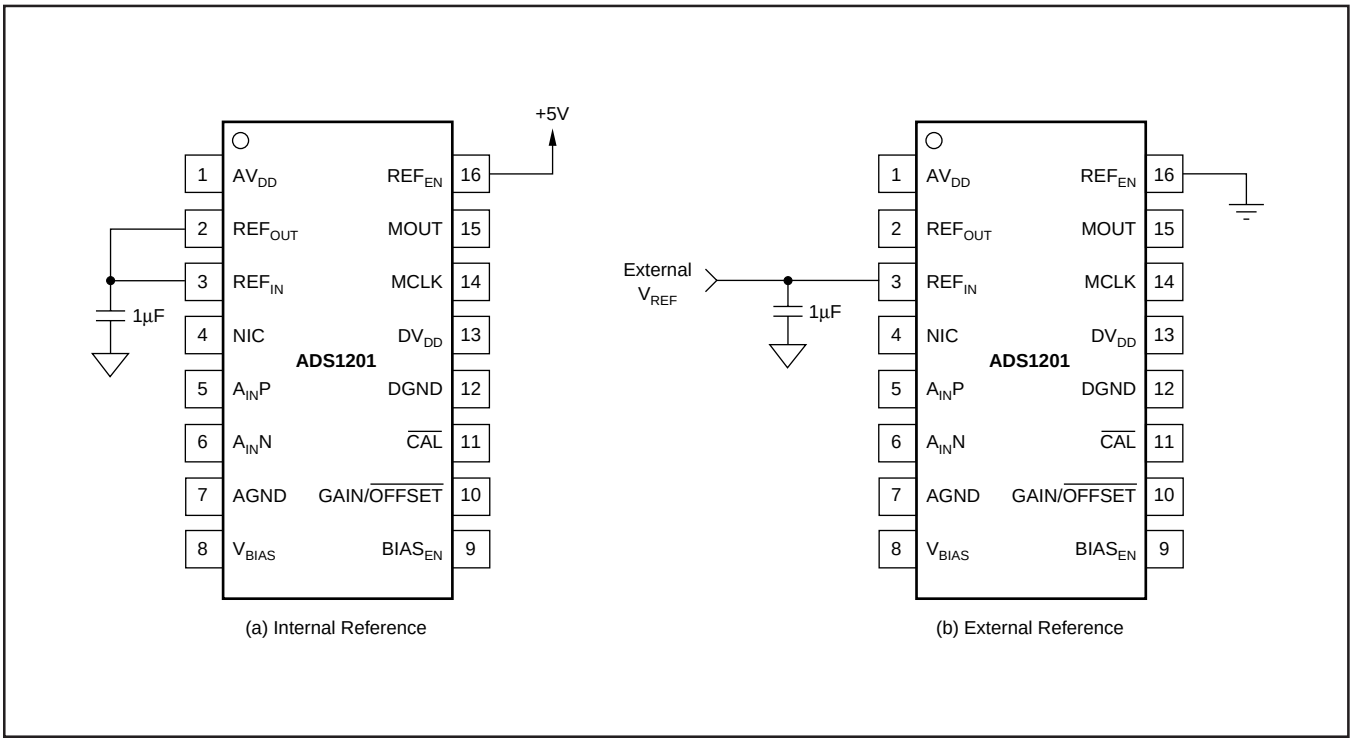


FIGURE 5. Two Voltage Reference Connection Alternatives for the ADS1201.

The reference input voltage can vary between 2V and 3V. Higher reference voltages will cause the full-scale range to increase while the internal circuit noise of the converter remains approximately the same. This will increase the LSB weight but not the internal noise, resulting in increased signal-to-noise ratio. Likewise, lower reference voltages will decrease the signal-to-noise ratio.

The internal reference, which generates +2.5V, can be disabled when an external reference is used. This internal reference is disabled with the REF_{EN} pin. When the reference is disabled, the supply current (AV_{DD}) of the converter will reduce by approximately 1.6mA.

REFERENCE OUTPUT ($VREF_{OUT}$)

The ADS1201 contains an internal +2.5V reference. When using this feature, REF_{EN} must be HIGH (see Figure 5). Tolerances, drift, noise, and other specifications for this reference are given in the Specifications table. Note that this reference is not designed to sink or to source more than 1mA of current. In addition, loading the reference with a dynamic or variable load is not recommended. This can result in small changes in reference voltage as the load changes.

VOLTAGE BIAS OUTPUT (V_{BIAS})

The V_{BIAS} output voltage is dependent on the reference input (REF_{IN}) voltage and is approximately 1.33 times as great. The output of V_{BIAS} is used to bias input signals of greater than 5V. If a resistor network is used in combination with the V_{BIAS} output, the signal range can be scaled and level shifted to match the input range of the ADS1201. Figure 6 shows a connection diagram which will allow the ADS1201 to accept a ±10V input signal (20V full-scale range). If $BIAS_{EN}$ is HIGH, the voltage at V_{BIAS} will be 3.3V (assumes a 2.5V nominal V_{REF}).

REF_{EN}	REF_{OUT}
LOW	High Impedance
HIGH	2.5V (nominal)

TABLE I. Reference Enable.

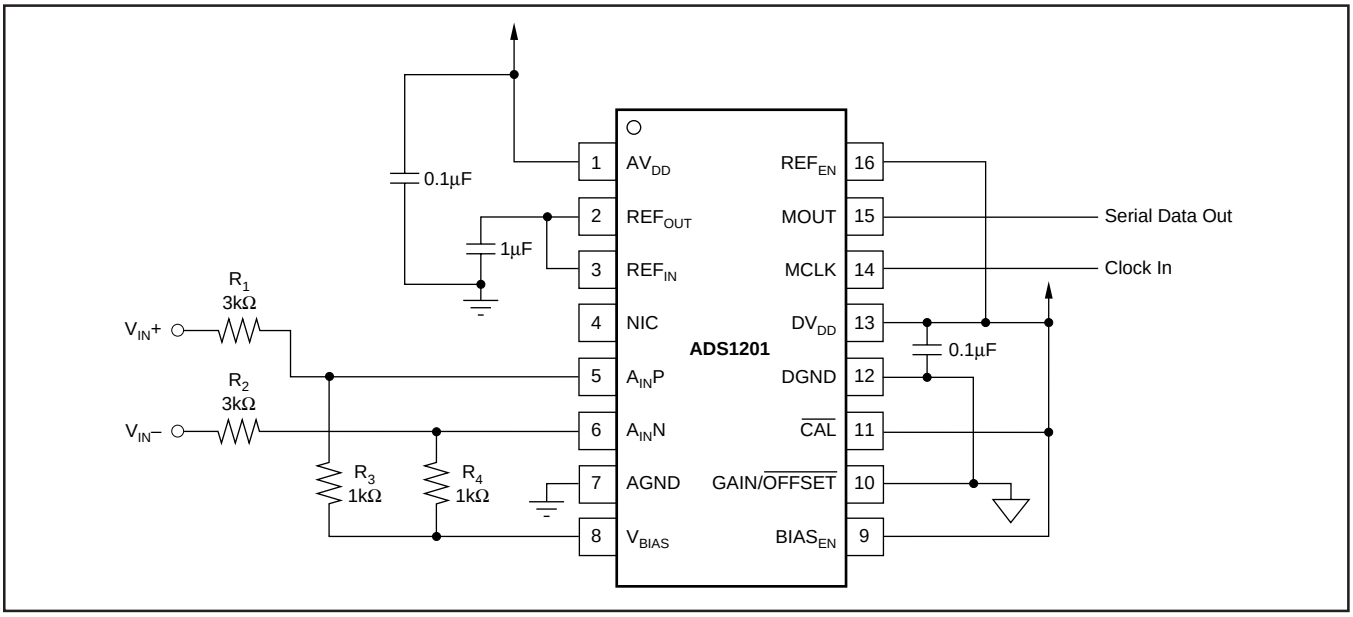
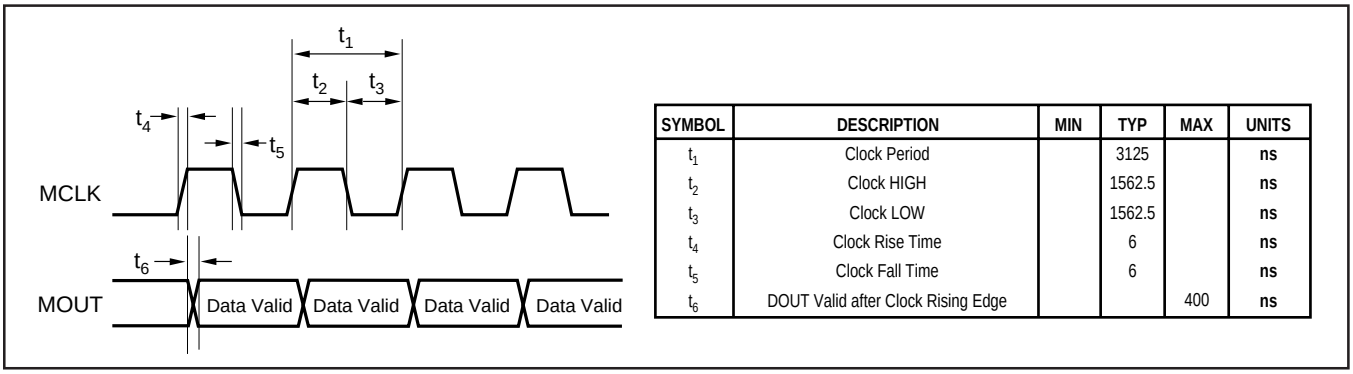


FIGURE 6. ±10V Bipolar Input Configuration Using V_{BIAS}.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Clock Period		3125		ns
t_2	Clock HIGH		1562.5		ns
t_3	Clock LOW		1562.5		ns
t_4	Clock Rise Time		6		ns
t_5	Clock Fall Time		6		ns
t_6	DOUT Valid after Clock Rising Edge			400	ns

FIGURE 7. Timing Diagram for the Digital Interface of the ADS1201.

$BIAS_{EN}$	V_{BIAS}
LOW	High Impedance
HIGH	1.33V • V_{REF}

TABLE II. Bias Enable.

When enabled, the V_{BIAS} circuitry consumes approximately 1mA with no external load. The maximum current into or out of V_{BIAS} should not exceed 10mA.

On power-up, external signals may be present before V_{BIAS} is enabled. This can create a situation in which a negative voltage is applied to the analog inputs, reverse biasing the negative input protection diode of the ADS1201. This situation should not be a problem as long as the resistors R_1 and R_2 limit the current being sourced by each analog input to be under 10mA. A potential of 0V at the analog input pin (A_{IN}P or A_{IN}N) should be used in the calculation.

DIGITAL OUTPUT

The timing diagram for the ADS1201 data retrieval is shown in Figure 7. MCLK initiates the modulator process for the ADS1201 and is used as a system clock by the ADS1201, as well as a framing clock for data out. The modulator output data, which is a serial stream, is available on the MOUT pin. Typically, MOUT is read on the falling edge of MCLK. Under any situation with MCLK, the duty cycle must be kept constant for reliable, repeatable results.

An input differential signal of 0V will ideally produce a stream of ones and zeros that are HIGH 50% of the time and LOW 50% of the time. A differential input of 5V will produce a stream of ones and zeros that are HIGH 90% of the time. A differential input of –5V will produce a stream of ones and zeros that are HIGH 10% of the time. The input voltage versus the output modulator signal is shown in Figure 8.

OFFSET and GAIN CALIBRATION

The ADS1201 offers a self-calibration function that is implemented with the GAIN/$\overline{\text{OFFSET}}$ and $\overline{\text{CAL}}_{EN}$ pins. Both conditions provide an output stream of data, similar to normal operation where the converter is configured to sample an input signal at A_{IN}.

The offset and gain errors of the ADS1201 are calibrated independently. For best operation, the offset should be calibrated first, followed by the gain. The calibration implementation timing diagram is shown in Figure 9. The calibration mode pins control the calibration functions of the ADS1201.

Calibration should be performed once and then normal operation can be resumed. Calibration of offset and gain is recommended immediately after power-on and whenever there is a "significant" change in the operating environment. Significant changes in the operating environment include a change of the MCLK frequency, MCLK duty cycle, power

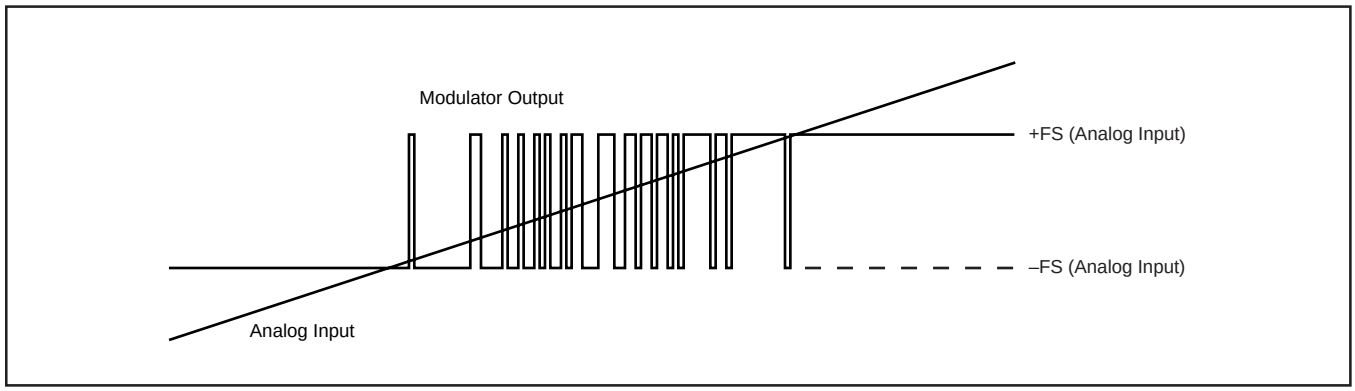
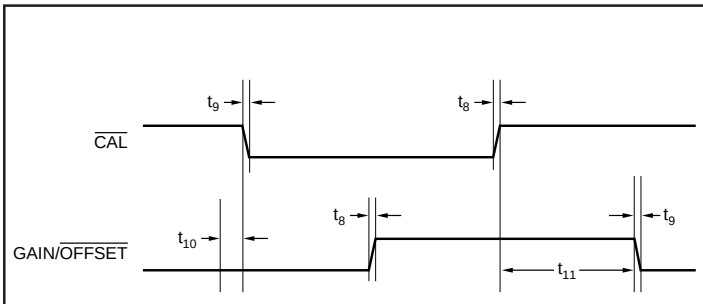


FIGURE 8. Analog Input versus Modulator Output of the ADS1201.



SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_8	CAL and GAIN/OFFSET Rise Time		10		ns
t_9	CAL and GAIN/OFFSET Fall Time		10		ns
t_{10}	GAIN/OFFSET to CAL Setup Time	0			ns
t_{11}	GAIN/OFFSET to CAL Hold Time	2.5 T_{MCLK}(1)			ns

NOTE: (1) T_{MCLK} is the clock period of MCLK.

FIGURE 9. Timing Diagram for the Calibration Feature of the ADS1201.

GAIN/$\overline{\text{OFFSET}}$	$\overline{\text{CAL}}_{\text{EN}}$	
0	1	Normal Mode
0	0	Offset Calibration, Analog inputs shorted to ground internally.
1	0	Full-Scale Calibration, Analog inputs are referenced to V_{REF} internally.

TABLE III. Calibration Enable.

supply, V_{REF}, or temperature. The amount of change which could cause a re-calibration is dependent on the application and effective resolution of the system.

The results of the calibration calculations are stored in two registers in the processor chip (see Figure 1). These two calibration results can then be used to calibrate the input signal results with one of the following formulas:

Equivalent Calibrated Output Code = FSC $(FO_1 - FO_2)/(FO_3 - FO_2)$

where FO_1 = Filter output code of an applied input voltage

FO_2 = Filter output code of the offset calibration

FO_3 = Filter output code of the gain calibration

FSC = Desired full-scale output

With a simple sinc filter, the calibrated A/D conversion would equal:

Equivalent Calibrated Input Voltage = $(N_1 - N_2) \bullet V_{REF}/(N_3 - N_2)$

where N_1 = number of ones counted (or digital equivalent after filtering) over given time (t_M) with an applied input voltage

N_2 = number of ones counted (or digital equivalent after filtering) during offset calibration where $t_{12} = t_M$

N_3 = number of ones counted (or digital equivalent after filtering) during gain calibration where $t_{13} = t_M$

A system calibration can be performed by applying two known voltage levels to the input of the converter. In this situation, the GAIN/$\overline{\text{OFFSET}}$ and $\overline{\text{CAL}}_{\text{EN}}$ pins are not used. Rather, the digital output of these two known voltages are accumulated by the processor. With this data, the processor can determine the calibration register values that are appropriate for the application.

LAYOUT CONSIDERATIONS

POWER SUPPLIES

The ADS1201 requires the digital supply (DV_{DD}) to be no greater than the analog supply (AV_{DD}). Failure to observe this condition could cause permanent damage to the ADS1201. The best scheme is to power the analog section of the design and AV_{DD} from one +5V line and the digital section and DV_{DD} from a separate +5V line (from the same supply). If there are separate analog and digital power supplies for the ADS1201, a good design approach would be to have the analog supply come up first, followed by the digital supply. Another approach that can be used to control the analog and digital power supply differences is shown in Figure 10. In this circuit, a connection has been made between the ADS1201 supply pins via a 10Ω resistor. The combination of this resistor and the decoupling capacitors provides some filtering between DV_{DD} and AV_{DD}.

The analog supply should be well regulated and low noise. For designs requiring very high resolution from the ADS1201, power supply rejection will be a concern. The requirements for the digital supply are not strict. However, high frequency noise on DV_{DD} can capacitively couple into the analog portion of the ADS1201. This noise can originate from switching power supplies, microprocessors or digital signal processors.

For either supply, high frequency noise will generally be rejected by the external digital filter at integer multiples of MCLK. Just below and above these frequencies, noise will alias back into the pass-band of the digital filter, affecting the conversion result.

Inputs to the ADS1201, such as A_{IN}, REF_{IN}, and MCLK, should not be present before the analog and digital supplies are on. Violating this condition could cause latch-up. If these signals are present before the supplies are on, series resistors should be used to limit the input current.

If one supply must be used to power the ADS1201, the system's analog supply should be used to power both AV_{DD} and DV_{DD}. Experimentation may be the best way to determine the appropriate connection between AV_{DD} and DV_{DD}.

GROUNDING

The analog and digital sections of the design should be carefully and cleanly partitioned. Each section should have its own ground plane with no overlap between them. AGND should be connected to the analog ground plane as well as all other analog grounds. DGND should be connected to the digital ground plane and all digital signals referenced to this plane.

The ADS1201 pinout is such that the converter is cleanly separated into an analog and digital portion. This should allow simple layout of the analog and digital sections of the design.

For a signal converter system, AGND and DGND of the ADS1201 can be connected together. Do not join the ground planes, but connect the two with a moderate signal trace underneath the converter. For multiple converters, connect the two ground planes at one location as central to all of the converters as possible. In some cases, experimentation may be required to find the best point to connect the two planes together. Experimentation may be the best way to determine the appropriate connection between AGND and DGND.

DECOUPLING

Good decoupling practices should be used for the ADS1201 and for all components in the design. All decoupling capacitors, specifically the 0.1µF ceramic capacitors, should be placed as close as possible to the pin being decoupled. A 1µF and 10µF capacitor, in parallel with the 0.1µF ceramic capacitor, should be used to decouple AV_{DD} to AGND. At a minimum, a 0.1µF ceramic capacitor should be used to decouple DV_{DD} to DGND, as well as for the digital supply on each digital component.

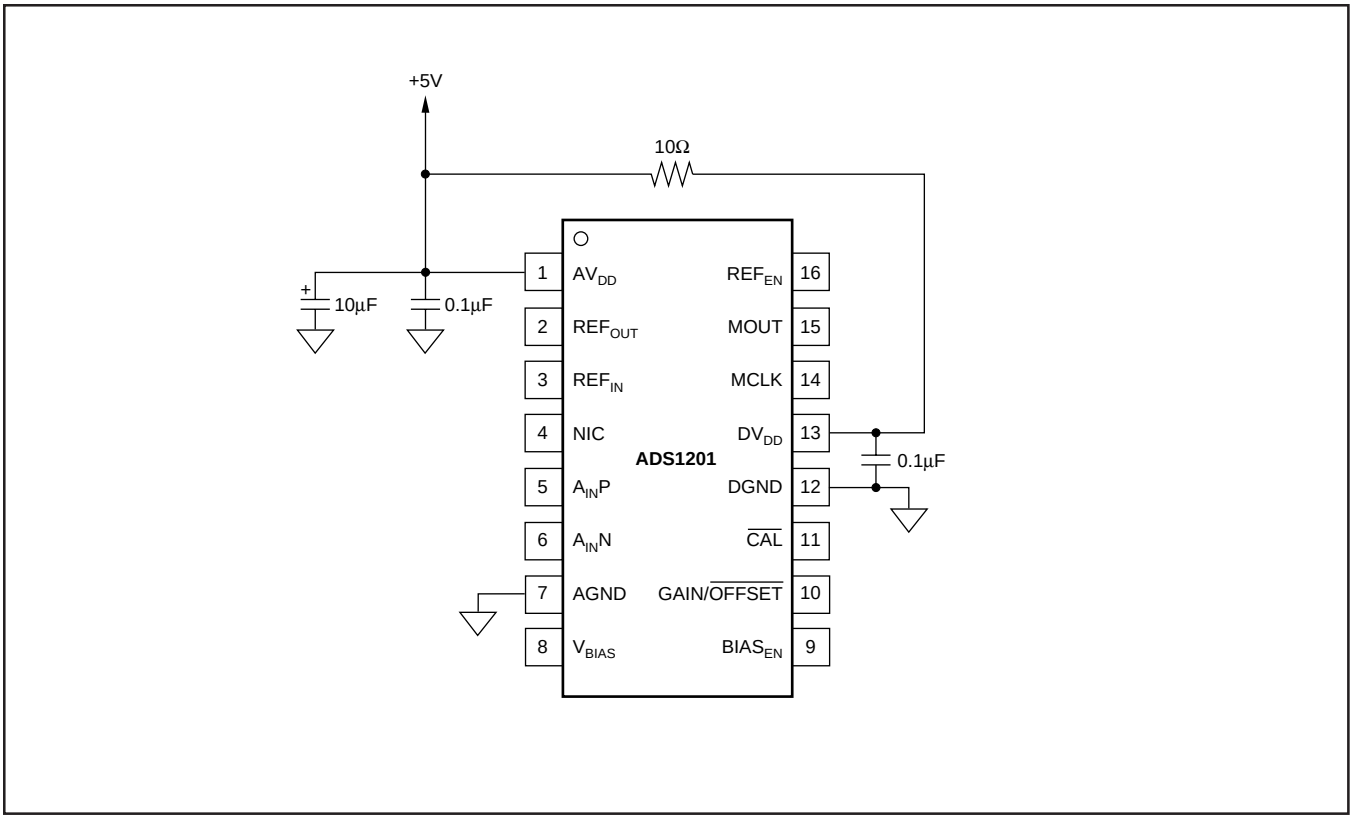


FIGURE 10. Power Supply Connection Using One Power Plane and One Digital Plane.

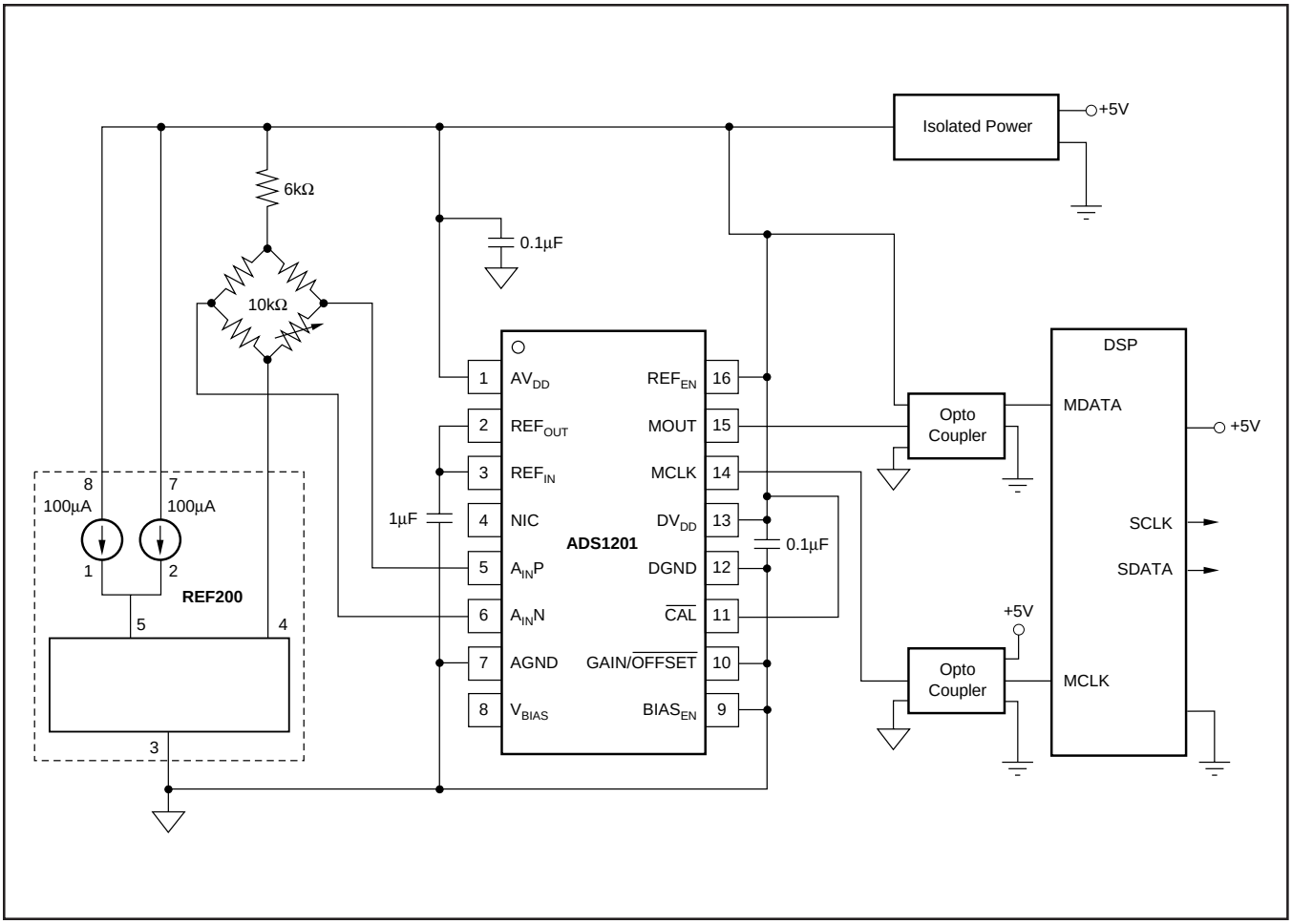


FIGURE 11. Bridge Transducer Interface with Current Excitation.

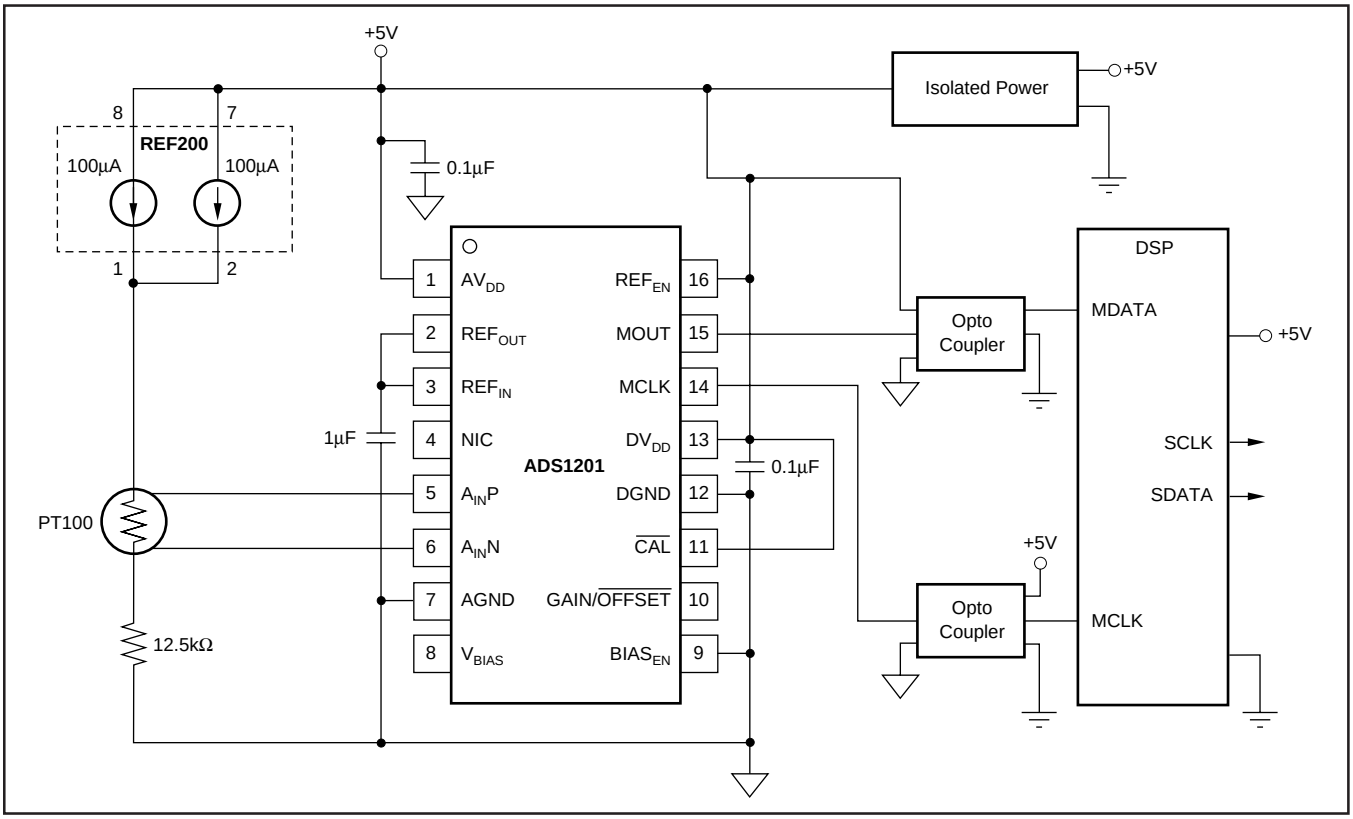


FIGURE 12. PT100 Interface with Current Excitation.

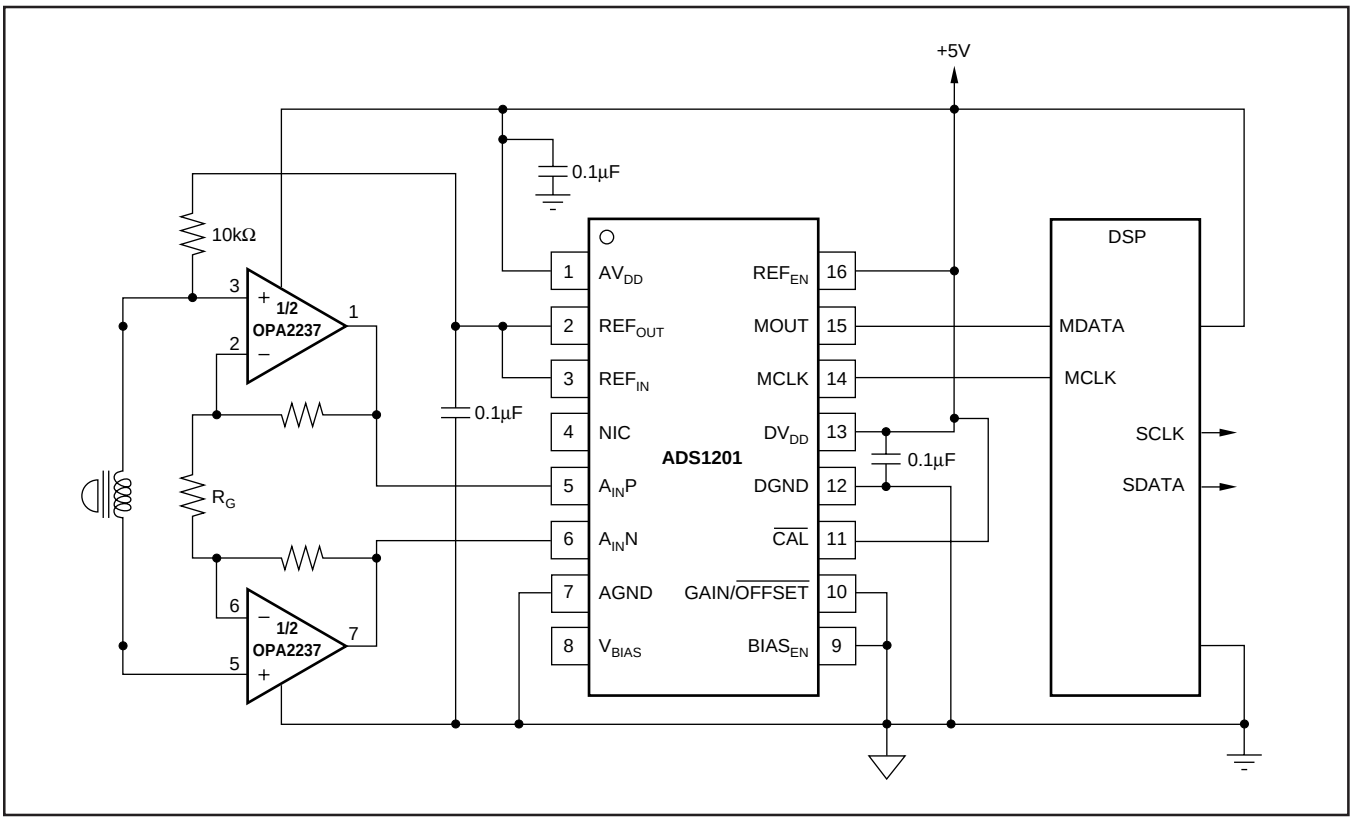


FIGURE 13. Geophone Interface.

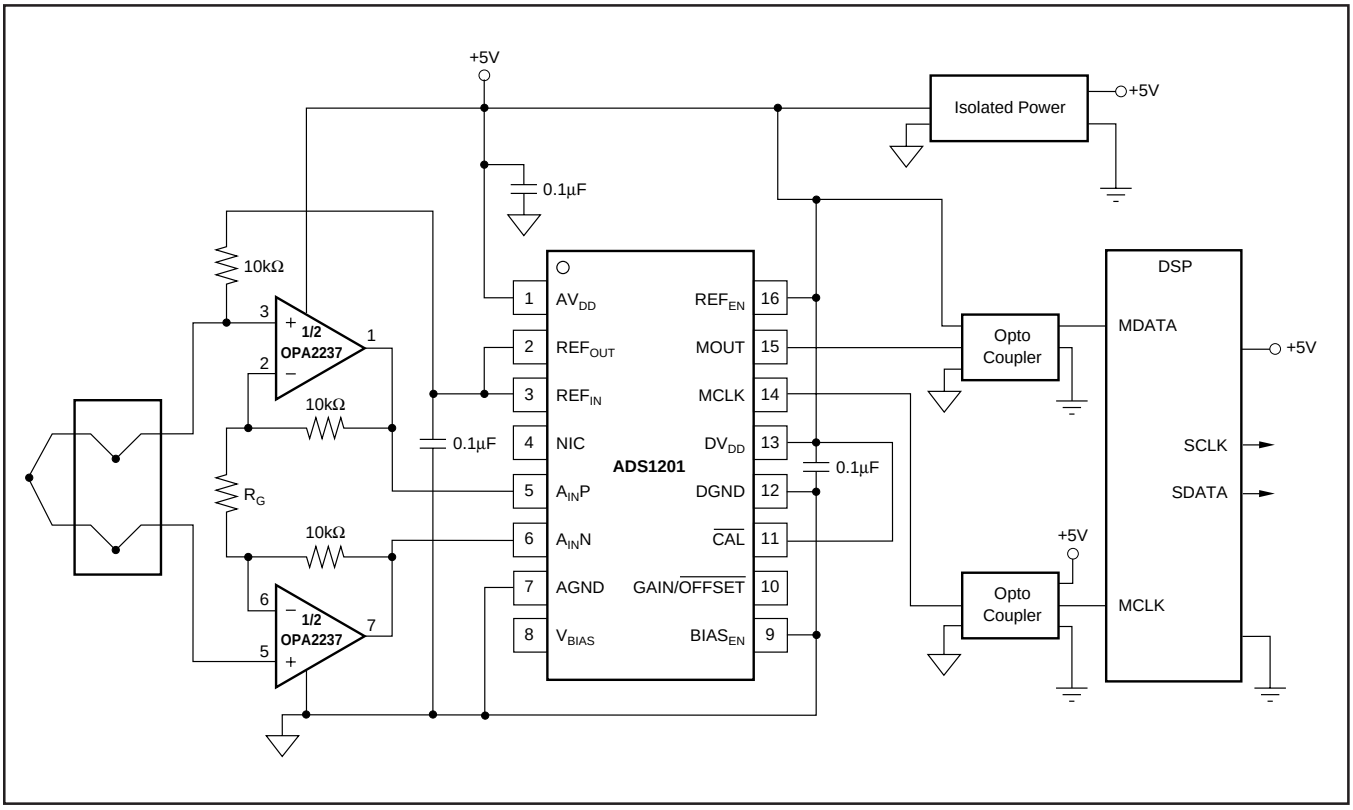


FIGURE 14. Single-Supply, High Accuracy Thermocouple Interface.

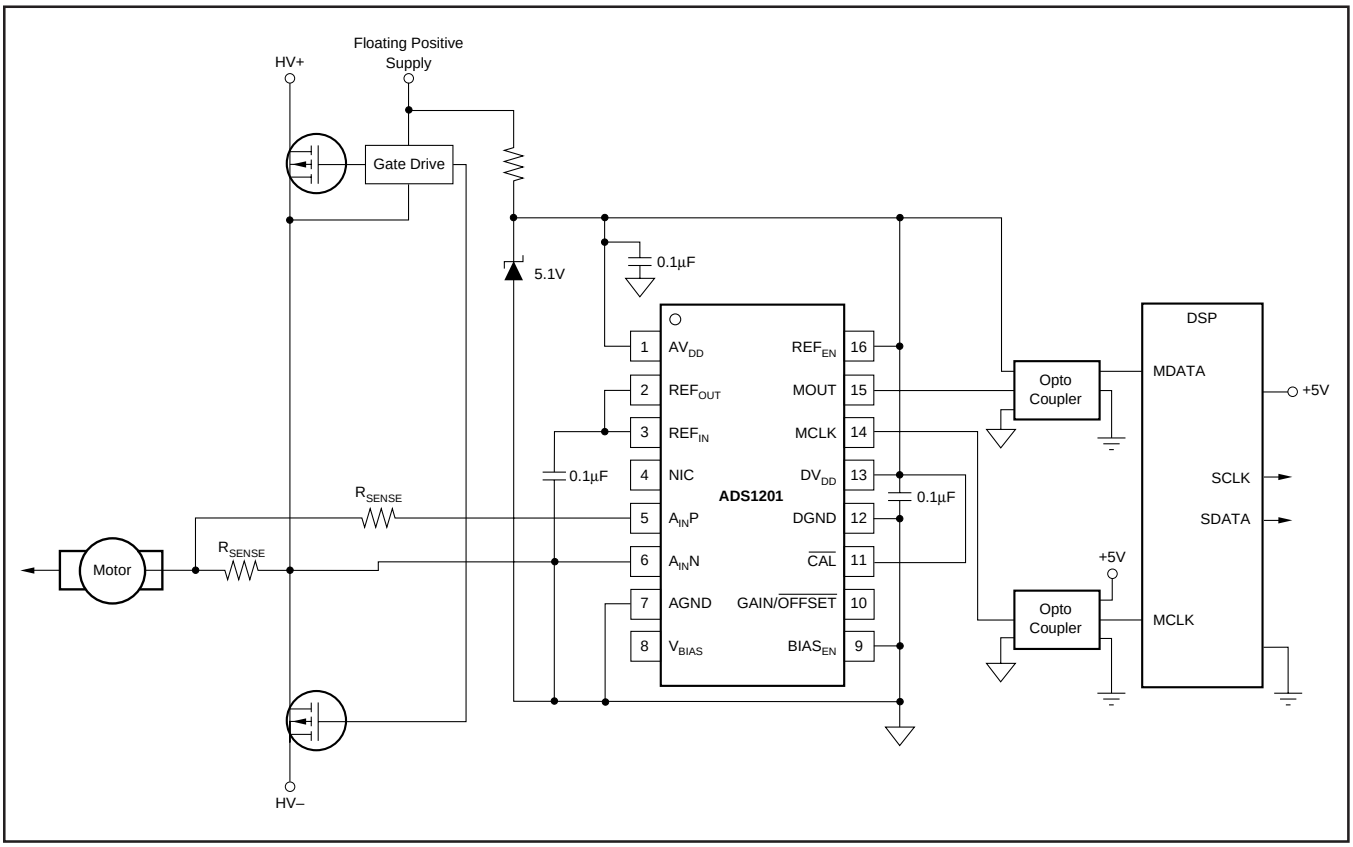


FIGURE 15. Motor Controller Sensing Circuit.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1201U	ACTIVE	SOIC	DW	16	40	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1201U	Samples
ADS1201U/1K	ACTIVE	SOIC	DW	16	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS1201U	Samples
ADS1201UG4	ACTIVE	SOIC	DW	16	40	TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

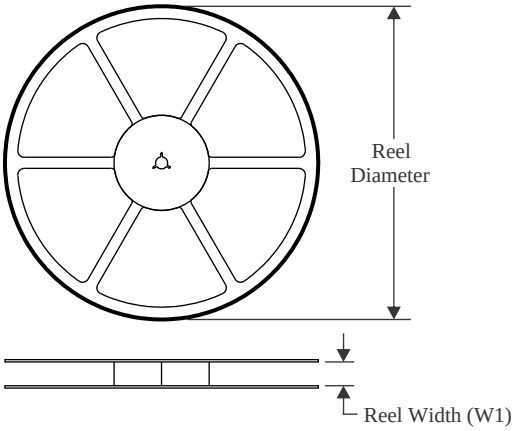
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

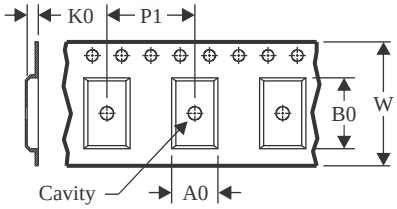
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

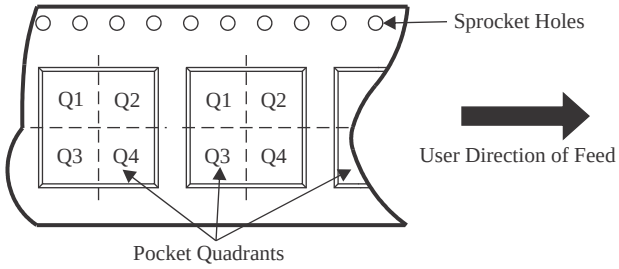


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

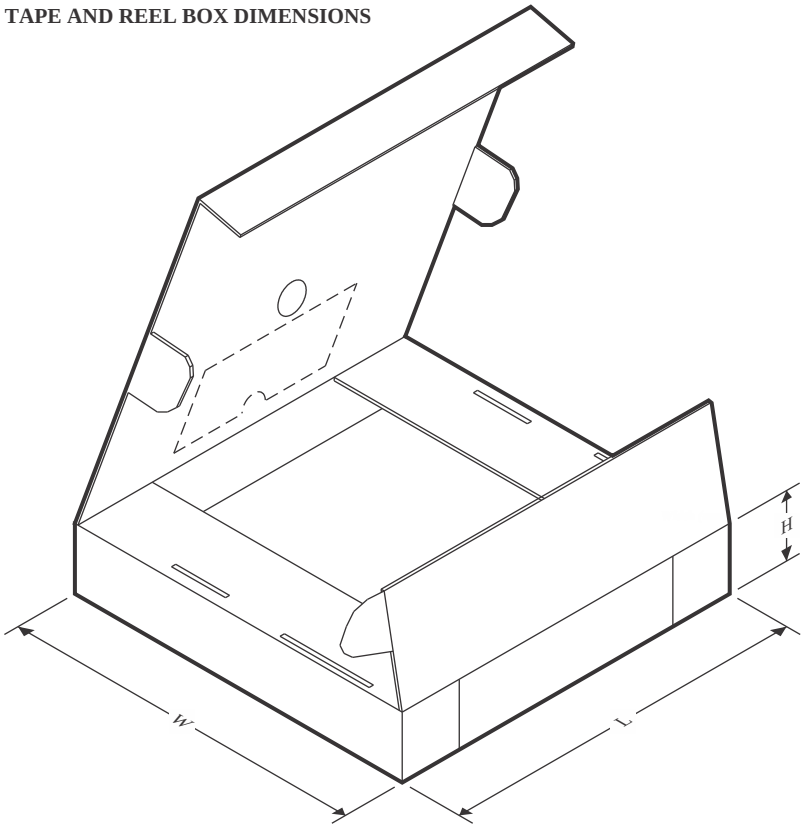
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1201U/1K	SOIC	DW	16	1000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

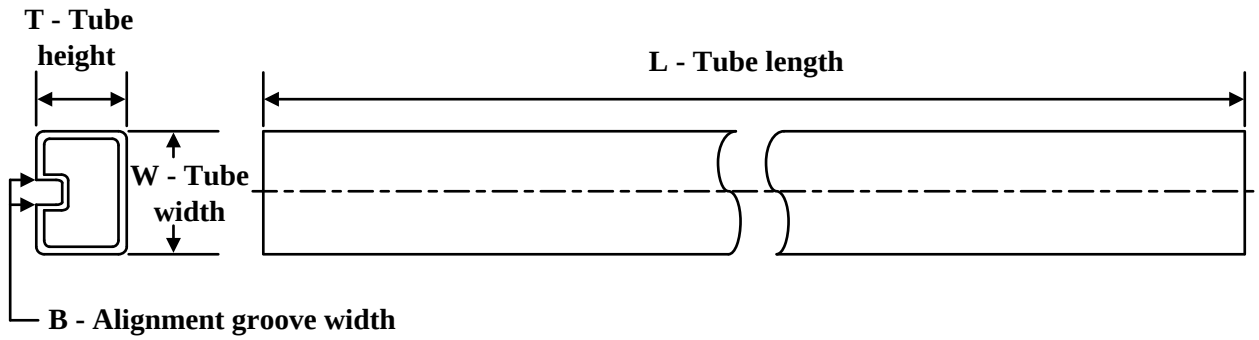
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1201U/1K	SOIC	DW	16	1000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS1201U	DW	SOIC	16	40	507	12.83	5080	6.6

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265