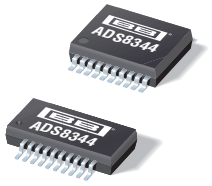
ADS8344



SBAS139E – SEPTEMBER 2000 – REVISED SEPTEMBER 2006

16-Bit, 8-Channel Serial Output Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- PIN FOR PIN WITH ADS7844
- SINGLE SUPPLY: 2.7V to 5V
- 8-CHANNEL SINGLE-ENDED OR 4-CHANNEL DIFFERENTIAL INPUT
- UP TO 100kHz CONVERSION RATE
- 84dB SINAD
- SERIAL INTERFACE
- QSOP-20 AND SSOP-20 PACKAGES

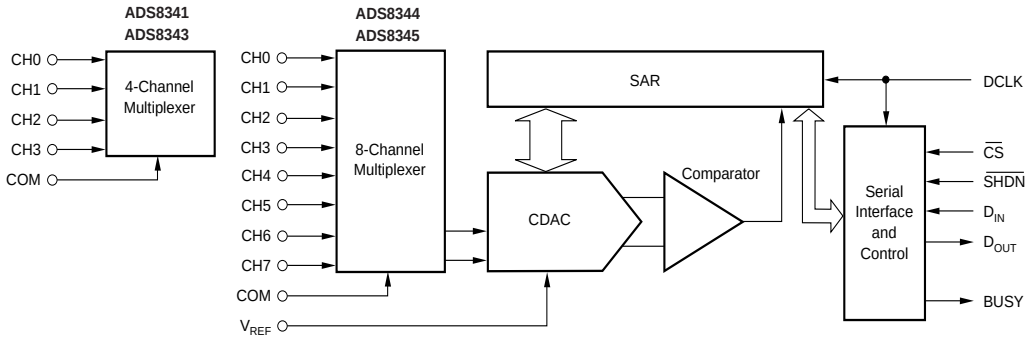
APPLICATIONS

- DATA ACQUISITION
- TEST AND MEASUREMENT EQUIPMENT
- INDUSTRIAL PROCESS CONTROL
- PERSONAL DIGITAL ASSISTANTS
- BATTERY-POWERED SYSTEMS

DESCRIPTION

The ADS8344 is an 8-channel, 16-bit, sampling Analog-to-Digital (A/D) converter with a synchronous serial interface. Typical power dissipation is 10mW at a 100kHz throughput rate and a +5V supply. The reference voltage (V_{REF}) can be varied between 500mV and V_{CC}, providing a corresponding input voltage range of 0V to V_{REF}. The device includes a shutdown mode that reduces power dissipation to under 15µW. The ADS8344 is tested down to 2.7V operation.

Low power, high speed, and an on-board multiplexer make the ADS8344 ideal for battery-operated systems such as personal digital assistants, portable multi-channel data loggers, and measurement equipment. The serial interface also provides low-cost isolation for remote data acquisition. The ADS8344 is available in a QSOP-20 or SSOP-20 package and is ensured over the –40°C to +85°C temperature range.



ABSOLUTE MAXIMUM RATINGS[1]

$+V_{CC}$ to GND	–0.3V to +6V
Analog Inputs to GND	–0.3V to $+V_{CC}$ + 0.3V
Digital Inputs to GND	–0.3V to +6V
Power Dissipation	250mW
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

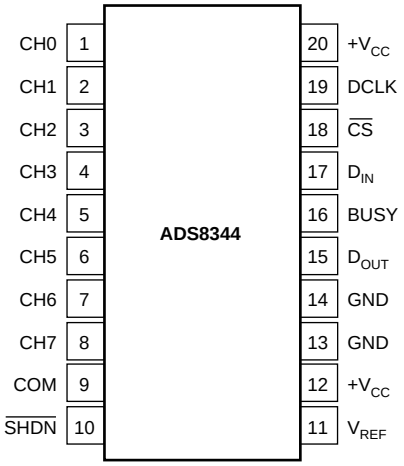
PACKAGE/ORDERING INFORMATION[1]

PRODUCT	MINIMUM RELATIVE ACCURACY (LSB)	MAXIMUM GAIN ERROR (%)	SPECIFIED TEMPERATURE RANGE	PACKAGE DESIGNATOR	PACKAGE-LEAD	PACKAGE DRAWING NUMBER	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8344E	8	±0.05	–40°C to +85°C	DBQ	QSOP-20	DBQ	ADS8344E	Rails, 56
"	"	"	"	"	"	"	ADS8344E/2K5	Tape and Reel, 2500
ADS8344N	"	"	"	DB	SSOP-20	DB	ADS8344N	Rails, 68
"	"	"	"	"	"	"	ADS8344N/1K	Tape and Reel, 1000
ADS8344EB	6	±0.024	–40°C to +85°C	DBQ	QSOP-20	DBQ	ADS8344EB	Rails, 56
"	"	"	"	"	"	"	ADS8344EB/2K5	Tape and Reel, 2500
ADS8344NB	"	"	"	DB	SSOP-20	DB	ADS8344NB	Rails, 68
"	"	"	"	"	"	"	ADS8344NB/1K	Tape and Reel, 1000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

PIN CONFIGURATION

Top View **SSOP**



PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	CH0	Analog Input Channel 0
2	CH1	Analog Input Channel 1
3	CH2	Analog Input Channel 2
4	CH3	Analog Input Channel 3
5	CH4	Analog Input Channel 4
6	CH5	Analog Input Channel 5
7	CH6	Analog Input Channel 6
8	CH7	Analog Input Channel 7
9	COM	Ground reference for analog inputs. Sets zero code voltage in single–ended mode. Connect this pin to ground or ground reference point.
10	$\overline{SHDN}$	Shutdown. When LOW, the device enters a very low-power shutdown mode.
11	V_{REF}	Voltage Reference Input. See Electrical Characteristics Table for ranges.
12	$+V_{CC}$	Power Supply, 2.7V to 5V
13	GND	Ground
14	GND	Ground
15	D_{OUT}	Serial Data Output. Data is shifted on the falling edge of DCLK. This output is high impedance when $\overline{CS}$ is HIGH.
16	BUSY	Busy Output. Busy goes LOW when the D_{IN} control bits are being read and also when the device is converting. The Output is high impedance when $\overline{CS}$ is HIGH.
17	D_{IN}	Serial Data Input. If $\overline{CS}$ is LOW, data is latched on rising edge of D_{CLK}.
18	$\overline{CS}$	Chip Select Input. Active LOW. Data will not be clocked into D_{IN} unless $\overline{CS}$ is LOW. When $\overline{CS}$ is HIGH, D_{OUT} is high impedance.
19	DCLK	External Clock Input. The clock speed determines the conversion rate by the equation $f_{DCLK} = 24 \cdot f_{SAMPLE}$.
20	$+V_{CC}$	Power Supply

ELECTRICAL CHARACTERISTICS: +5V

At T_A = –40°C to +85°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS8344E, N			ADS8344EB, NB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			**16**				*	**BITS**
ANALOG INPUT								
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ + 0.2	*		*	V
	Negative Input	–0.2		+1.25	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		14			15			Bits
Integral Linearity Error				8			6	LSB
Offset Error				±2			±1	mV
Offset Error Match			1.2	4		*	*	LSB(1)
Gain Error				±0.05			±0.024	%
Gain Error Match			1.0	4		*	*	LSB
Noise			20			*		µVrms
Power-Supply Rejection	+4.75V < V_{CC} < 5.25V		3			*		LSB(1)
SAMPLING DYNAMICS								
Conversion Time				16			*	CLK Cycles
Acquisition Time		4.5			*			CLK Cycles
Throughput Rate				100			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
Internal Clock Frequency	$\overline{SHDN}$ = V_{DD}		2.4			*		MHz
External Clock Frequency		0.024		2.4	*		*	MHz
	Data Transfer Only	0		2.4	*		*	MHz
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion(2)	V_{IN} = 5Vp-p at 10kHz		–90			*		dB
Signal-to-(Noise + Distortion)	V_{IN} = 5Vp-p at 10kHz		86			*		dB
Spurious–Free Dynamic Range	V_{IN} = 5Vp-p at 10kHz		92			*		dB
Channel-to-Channel Isolation	V_{IN} = 5Vp-p at 10kHz		100			*		dB
REFERENCE INPUT								
Range		0.5		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			40	100		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	| I_{IH} | ≤ +5µA	3.0		5.5	*		*	V
V_{IL}	| I_{IL} | ≤ +5µA	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	3.5			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER-SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	4.75		5.25	*		*	V
Quiescent Current			1.5	2.0			*	mA
	f_{SAMPLE} = 100kHz		300			*		µA
	Power-Down Mode(3), $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation			7.5	10			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

* Same specifications as ADS8344E, N.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +5.0V, one LSB is 76µV. (2) First nine harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

ELECTRICAL CHARACTERISTICS: +2.7V

At T_A = –40°C to +85°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.7V, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

PARAMETER	CONDITIONS	ADS8344E, N			ADS8344EB, NB			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
RESOLUTION			**16**				*	**BITS**
ANALOG INPUT								
Full-Scale Input Span	Positive Input - Negative Input	0		V_{REF}	*		*	V
Absolute Input Range	Positive Input	–0.2		$+V_{CC}$ + 0.2	*		*	V
	Negative Input	–0.2		+0.2	*		*	V
Capacitance			25			*		pF
Leakage Current			±1			*		µA
SYSTEM PERFORMANCE								
No Missing Codes		14			15			Bits
Integral Linearity Error				12			8	LSB
Offset Error				±1			0.5	mV
Offset Error Match			1.2	4		*	*	LSB
Gain Error				±0.05			±0.024	% of FSR
Gain Error Match			1	4		*	*	LSB
Noise			20			*		µVrms
Power-Supply Rejection	+2.7 < V_{CC} < +3.3V		3			*		LSB[1]
SAMPLING DYNAMICS								
Conversion Time				16			*	CLK Cycles
Acquisition Time		4.5			*			CLK Cycles
Throughput Rate				100			*	kHz
Multiplexer Settling Time			500			*		ns
Aperture Delay			30			*		ns
Aperture Jitter			100			*		ps
Internal Clock Frequency	$\overline{SHDN}$ = V_{DD}		2.4			*		MHz
External Clock Frequency		0.024		2.4				MHz
	When used with Internal Clock	0.024		2.0	*		*	MHz
	Data Transfer Only	0		2.4	*		*	MHz
DYNAMIC CHARACTERISTICS								
Total Harmonic Distortion[2]	V_{IN} = 2.5Vp-p at 1kHz		–90			*		dB
Signal-to-(Noise + Distortion)	V_{IN} = 2.5Vp-p at 1kHz		86			*		dB
Spurious-Free Dynamic Range	V_{IN} = 2.5Vp-p at 1kHz		92			*		dB
Channel-to-Channel Isolation	V_{IN} = 2.5Vp-p at 10kHz		100			*		dB
REFERENCE INPUT								
Range		0.5		$+V_{CC}$	*		*	V
Resistance	DCLK Static		5			*		GΩ
Input Current			13	40		*	*	µA
	f_{SAMPLE} = 12.5kHz		2.5			*		µA
	DCLK Static		0.001	3		*	*	µA
DIGITAL INPUT/OUTPUT								
Logic Family			CMOS			*		
Logic Levels								
V_{IH}	| I_{IH} | ≤ +5µA	$+V_{CC}$ • 0.7		5.5	*		*	V
V_{IL}	| I_{IL} | ≤ +5µA	–0.3		+0.8	*		*	V
V_{OH}	I_{OH} = –250µA	$+V_{CC}$ • 0.8			*			V
V_{OL}	I_{OL} = 250µA			0.4			*	V
Data Format			Straight Binary			*		
POWER-SUPPLY REQUIREMENTS								
$+V_{CC}$	Specified Performance	2.7		3.6	*		*	V
Quiescent Current			1.2	1.85		*	*	mA
	f_{SAMPLE} = 100kHz		220			*		µA
	Power-Down Mode[3], $\overline{CS}$ = $+V_{CC}$			3			*	µA
Power Dissipation			3.2	5			*	mW
TEMPERATURE RANGE								
Specified Performance		–40		+85	*		*	°C

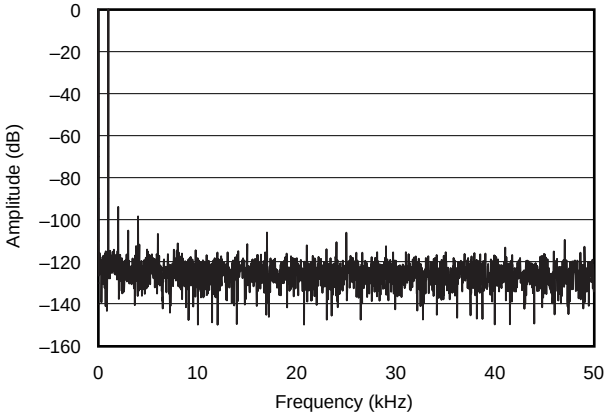
* Same specifications as ADS8344E, N.

NOTES: (1) LSB means Least Significant Bit. With V_{REF} equal to +2.5V, one LSB is 38µV. (2) First nine harmonics of the test frequency. (3) Auto power-down mode (PD1 = PD0 = 0) active or $\overline{SHDN}$ = GND.

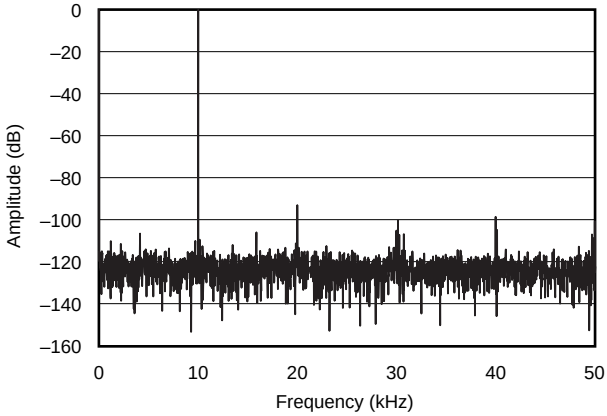
TYPICAL CHARACTERISTICS: +5V

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 100kHz, and f_{DCLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

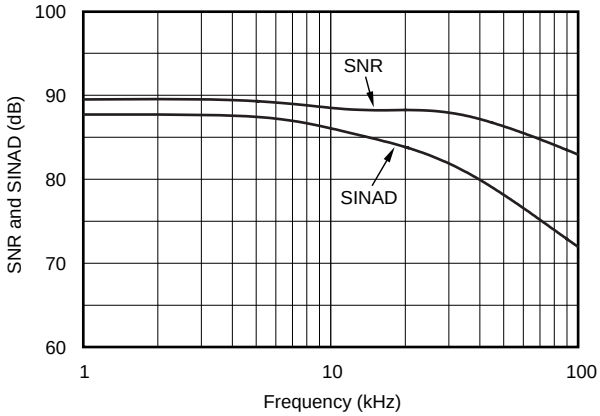
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1.001kHz, –0.2dB)



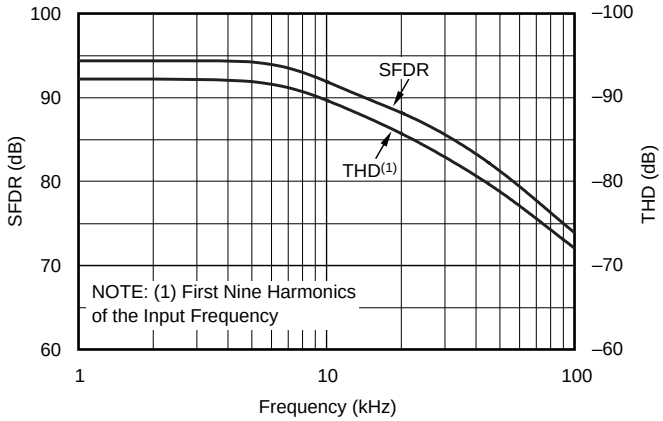
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 9.985kHz, –0.2dB)



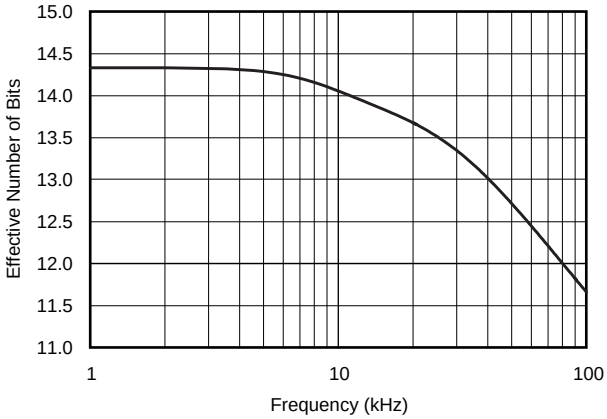
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



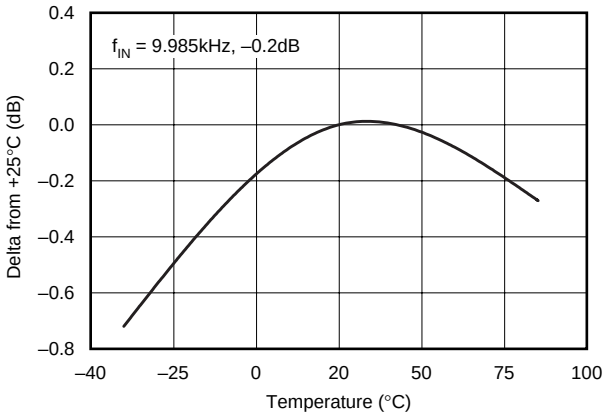
SPURIOUS-FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



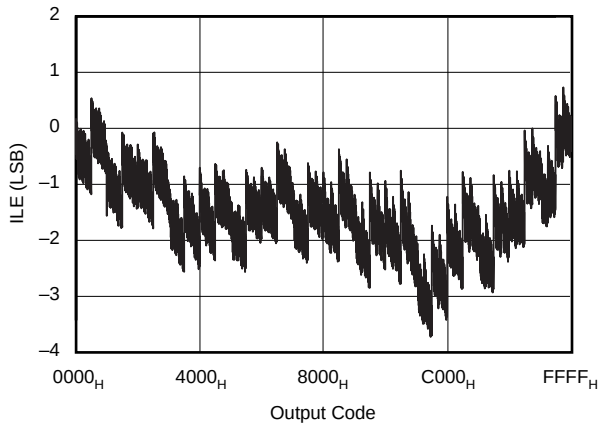
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



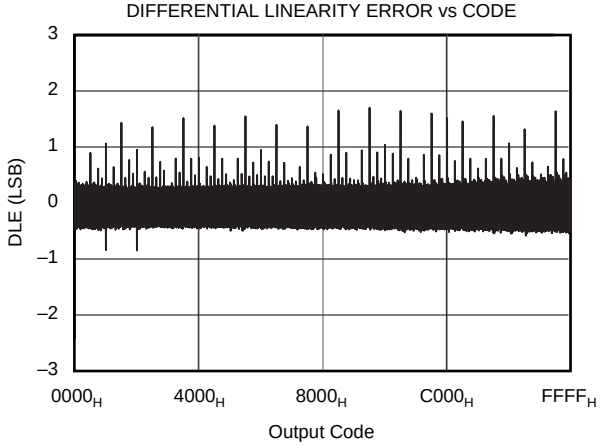
TYPICAL CHARACTERISTICS: +5V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 100kHz, and f_{DCLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

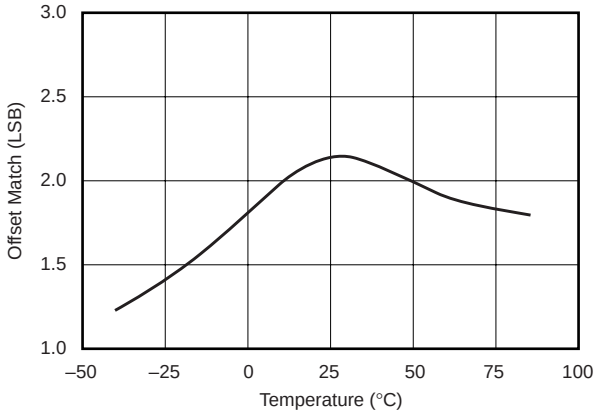
INTEGRAL LINEARITY ERROR vs CODE



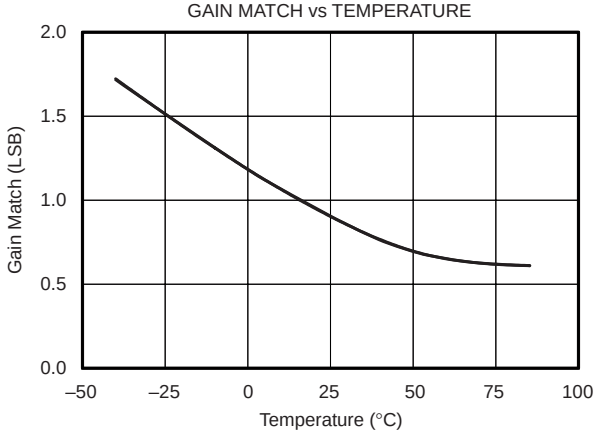
DIFFERENTIAL LINEARITY ERROR vs CODE



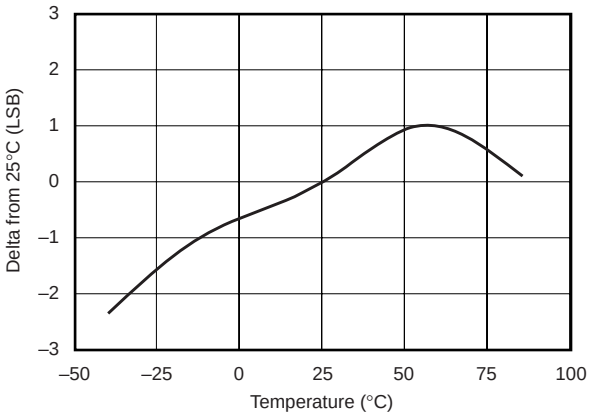
WORST CASE CHANNEL-TO-CHANNEL OFFSET MATCH vs TEMPERATURE



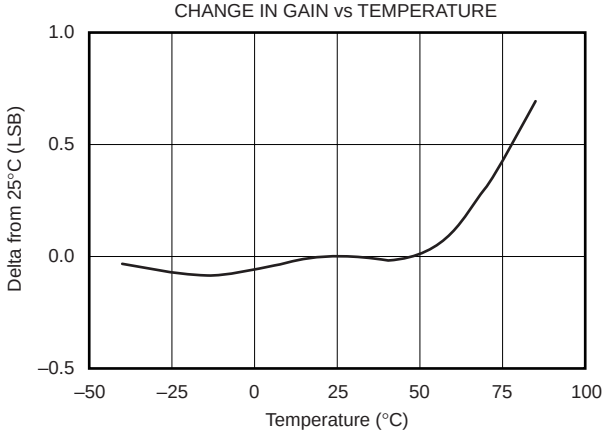
WORST CASE CHANNEL-TO-CHANNEL GAIN MATCH vs TEMPERATURE



CHANGE IN OFFSET vs TEMPERATURE



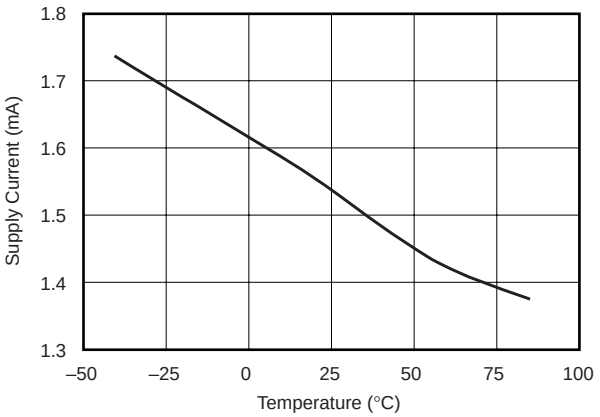
CHANGE IN GAIN vs TEMPERATURE



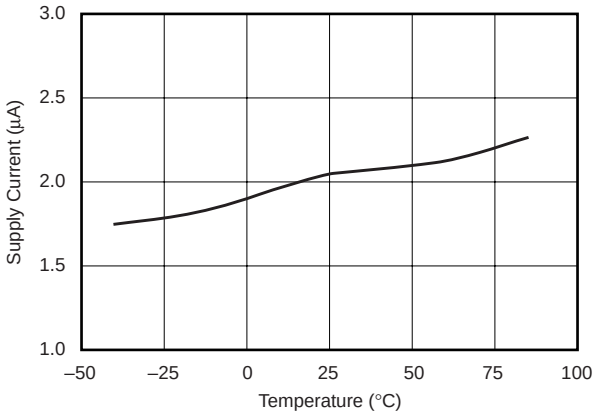
TYPICAL CHARACTERISTICS: +5V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +5V, V_{REF} = +5V, f_{SAMPLE} = 100kHz, and f_{DCLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

SUPPLY CURRENT vs TEMPERATURE



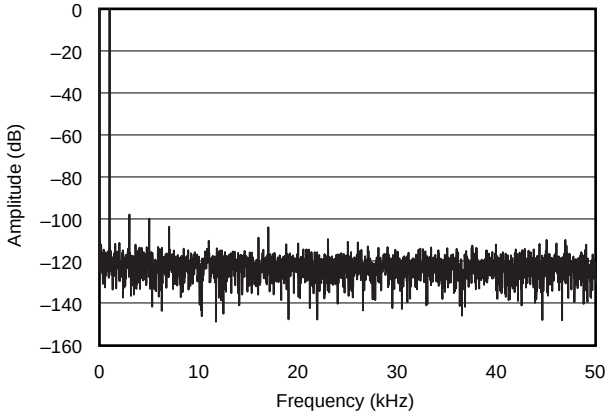
POWER DOWN SUPPLY CURRENT vs TEMPERATURE



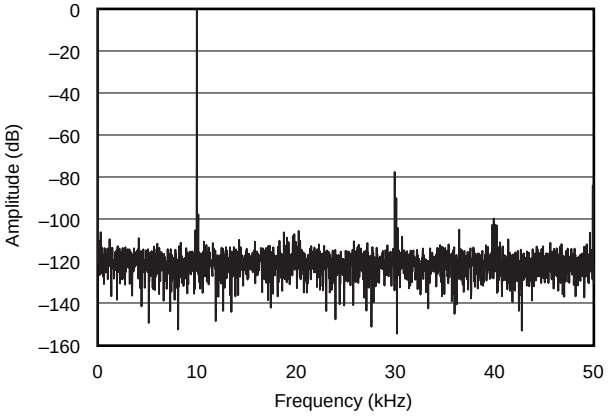
TYPICAL CHARACTERISTICS: +2.7V

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.7V, f_{SAMPLE} = 100kHz, and f_{DCLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

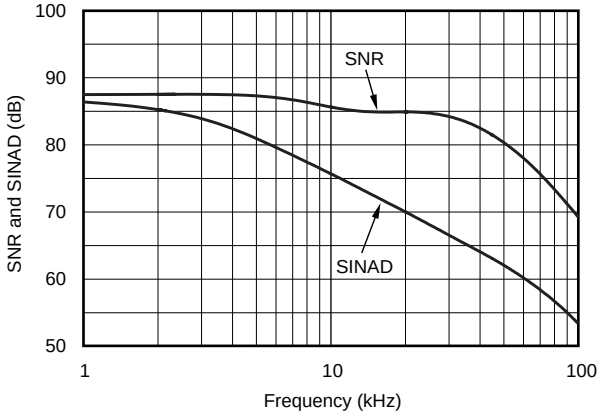
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 1.001kHz, –0.2dB)



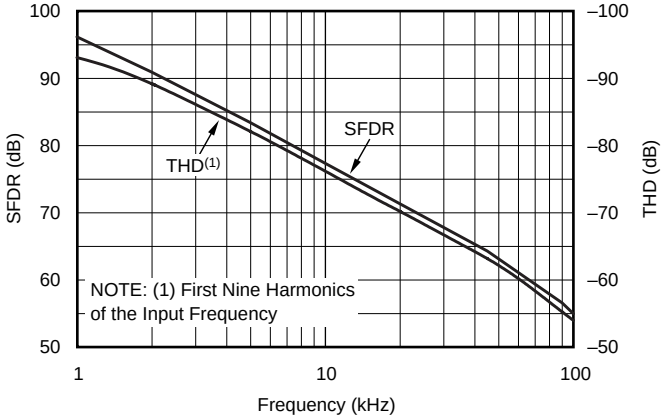
FREQUENCY SPECTRUM
(4096 Point FFT; f_{IN} = 9.985kHz, –0.2dB)



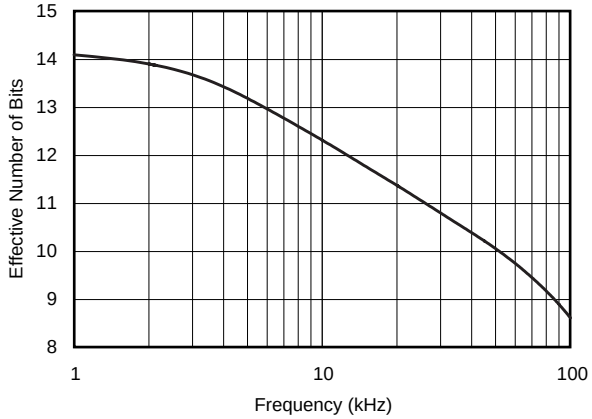
SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-
(NOISE+DISTORTION) vs INPUT FREQUENCY



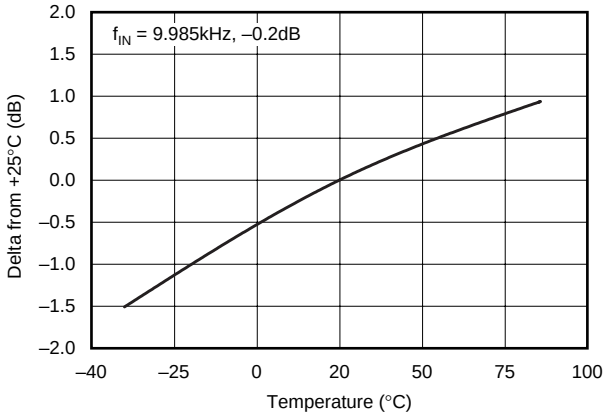
SPURIOUS-FREE DYNAMIC RANGE AND TOTAL
HARMONIC DISTORTION vs INPUT FREQUENCY



EFFECTIVE NUMBER OF BITS
vs INPUT FREQUENCY



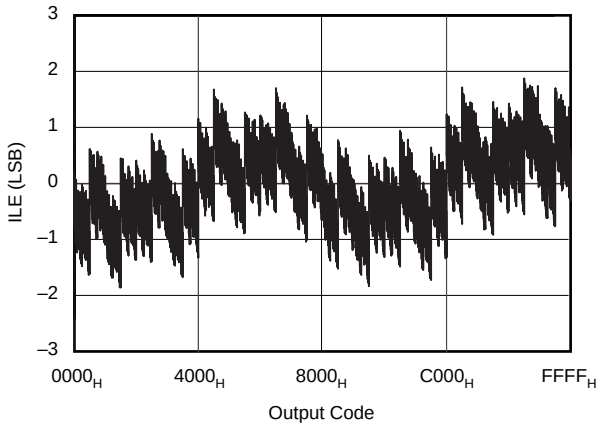
CHANGE IN SIGNAL-TO-(NOISE+DISTORTION)
vs TEMPERATURE



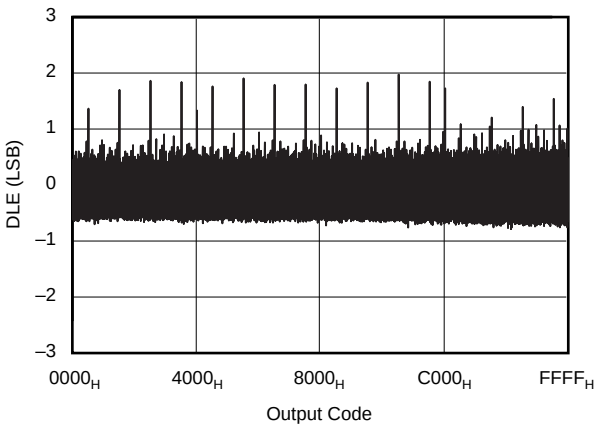
TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.7V, f_{SAMPLE} = 100kHz, and f_{DCLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

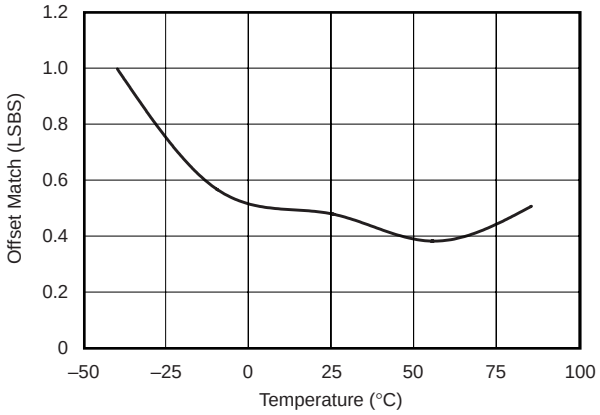
INTEGRAL LINEARITY ERROR vs CODE



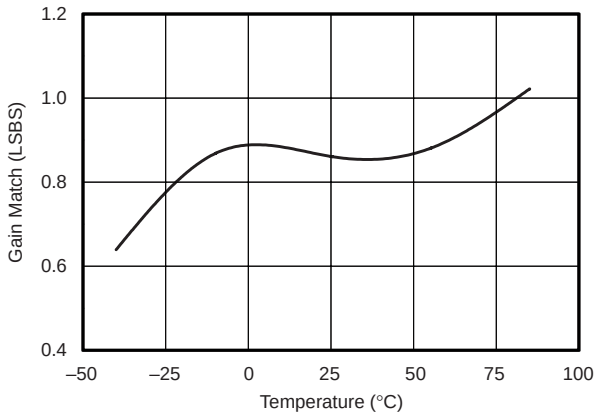
DIFFERENTIAL LINEARITY ERROR vs CODE



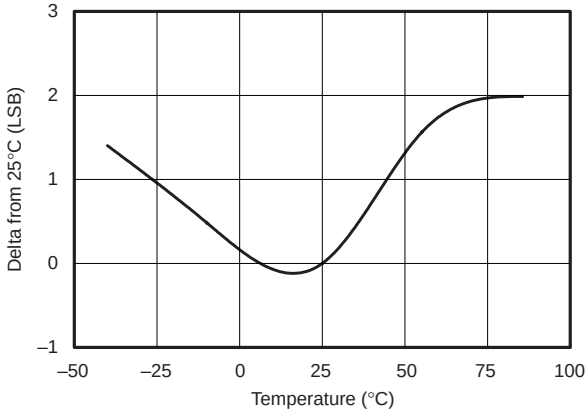
WORST CASE CHANNEL-TO-CHANNEL OFFSET MATCH vs TEMPERATURE



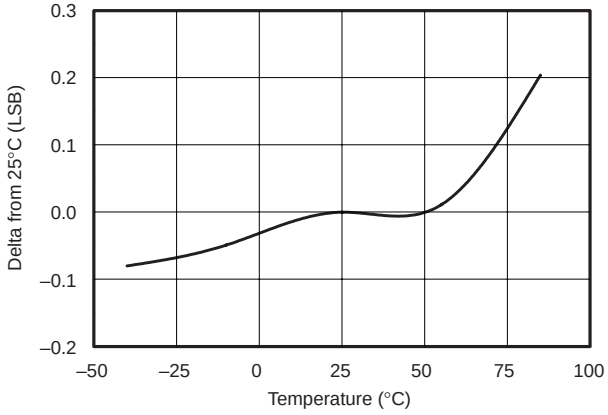
WORST CASE CHANNEL-TO-CHANNEL GAIN MATCH vs TEMPERATURE



CHANGE IN OFFSET vs TEMPERATURE



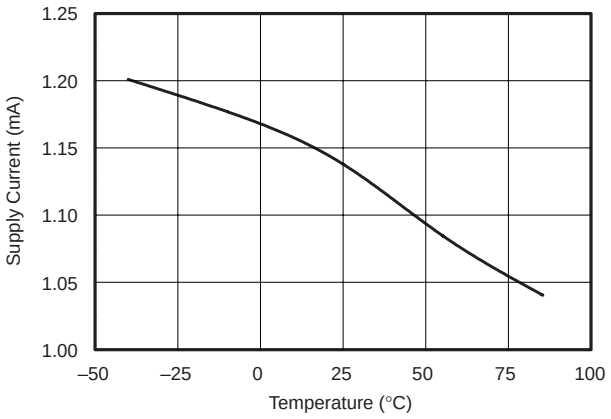
CHANGE IN GAIN vs TEMPERATURE



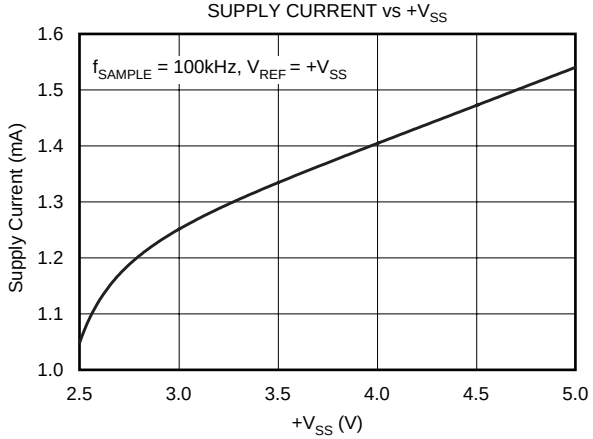
TYPICAL CHARACTERISTICS: +2.7V (Cont.)

At T_A = +25°C, $+V_{CC}$ = +2.7V, V_{REF} = +2.7V, f_{SAMPLE} = 100kHz, and f_{DCLK} = 24 • f_{SAMPLE} = 2.4MHz, unless otherwise noted.

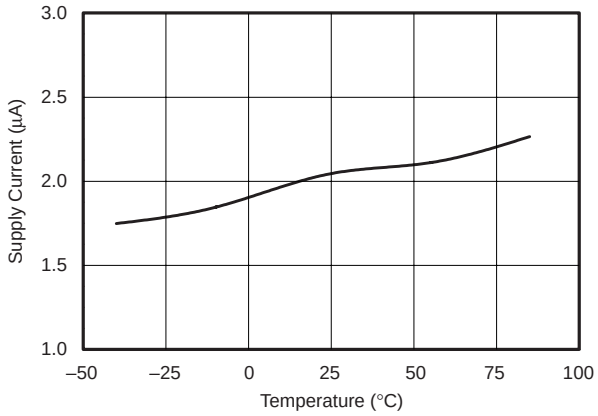
SUPPLY CURRENT vs TEMPERATURE



SUPPLY CURRENT vs $+V_{SS}$



POWER DOWN SUPPLY CURRENT
vs TEMPERATURE



THEORY OF OPERATION

The ADS8344 is a classic Successive Approximation Register (SAR) A/D converter. The architecture is based on capacitive redistribution that inherently includes a sample-and-hold function. The converter is fabricated on a 0.6µs CMOS process.

The basic operation of the ADS8344 is shown in Figure 1. The device requires an external reference and an external clock. It operates from a single supply of 2.7V to 5.25V. The external reference can be any voltage between 500mV and $+V_{CC}$. The value of the reference voltage directly sets the input range of the converter. The average reference input current depends on the conversion rate of the ADS8344.

The analog input to the converter is differential and is provided via an 8-channel multiplexer. The input can be provided in reference to a voltage on the COM pin (which is generally ground) or differentially by using four of the eight input channels (CH0 - CH7). The particular configuration is selectable via the digital interface.

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7	COM
0	0	0	+IN								–IN
1	0	0		+IN							–IN
0	0	1			+IN						–IN
1	0	1				+IN					–IN
0	1	0					+IN				–IN
1	1	0						+IN			–IN
0	1	1							+IN		–IN
1	1	1								+IN	–IN

TABLE I. Single-Ended Channel Selection (SGL/$\overline{DIF}$ HIGH).

ANALOG INPUT

See Figure 2 for a block diagram of the input multiplexer on the ADS8344. The differential input of the converter is derived from one of the eight inputs in reference to the COM pin, or four of the eight inputs. Table I and Table II show the relationship between the A2, A1, A0, and SGL/$\overline{DIF}$ control bits and the configuration of the analog multiplexer. The control bits are provided serially via the D_{IN} pin (see the Digital Interface section of this data sheet for more details).

When the converter enters the hold mode, the voltage difference between the +IN and –IN inputs is captured on the internal capacitor array (see Figure 2). The voltage on the –IN input is limited between –0.2V and 1.25V, allowing the input to reject small signals that are common to both the +IN and –IN input. The +IN input has a range of –0.2V to $+V_{CC}$ + 0.2V.

The input current on the analog inputs depends on the conversion rate of the device. During the sample period, the source must charge the internal sampling capacitor (typically 25pF). After the capacitor has been fully charged, there is no further input current. The rate of charge transfer from the analog source to the converter is a function of conversion rate.

A2	A1	A0	CH0	CH1	CH2	CH3	CH4	CH5	CH6	CH7
0	0	0	+IN	–IN						
0	0	1			+IN	–IN				
0	1	0					+IN	–IN		
0	1	1							+IN	–IN
1	0	0	–IN	+IN						
1	0	1			–IN	+IN				
1	1	0					–IN	+IN		
1	1	1							–IN	+IN

TABLE II. Differential Channel Control (SGL/$\overline{DIF}$ LOW).

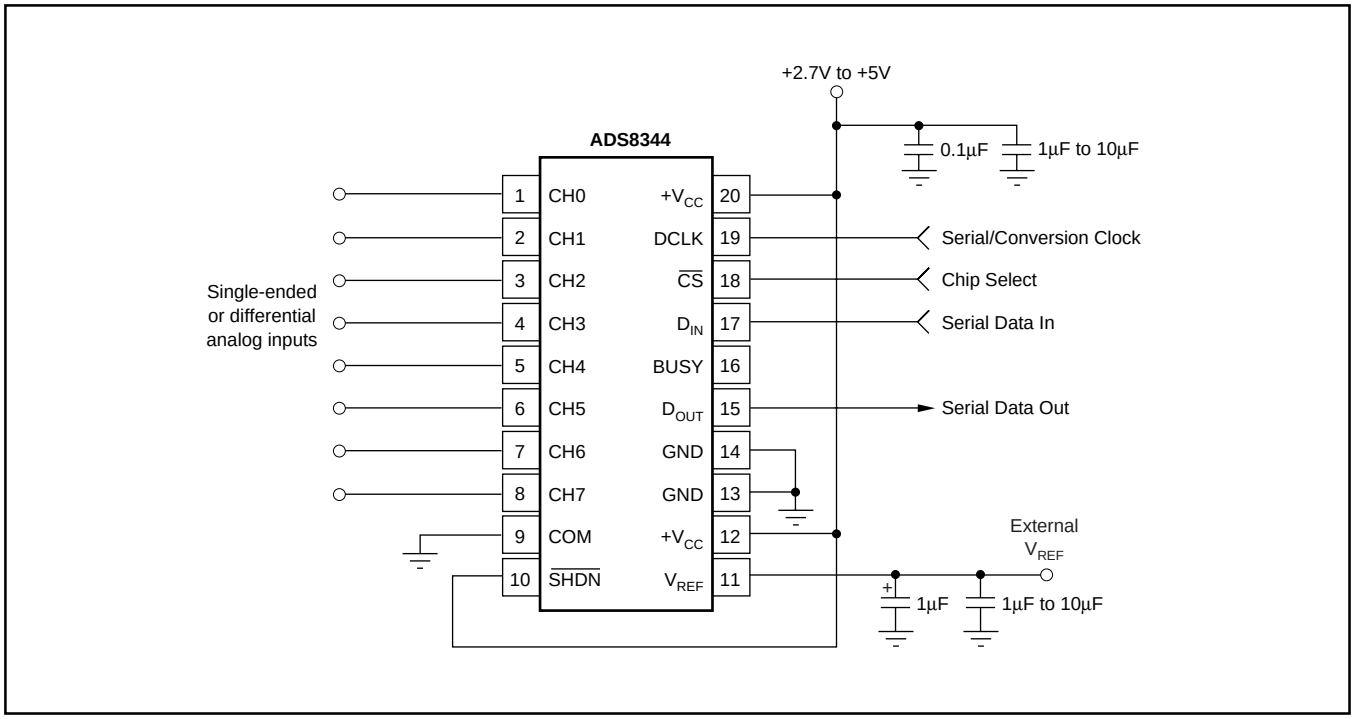


FIGURE 1. Basic Operation of the ADS8344.

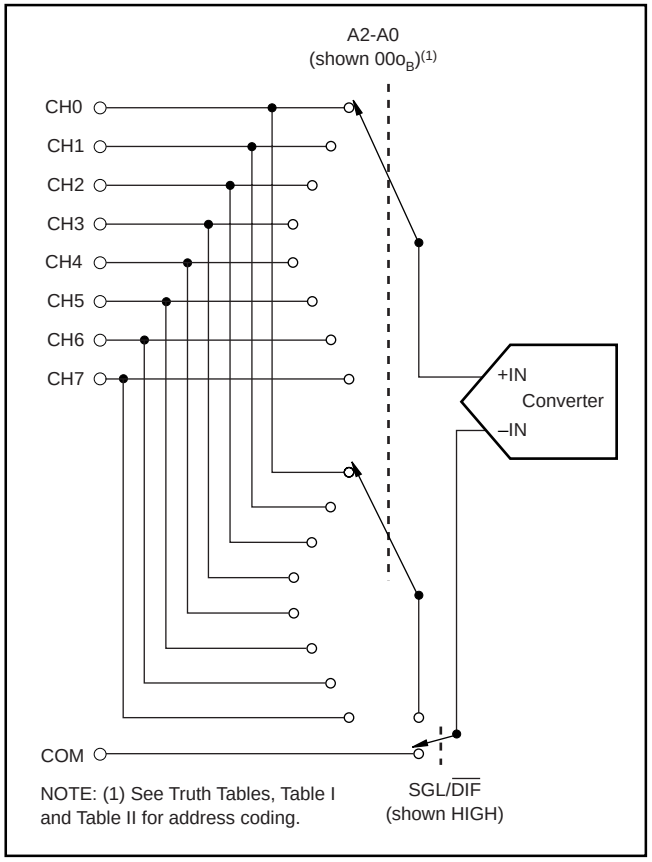


FIGURE 2. Simplified Diagram of the Analog Input.

REFERENCE INPUT

The external reference sets the analog input range. The ADS8344 will operate with a reference in the range of 100mV to +V_{CC}. Keep in mind that the analog input is the difference between the +IN input and the –IN input, as shown in Figure 2. For example, in the single-ended mode, a 1.25V reference with the COM pin grounded, the selected input channel (CH0 - CH7) will properly digitize a signal in the range of 0V to 1.25V. If the COM pin is connected to 0.5V, the input range on the selected channel is 0.5V to 1.75V.

There are several critical items concerning the reference input and its wide-voltage range. As the reference voltage is reduced, the analog voltage weight of each digital output code is also reduced. This is often referred to as the LSB (Least Significant Bit) size and is equal to the reference voltage divided by 65536. Any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For example, if the offset of a given converter is 2LSBs with a 2.5V reference, then it will typically be 10LSBs with a 0.5V reference. In each case, the actual offset of the device is the same, 76.3µV.

Likewise, the noise or uncertainty of the digitized output will increase with lower LSB size. With a reference voltage of 500mV, the LSB size is 7.6µV. This level is below the internal noise of the device. As a result, the digital output code will not be stable and will vary around a mean value by a number of LSBs. The distribution of output codes will be gaussian and the noise can be reduced by simply averaging consecutive conversion results or applying a digital filter.

With a lower reference voltage, care should be taken to provide a clean layout including adequate bypassing, a clean (low-noise, low-ripple) power supply, a low-noise reference, and a low-noise input signal. Because the LSB size is lower, the converter will also be more sensitive to nearby digital signals and electromagnetic interference.

The voltage into the V_{REF} input is not buffered and directly drives the Capacitor Digital-to-Analog Converter (CDAC) portion of the ADS8344. Typically, the input current is 13µA with a 2.5V reference. This value will vary by microamps depending on the result of the conversion. The reference current diminishes directly with both conversion rate and reference voltage. As the current from the reference is drawn on each bit decision, clocking the converter more quickly during a given conversion period will not reduce overall current drain from the reference.

DIGITAL INTERFACE

The ADS8344 has a four-wire serial interface compatible with several microprocessor families (note that the digital inputs are over-voltage tolerant up to +5.5V, regardless of +V_{CC}). Figure 3 shows the typical operation of the ADS8344 digital interface.

Most microprocessors communicate using 8-bit transfers; the ADS8344 can complete a conversion with three such transfers, for a total of 24 clock cycles on the DCLK input, provided the timing is as shown in Figure 3.

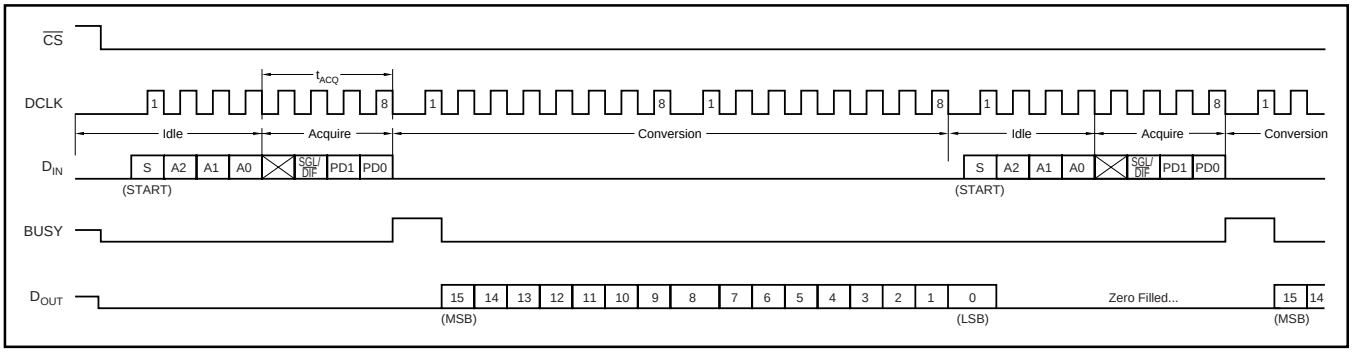


FIGURE 3. Conversion Timing, 24-Clocks per Conversion, 8-Bit Bus Interface. No DCLK Delay Required with Dedicated Serial Port.

The first eight clock cycles are used to provide the control byte via the D_{IN} pin. When the converter has enough information about the following conversion to set the input multiplexer appropriately, it enters the acquisition (sample) mode. After four more clock cycles, the control byte is complete and the converter enters the conversion mode. At this point, the input sample-and-hold goes into the Hold mode. The next sixteen clock cycles accomplish the actual A/D conversion.

Control Byte

See Figure 3 for placement and order of the control bits within the control byte. Tables III and IV give detailed information about these bits. The first bit, the "S" bit, must always be HIGH and indicates the start of the control byte. The ADS8344 will ignore inputs on the D_{IN} pin until the START bit is detected. The next three bits (A2-A0) select the active input channel or channels of the input multiplexer (see Tables I and II and Figure 2).

BIT 7 (MSB)	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0 (LSB)
S	A2	A1	A0	—	SGL/$\overline{\text{DIF}}$	PD1	PD0

TABLE III. Order of the Control Bits in the Control Byte.

BIT	NAME	DESCRIPTION
7	S	Start Bit. Control byte starts with first HIGH bit on D_{IN}.
6 - 4	A2 - A0	Channel Select Bits. Along with the SGL/$\overline{\text{DIF}}$ bit, these bits control the setting of the multiplexer input, see Tables I and II.
2	SGL/$\overline{\text{DIF}}$	Single-Ended/Differential Select Bit. Along with bits A2 - A0, this bit controls the setting of the multiplexer input, see Tables I and II.
1 - 0	PD1 - PD0	Power-Down Mode Select Bits. See Table V for details.

TABLE IV. Descriptions of the Control Bits within the Control Byte.

The SGL/$\overline{\text{DIF}}$-bit controls the multiplexer input mode: either in single-ended mode, where the selected input channel is referenced to the COM pin, or in differential mode, where the two selected inputs provide a differential input. See Tables I and II and Figure 2 for more information. The last two bits (PD1 - PD0) select the power-down mode and Clock mode, as shown in Table V. If both PD1 and PD0 are HIGH, the device is always powered up. If both PD1 and PD0 are LOW, the device enters a power-down mode between conversions. When a new conversion is initiated, the device will resume normal operation instantly—no delay is needed to allow the device to power up and the very first conversion will be valid.

PD1	PD0	DESCRIPTION
0	0	Power-down between conversions. When each conversion is finished, the converter enters a low-power mode. At the start of the next conversion, the device instantly powers up to full power. There is no need for additional delays to assure full operation and the very first conversion is valid.
1	0	Selects Internal Clock Mode.
0	1	Reserved for Future Use.
1	1	No power-down between conversions, device always powered. Selects external clock mode.

TABLE V. Power-Down Selection.

Clock Modes

The ADS8344 can be used with an external serial clock or an internal clock to perform the successive-approximation conversion. In both clock modes, the external clock shifts data in and out of the device. Internal clock mode is selected when PD1 is HIGH and PD0 is LOW.

If the user decides to switch from one clock mode to the other, an extra conversion cycle will be required before the ADS8344 can switch to the new mode. The extra cycle is required because the PD0 and PD1 control bits need to be written to the ADS8344 prior to the change in clock modes.

When power is first applied to the ADS8344, the user must set the desired clock mode. It can be set by writing PD1 = 1 and PD0 = 0 for internal clock mode or PD1 = 1 and PD0 = 1 for external clock mode. After enabling the required clock mode, only then should the ADS8344 be set to power-down between conversions (i.e., PD1 = PD0 = 0). The ADS8344 maintains the clock mode it was in prior to entering the power-down modes.

External Clock Mode

In external clock mode, the external clock not only shifts data in and out of the ADS8344, it also controls the A/D conversion steps. BUSY will go HIGH for one clock period after the last bit of the control byte is shifted in. Successive-approximation bit decisions are made and appear at D_{OUT} on each of the next 16 DCLK falling edges (see Figure 3). Figure 4 shows the BUSY timing in external clock mode.

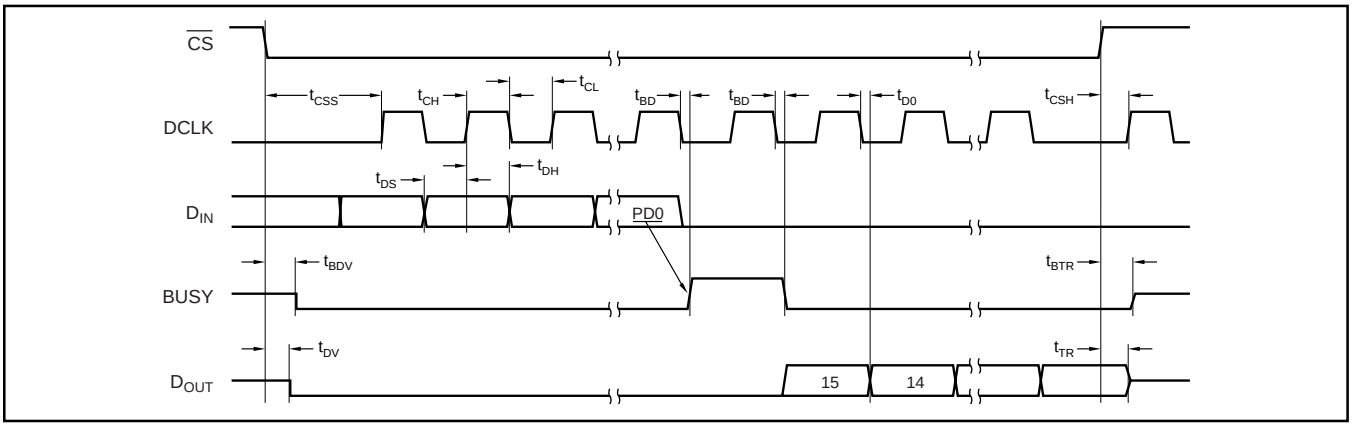


FIGURE 4. Detailed Timing Diagram.

Since one clock cycle of the serial clock is consumed with BUSY going HIGH (while the MSB decision is being made), 16 additional clocks must be given to clock out all 16 bits of data; thus, one conversion takes a minimum of 25 clock cycles to fully read the data. Since most microprocessors communicate in 8-bit transfers, this means that an additional transfer must be made to capture the LSB.

There are two ways of handling this requirement. One is where the beginning of the next control byte appears at the same time the LSB is being clocked out of the ADS8344 (see Figure 3). This method allows for maximum throughput and 24 clock cycles per conversion.

The other method is shown in Figure 5, which uses 32 clock cycles per conversion; the last seven clock cycles simply shift out zeros on the D_{OUT} line. BUSY and D_{OUT} go into a high-impedance state when $\overline{CS}$ goes HIGH; after the next $\overline{CS}$ falling edge, BUSY will go LOW.

Internal Clock Mode

In internal clock mode, the ADS8344 generates its own conversion clock internally. This relieves the microprocessor from having to generate the SAR conversion clock and allows the conversion result to be read back at the processor's convenience, at any clock rate from 0MHz to 2.0MHz. BUSY goes LOW at the start of a conversion and then returns HIGH when the conversion is complete. During the conversion, BUSY will remain LOW for a maximum of 8µs. Also, during the conversion, DCLK should remain LOW to achieve the best noise performance. The conversion result is stored in an internal register; the data may be clocked out of this register any time after the conversion is complete.

If $\overline{CS}$ is LOW when BUSY goes LOW following a conversion, the next falling edge of the external serial clock will write out the MSB on the D_{OUT} line. The remaining bits (D14-D0) will be clocked out on each successive clock cycle following the MSB. If $\overline{CS}$ is HIGH when BUSY goes LOW then the D_{OUT} line will remain in tri-state until $\overline{CS}$ goes LOW, as shown in Figure 6. $\overline{CS}$ does not need to remain LOW once a conversion has started. Note that BUSY is not tri-stated when $\overline{CS}$ goes HIGH in internal clock mode.

Data can be shifted in and out of the ADS8344 at clock rates exceeding 2.4MHz, provided that the minimum acquisition time t_{ACQ}, is kept above 1.7µs.

Digital Timing

Figure 4 and Tables VI and VII provide detailed timing for the digital interface of the ADS8344.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.5			µs
t_{DS}	D_{IN} Valid Prior to DCLK Rising	100			ns
t_{DH}	D_{IN} Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to D_{OUT} Valid			200	ns
t_{DV}	$\overline{CS}$ Falling to D_{OUT} Enabled			200	ns
t_{TR}	$\overline{CS}$ Rising to D_{OUT} Disabled			200	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	100			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	200			ns
t_{CL}	DCLK LOW	200			ns
t_{BD}	DCLK Falling to BUSY Rising			200	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			200	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			200	ns

TABLE VI. Timing Specifications ($+V_{CC}$ = +2.7V to 3.6V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

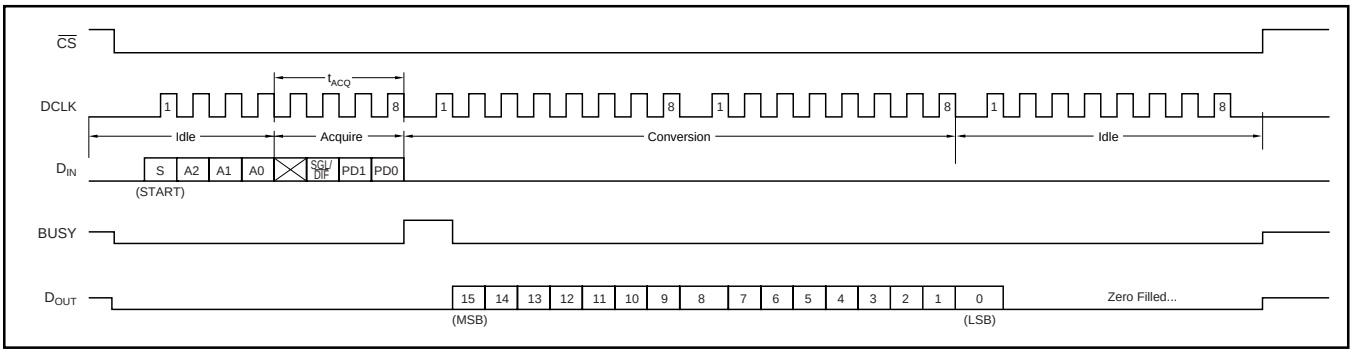


FIGURE 5. External Clock Mode, 32 Clocks Per Conversion.

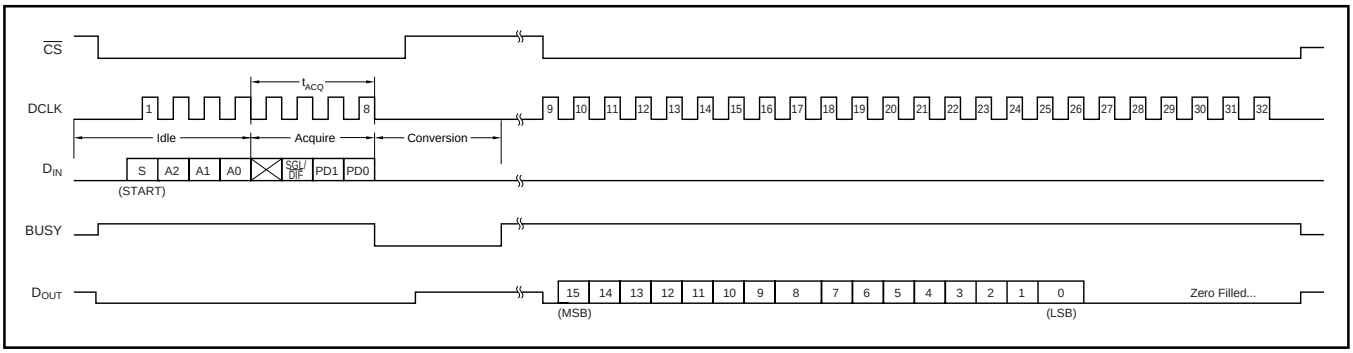


FIGURE 6. Internal Clock Mode Timing.

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{ACQ}	Acquisition Time	1.7			µs
t_{DS}	D_{IN} Valid Prior to DCLK Rising	50			ns
t_{DH}	D_{IN} Hold After DCLK HIGH	10			ns
t_{DO}	DCLK Falling to D_{OUT} Valid			100	ns
t_{DV}	$\overline{CS}$ Falling to D_{OUT} Enabled			70	ns
t_{TR}	$\overline{CS}$ Rising to D_{OUT} Disabled			70	ns
t_{CSS}	$\overline{CS}$ Falling to First DCLK Rising	50			ns
t_{CSH}	$\overline{CS}$ Rising to DCLK Ignored	0			ns
t_{CH}	DCLK HIGH	150			ns
t_{CL}	DCLK LOW	150			ns
t_{BD}	DCLK Falling to BUSY Rising			100	ns
t_{BDV}	$\overline{CS}$ Falling to BUSY Enabled			70	ns
t_{BTR}	$\overline{CS}$ Rising to BUSY Disabled			70	ns

TABLE VII. Timing Specifications ($+V_{CC}$ = +4.75V to +5.25V, T_A = –40°C to +85°C, C_{LOAD} = 50pF).

Data Format

The ADS8344 output data is in straight binary format, as shown in Figure 7. This figure shows the ideal output code for the given input voltage and does not include the effects of offset, gain, or noise.

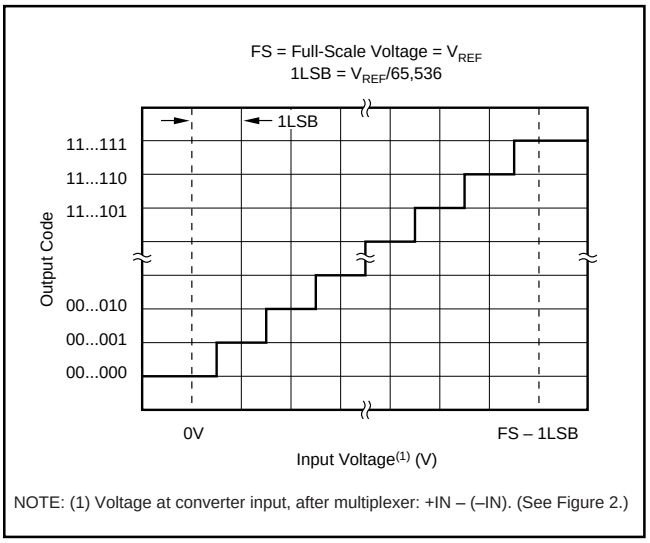


FIGURE 7. Ideal Input Voltages and Output Codes.

POWER DISSIPATION

There are three power modes for the ADS8344: full-power (PD1 - PD0 = 11B), auto power-down (PD1 - PD0 = 00B), and shutdown ($\overline{SHDN}$ LOW). The effects of these modes varies depending on how the ADS8344 is being operated. For example, at full conversion rate and 24-clocks per conversion, there is very little difference between full-power mode and auto power-down; a shutdown will not lower power dissipation.

When operating at full-speed and 24-clocks per conversion (see Figure 3), the ADS8344 spends most of its time acquiring or converting. There is little time for auto power-down, assuming that this mode is active. Thus, the difference between full-power mode and auto power-down is negligible. If the conversion rate is decreased by simply slowing the frequency of the DCLK input, the two modes remain approximately equal. However, if the DCLK frequency is kept at the maximum rate during a conversion, but conversions are simply done less often, then the difference between the two modes is dramatic. In the latter case, the converter spends an increasing percentage of its time in power-down mode (assuming the auto power-down mode is active).

If DCLK is active and $\overline{CS}$ is LOW while the ADS8344 is in auto power-down mode, the device will continue to dissipate some power in the digital logic. The power can be reduced to a minimum by keeping $\overline{CS}$ HIGH.

Operating the ADS8344 in auto power-down mode will result in the lowest power dissipation, and there is no conversion time "penalty" on power-up. The very first conversion will be valid. $\overline{SHDN}$ can be used to force an immediate power-down.

NOISE

The noise floor of the ADS8344 itself is extremely low, as shown in Figures 8 thru 11, and is much lower than competing A/D converters. The ADS8344 was tested at both 5V and 2.7V, and in both the internal and external clock modes. A low-level DC input was applied to the analog-input pins and the converter was put through 5,000 conversions. The digital output of the A/D converter will vary in output code due to the internal noise of the ADS8344. This is true for all 16-bit SAR-type A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions will represent the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this will yield the ±3σ distribution, or 99.7%, of all codes. Statistically, up to 3 codes could fall outside the distribution when executing 1,000 conversions. The ADS8344, with < 3 output codes for the ±3σ distribution, will yield a < ±0.5LSB transition noise at 5V operation. Remember, to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be < 50µV.

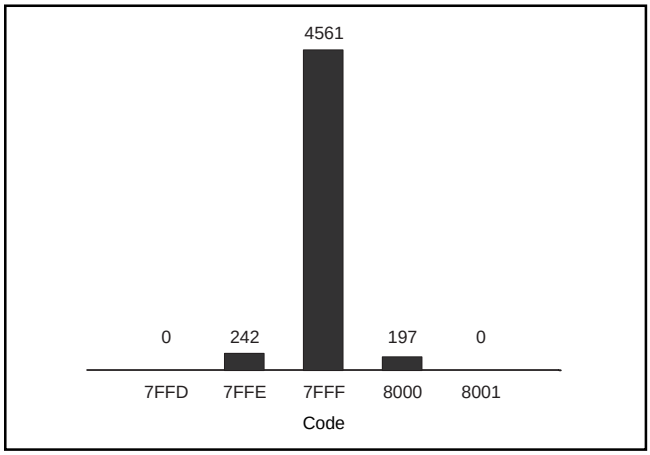


FIGURE 8. Histogram of 5,000 Conversions of a DC Input at the Code Transition, 5V operation external clock mode.

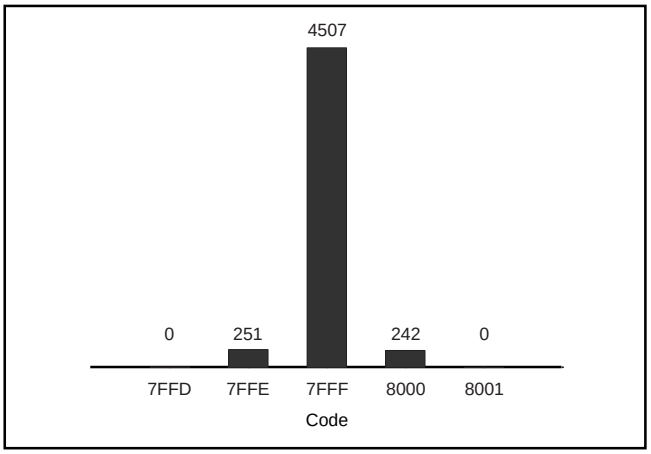


FIGURE 9. Histogram of 5,000 Conversions of a DC Input at the Code Center, 5V operation internal clock mode.

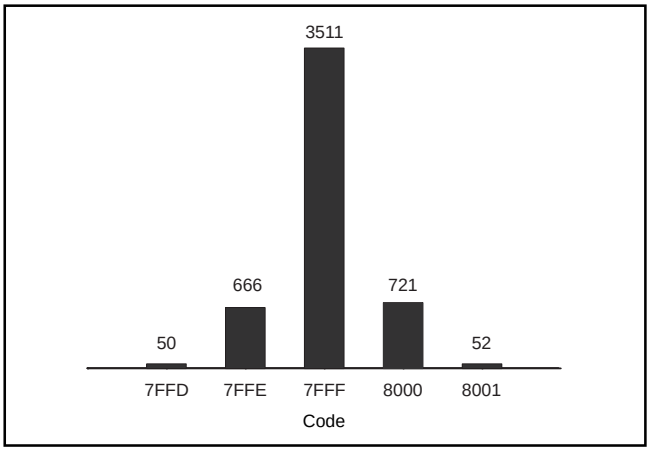


FIGURE 10. Histogram of 5,000 Conversions of a DC Input at the Code Transition, 2.7V operation external clock mode.

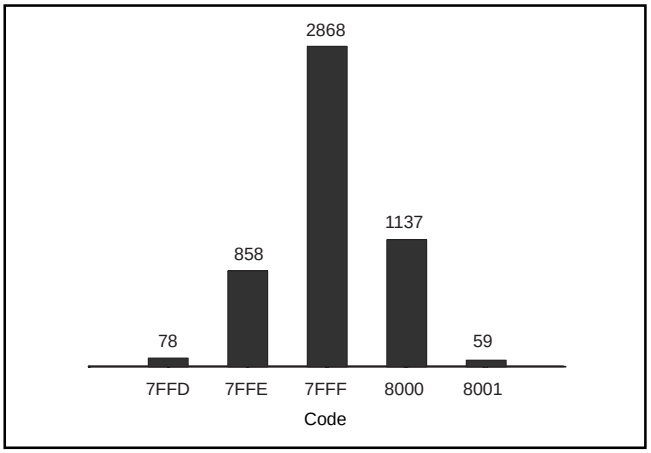


FIGURE 11. Histogram of 5,000 Conversions of a DC Input at the Code Center, 2.7V operation internal clock mode.

AVERAGING

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$, where *n* is the number of averages. For example, averaging 4 conversion results will reduce the transition noise by 1/2 to ±0.25LSBs. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging: for every decimation by 2, the signal-to-noise ratio will improve 3dB.

LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8344 circuitry. This is particularly true if the reference voltage is LOW and/or the conversion rate is HIGH.

The basic SAR architecture is sensitive to glitches or sudden changes on the power supply, reference, ground connections, and digital inputs that occur just prior to latching the output of the analog comparator. Thus, during any single conversion for an *n*-bit SAR converter, there are *n* "windows" in which large external transient voltages can easily affect the conversion result. Such glitches might originate from switching power supplies, nearby digital logic, and high-power devices. The degree of error in the digital output depends on the reference voltage, layout, and the exact timing of the external event. The error can change if the external event changes in time with respect to the DCLK input.

With this in mind, power to the ADS8344 should be clean and well bypassed. A 0.1µF ceramic bypass capacitor should be placed as close to the device as possible. In addition, a 1µF to 10µF capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 0.1µF capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that it can drive the bypass capacitor without oscillation (the series resistor can help in this case). The ADS8344 draws very little current from the reference on average, but it does place larger demands on the reference circuitry over short periods of time (on each rising edge of DCLK during a conversion).

The ADS8344 architecture offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out as discussed in the previous paragraph, voltage variation due to line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin should be connected to a clean ground point. In many cases, this will be the "analog" ground. Avoid connections that are too near the grounding point of a microcontroller or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply entry point. The ideal layout will include an analog ground plane dedicated to the converter and associated analog circuitry.

Revision History

DATE	REVISION	PAGE	SECTION	DESCRIPTION
9/06	E	2	Package/Ordering Info	Added quantity to last column.
		4	Electrical Characteristics	Fixed typo. Changed +2.7V Gain Error minimum value (for EB, NB grade) from ±0.0024 to ±0.024.

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
ADS8344E	Active	Production	SSOP (DBQ) | 20	50 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8344E
ADS8344E/2K5	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	ADS8344E
ADS8344EB	Active	Production	SSOP (DBQ) | 20	50 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	ADS8344E B
ADS8344EB/2K5	Active	Production	SSOP (DBQ) | 20	2500 | LARGE T&R	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	ADS8344E
ADS8344EBG4	Active	Production	SSOP (DBQ) | 20	50 | TUBE	Yes	Call TI	Level-3-260C-168 HR	-40 to 85	ADS8344E B
ADS8344N	Active	Production	SSOP (DB) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8344N B
ADS8344N/1K	Active	Production	SSOP (DB) | 20	1000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8344N B
ADS8344N/1KG4	Active	Production	SSOP (DB) | 20	1000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8344N B
ADS8344NB	Active	Production	SSOP (DB) | 20	70 | TUBE	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8344N
ADS8344NB/1K	Active	Production	SSOP (DB) | 20	1000 | LARGE T&R	Yes	Call TI	Level-2-260C-1 YEAR	-40 to 85	ADS8344N
ADS8344NG4	Active	Production	SSOP (DB) | 20	70 | TUBE	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8344N B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

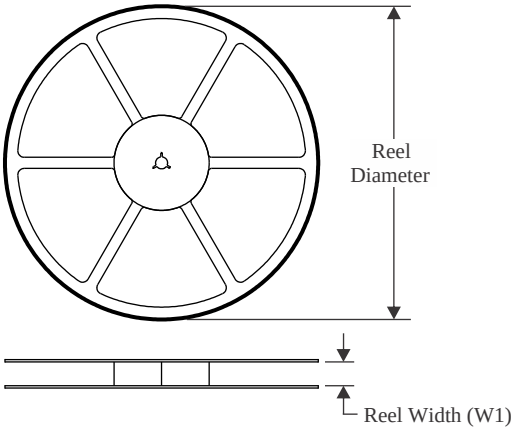
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) Part marking: There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

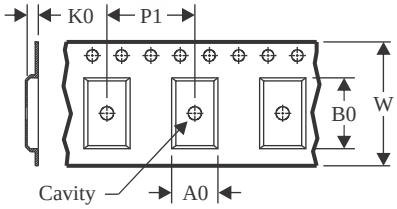
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

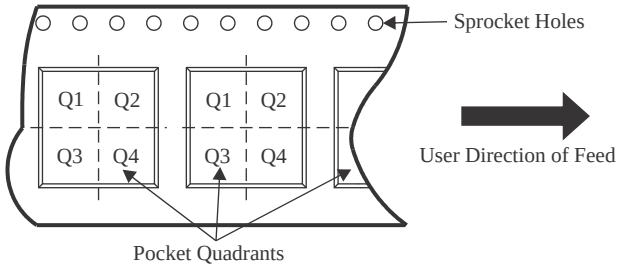


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

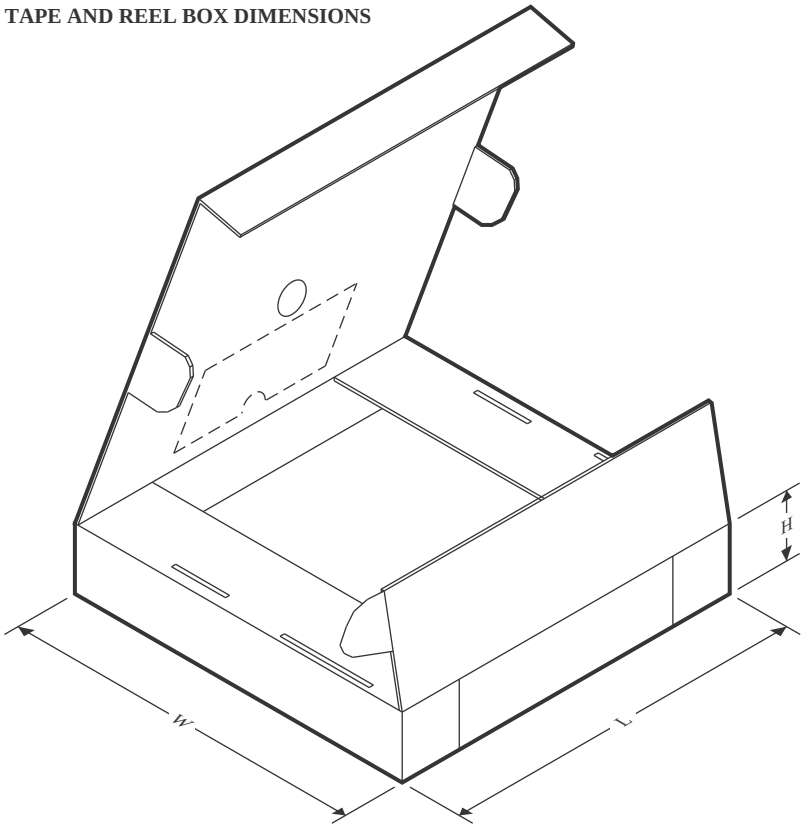
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8344E/2K5	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
ADS8344EB/2K5	SSOP	DBQ	20	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
ADS8344N/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1
ADS8344NB/1K	SSOP	DB	20	1000	330.0	16.4	8.2	7.5	2.5	12.0	16.0	Q1

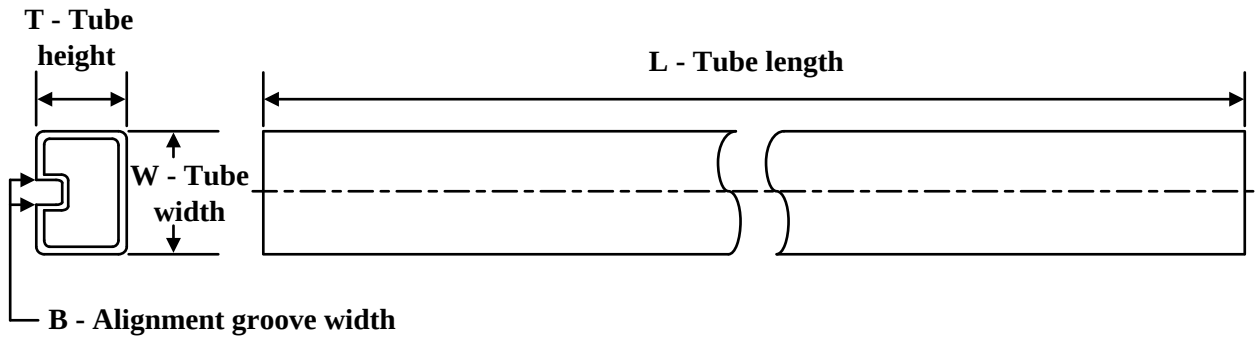
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8344E/2K5	SSOP	DBQ	20	2500	356.0	356.0	35.0
ADS8344EB/2K5	SSOP	DBQ	20	2500	356.0	356.0	35.0
ADS8344N/1K	SSOP	DB	20	1000	356.0	356.0	35.0
ADS8344NB/1K	SSOP	DB	20	1000	356.0	356.0	35.0

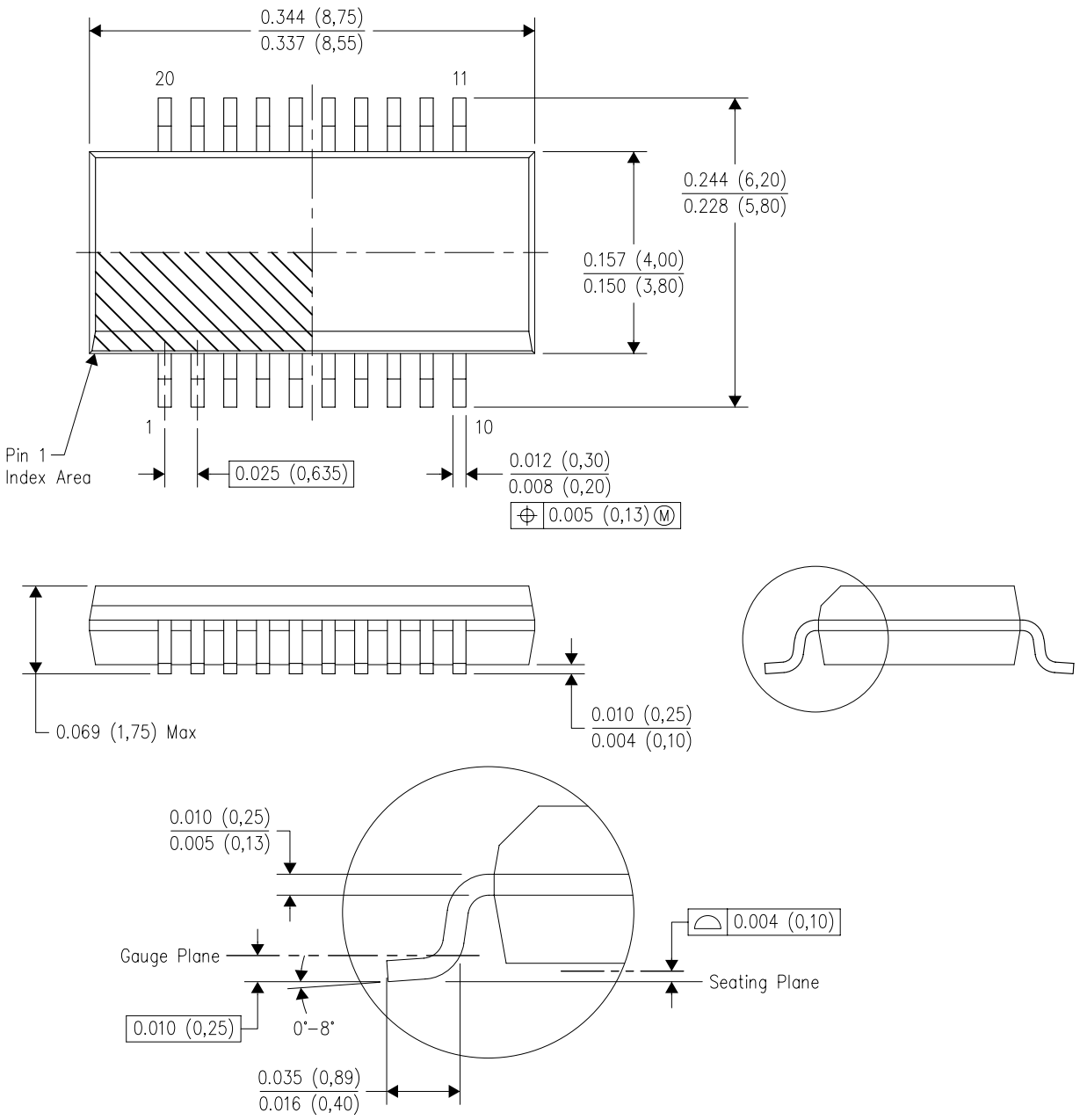
TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
ADS8344E	DBQ	SSOP	20	50	506.6	8	3940	4.32
ADS8344EB	DBQ	SSOP	20	50	506.6	8	3940	4.32
ADS8344EBG4	DBQ	SSOP	20	50	506.6	8	3940	4.32
ADS8344EG4	DBQ	SSOP	20	50	506.6	8	3940	4.32
ADS8344N	DB	SSOP	20	70	530	10.5	4000	4.1
ADS8344NB	DB	SSOP	20	70	530	10.5	4000	4.1
ADS8344NBG4	DB	SSOP	20	70	530	10.5	4000	4.1
ADS8344NG4	DB	SSOP	20	70	530	10.5	4000	4.1

DBQ (R–PDSO–G20) PLASTIC SMALL–OUTLINE PACKAGE



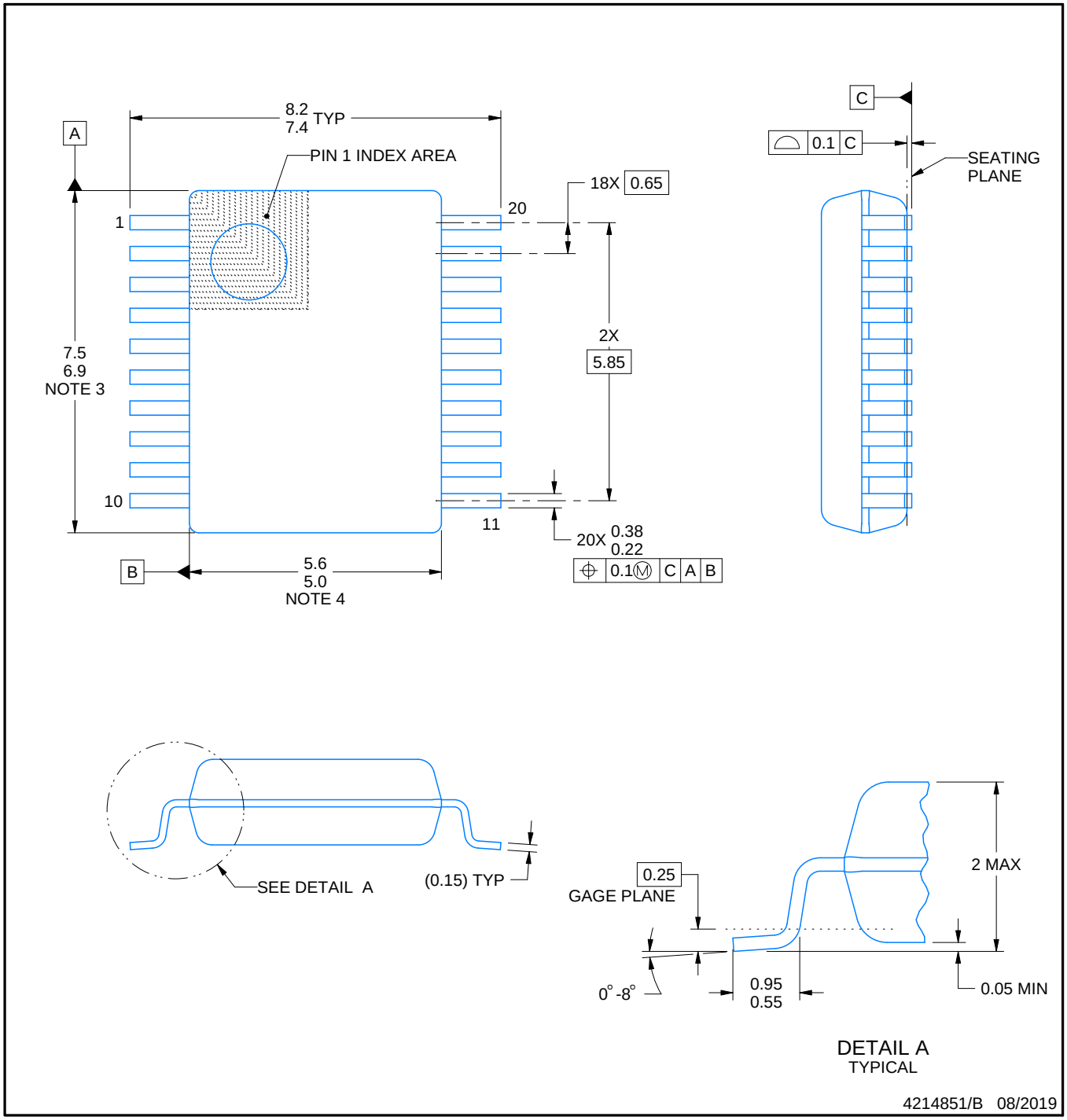
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AD.

PACKAGE OUTLINE

DB0020A

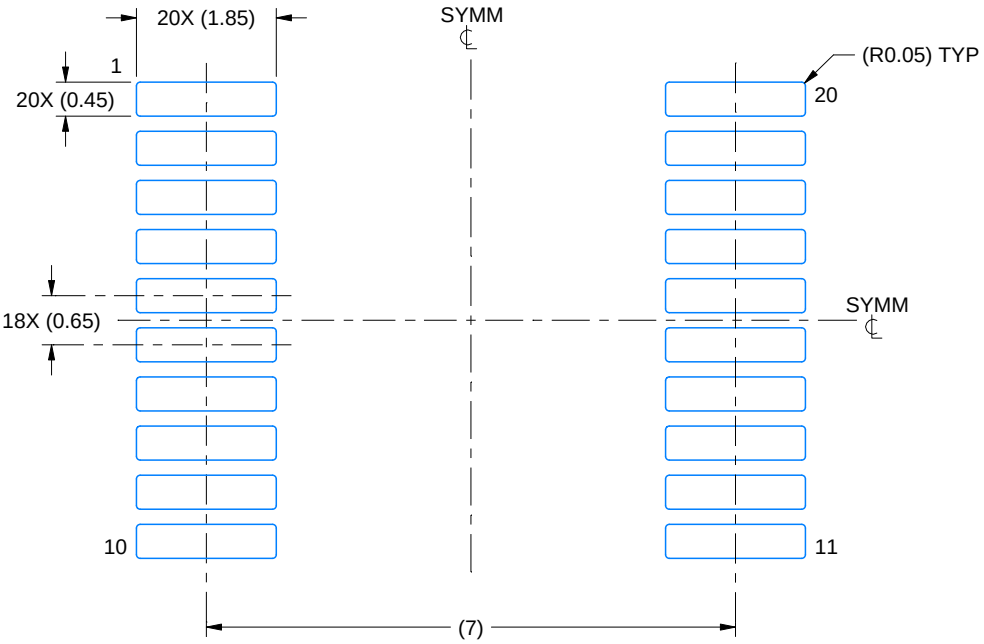
SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

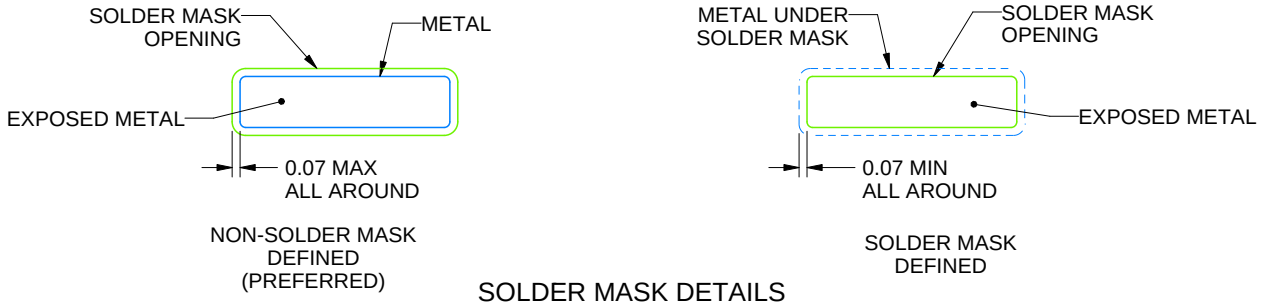


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

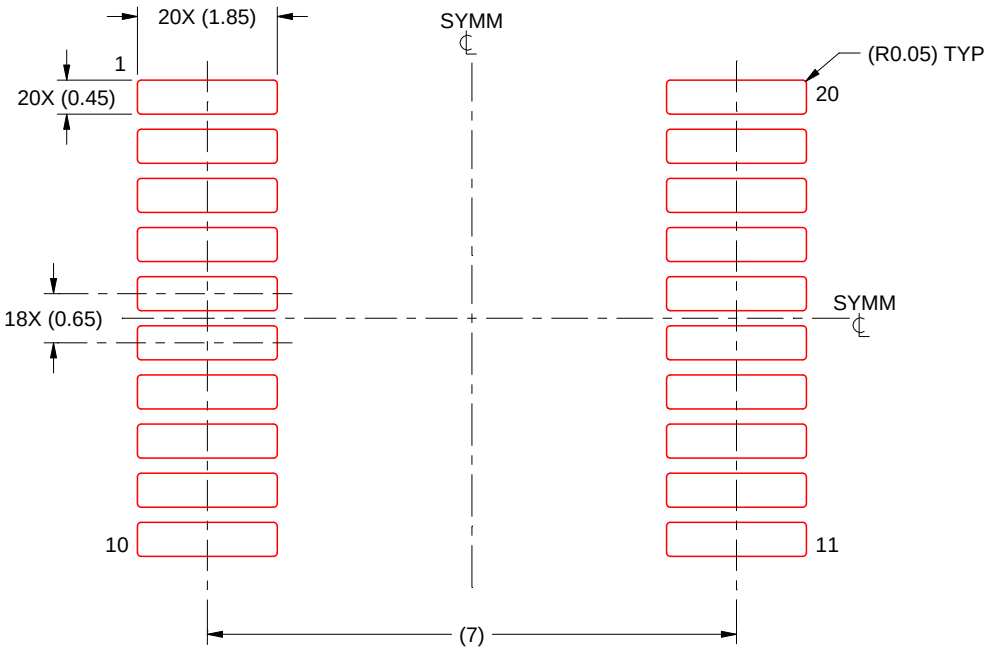
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0020A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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