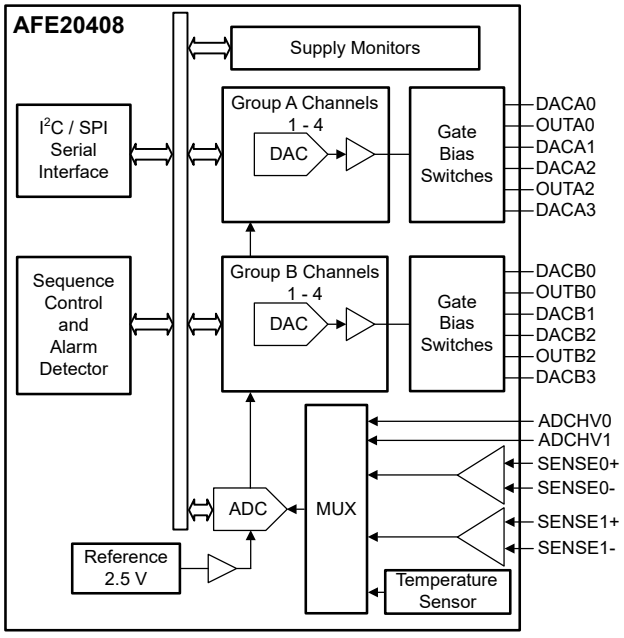
AFE20408 8-Channel Power-Amplifier Monitor and Controller

1 Features

- Eight analog outputs
  - Eight monotonic DACs: 1.22mV resolution
  - Automatically configured output ranges:
    - Positive output voltage: 0V to 10V
    - Negative output voltage: –10V to 0V
  - High current drive capability
  - High capacitive load tolerance
- Output on and off control switches
  - Fast switching time
  - Low resistance
- Multichannel ADC monitor
  - Two high-voltage external inputs: 0V to 85V
  - Two high-side current-sense amplifiers: up to 85V common mode range
  - Local temperature sensor: ±2.5°C error
- Output sequence control for start-up and shutdown events
- Internal 2.5V reference
- SPI and I^2C interface: 1.65V to 3.6V operation
  - SPI: 4-wire interface
  - I^2C: 16 target addresses
- Specified temperature range: –40°C to +125°C
- Operating temperature range –55°C to +150°C



Simplified Schematic

2 Applications

- Radar
- Electronic warfare
- Software defined radio
- Seeker front end

3 Description

The AFE20408 is a highly integrated power-amplifier (PA) monitor and control device capable of temperature, current, and voltage supervision.

The AFE20408 bias controller is based around eight digital-to-analog converters (DACs) with programmable output ranges. The eight gate bias outputs are switched on and off through dedicated control pins. The gate bias switches are designed for fast response and enable correct power sequencing and protection of depletion-mode transistors, such as GaAs and GaN.

The AFE20408 supervisor is based around an accurate multichannel analog-to-digital converter (ADC). The device integrates two high-voltage inputs, two high-side current-sense amplifiers and an accurate on-chip temperature sensor.

The function integration and wide operating temperature range make the AFE20408 an excellent choice as an all-in-one, bias control circuit for power amplifiers. The flexible DAC output ranges and built-in sequencing features let the device be used as a biasing controller for a large variety of transistor technologies, such as LDMOS, GaAs, and GaN.

Device Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AFE20408	RHB (VQFN, 32)	5mm × 5mm

(1) For more information, see Section 11.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

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4 Pin Configuration and Functions

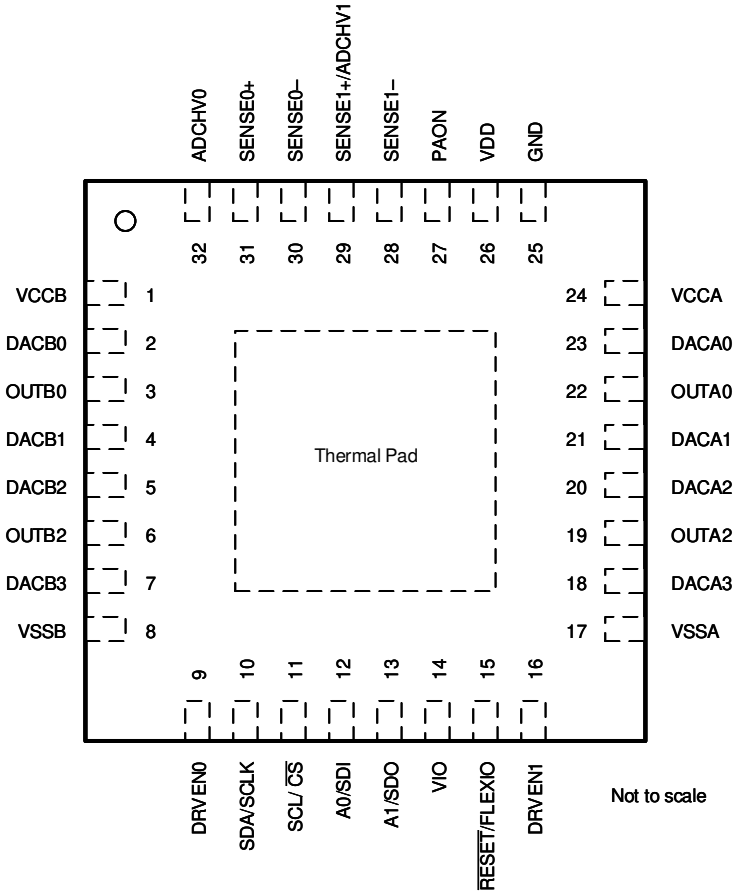


Figure 4-1. RHB Package, 32-Pin VQFN (Top View)

Table 4-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VCCB	Power	Group B output buffers positive analog power supply.
2	DACB0	Output	DACB0 buffer output.
3	OUTB0	Output	DACB0 switch output.
4	DACB1	Output	DACB1 buffer output.
5	DACB2	Output	DACB2 buffer output.
6	OUTB2	Output	DACB2 switch output.
7	DACB3	Output	DACB3 buffer output.
8	VSSB	Power	Group B output buffers negative analog power supply.
9	DRVEN0	Input	Asynchronous switch control signal.
10	SDA/SCLK	Input/Output	I^2C: bidirectional data line. SPI: Clock input.
11	SCL/ $\overline{CS}$	Input	I^2C: Clock input. SPI: Active-low serial data enable. This input is the frame synchronization signal for the serial data. When the signal goes low, this pin enables the serial interface input shift register.
12	A0/SDI	Input	I^2C: Target address selector. SPI: Data input. Data are clocked into the input shift register on each falling edge of the SCLK pin.
13	A1/SDO	Input/Output	I^2C: Target address selector. SPI: Data output. Data are clocked out of the input shift register on either rising or falling edges of the SCLK pin as specified by the FSDO bit.
14	VIO	Power	IO supply voltage. This pin sets the I/O operating voltage for the device.
15	$\overline{RESET}$/FLEXIO	Input	Active low reset input. Logic low on this pin causes the device to initiate a reset event. Also referred to as FLEXIO, as this pin can be configured as $\overline{RESET}$ (default), GPIO, $\overline{ALARMOUT}$ output, $\overline{ALARMIN}$ input, DRVEN2, or $\overline{LDAC}$.
16	DRVEN1	Input	Asynchronous switch control signal.
17	VSSA	Power	Group A output buffers negative analog power supply.
18	DACA3	Output	DACA3 buffer output.
19	OUTA2	Output	DACA2 switch output.
20	DACA2	Output	DACA2 buffer output.
21	DACA1	Output	DACA1 buffer output.
22	OUTA0	Output	DACA0 switch output.
23	DACA0	Output	DACA0 buffer output.
24	VCCA	Power	Group A output buffers positive analog power supply.
25	GND	Ground	Ground reference point for all circuitry on the device.
26	VDD	Power	Analog supply voltage.
27	PAON	Output	Synchronization signal for PA biasing.
28	SENSE1–	Input	Current sensor 1 connection.
29	SENSE1+/ ADCHV1	Input	Current sensor 1 connection. Alternatively can be used as a high voltage ADC analog input.
30	SENSE0–	Input	Current sensor 0 connections.
31	SENSE0+	Input	Current sensor 0 connections.
32	ADCHV0	Input	High voltage ADC analog input 0.
Thermal Pad	Thermal Pad	—	The thermal pad is located on the package underside. Connect the thermal pad to any internal PCB ground plane through multiple vias for good thermal performance.

5 Specifications

5.1 Absolute Maximum Ratings

all ratings over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
	Supply voltage(2)	V_{DD} to GND	–0.3	6	V
		V_{IO} to GND	–0.3	6	
		$V_{CC[A,B]}$ to GND	–0.3	12	
		$V_{SS[A,B]}$ to GND	–12	0.3	
		$V_{CC[A,B]}$ to $V_{SS[A,B]}$	–0.3	12	
	Pin voltage	DACA[0:3] output pins to GND	V_{SSA} – 0.3	V_{CCA} + 0.3	V
		DACB[0:3] output pins to GND	V_{SSB} – 0.3	V_{CCB} + 0.3	
		OUTA[0,2] output pins to GND	V_{SSA} – 0.3	V_{CCA} + 0.3	
		OUTB[0,2] output pins to GND	V_{SSB} – 0.3	V_{CCB} + 0.3	
		ADCHV0 and ADCHV1 input pins to GND	–0.3	85	
		Digital pins to GND	–0.3	V_{IO} + 0.3	
		SENSE0[+/−] and SENSE1[+/−] input pins to GND	–0.3	85	
		SENSE[0:1]+ to SENSE[0:1]− differential input(3)	–85	85	
T_J	Junction temperature		–55	150	°C
T_{stg}	Storage temperature		–65	150	

(1) Operation outside the Absolute Maximum Ratings can cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) The device can be configured to operate with mixed range output; that is, positive output on one group of DACs, and negative output range on the other group of DACs. In this case, the supply voltages for the device must be set up such that $V_{SSA} \leqq V_{SSB}$, and $V_{CCA} \leqq V_{CCB}$ (that is, DAC group B must operate in positive output range mode, while DAC group A must operate in negative output range mode).

(3) Do not maintain an –85V differential input over a very extended period of time (≥ 5 years) because doing so can degrade the internal clamp diodes that serve to prevent current from flowing directly from VCC to VSS (that is, to protect the device from short circuiting).

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Analog supply voltage	3.0		5.5	V
V_{IO}	Digital IO supply voltage	1.65		3.6	V
$V_{CC[A,B]}$ (1)	Output buffer positive supply voltage	3.0		11.0	V
$V_{SS[A,B]}$ (2)	Output buffer negative supply voltage	–11.0		–3.0	V
$V_{CCA} – V_{SSA}$	Group A output buffer supply voltage range	3.0		11.0	V
$V_{CCB} – V_{SSB}$	Group B output buffer supply voltage range	3.0		11.0	V
$V_{CC[A,B]} – V_{SS[B,A]}$	Mixed DAC range supply voltage range	3.0		18.0	V
$V_{CM} – V_{SS[A,B]}$	SENSE pins common-mode input range	–0.3		85	V
$V_{IN} – V_{SS[A,B]}$	ADCHV pins input voltage range	0		85	V
T_J	Specified junction temperature	–40		125	°C
	Operating junction temperature	–55		150	

(1) $V_{CC[A,B]}$ must be connected to GND when the corresponding DAC group is configured for negative output voltage range operation.
(2) $V_{SS[A,B]}$ must be connected to GND when the corresponding DAC group is configured for positive output voltage range operation.

5.4 Thermal Information

THERMAL METRIC(1)		AFE20408 RHB (VQFN) 32 PINS	UNIT
θ_{JA}	Junction-to-ambient thermal resistance	34.7	°C/W
$\theta_{JC(top)}$	Junction-to-case (top) thermal resistance	19.5	°C/W
θ_{JB}	Junction-to-board thermal resistance	14.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	14.5	°C/W
$\theta_{JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.7	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

5.5 Electrical Characteristics

all minimum and maximum values at T_J = –40°C to +125°C; all typical values at T_J = 25°C, V_{DD} = 3.0V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: $V_{CC[A,B]}$ = 3.0V to 11.0V, $V_{SS[A,B]}$ = GND, negative output range: $V_{SS[A,B]}$ = –11.0V to –3.0V, $V_{CC[A,B]}$ = GND, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC CHARACTERISTICS(1)						
	Resolution		13			Bits
	Full scale output voltage range	Set at start-up through autorange detection	–10		0	V
		Set at start-up through autorange detection	0		10	
DNL	Differential nonlinearity	Specified 13-bit monotonic	–1		1	LSB
INL	Integral nonlinearity		–4		4	LSB
TUE	Total unadjusted error		–0.6	±0.1	0.6	%FSR
TUE	Total unadjusted error (4)	Operating in extended temperature range (T_J = –55°C to +150°C)	–2	±0.1	2	%FSR
	Total adjusted error	After one point calibration at 25°C, DAC output at 1/4 of full-scale range	–0.1	±0.01	0.1	%FSR
	Offset error	Positive output range	–40	±5	40	mV
		Negative output range	–40	±5	40	
	Offset error temperature drift			±5		ppm/°C
	Gain error		–0.5	±0.01	0.5	%FSR
	Gain error temperature drift			±20		ppm/°C
	Zero-scale error	Positive output range: all zeros code	0	5	35	mV
		Negative output range: all ones code	–35	–5	0	
	Zero-scale error temperature drift			±5		ppm/°C
	Full-scale error	Positive output range: all ones code	–0.7	±0.05	0.7	%FSR
		Negative output range: all zeros code	–0.7	±0.05	0.7	
	Full-scale error temperature drift			±20		ppm/°C
	Short circuit current(2)	Start-up current mode		15		mA
		Low-current mode		30		
		Normal-current mode		90		
		High-current mode		120		
	Capacitive load stability(3)		0		15	µF
	DC output impedance	Midscale code		3		Ω
	Output voltage settling time	C_L = 15µF, 2.5V step to within 2.5mV		400		µs
	Output noise	0.1Hz to 10Hz, midscale code		70		µVpp
	Output noise density	1kHz, midscale code		700		nV/√Hz
$PSRR_{AC}$	Power supply ac rejection ratio	Midscale code, frequency = 60Hz, amplitude = 200mVpp superimposed on $V_{CC[A,B]}$ or $V_{SS[A,B]}$		66		dB
		Midscale code, frequency = 60Hz, amplitude = 200mVpp superimposed on V_{DD}		70		
$PSRR_{DC}$	Power supply dc rejection ratio	Midscale code, V_{DD} = 5V ±10%, $V_{CC[A,B]}$ = 10V ±10%, V_{SS} = –10V ±10%		500		µV/V
	Channel-to-channel dc crosstalk	Measured DAC output at midscale, all other DAC outputs at full-scale		150		µV

5.5 Electrical Characteristics (continued)

all minimum and maximum values at T_J = –40°C to +125°C; all typical values at T_J = 25°C, V_{DD} = 3.0V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: $V_{CC[A,B]}$ = 3.0V to 11.0V, $V_{SS[A,B]}$ = GND, negative output range: $V_{SS[A,B]}$ = –11.0V to –3.0V, $V_{CC[A,B]}$ = GND, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT SWITCH DC CHARACTERISTICS						
R_{DAC}	Resistance between DAC buffers and output pins	1.5V headroom from supply		3	5	Ω
R_{VSS}	Resistance between $V_{SS[A,B]}$ and output pins			4	7	Ω
SUPPLY MONITOR CHARACTERISTICS						
V_{SSTH}	V_{SS} threshold detector	Low V_{SS} supply failure detect	–2.2		–1.7	V
		Mid V_{SS} supply failure detect	–3.7		–3.2	
		High V_{SS} supply failure detect	–6.7		–6.2	
V_{CCTH}	V_{CC} threshold detector	V_{CC} supply failure detect	1.7		2.2	V
HIGH-VOLTAGE SENSE CHARACTERISTICS						
V_{IN}	Analog input range	$V_{SS[A,B]}$ = 0V	0		85	V
	Offset voltage	V_{IN} = 20mV		±1.5	±13	mV
	Offset voltage[4]	V_{IN} = 20mV, operation in extended temperature range (T_J = –55°C to +150°C)		±5	±40	mV
	Offset voltage drift			±20		µV/°C
	Gain error			±0.1	±1.0	%
	Gain error[4]	Operation in extended temperature range (T_J = –55°C to +150°C)		±0.3	±3.0	%
	Gain error drift			±20		ppm/°C
	Input impedance	Active mode		1		MΩ
	Pin leakage current	Shutdown mode, V_{IN} = 85V		1		µA
	Resolution			3.125		mV
CURRENT SENSE CHARACTERISTICS						
V_{CM}	Common-mode input range	$V_{SS[A,B]}$ = 0V	–0.3		85	V
V_{DIFF}	Shunt voltage input range	SHUNT_RANGE = 0	–163.84		163.84	mV
		SHUNT_RANGE = 1	–40.96		40.96	
	Shunt offset voltage	V_{CM} = 48V, T_{CT} > 280µs		±10	±100	µV
		V_{CM} = 0V, T_{CT} > 280µs		±10	±100	
	Shunt offset voltage drift			±100		nV/°C
	Shunt voltage gain error	V_{CM} = 24V		±0.1	±1.0	%
	Shunt voltage gain error	V_{CM} = 24V, operation in extended temperature range (T_J = –55°C to 150°C)		±0.3	±3.0	%
	Shunt voltage gain error drift			±50		ppm/°C
	Common-mode rejection ratio			120		dB
	Input bias current	SENSE+ and SENSE– inputs, V_{CM} = 85V		1		µA
	Input differential impedance	Active mode, V_{DIFF} < 164mV		92		kΩ
	Resolution	Shunt voltage, SHUNT_RANGE = 0		5		µV
		Shunt voltage, SHUNT_RANGE = 1		1.25		
TEMPERATURE SENSE CHARACTERISTICS						
	Accuracy	T_J = –40°C to +125°C	–2.5	±0.25	2.5	°C
	Resolution	LSB size		7.8125		m°C

5.5 Electrical Characteristics (continued)

all minimum and maximum values at T_J = –40°C to +125°C; all typical values at T_J = 25°C, V_{DD} = 3.0V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: $V_{CC[A,B]}$ = 3.0V to 11.0V, $V_{SS[A,B]}$ = GND, negative output range: $V_{SS[A,B]}$ = –11.0V to –3.0V, $V_{CC[A,B]}$ = GND, and DAC outputs unloaded (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT CHARACTERISTICS						
V_{IH}	High-level input voltage		0.7 × V_{IO}			V
V_{IL}	Low-level input voltage				0.3 × V_{IO}	V
	Input current			2		µA
	Input pin capacitance			8		pF
DIGITAL OUTPUT CHARACTERISTICS						
V_{OH}	High-level output voltage	I_{SOURCE} = 0.2mA	V_{IO} – 0.4			V
V_{OL}	Low-level output voltage	I_{SINK} = –0.2mA			0.4	V
	Output pin capacitance			8		pF
V_{OL}	Open-drain low-level output voltage	I_{SINK} = 2mA			0.4	V
POWER CONSUMPTION CHARACTERISTICS						
I_{VDD}	V_{DD} supply current(4)	Positive output range			5	mA
		Negative output range			6	
		Positive output range, operating in extended temperature range (T_J = –55°C to +150°C)			10	
		Negative output range, operating in extended temperature range (T_J = –55°C to +150°C)			12	
I_{VCC}	V_{CC} supply current(4)	Positive output range, midscale output			6	mA
		Positive output range, midscale output, operating in extended temperature range (T_J = –55°C to +150°C)			12	
I_{VSS}	V_{SS} supply current(4)	Negative output range, 1/4 of full-scale output			7	mA
		Negative output range, 1/4 of full-scale output, operating in extended temperature range (T_J = –55°C to +150°C)			15	
I_{VIO}	V_{IO} supply current(4)				5	µA
		Operating in extended temperature range (T_J = –55°C to +150°C)			10	

(1) End point fit between codes 64 to 8128 for negative output range and 64 to 8128 for positive output range.
(2) Overload condition protection. Junction temperature can be exceeded during current limit. Operation greater than the specified maximum junction temperature can impair device reliability.
(3) No continuous oscillations when DAC transitions between codes.
(4) All values provided for extended temperature range (–55°C to +150°C) are specified by characterization

5.6 Timing Requirements

all minimum and maximum values at T_J = –40°C to +125°C; all typical values at T_J = 25°C, V_{DD} = 3.0V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: $V_{CC[A,B]}$ = 3.0V to 11.0V, $V_{SS[A,B]}$ = GND, negative output range: $V_{SS[A,B]}$ = –11.0V to –3.0V, $V_{CC[A,B]}$ = GND, and DAC outputs unloaded (unless otherwise noted)

		MIN	NOM	MAX	UNIT
I²C TIMING REQUIREMENTS					
$f_{(SCL)}$	I²C clock frequency	10		400	kHz
$t_{(LOW)}$	SCL clock low period	1.3			µs
$t_{(HIGH)}$	SCL clock high period	0.6			µs
$t_{(HDSTA)}$	Hold time after repeated start condition. After this period, the first clock is generated	0.6			µs
$t_{(SUSTA)}$	Repeated start condition setup time	0.6			µs
$t_{(SUSTO)}$	Stop condition setup time	0.6			µs
$t_{(BUF)}$	Bus free time between stop and start condition	1.3			µs
$t_{(SUDAT)}$	Data setup time	100			ns
$t_{(HDDAT)}$	Data hold time	0		900	ns
$t_{F,SDA}$	Data fall time	20		300	ns
$t_{F,SCL}$	Clock fall time			300	ns
$t_{R,SCL}$	Clock rise time			300	ns
$t_{R,SCL100}$	Rise time for SCL ≤ 100kHz			1000	ns
	SCL and SDA timeout	20		30	ms
SPI TIMING REQUIREMENTS, FSDO = 0					
$f_{(SCLK)}$	SCLK frequency			20	MHz
$t_{(SCLKH)}$	SCLK high time	23			ns
$t_{(SCLKL)}$	SCLK low time	23			ns
$t_{(SDIS)}$	SDI setup time	7			ns
$t_{(SDIH)}$	SDI hold time	7			ns
$t_{(SDOTOZ)}$	SDO driven to tri-state condition	0		17	ns
$t_{(SDOTOD)}$	SDO tri-state condition to driven	0		21	ns
$t_{(SDODLY)}$	SDO output delay	0		23	ns
$t_{(CSS)}$	$\overline{CS}$ setup time	21			ns
$t_{(CSH)}$	$\overline{CS}$ hold time	20			ns
$t_{(CSHIGH)}$	$\overline{CS}$ high time	20			ns
SPI TIMING REQUIREMENTS, FSDO = 1					
$f_{(SCLK)}$	SCLK frequency			25	MHz
$t_{(SCLKH)}$	SCLK high time	17			ns
$t_{(SCLKL)}$	SCLK low time	17			ns
$t_{(SDIS)}$	SDI setup time	7			ns
$t_{(SDIH)}$	SDI hold time	7			ns
$t_{(SDOTOZ)}$	SDO driven to tri-state condition	0		17	ns
$t_{(SDOTOD)}$	SDO tri-state condition to driven	0		21	ns
$t_{(SDODLY)}$	SDO output delay	3.5		32	ns
$t_{(CSS)}$	$\overline{CS}$ setup time	21			ns
$t_{(CSH)}$	$\overline{CS}$ hold time	20			ns
$t_{(CSHIGH)}$	$\overline{CS}$ high time	20			ns

5.7 Switching Characteristics

all minimum and maximum values at T_J = –40°C to +125°C; all typical values at T_J = 25°C, V_{DD} = 3.0V to 5.5V, V_{IO} = 1.65V to 3.6V, positive output range: $V_{CC[A,B]}$ = 3.0V to 11.0V, $V_{SS[A,B]}$ = GND, negative output range: $V_{SS[A,B]}$ = –11.0V to –3.0V, $V_{CC[A,B]}$ = GND, and DAC outputs unloaded (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OUTPUT SWITCH AC CHARACTERISTICS						
t_{ON}	On-time digital response time	Midscale code, measured from DRVEN[0,1] trigger			400	ns
t_{OFF}	Off-time digital response time	Midscale code, measured from DRVEN[0,1] trigger			400	ns
PA_ON CHARACTERISTICS						
t_{PA_OFF}	PA_ON turn-off time	Measured from an $\overline{\text{ALARMIN}}$ alarm event, unloaded			50	ns

5.8 Timing Diagrams

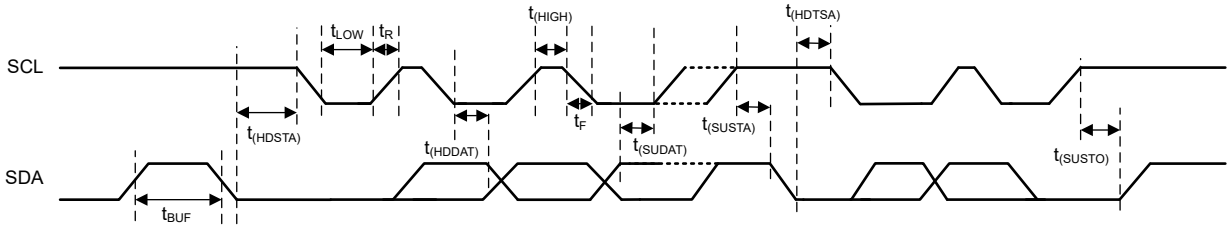


Figure 5-1. I²C Timing Diagram

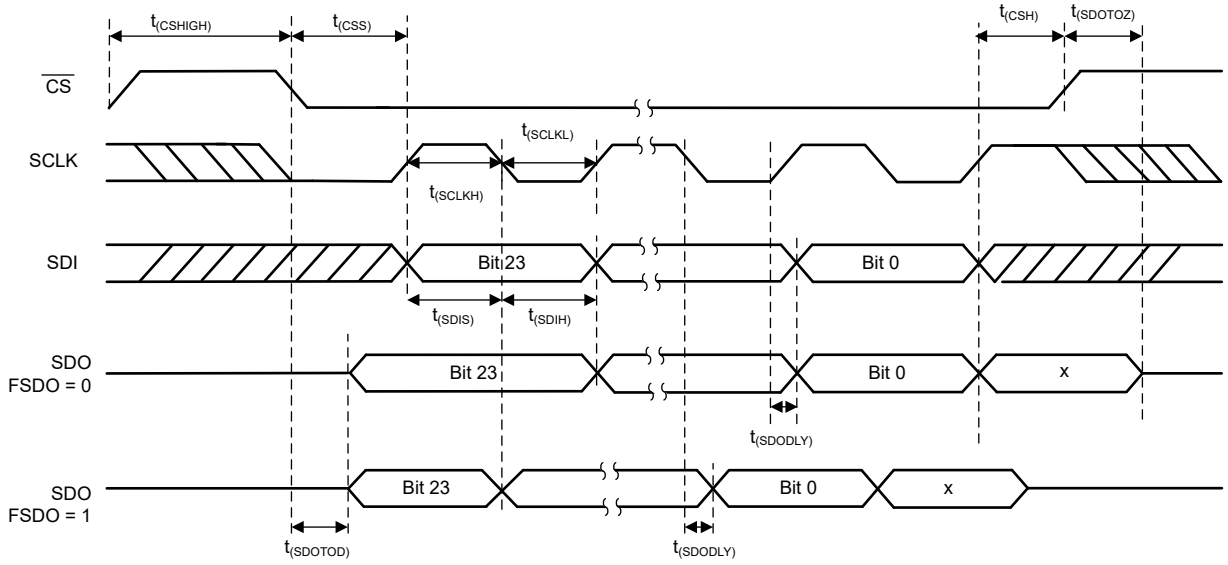


Figure 5-2. SPI Timing Diagram

5.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)

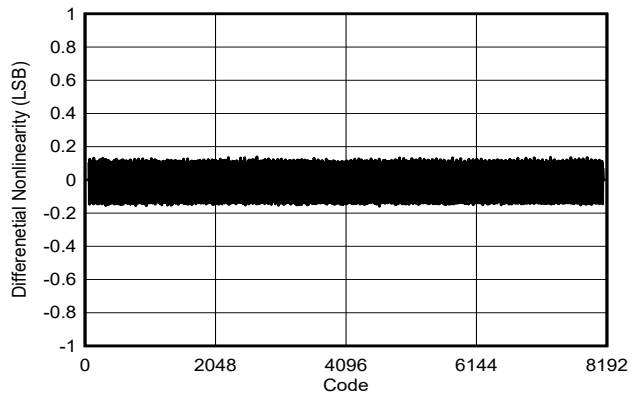


Figure 5-3. DAC DNL vs Digital Input Code

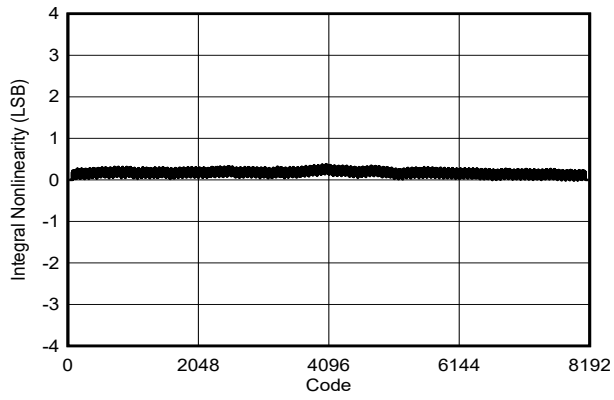


Figure 5-4. DAC INL vs Digital Input Code

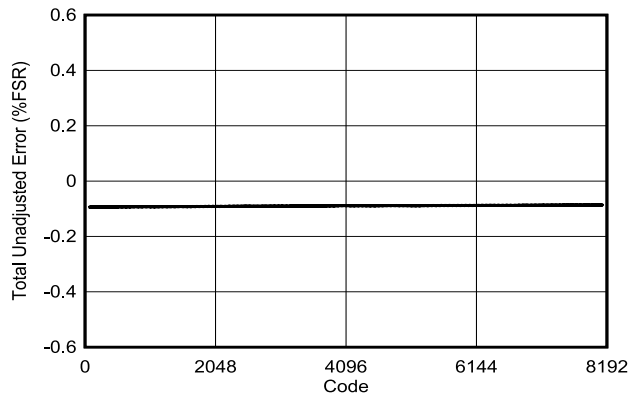


Figure 5-5. DAC TUE vs Digital Input Code

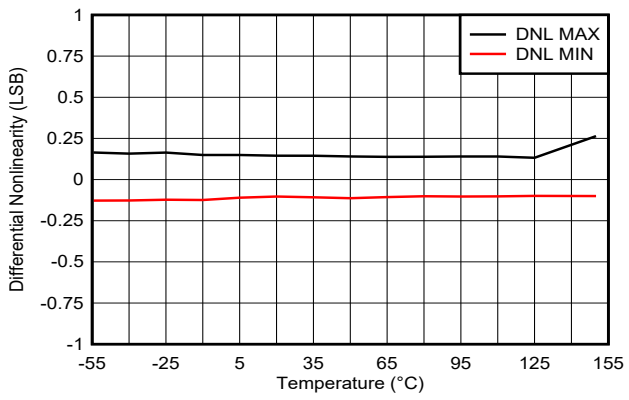


Figure 5-6. DAC DNL vs Temperature

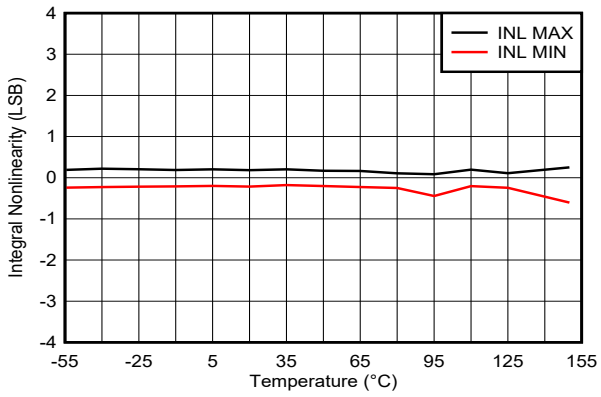


Figure 5-7. DAC INL vs Temperature

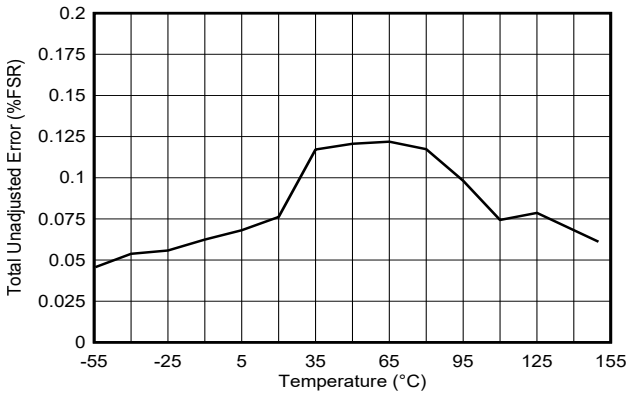


Figure 5-8. DAC Total Unadjusted Error vs Temperature

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)

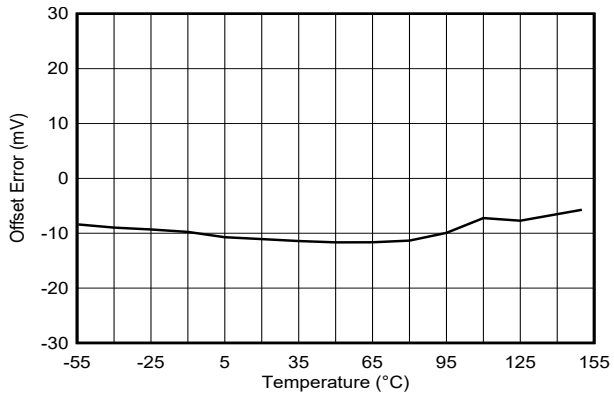


Figure 5-9. DAC Offset Error vs Temperature

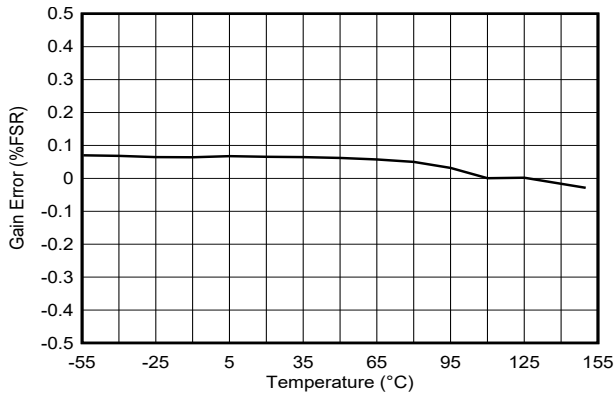
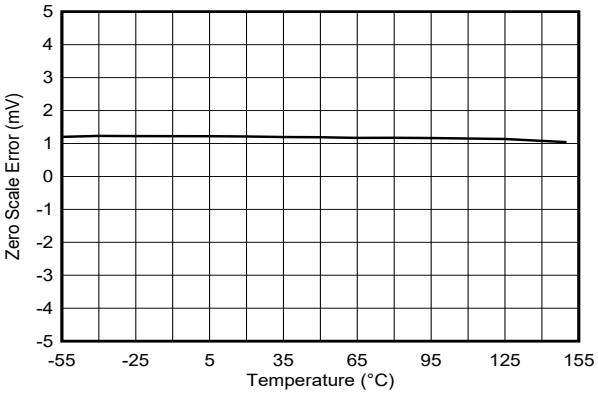
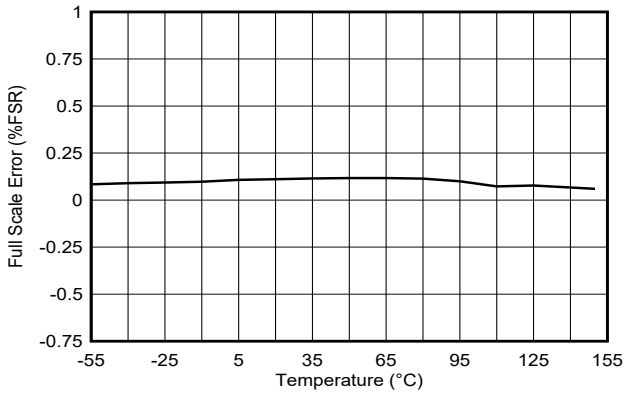


Figure 5-10. DAC Gain Error vs Temperature



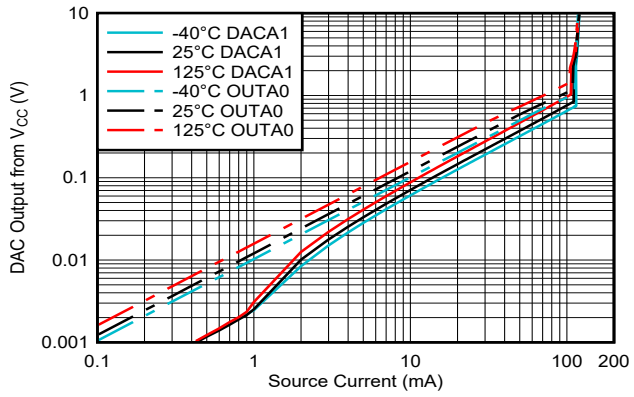
DAC code = 0x1FFF

Figure 5-11. DAC Zero-Scale Error vs Temperature



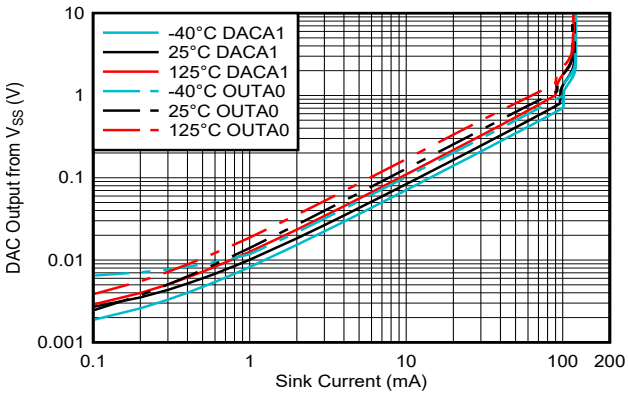
DAC code = 0x0000

Figure 5-12. DAC Full-Scale Error vs Temperature



DAC code = 0x1FFF

Figure 5-13. DAC Headroom vs High-Mode Sourcing Current



DAC code = 0x0000

Figure 5-14. DAC Headroom vs High-Mode Sinking Current

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)

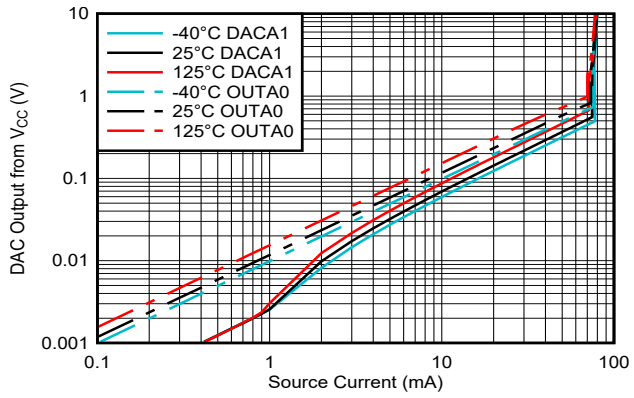


Figure 5-15. DAC Headroom vs Normal-Mode Sourcing Current

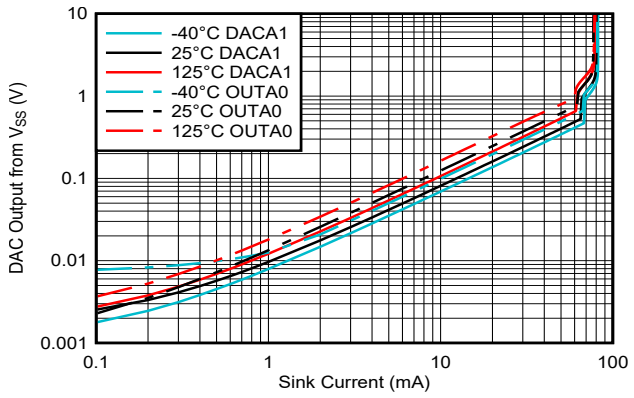
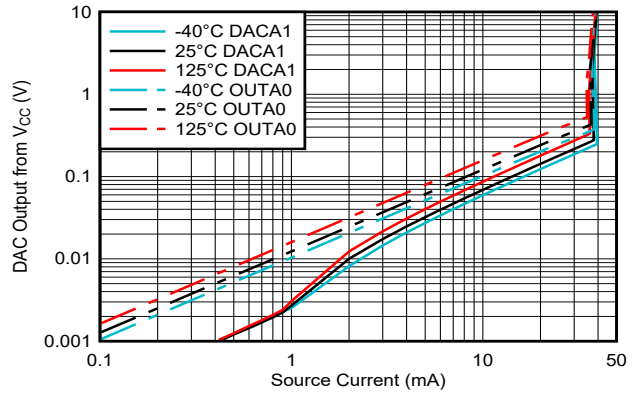
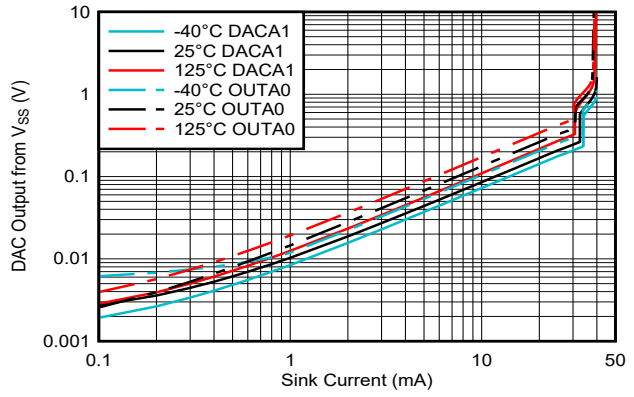


Figure 5-16. DAC Headroom vs Normal-Mode Sinking Current



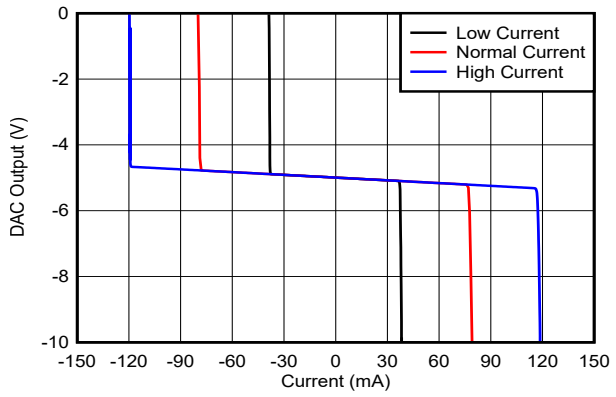
DAC code = 0x1FFF

Figure 5-17. DAC Headroom vs Low-Mode Sourcing Current



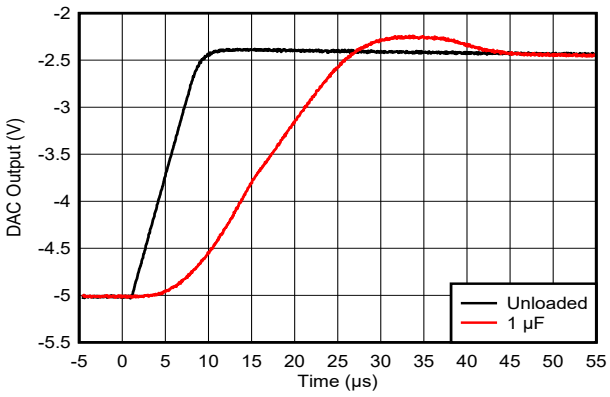
DAC code = 0x0000

Figure 5-18. DAC Headroom vs Low-Mode Sinking Current



DAC code = 0x1000

Figure 5-19. Source and Sink Current Capability

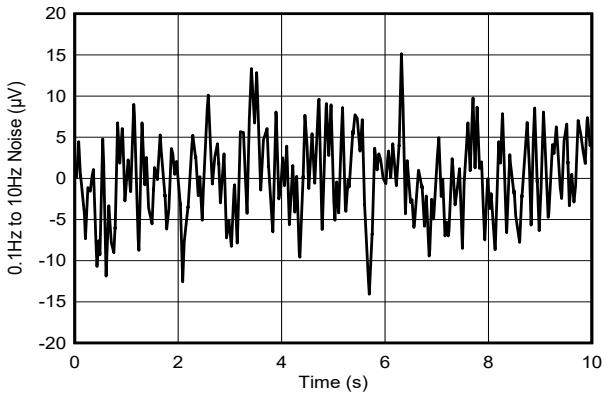


DAC step size: –5V to –2.5V

Figure 5-20. DAC Settling Time vs Capacitive Load

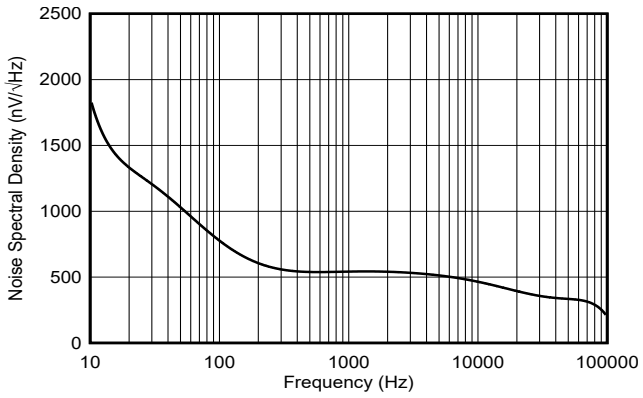
5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)



DAC code = 0x1000

Figure 5-21. DAC Output Noise, 0.1Hz to 10Hz



DAC code = 0x1000

Figure 5-22. DAC Output Noise Density vs Frequency

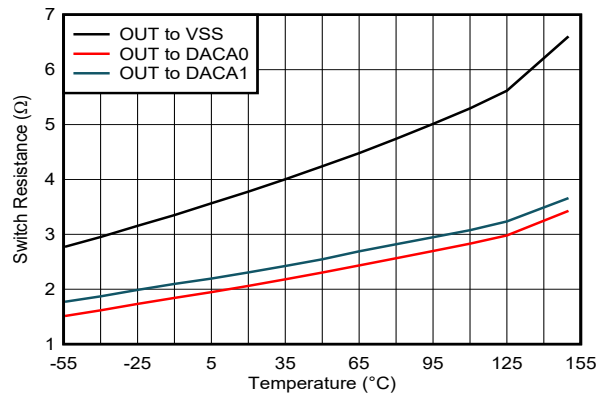
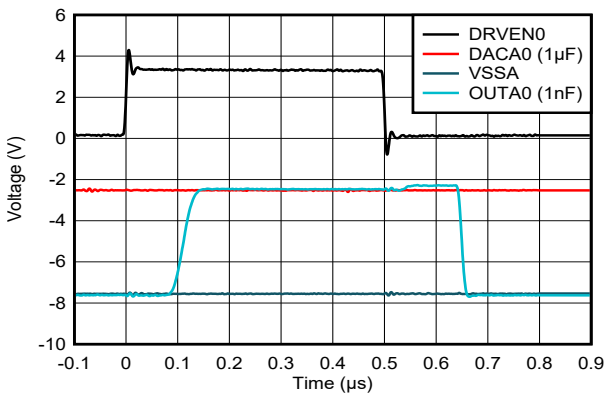
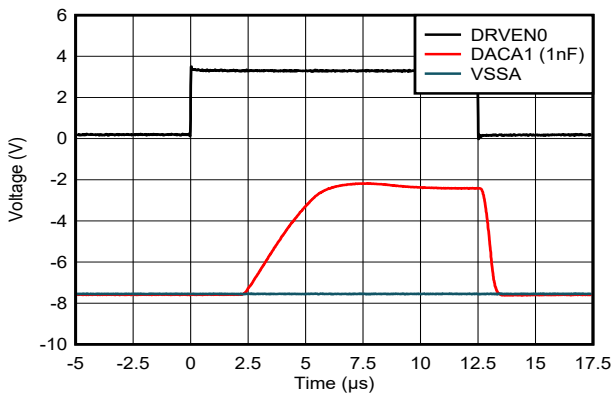


Figure 5-23. Switch Resistance vs Temperature



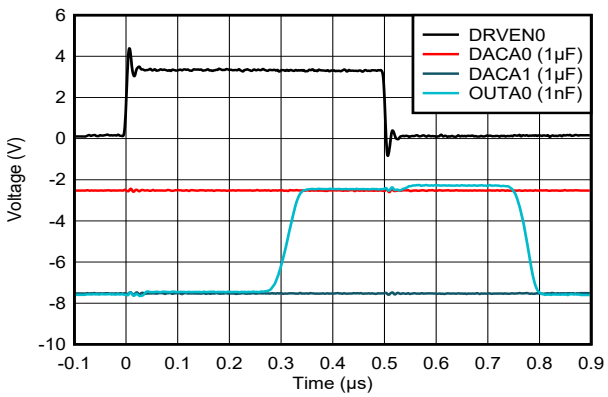
DACA0 output: –2.5V C_L = 1nF
VSS: –7V

Figure 5-24. OUT Pin: DAC to VSS Switch Response



DACA1 output: –2.5V C_L = 1nF
VSS: –7V

Figure 5-25. OUT Pin: DACA1 to VSS Switch Response



DACA0 output: –2.5V C_L = 1nF
DACA1 output: –7V

Figure 5-26. OUT Pin: DAC to DAC Switch Response

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)

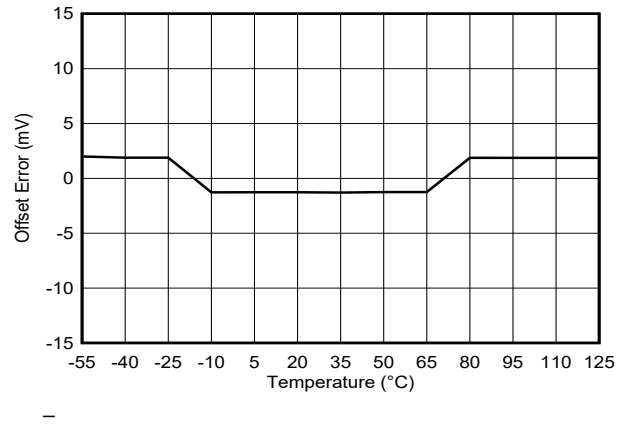


Figure 5-27. ADC Input Offset Error vs Temperature

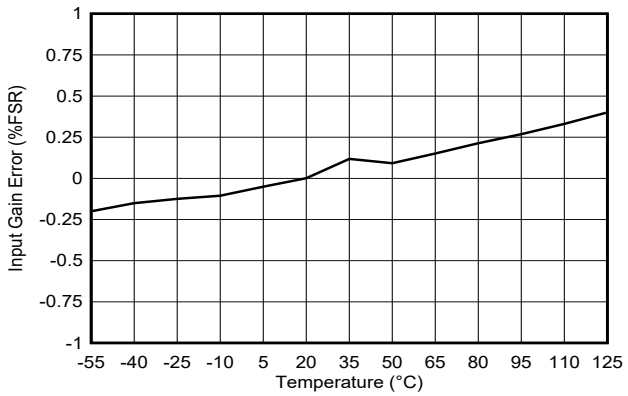


Figure 5-28. ADC Input Gain Error vs Temperature

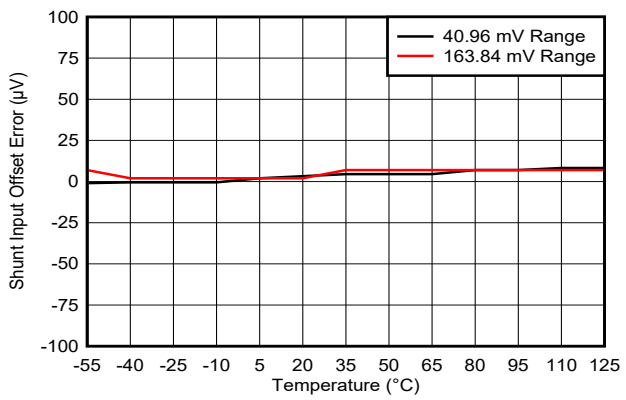


Figure 5-29. Shunt Offset Error vs Temperature

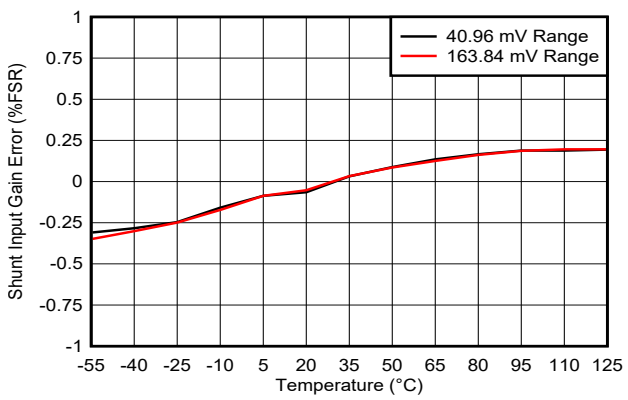


Figure 5-30. Shunt Gain Error vs Temperature

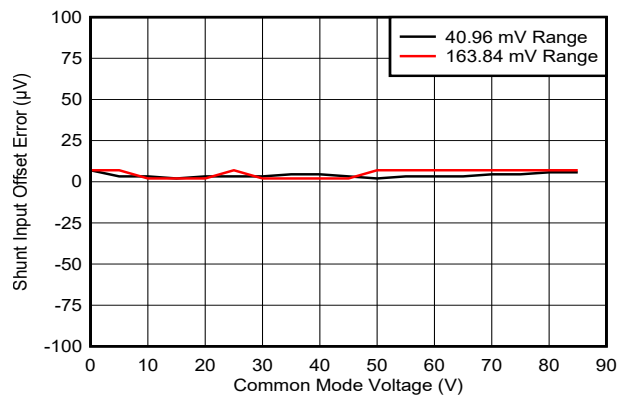


Figure 5-31. Shunt Input Offset Error vs Common-Mode Voltage

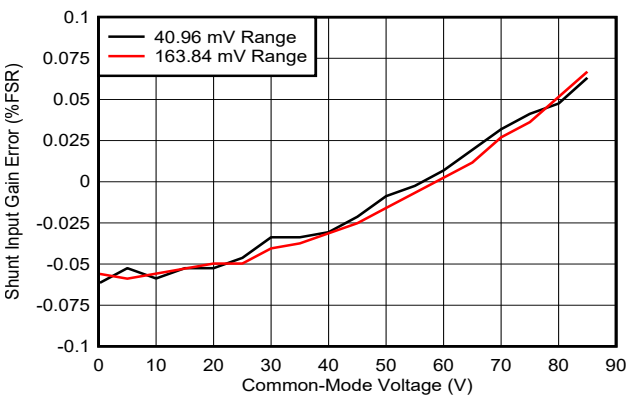


Figure 5-32. Shunt Input Gain Error vs Common-Mode Voltage

5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)

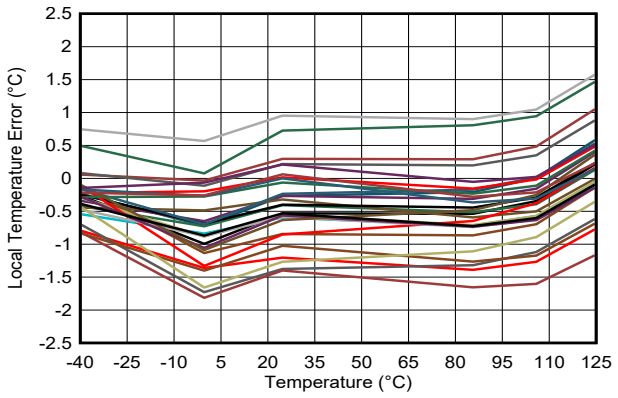


Figure 5-33. Local Temperature Sensor Error vs Temperature

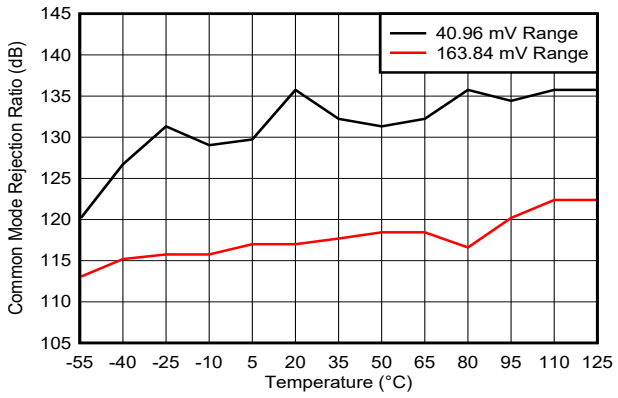


Figure 5-34. Common-Mode Rejection Ratio vs Temperature

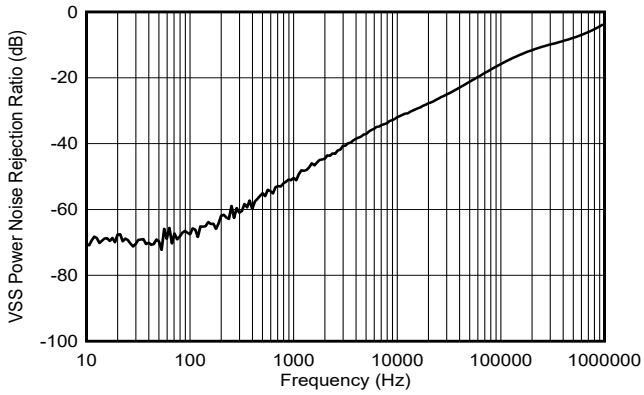


Figure 5-35. V_{SS} AC Power Supply Rejection Ratio

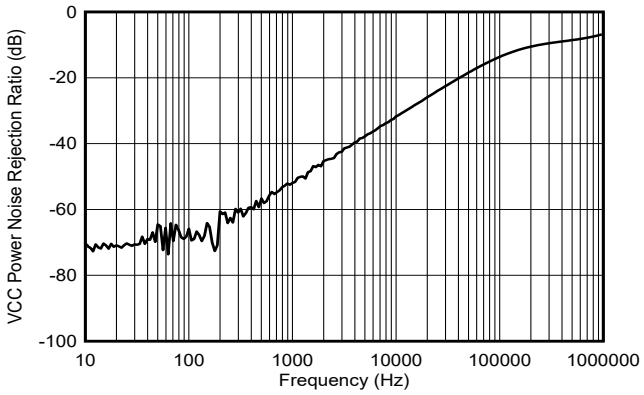


Figure 5-36. V_{CC} AC Power Supply Rejection Ratio

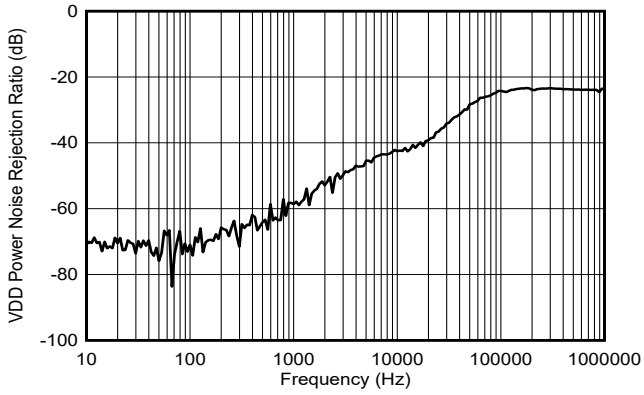
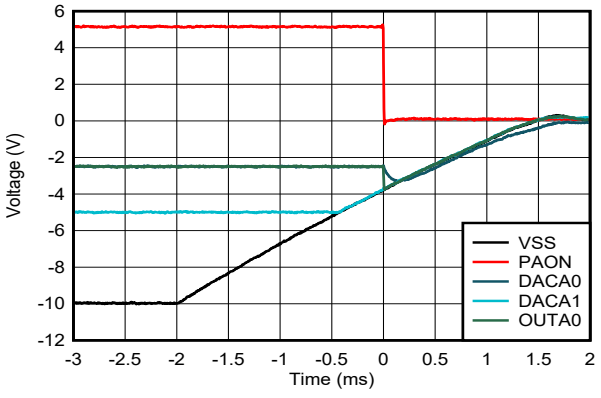


Figure 5-37. V_{DD} AC Power Supply Rejection Ratio

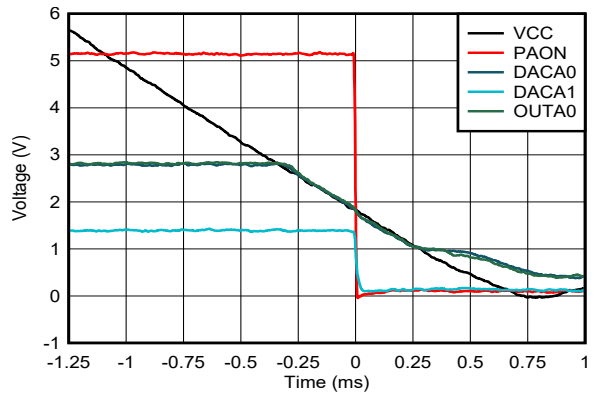


V_{SS} = –10V

Figure 5-38. V_{SS} Supply Collapse Response

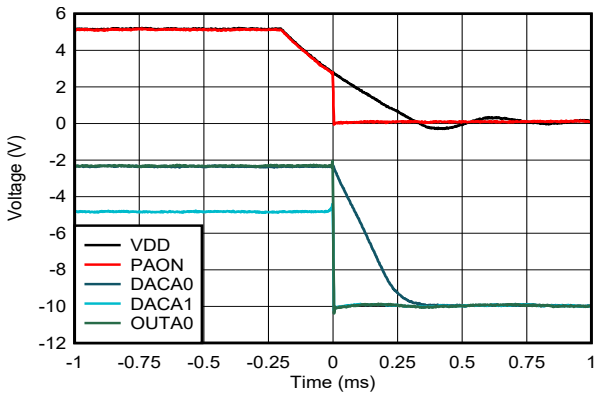
5.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 5V, V_{IO} = 3.3V, negative output range: V_{CC} = GND, V_{SS} = –11V, and DAC outputs unloaded (unless otherwise noted)



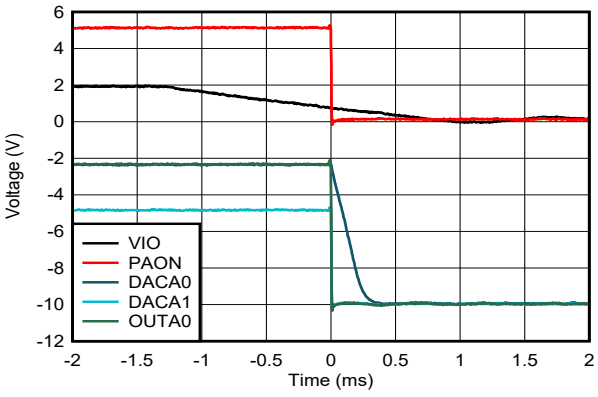
V_{CC} = 5.5V

Figure 5-39. V_{CC} Supply Collapse Response



V_{DD} = 5V

Figure 5-40. V_{DD} Supply Collapse Response



V_{IO} = 1.8V

Figure 5-41. V_{IO} Supply Collapse Response

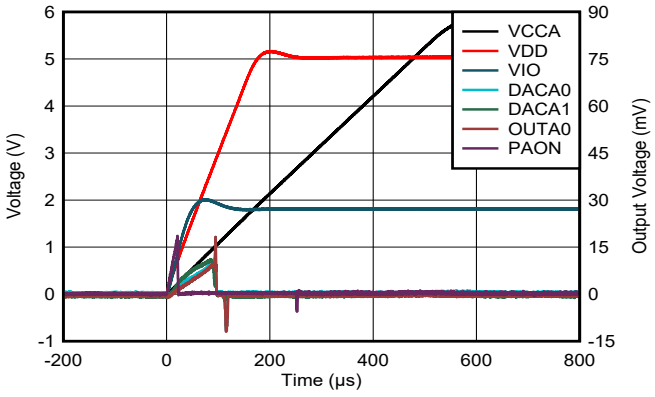


Figure 5-42. PAON Supply Response (Device Start-Up, Positive Range)

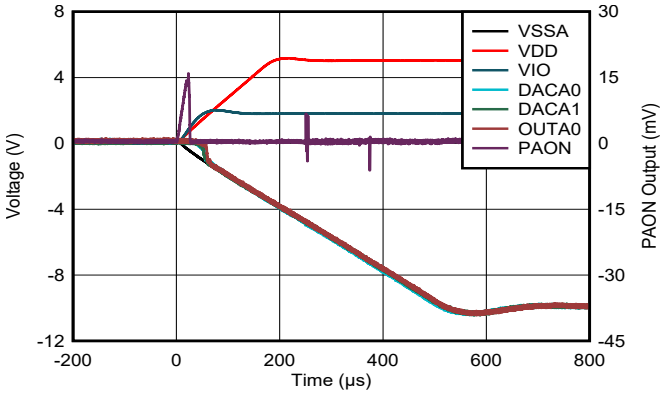


Figure 5-43. PAON Supply Response (Device Start-Up, Negative Range)

6 Detailed Description

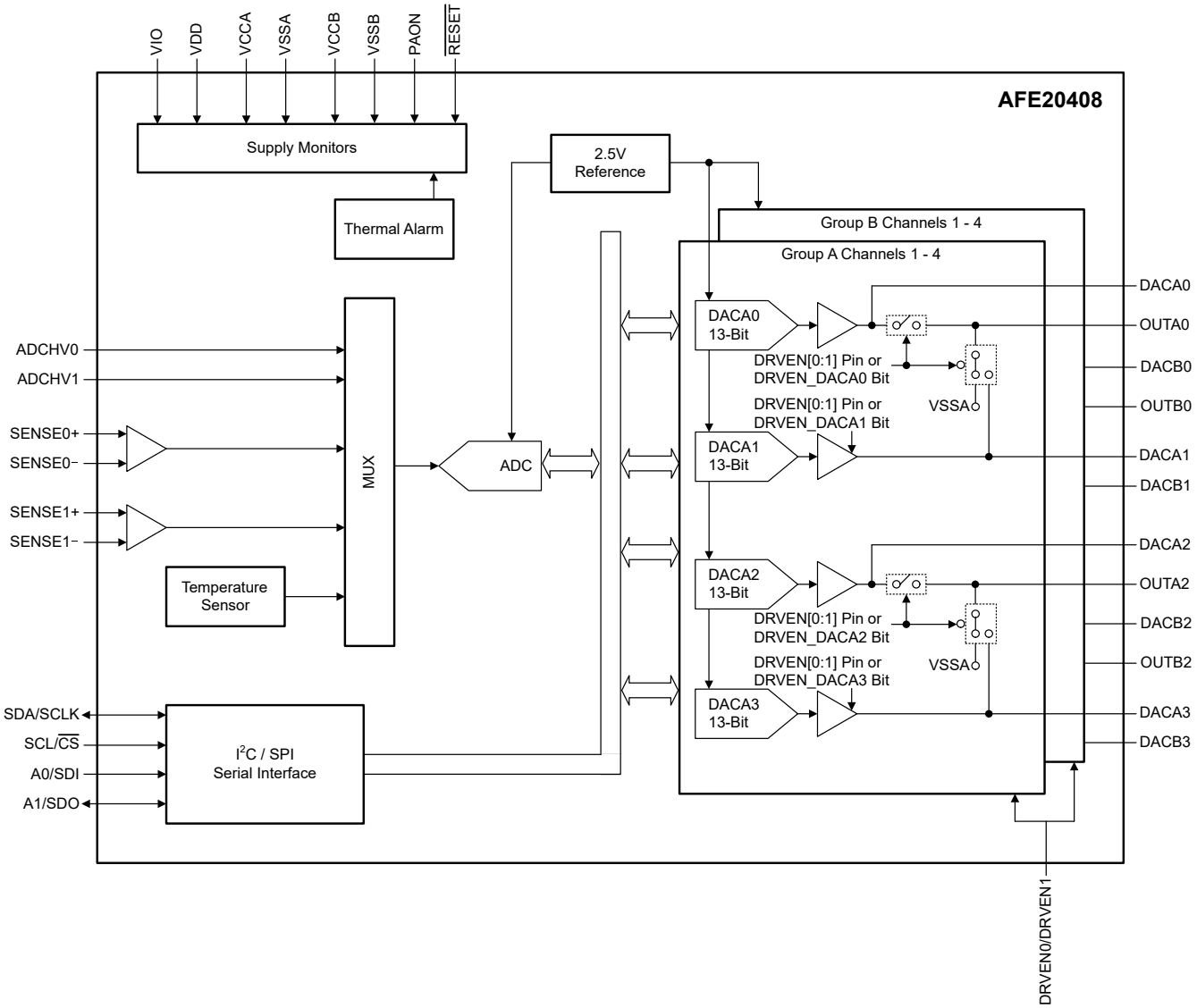
6.1 Overview

The AFE20408 is an eight-channel power amplifier (PA) controller with dedicated gate bias switch control, as well as voltage, current, and temperature supervision capabilities.

The AFE20408 eight gate bias outputs are separated into two groups, each with four digital-to-analog converters (DACs). The two output groups have dedicated supply inputs, enabling each group to operate with independent output voltage ranges. The eight gate bias outputs can be switched on and off through digital control pins or software. The output switching is designed for fast response and in combination with the device sequencing features enables a robust PA control system.

The AFE20408 external signal supervisor uses an accurate analog-to-digital converter (ADC). The supervisor is capable of monitoring two high-voltage external inputs, two high-common mode current sense inputs, and the device internal temperature. Communication to the device is performed through an SPI and I^2C compatible interface.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Digital-to-Analog Converter (DAC) Overview

The device features eight analog control channels. Each control channel is centered on a DAC that operates from the device voltage reference. Four of these DACs can be used for setting the internal switches off voltages. The DACs in the device consist of a 13-bit string DAC and an output voltage buffer. Figure 6-1 shows a block diagram of the DAC architecture.

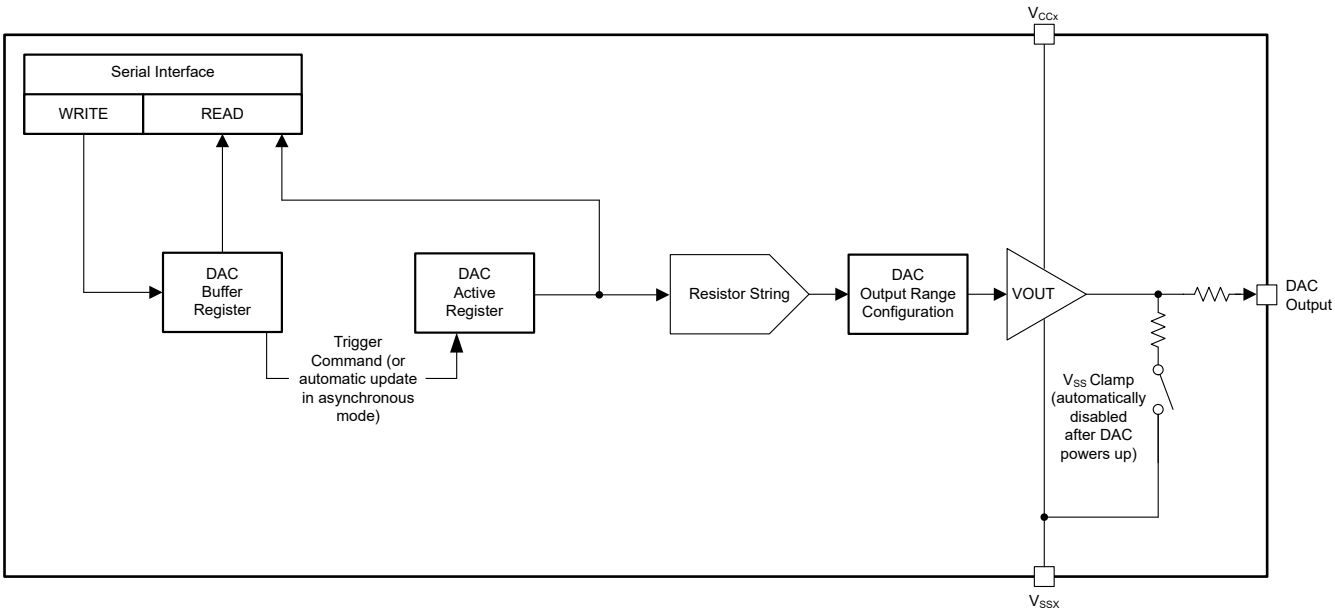


Figure 6-1. DAC Block Diagram

The DACs can be configured for positive- or negative-output-range operation with identical voltage resolution. In positive-output-range operation, the full-scale range is 0V to 10V; however, the output voltage is limited by V_{CC}. In negative-output-range operation, the full-scale range is –10V to 0V, and the output voltage is limited by V_{SS}.

After a reset event, all the DAC registers are set to zero-code, the DAC output amplifiers are powered down, and the DAC outputs are clamped to V_{SS}. Each DAC can be independently enabled through software, by writing a 1 to the appropriate bit of the PWR_EN register (located in the DAC Configuration page of the register map).

6.3.1.1 DAC Resistor String

The resistor string structure consists of a series of resistors, each of value R, as shown in Figure 6-2. The code loaded to the DAC determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one or more of the switches connecting the string to the amplifier. This resistor string architecture has inherent monotonicity, voltage output, and low glitch.

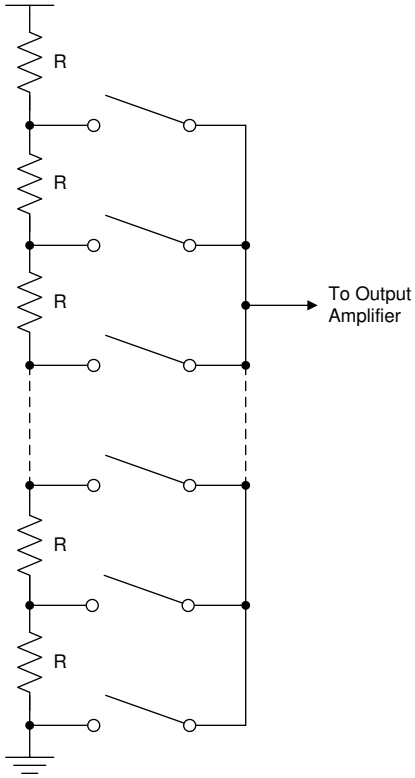


Figure 6-2. DAC Resistor String

6.3.1.2 DAC Register Structure

The DAC produces unipolar output voltages proportional to a 13-bit input data code. Input data are written to the DAC data register in straight binary format for all output ranges.

The DAC transfer function is given by:

$$V_{DAC} = \left(\frac{DACIN}{2^{13}} \times FSR\right) + V_{MIN} \quad (1)$$

where

- DACIN = the decimal equivalent of the binary code loaded to the DAC register. DACIN range = 0 to $2^{13} – 1$.
- FSR = DAC full-scale range for the selected output range. FSR is 10V for the 0V to 10V and –10V to 0V ranges.
- V_{MIN} = the lowest voltage for the selected DAC output range. Either 0V for the 0V to 10V ranges, or –10V for the –10V to 0V range.

The DAC output spans the voltage ranges shown in Table 6-1.

Table 6-1. DAC Data Format

DAC DATA REGISTER		DAC OUTPUT VOLTAGE (V)	
BINARY	HEX	0V to 10V RANGE V_{CC} = 11V V_{SS} = GND	–10V to 0V RANGE V_{SS} = –11V V_{CC} = GND
0000 0000 0000 0000	0000	0	–10
0000 0000 0000 0001	0001	0.001221	–9.998779
0001 0000 0000 0000	1000	5	–5
0001 1111 1111 1110	1FFE	9.997559	–0.002441
0001 1111 1111 1111	1FFF	9.998779	–0.001221

By setting the corresponding BCEN bits in the DAC_SYNC_CFG register (located in the DAC configuration register page), each DAC can be configured to operate in broadcast mode. When a value is written to the DAC_BCAST register (in the global register page), this value is automatically stored in the buffer and active data registers of all DACs operating in broadcast mode. Additionally, a DAC code limit feature is included, which can be used to digitally limit the DAC code to one of 64 different limits. When enabled, a limit is placed on the upper six bits of the DAC code written to the data registers. The limit is only enforced on the DAC active register, and on codes which are written after the DAC code limit has been set to a code less than full scale. The user needs to configure the DAC code limit register, and then subsequent DAC writes are subjected to the currently set DAC code limit. Code limits are specified by writing to the DAC_CODE_LIMIT registers in the DAC Configuration register page (see Section 7.5 for more details).

6.3.1.2.1 DAC Synchronous Operation

The update mode for each DAC channel is determined by the value of the corresponding SYNCEN bit in the DAC_SYNC_CFG register (in the DAC Configuration Register page). In asynchronous mode, a write to the DAC buffer data register results in an immediate update of the DAC active register and DAC outputs. In synchronous mode, writing to the DAC data register does not automatically update the DAC output. Instead, the update occurs only after a DAC trigger event. A DAC trigger signal is generated either by setting the DAC_TRIG bit in the TRIGGER register (located in the global register page) or by the FLEXIO pin when configured as $\overline{\text{LDAC}}$ (the $\overline{\text{LDAC}}$ pin can only be used to trigger DACA0 and DACA2). The synchronous update mode enables simultaneous update of multiple DAC outputs.

6.3.1.3 DAC Buffer Amplifier

The DAC output buffer amplifiers are capable of rail-to-rail operation. The amplifier outputs are available at the DAC output pins. The buffer amplifiers for the two DAC groups are biased from dedicated supply rails: $V_{CC[A,B]}$ and $V_{SS[A,B]}$. The maximum DAC group output voltage range is limited by these supplies.

The output amplifier is designed to drive capacitive loads without oscillation. The output buffers are able to source and sink up to 120mA. The device implements short-circuit protection for momentary output shorts to ground and either supply. The source and sink short-circuit current can be configured to either 30mA for low-current mode, 90mA for normal-current mode, or 120mA for high-current mode. The desired current mode can be set by writing to the DAC_CURRENT register in the DAC Configuration register page.

The high output current of the device gives good slewing characteristics even with large capacitive loads. To estimate the positive and negative slew rates for large capacitive loads, divide the source and sink short-circuit current value by the capacitor.

After start up, the DAC outputs are set automatically into V_{SS} clamp mode and the range for each group is configured automatically by the voltage present in the V_{SS}[A,B] and V_{CC}[A,B] pins. In V_{SS} clamp mode, the DAC output pins are internally connected to the V_{SS}[A,B] pins through a current limited discharge path. The DAC outputs remain in V_{SS} clamp mode until the DAC output buffers are powered up through the power enable registers.

6.3.1.3.1 Autorange Detection

The DAC buffer amplifiers are automatically configured at start up for positive voltage operation when V_{SS} = 0V and 3V ≤ V_{CC} ≤ 11V. Alternatively, the amplifiers are configured at start up for negative voltage operation (–10V to 0V, default) when V_{CC} = 0V and –3V ≤ V_{SS} ≤ –11V. The autorange detector results for each DAC group are stored in the power status register (PWR_STATUS_0).

Note

The clamp voltage of each DAC group is set by the corresponding VSS[A,B] pin. The autorange detector sets the DAC output range based on the clamp voltage. Make sure that the DAC output range setting matches the DAC clamp voltage. For positive output ranges the VSS[A,B] pins must be connected to GND, in which case the clamp voltage is 0V. For negative output ranges, the VSS[A,B] pins must be connected to negative supply voltages, in which case the unloaded clamp voltage for each group is determined by the value of the negative supply voltage (see Figure 6-3).

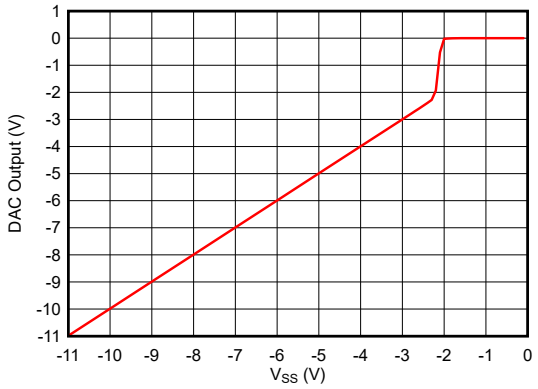


Figure 6-3. DAC Clamp Output vs V_{SS}

6.3.1.3.2 Power-Supply Monitoring

The device continuously monitors the buffer amplifier supplies of each DAC group to provide proper operation. The valid supply range for each DAC group is shown in Table 6-2.

Table 6-2. Valid Supply Matrix

DAC GROUP SUPPLY CONFIGURATION	SUPPLY	
	VCC[A,B]	VSS[A,B]
Invalid configuration	0V ≤ V_{CC} < 3V	–3V < V_{SS} ≤ 0V
V_{CC} configuration	3V ≤ V_{CC} ≤ 11V	V_{SS} = 0V
Invalid configuration	3V ≤ V_{CC} ≤ 11V	V_{SS} < 0V
V_{SS} configuration	V_{CC} = 0V	–11V ≤ V_{SS} < –3V
Invalid configuration	V_{CC} > 0V	–11V ≤ V_{SS} < –3V

During operation, if V_{DD} drops below 3V, or V_{IO} drops below 1.65V, a power-on reset event is generated, and all DAC outputs return to the V_{SS} clamp mode. If $V_{CC[A,B]}$, $V_{SS[A,B]}$ or the internal reference voltage fall below a specified threshold value, there is no power-on reset; however the corresponding alarm bits are activated in the ALARM_STATUS registers (all located within the global register page), which in turn can be used to automatically power down any DAC output.

6.3.2 Analog-to-Digital Converter (ADC)

The AFE20408 features a monitoring system centered on a 16-bit delta-sigma ADC. The ADC measures shunt voltage, bus voltage, and internal temperature. Programmable registers allow flexible configuration for measurement precision as well as automatic or direct operation

6.3.2.1 Versatile High-Voltage Measurement Capability

The ADC can measure voltage and current on rails as high as 85V. Measure the current by sensing the voltage drop across an external shunt resistor at the SENSE+ and SENSE– pins. The voltage drop across the SENSE pins can be measured by the ADC using one of two full-scale range settings. Configure these settings by writing to the SHUNT_RANGE bit in the ADC_GEN_CFG register (located in the ADC configuration register page). The input stage of the ADC is designed such that the input common-mode voltage can be higher than the device supply voltage. The supported common-mode voltage range at the input pins is –0.3V to +85V, which makes the device an excellent choice for both high-side and low-side current measurements. There are no special considerations for power-supply sequencing because the common-mode input range and device supply voltage are independent of each other; therefore, the bus voltage can be present with the supply voltage off, and vice-versa without damaging the device.

The device also measures the bus supply voltage through the ADC pins and temperature through the integrated temperature sensor. The differential shunt voltage is measured between the SENSE+ and SENSE– pins, while the bus voltage is measured with respect to device ground. Monitored bus voltages can range from 0V to 85V, while monitored temperatures can range from –40°C to +125°C. Figure 6-4 shows how the shunt voltage, bus voltage, and temperature measurements are multiplexed internally to the ADCs.

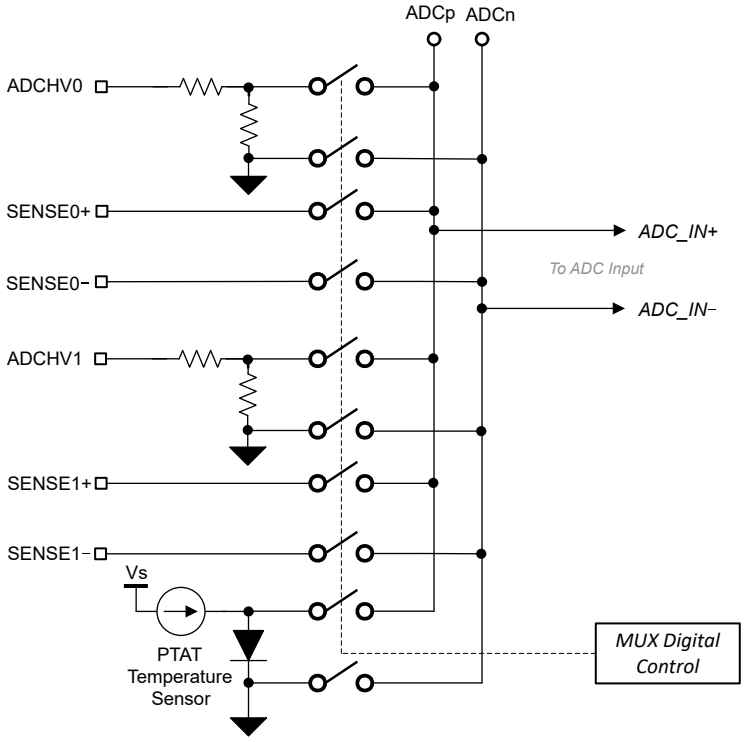


Figure 6-4. High Voltage Input Multiplexer

6.3.2.2 High-Precision Delta-Sigma ADC

The integrated ADC is a high-performance, low-offset, low-drift, delta-sigma ADC designed to support bidirectional current flow at the shunt voltage measurement channel. The measured inputs are selected through the high-voltage input multiplexer to the ADC inputs. The ADC architecture enables lower drift measurement across temperature and consistent offset measurements across the common-mode voltage, temperature, and power supply variations. A low-offset ADC is preferred in current sensing applications to provide a near 0V offset voltage that maximizes the useful dynamic range of the system.

ADC conversion time for each input can be set independently by the CONV_RATE_SENSE, CONV_RATE_ADC, and CONV_RATE_TMP bits in register ADC_CONV_CFG_0 (located in the ADC Configuration register page), in the range of 52µs to 4.122ms. Furthermore, a sample averaging function in the range of 1 × to 1024 × is implemented and can be selected by the AVG_SENSE, AVG_ADC, and AVG_TMP bits in ADC_CONV_CFG_1 register (also located in the ADC Configuration register page).

The device can measure the shunt voltage, bus voltage, and die temperature, or a combination of any based on the selected bits setting in the ADC_CCS_IDS registers (described further in Section 6.3.2.2.1). This permits selecting modes to convert only the shunt voltage or bus voltage to further allow the user to configure the monitoring function to fit the specific application requirements. When no averaging is selected, once an ADC conversion is completed, the converted values are independently updated in the corresponding registers and can be read through the digital interface at the time of conversion end. The conversion time for shunt voltage, bus voltage, and temperature inputs are set independently from 52µs to 4.122ms depending on the values programmed in the ADC_CONV_CFG_0 register. Enabled measurement inputs are converted sequentially so the total time to convert all inputs depends on the conversion time for each input and the number of inputs enabled. When averaging is used, the intermediate values are subsequently stored in an averaging accumulator, and the conversion sequence repeats until the number of averages is reached. After all of the averaging has been completed, the final values are updated in the corresponding registers that can then be read. These values remain in the data output registers until the next fully completed conversion results are ready. In this case, reading the data output registers does not affect a conversion in progress.

The ADC has two conversion modes—auto and direct—set by the CMODE bit in the ADC_GEN_CFG register. In auto-conversion mode, the ADC can continuously convert the input measurements and update the output registers in an indefinite loop. In direct-conversion mode, the ADC converts the input measurements, after which the ADC goes into shutdown mode until another single-shot trigger is generated by writing to the ADC_TRIG bit in the TRIGGER register (located in the global register page). Writing the ADC_TRIG bit interrupts and restarts auto or direct conversions that are in progress. Although the device can be read at any time, and the data from the last conversion remains available, the ADC not ready flag ($\overline{\text{ADC\_READY}}$ bit of the GEN_STATUS register, in the global register page) is provided to help coordinate triggered conversions in direct mode. This bit is cleared after all conversions and averaging are completed.

The data stored in each ADC data register can be manually overridden by a previously specified code, bypassing all ADC data conversions. This code can be set by writing to the ADC_BYP register in the ADC Configuration page of the register map. By writing a 1 to the ADC_BYP_EN bit in the GLOBAL_CFG register (located in the global register page), the codes stored in all ADC data registers are overwritten by the specified bypass value.

6.3.2.2.1 ADC Custom Channel Sequencer

The device incorporates an ADC custom channel sequencer. The ADC sequencer is used to specify which channels are converted and in which order. In this way, channels that are of greater importance can be converted more often than other lower-priority channels. The sequencer consists of 63 indexed slots that provide a high level of flexibility in the channel-order configuration. In addition, the sequencer also provides programmable start and stop index fields to configure the start and stop conversion points. In direct-mode conversion, the ADC converts from the start index to the stop index once and then stops. In auto-mode conversion, the ADC converts from the start to stop index repeatedly until the ADC is stopped.

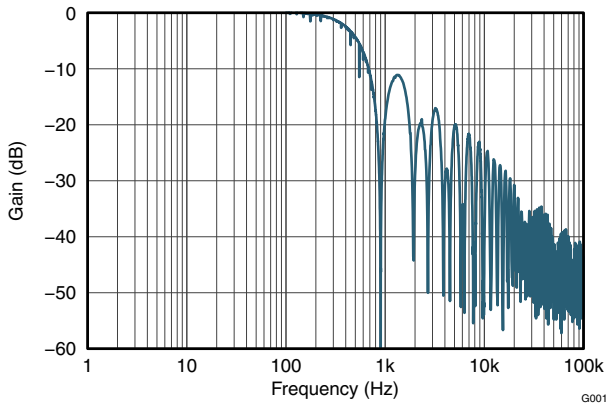
The ADC input channel assignments for the sequencer are listed in Table 6-3.

Table 6-3. Custom Channel Sequence ADC Input Assignments

CCS_ID[2:0]	ADC INPUT
000	GND
001	SENSE0
010	SENSE1
011	ADC0
100	ADC1
101	TMP

6.3.2.3 Low Latency Digital Filter

The device integrates a low-pass digital filter that performs both decimation and filtering on the ADC output data, which helps with noise reduction. The digital filter is automatically adjusted for the different output data rates and always settles within one conversion cycle. The user has the flexibility to choose different output conversion time periods (T_{CT}) from 52µs to 4.122ms. With this configuration the first amplitude notch appears at the Nyquist frequency of the output signal which is determined by the selected conversion time period and defined as f_{NOTCH}= 1 / (2 × T_{CT}). This means that the filter cut-off frequency scales proportionally with the data output rate. Figure 6-5 shows the filter response when the 1.054ms conversion time period is selected



Conversion time = 1.054ms, single conversion only

Figure 6-5. ADC Frequency Response

6.3.2.4 Flexible Conversion Times and Averaging

ADC conversion times for shunt voltage, bus voltage and temperature can be set independently from 52µs to 4.122ms. The flexibility in conversion time allows for robust operation in a variety of noisy environments. The device also allows for programmable averaging times from a single conversion all the way to an average of 1024 conversions. The amount of averaging selected applies uniformly to all active measurement inputs. Figure 6-6 and Figure 6-7 illustrate the effect of conversion time and averaging on a constant input signal.

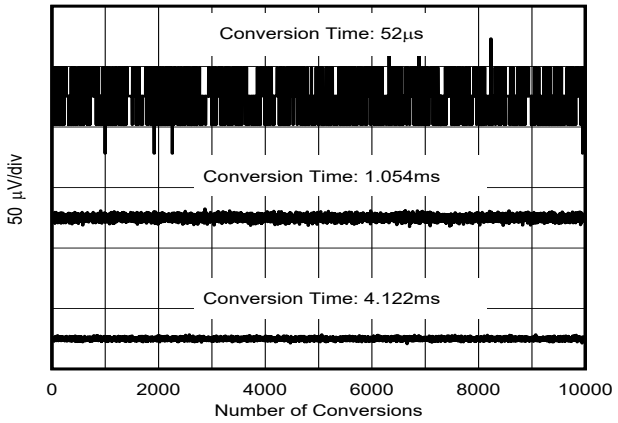


Figure 6-6. Noise vs Conversion Time (Averaging = 1)

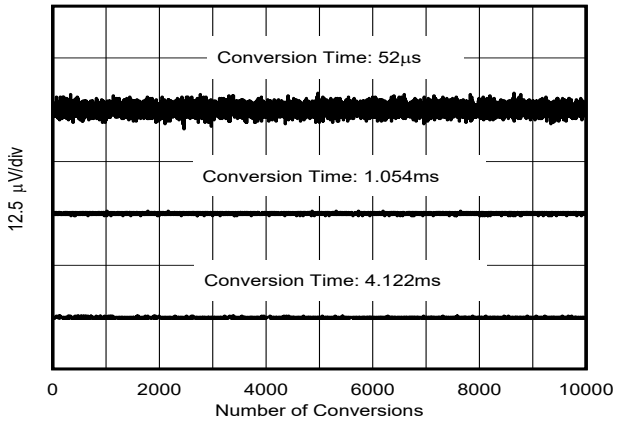


Figure 6-7. Noise vs Conversion Time (Averaging = 128)

6.3.2.5 Integrated Precision Oscillator

The internal timebase of the device is provided by an internal oscillator that is trimmed to less than 0.5% tolerance at room temperature. The precision oscillator is the timing source for ADC conversions, as well as the time-count used for calculation of energy and charge. The digital filter response varies with conversion time; therefore, the precise clock maintains filter response and notch frequency consistency across temperature. At power up, the internal oscillator and ADC take roughly 300µs to reach < 1% error stability.

6.3.3 Output Switch Overview

The AFE20408 facilitates rapid turn-on and turn-off of the voltage at the device OUT outputs. The OUT0 and OUT2 outputs (from groups A and B) can be switched on or off by the DRVEN inputs or alternatively through software. The ON voltages are set by the DAC0 and DAC2 outputs of each respective DAC group, while the OFF voltages are set by either V_{SS} or a specified clamp voltage for each DAC. The OUT0 and OUT2 pins are driven by DAC0 and DAC2 when the corresponding switch control pin or bit is asserted high (drive enabled). Otherwise, the OUT pins are in drive disabled state and driven to either V_{SS} or the corresponding clamp DAC.

Additionally, the DAC1 and DAC3 outputs from each group include a simplified switch network that facilitates fast turnoff. The DAC1 and DAC3 pins can be switched on or off, either through one of the DRVEN pins or through software. The DAC1 and DAC3 output pins are driven by the DAC1 and DAC3 buffers when on, and to V_{SS} when off. While fast turnoff is possible, turn-on time is limited by the DAC1 and DAC3 buffer bandwidth, and also DAC1 and DAC3 have to exit the power-down state.

The switches are designed to be bidirectional, allowing for two-way current when powered ON and blocking voltage when powered OFF. The switch control is optimized for minimum delay between the DRVEN input and the output pins voltage switching. The switches default to the off (drive disabled) state at start-up or after an alarm event. Along with a V_{DD} supply collapse, there are three additional reset events: a logic low on the $\overline{\text{RESET}}$ pin, a software reset command, or an I^2C general-call reset. All reset events generate a power-down, drive disable sequence. At reset, the DAC and OUT outputs go to V_{SS}.

Figure 6-8 shows the configuration of switching channels in the AFE20408, for both DAC output groups.

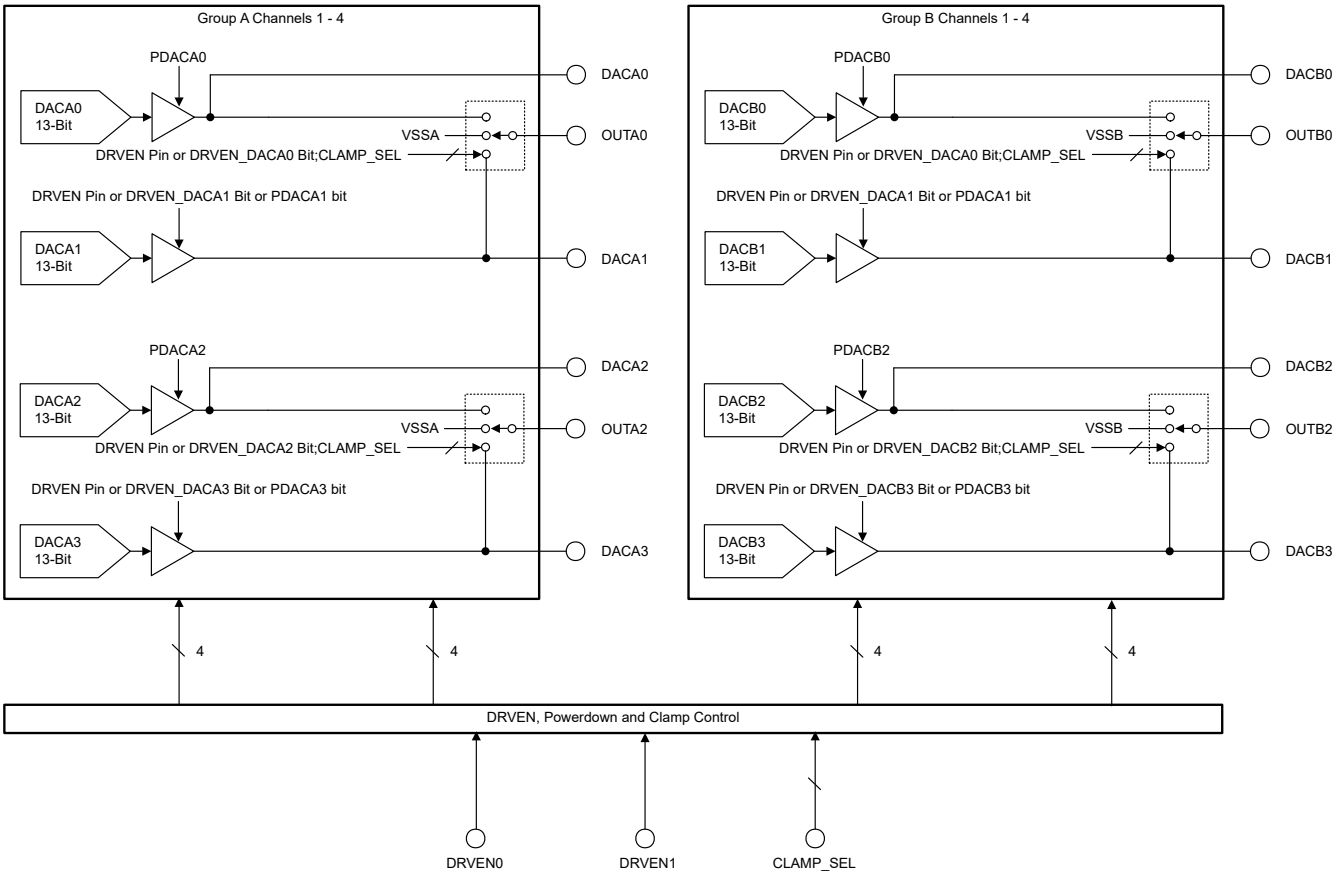


Figure 6-8. Switch Block Diagram

6.3.4 Drain Switch Control

The AFE20408 device includes an output-control voltage (PAON pin) capable of driving an external MOSFET switch that turns on and off the drain current to a PA FET. The use of this control signal in conjunction with the DAC clamp option allows control of the sequence in which the PA FET is powered up and powered down.

The PAON pin is disabled on start-up. After the device powers on, the PAON pin can be enabled by setting the PAON bit to 1, in the PWR_EN register (located in the global register page). During operation, the status of the PAON pin can be monitored by reading the PAON_STS bit in the GEN_STATUS register (located in the global register page). By default, the PAON pin is pulled to GND, and is in the OFF state.

The maximum output voltage is determined by the voltage at the VDD pin. When enabled, the PAON can be turned off by any alarm generated by the various monitoring circuits in the device, including thermal, supply, ADC, and reference alarms. This configuration is done by writing to the appropriate bits in the PAON_SRC_0 and PAON_SRC_1 registers (located in the general configuration register page).

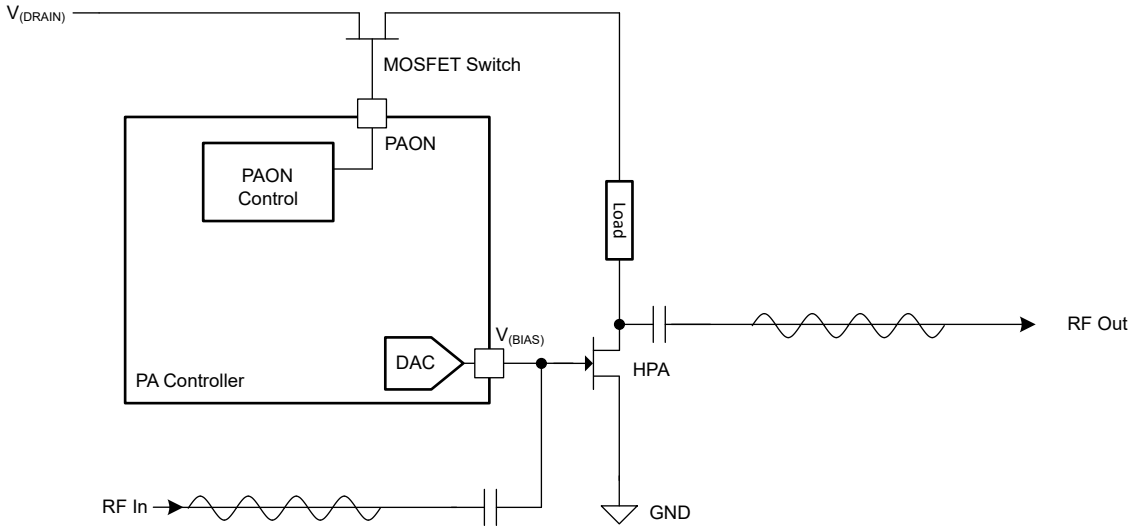


Figure 6-9. PAON Operation

The PAON pin operates in push-pull mode by default. The PAON pin can be configured to operate in open-drain mode by setting the PAON_ODE bit in the GEN_CFG_0 register (located in the general configuration register page). In push-pull mode, the PAON pin is internally connected to VDD via a pullup resistor. As a result, the PAON pin outputs 0V (or the voltage at GND) while in the OFF state, and V_{DD} while in the ON state. In the open drain mode, there is no internal pullup resistor to the VDD pin, and the user must install an external pullup resistor to VDD. This is further described in Section 8.2.2.4.

Additionally, the PAON pin can be configured to invert the ON and OFF states (so that the high voltage is off and the low voltage is on) by setting the PAON_POL bit in the GEN_CFG_0 register (located in the general configuration register page).

For FETs requiring a negative bias voltage, such as GaN, making sure that the bias voltage remains within an acceptable range is crucial; otherwise, significant and irreversible damage to the FET can occur. The AFE20408 bipolar DAC operation and clamping mechanism rely on the V_{DD} and V_{SS} voltages for proper operation. For this reason, when either the V_{DD} or V_{SS} voltage falls outside the acceptable range, turning off the drain current to the FET is desirable.

6.3.5 FLEXIO Pin

The AFE20408 features a FLEXIO pin that can be independently configured as a GPIO or a special function pin. The function performed by the FLEXIO pin depends on the value written to the FLEXIO_FUNC field of the GEN_CFG_1 register (located in the General Configuration page of the register map).

On the AFE20408, the following functions are performed by the FLEXIO pin. To enable FLEXIO special functions on any DAC, the corresponding bits in the FLEXIO_EN register (located in the DAC Configuration register page) must be set.

1. $\overline{\text{RESET}}$: When FLEXIO_FUNC is 0x01, the FLEXIO pin acts as an active-low external reset. This is the default function of the FLEXIO pin
2. $\overline{\text{ALARMOUT}}$: When FLEXIO_FUNC is set to 0x02, the FLEXIO pin acts as an active-low alarm output. The $\overline{\text{ALARMOUT}}$ pin is by default active-low, push-pull, but both the active level and the drive type can be configured by writing to the FLEXIO_OUT_POL and FLEXIO_OUT_ODE bits; see also Section 7.2.1.4. The ALARMOUT_SRC registers (addresses 0x48 and 0x49 in the General Configuration register page) are used to configure the alarms that assert the pin; see also Section 7.2.
3. GPIO: When FLEXIO_FUNC is set to 0x04, the FLEXIO pin acts as a GPIO pin. The GPIO acts as an output during write operations, and as an input during read operations. When a GPIO pin acts as an output, the pin state can be set by writing to the GPIO bit in the GPIO_DATA register, located in the global register map. As with the $\overline{\text{ALARMOUT}}$ function, the GPIO output is by default active-low, push-pull, but both the active level and the drive type can be configured by writing to the FLEXIO_OUT_POL and FLEXIO_OUT_ODE bits. When a GPIO pin acts as input, the digital value on the pin is acquired by reading the GPIO_DATA register address. After a power-on reset or any forced reset, all GPIO_DATA bits are reset to 1.
4. $\overline{\text{LDAC}}$: When FLEXIO_FUNC is set to 0x08, the FLEXIO pin acts as a trigger input for DAC outputs DACA0 and DACA2. Specifically, when these DACs are configured to operate in synchronous mode, the active data registers for these DACs only update once the pin has been pulled to logic 0.
5. $\overline{\text{ALARMIN}}$: When FLEXIO_FUNC is set to 0x10, the FLEXIO pin acts as an active-low alarm input pin. On the AFE20408, the $\overline{\text{ALARMIN}}$ inputs can trigger DAC auto-power-down and OUT pin auto-power-down events by setting the appropriate bits in the DAC_APD_SRC and OUT_APD_SRC registers, located in the DAC Configuration register page.
6. DRVEN: When FLEXIO_FUNC is set to 0x20, the FLEXIO pin acts as an additional switch control input DRVEN2, in addition to the existing DRVEN0 and DRVEN1 pins on the device. By writing to the respective bits in the FLEXIO_EN register (located in the DAC Configuration register map) DRVEN2 control can be enabled on any desired DAC.

6.3.6 Internal Temperature Sensor

The device has an on-chip temperature sensor that measures the device die temperature. The normal operating temperature range for the internal temperature sensor is limited by the operating temperature range of the device (–55°C to +150°C).

The temperature sensor has a resolution of 16 bits (0.0078°C) and conversion is independent from the device SAR ADC. Temperature data results are represented in binary format, as shown in Table 6-4. The temperature data format allows for representation of negative temperatures using signed 2's complement representation. Make sure to observe the parameter values listed in the *Absolute Maximum Ratings* table.

Table 6-4. Temperature Data Format (ADC_TMP [15:0])

TEMPERATURE (°C)	INTERNAL TEMPERATURE REGISTER VALUE	
	BINARY	HEX
–55	1111 1111 1100 1001	FFC9
–25	1111 1111 1110 0111	FFE7
–1	1111 1111 1111 1111	FFFF
0	0000 0000 0000 0000	0000
1	0000 0000 1000 0000	0080
10	0000 0101 0000 0000	0500
25	0000 1100 1000 0000	0C80
50	0001 1001 0000 0000	1900
75	0010 0101 1000 0000	2580
100	0011 0010 0000 0000	3200
125	0011 1110 1000 0000	3E80
127	0011 1111 1000 0000	3F80
150	0100 1011 0000 0000	4B00

The temperature data registers are accessed by reading the ADC_TMP register, located in the global register page.

6.3.7 Programmable Out-of-Range Alarms

The AFE20408 is capable of continuously analyzing the supplies, reference, external ADC inputs, and internal temperature for normal operation. Normal operation for the conversion results is established through the lower- and upper-threshold registers. When any of the monitored inputs is out of the specified range, the corresponding alarm bit in the alarm status registers is set. In addition, the global alarm bit (GALR in the GEN_STATUS register) is also set.

All of the alarms can be set to activate the FLEXIO pin, when configured as $\overline{\text{ALARMOUT}}$. Any alarm event can activate the pin as long as the alarm is not masked in the ALARMOUT_SRC registers. When an alarm event is masked, the occurrence of the event sets the corresponding status bit in the alarm status registers, but does not activate the $\overline{\text{ALARMOUT}}$ pin.

The ALARM_LATCH_DIS bit (located in the GEN_CFG_0 register, part of the General Configuration register page) sets the latching behavior for the internal device alarms, as well as the $\overline{\text{ALARMOUT}}$ pin. When the ALARM_LATCH_DIS bit is cleared to 0, the alarms are latched. The alarms are referred to as being latched because the GALR bit and $\overline{\text{ALARMOUT}}$ pin remain active until the GEN_STATUS register is read by software, even if the alarm condition subsides before the read. This design makes sure that out-of-limit events cannot be missed if the software is polling the device periodically. When the ALARM_LATCH_DIS bit is set to 1, the alarm bits are not latched. In this case, the GALR bit and $\overline{\text{ALARMOUT}}$ pin are deactivated as soon as the error condition subsides, regardless of whether the GEN_STATUS register is read or not. Regardless of the ALARM_LATCH_DIS bit value, all bits in the alarm status registers are cleared only after a software read. Read the alarm status registers twice to confirm that the bits have cleared after the alarm condition subsides. These bits are reasserted if the out-of limit condition still exists on the next monitoring cycle.

In addition, all of the alarms can be set to force one or more DACs to the power-down state. To enable this functionality, the alarm event must be enabled as a power-down source by writing to the appropriate bits within the DAC_APD_SRC and OUT_APD_SRC registers (all located within the DAC Configuration register page). Additionally, the DAC outputs to be controlled by the alarm event must be specified. In this application, when a DAC control alarm event is detected, all the DACs that are set to power down in response to the alarm do so. When the alarm event is cleared, the DACs are reloaded with the contents of the DAC active registers, which allows the DAC outputs to return to the previous operating point without any additional commands.

6.3.7.1 Temperature Sensor Alarm Function

The AFE20408 continuously monitors the internal die temperature. The device includes a thermal error alarm bit (THERMERR_ALR) that is set when the die temperature exceeds 150°C. A thermal error alarm can be configured to set the $\overline{\text{ALARMOUT}}$ pin, as well as configures all DAC outputs into the power-down state. If a power-down event occurs due to a thermal alarm, the DAC outputs remain in power-down mode even after the device temperature lowers below 150°C. To resume normal operation, the thermal error alarm must be cleared while the DAC channels are in power-down mode. Apart from the thermal error alarm, the device also features a temperature alarm with a configurable threshold (written to the TMP_UP_THRESH register in the ADC Configuration register page). The TMP_ALR bit, located in the ALARM_STATUS_0 global register, is set when the temperature exceeds the threshold, and can be configured to set the $\overline{\text{ALARMOUT}}$ pin or trigger DAC power-down events.

6.3.7.2 Supply Out-of-Range Alarm Function

The AFE20408 is capable of monitoring all power supply voltages, including the internal reference. For VSS and VCC power supply pins, after the voltage supply reaches the power-on threshold, the corresponding bits in the Alarm Status registers are set if the magnitude of voltage at the respective supply pin is less than the supply collapse threshold. Table 6-5 shows the voltage thresholds for power-supply alarm activation.

Table 6-5. Supply Alarm Thresholds

POWER SUPPLY	ALARM THRESHOLD (POWER-ON)	ALARM THRESHOLD (SUPPLY COLLAPSE)
VDD	2.3V	2.6V
VCCA/VCCB	2.2V	1.7V
VSSA/VSSB (low-range)	–2.2V	–1.7V
VSSA/VSSB (mid-range)	–3.7V	–3.2V
VSSA/VSSB (high-range)	–6.7V	–6.2V

The alarm depends on voltage magnitude (not polarity); therefore, the VSSA and VSSB alarms are set when the respective pin voltages are less negative than the specified supply collapse thresholds. Additionally, the VSSA and VSSB alarm thresholds are determined based on the range selected for the respective DAC group; see also Section 7.2.1.5.

The device provides out-of-range detection for the high performance internal reference. If the internal reference voltage is less than 1.5V (after initially reaching a power-on threshold of 2.0V), the reference alarm flag is set. Verify that the reference alarm condition has not been issued prior to powering up the DAC output buffers.

By setting the appropriate bits in the DAC_APD_SRC and OUT_APD_SRC registers, both the power supply and internal reference alarms can be configured to trigger the alarm pin, a DAC auto power-down event, or both.

6.3.7.3 ADC Alarm Function

The device provides independent out-of-range detection for each of the ADC inputs. Figure 6-10 shows the out-of-range detection block. When the measurement is out-of-range, the corresponding alarm bit in the alarm status register is set to flag the out-of-range condition. The values in the ADC high limit and low limit registers define the upper and lower bound thresholds for the ADC inputs.

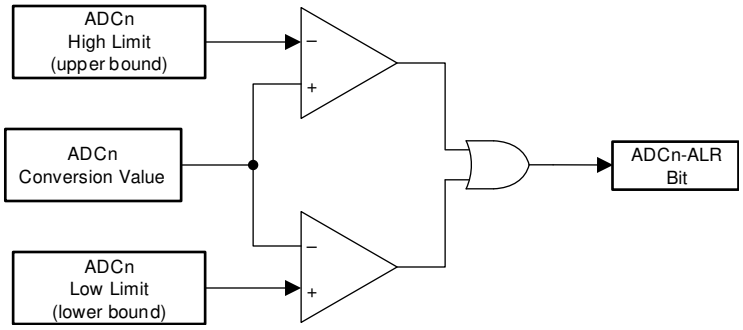


Figure 6-10. ADC Inputs Out-of-Range Alarms

To prevent false alarms, an alarm event is only registered when the monitored signal is out of range for an *N* number of consecutive conversions. If the monitored signal returns to the normal range before N consecutive conversions, an alarm event is not issued. The false alarm factor, N, for the ADC input alarms can be configured by writing to the FALR_ADC, FALR_SENSE and/or FALR_TMP fields in the ADC_GEN_CFG register (located in the ADC Configuration register page).

If an ADC input signal is out of range and the alarm is enabled, the corresponding alarm bit is set to 1. However, the alarm condition is cleared only when the conversion result returns either a value lower than the high limit register setting or higher than the low limit register setting by the number of codes specified in the ADC hysteresis setting (see Figure 6-11). The hysteresis for ADC alarms can be set by writing to bits 7 through 0 in the ADC_HYST_0 register. Hysteresis can also be set for the SENSE input alarms, by writing to bits 7 through 0 in the ADC_HYST_1 register. In both these cases, the hysteresis is a programmable value between 0 LSB to 127 LSB.

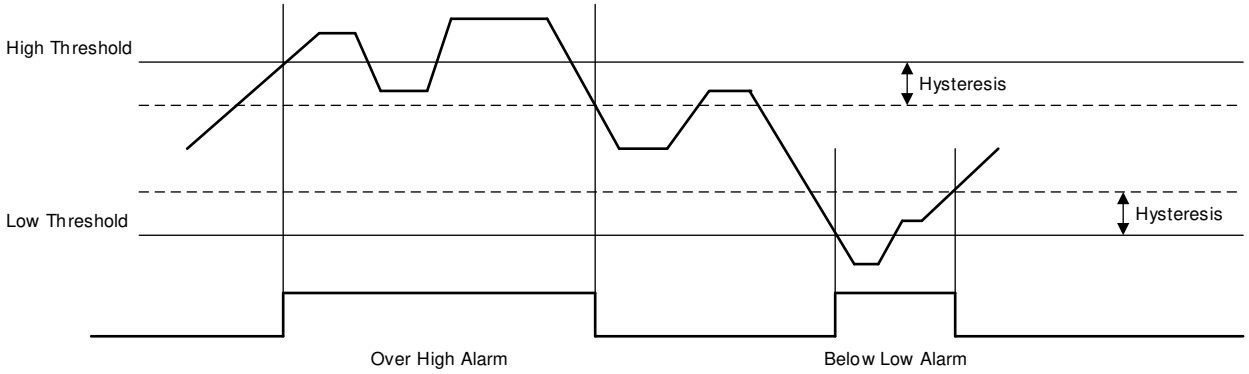


Figure 6-11. ADC Alarm Hysteresis

6.4 Device Functional Modes

The DACs in the AFE20408 are split into groups A and B, each with four DAC channels and two OUT channels. The output range and clamp voltage for each DAC group is set independently, and thus, enables the device to operate in one of the following modes:

- All-positive DAC range mode
- All-negative DAC range mode
- Mixed DAC range mode

6.4.1 All-Positive DAC Range Mode

In the AFE20408 all-positive DAC range mode, the two DAC groups are set to a positive-voltage output range (0V to 10V).

The minimum DAC output for each group cannot be less than the corresponding V_{SS} voltage. In all-positive DAC range mode, the minimum DAC output for both groups is 0V, and consequently, the VSSA and VSSB pins must be connected to GND.

The maximum DAC output for each group cannot be greater than the corresponding V_{CC} voltage. In all-positive DAC range mode, the VCCA and VCCB pins must be connected to a positive supply voltage; however these pins are not required to be tied to the same potential. Typically, the positive voltage at each VCC pin is dictated by the desired positive-voltage output range, but this configuration is not required. In the case where the V_{CC} supply voltage for a group is less than the positive full-scale range configuration, the maximum DAC voltage is limited to $V_{CC[A,B]}$. Table 6-6 lists the typical configurations for this mode.

Table 6-6. All-Positive DAC Range Mode Typical Configuration

PIN	TEST CONDITIONS	TYPICAL CONNECTION
VDD		4.5V to 5.5V
VIO	$V_{IO} \le V_{DD}$	1.65V to 5.5V
VCCA	$V_{DACA} \le V_{CCA}$	$3V \le V_{CCA} \le 11V$
VCCB	$V_{DACB} \le V_{CCB}$	$3V \le V_{CCB} \le 11V$
VSSA		GND
VSSB		GND
Thermal Pad		GND

After a reset event, the output range for each DAC group is automatically set by the autorange detector.

The VSS[A,B] pins set the clamp voltage for each DAC group. The clamp voltage depends only on the voltage in the VSS[A,B] pins; therefore, changes to the DAC range registers do not affect the clamp setting. With both VSSA and VSSB pins connected to GND, the clamp voltage for all DACs is 0V.

6.4.2 All-Negative DAC Range Mode

In the AFE20408 all-negative DAC range mode, the two DAC groups are set to a negative-voltage output range (–10V to 0V).

The maximum DAC output for each group cannot be less than the corresponding V_{CC} voltage. In all-negative DAC range mode, the maximum DAC output for both groups is 0V, and consequently, the VCCA and VCCB pins must be connected to GND.

The minimum DAC output for each group cannot be less than the corresponding V_{SS} voltage. In all-negative DAC range mode, the VSSA and VSSB pins must be connected to a negative supply voltage; however, these pins are not required to be tied to the same potential. Specifically, the voltage at the VSSA pin must always be less than (more negative) or equal to the VSSB voltage. Typically, the negative voltage at each VSS pin is dictated by the desired negative-voltage output range, but this configuration is not required. In the case where the V_{SS} supply voltage for a group is less than the negative full-scale range configuration, the minimum DAC voltage is limited to $V_{SS[A,B]}$. Table 6-7 lists the typical configurations for this mode.

Table 6-7. All-Negative DAC Range Mode Typical Configuration

PIN	TEST CONDITIONS	TYPICAL CONNECTION
VDD		4.5V to 5.5V
VIO	$V_{IO} \le V_{DD}$	1.65V to 5.5V
VCCA		GND
VCCB		GND
VSSA	$V_{DACA} \ge V_{SSA}$	$-11V \le V_{SSA} \le -3V$
VSSB	$V_{DACB} \ge V_{SSB}$	$-11V \le V_{SSB} \le -3V$
Thermal Pad		GND

After a reset event, the output range for each DAC group is automatically set by the autorange detector.

The VSS[A,B] pins set the clamp voltage for each DAC group. The clamp voltage depends only on the voltage in the VSS[A,B] pins; therefore, changes to the DAC range registers do not affect the clamp setting. With both VSSA and VSSB pins connected to negative supply voltages, the clamp voltage for DAC group A is equal to V_{SSA}, and the clamp voltage for DAC group B is equal to V_{SSB}.

6.4.3 Mixed DAC Range Mode

In the AFE20408 mixed DAC range mode, DAC group A is set to a negative-voltage output range (–10V to 0V) and DAC group B is set to a positive-voltage output range (0V to 10V). DAC group B cannot be set to a negative-voltage output range if DAC group A is set to a positive-voltage output range.

The VCC pin of DAC group B must be connected to a positive supply voltage. Typically, the positive voltage at the VCC pin is dictated by the desired positive-voltage output range, but this configuration is not required. In the case where the V_{CC} supply voltage for the positive-voltage output range group is less than the positive-voltage full-scale-range configuration, the maximum DAC voltage is limited to V_{CC}. The VSS pin of DAC group B must be connected to GND.

The VSS pin of DAC group A must be connected to a negative supply voltage. Typically, the negative voltage at the VSS pin is dictated by the desired negative-voltage output range, but this configuration is not required. In the case where the V_{SS} supply voltage for the negative output range group is less than the negative full-scale range configuration, the minimum DAC voltage is limited to V_{SS}. The VCC pin of DAC group A must be connected to GND. Table 6-8 lists the typical configurations for this mode.

Table 6-8. Mixed DAC Range Mode Typical Configuration

PIN	TEST CONDITIONS	TYPICAL CONNECTION
VDD		4.5V to 5.5V
VIO	$V_{IO} \le V_{DD}$	1.65V to 5.5V
VCCA		GND
VCCB	$V_{SS} \le V_{DACB} \le V_{CC}$	$3V \le V_{CC} \le 11V$
VSSA	$V_{SS} \le V_{DACA} \le V_{CC}$	$–11V \le V_{SS} \le –3V$
VSSB		GND
Thermal Pad		GND

The VSS[A,B] pins set the clamp voltage for each DAC group. The clamp voltage depends only on the voltage in the VSS[A,B] pins; therefore, changes to the DAC range registers do not affect the clamp setting. The clamp voltage for DAC group A is equal to V_{SSA}, and the clamp voltage for DAC group B is equal to V_{SSB}.

6.5 Programming

The device communicates with the system controller through a serial interface, which supports either an I^2C-compatible two-wire bus, or an SPI-compatible bus. The device includes a robust mechanism that detects between an SPI-compatible or I^2C-compatible controller, and automatically configures the interface accordingly. The interface detection mechanism operates at start-up, thus preventing protocol change during normal operation.

Figure 6-12 shows that the device uses a paging system to organize registers by functionality.

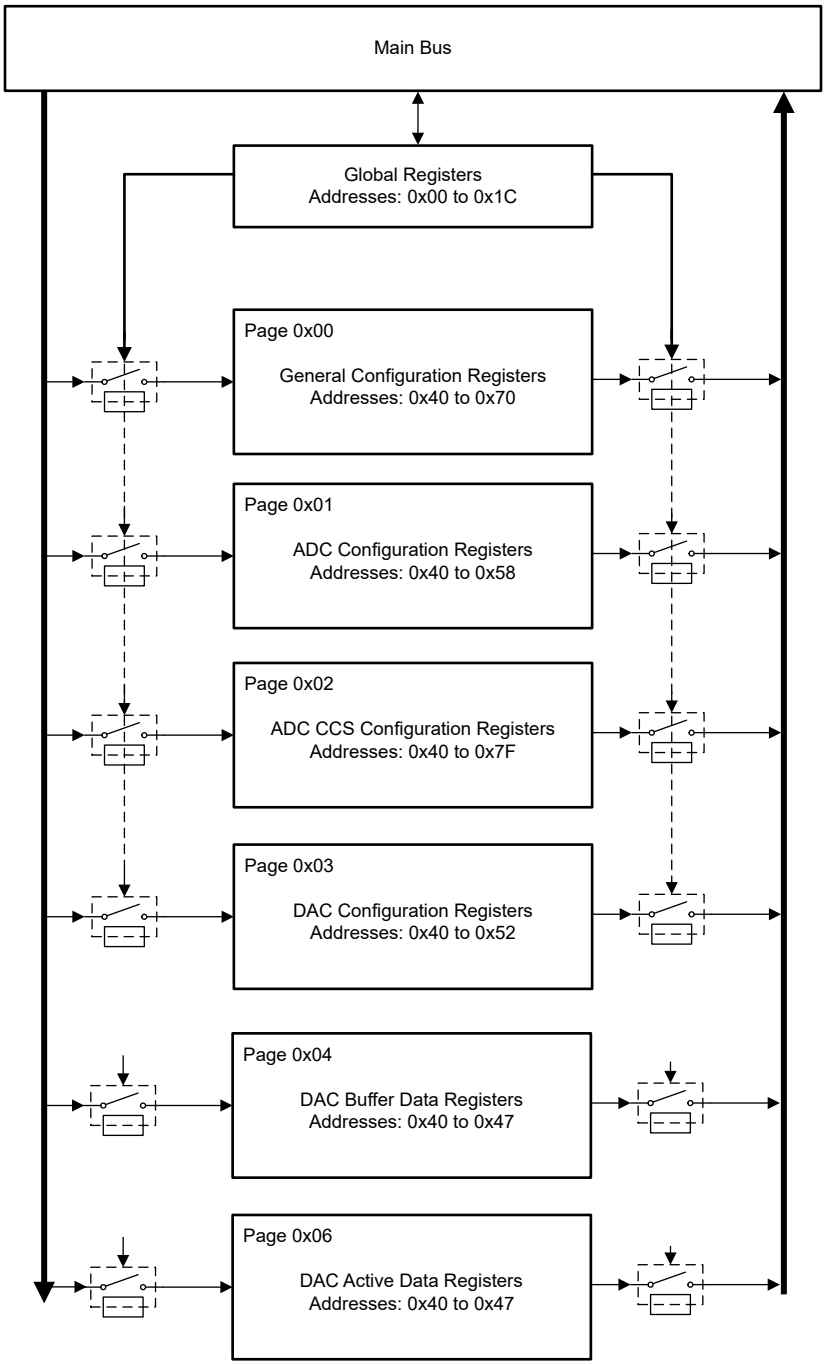


Figure 6-12. Register Page System

In both SPI and I²C configurations, address 0x01 is used to select the different pages in the device. To read and write to one of the device registers, the page for that register must first be selected by writing the 5-bit representation of the page number (PAGE[4:0]) to address 0x01, as shown in Figure 6-13. The page register holds the page value until a new page address is programmed to the device.

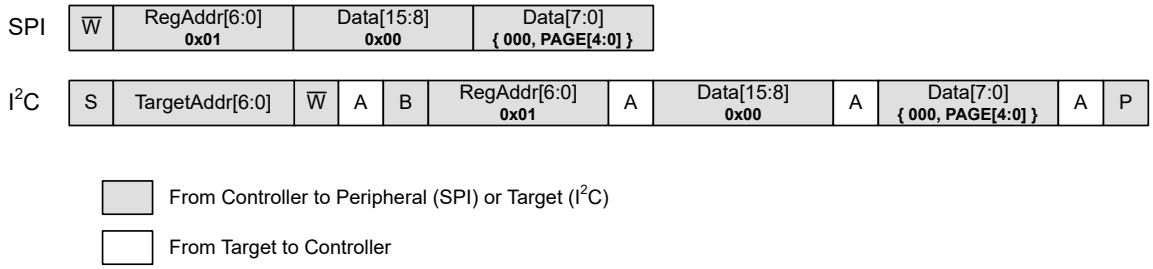


Figure 6-13. Page Access Format

Addresses 0x00 to 0x3F in each page are global registers, thus enabling access of these bits regardless of the page configuration.

6.5.1 I²C Serial Interface

In I²C mode, the device operates only as a target device on the two-wire bus. Connections to either bus are made using the open-drain I/O lines, SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The device supports the transmission protocol for fast mode (1kHz to 400kHz). All data bytes are transmitted MSB first.

6.5.1.1 I²C Bus Overview

The device is I²C compatible. In I²C protocol, the device that initiates the transfer is called a *controller*, and a device controlled by the controller is called a *target*. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates the START and STOP conditions.

To address a specific device, a START condition is initiated. A START condition is indicated by pulling the data line (SDA) from a high-to-low logic level while SCL is high. All targets on the bus receive the target address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an acknowledge bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high because any change in SDA while SCL is high is interpreted as a control signal.

After all data have been transferred, the controller generates a STOP condition. A STOP condition is indicated by pulling SDA from low to high, while SCL is high.

6.5.1.2 I²C Bus Definitions

The device is I²C-compatible and the bus definitions are listed in Table 6-9.

Table 6-9. I²C Symbol Set

CONDITION	SYMBOL	SOURCE	DESCRIPTION
START	S	Controller	Begins all bus transactions. A change in the state of the SDA line, from high to low, while the SCL line is high, defines a START condition. Each data transfer initiates with a START condition
STOP	P	Controller	Terminates all transactions and resets bus. A change in the state of the SDA line from low to high while the SCL line is high defines a STOP condition. Each data transfer terminates with a repeated START or STOP condition.
IDLE	I	Controller	Bus idle. Both SDA and SCL lines remain high.
ACK (Acknowledge)	A	Controller/Target	Handshaking bit (low). Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Take setup and hold times into account.
NACK (Not Acknowledge)	$\overline{A}$	Controller/Target	Handshaking bit (high). On a controller receive, data transfer termination can be signaled by the controller generating a not-acknowledge on the last byte that has been transmitted by the target.
READ	R	Controller	Active-high bit that follows immediately after the target address sequence. Indicates that the controller is initiating the target-to-controller data transfer. The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the controller device. The receiver acknowledges data transfer.
WRITE	$\overline{W}$	Controller	Active-low bit that follows immediately after the target address sequence. Indicates that the controller is initiating the controller-to-target data transfer. The number of data bytes transferred between a START and a STOP condition is not limited and is determined by the controller device. The receiver acknowledges data transfer.
REPEATED START	Sr	Controller	Generated by controller, same function as the START condition (highlights the fact that STOP condition is not strictly necessary.)
BLOCK ACCESS	B	Controller	Active-high bit that indicates the controller is initiating a block access data transfer.

6.5.1.3 I²C Target Address Selection

The I²C bus target address is selected by installing shunts from the A0 and A1 address pins to the V_{IO} or GND rails. The state of the address pins is tested after every occurrence of START condition on the I²C bus. The device discerns between four possible options for each pin, shunt to V_{IO} (logic 1), shunt to GND (logic 0), shunt to SDA, and shunt to SCL for a total of sixteen possible target addresses, as shown in Table 6-10.

Table 6-10. I²C Target Address Space

DEVICE PINS		I²C TARGET ADDRESS
A1	A0	[A6:A0]
0	0	101 0000
0	1	101 0001
0	SDA	101 0010
0	SCL	101 0011
1	0	101 0100
1	1	101 0101
1	SDA	101 0110
1	SCL	101 0111
SDA	0	101 1000
SDA	1	101 1001
SDA	SDA	101 1010
SDA	SCL	101 1011
SCL	0	101 1100
SCL	1	101 1101
SCL	SDA	101 1110
SCL	SCL	101 1111

6.5.1.4 I²C Read and Write Operations

When writing to the device, the value for the address register is the first byte transferred after the target address byte with the R/$\overline{W}$ bit low. Every write operation to the device requires a value for the address register, as shown in Figure 6-14.

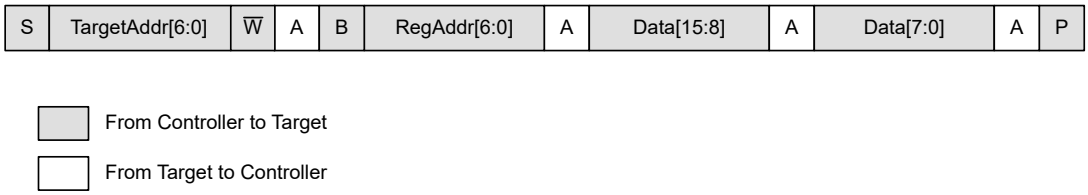


Figure 6-14. I²C Write Access Protocol

When reading from the device, the last value stored in the address register by a write operation is used to determine which register is read by a read operation. To change which register is read for a read operation, a new value must be written to the address register. This transaction is accomplished by issuing a target address byte with the R/$\overline{W}$ bit low, followed by the address register byte; no additional data are required. The controller can then generate a START condition and send the target address byte with the R/$\overline{W}$ bit high to initiate the read command.

If repeated reads from the same register are desired, there is no need to continually send the address register bytes because the device retains the address register value until the value is changed by the next write operation. The register bytes are big endian and left justified.

Terminate read operations by issuing a *not-acknowledge* command at the end of the last byte to be read. The controller must leave the SDA line high during the acknowledge time of the last byte that is read from the target, as shown in Figure 6-15.

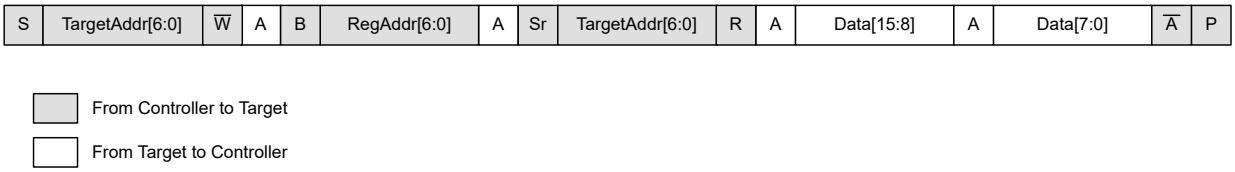


Figure 6-15. I²C Read Access Protocol

Block access functionality is provided to minimize the transfer overhead of large data sets. Block access enables multibyte transfers and is configured by setting the block access bit high. Until the transaction is terminated by the STOP condition, the device reads and writes the subsequent memory locations, as shown in Figure 6-16 and Figure 6-17. If the controller reaches address 0x7F in a page, the device continues reading and writing from this address until the transaction is terminated.

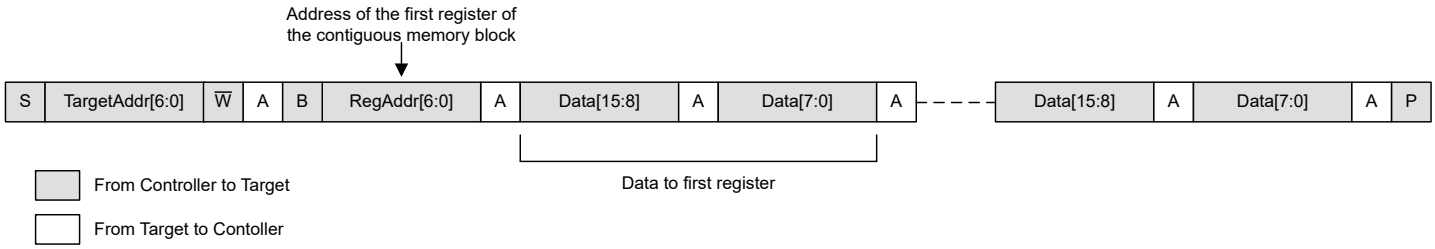


Figure 6-16. I²C Block Write Access

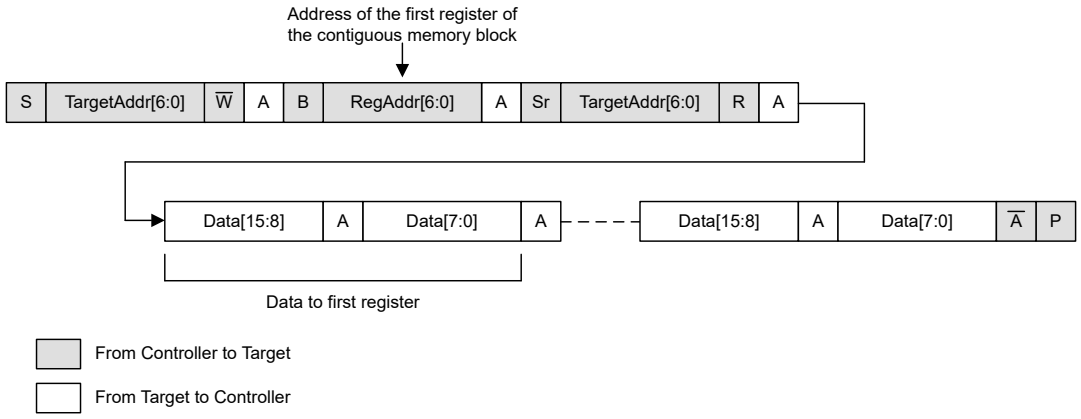


Figure 6-17. I²C Block Read Access

6.5.1.5 I²C Timeout Function

The device resets the serial interface if either SCL or SDA are held low for 25ms (typical) between a START and STOP condition. If the device is holding the bus low, the device releases the bus and waits for a START condition. After the bus is released, all previously received frames on the bus are discarded by the device, and any previous commands and acknowledgment requests are ignored. To avoid activating the timeout function, maintain a communication speed of at least 1kHz for the SCL operating frequency. Figure 6-18 shows the logic diagram for the timeout feature, while Figure 6-19 shows the timing diagram.

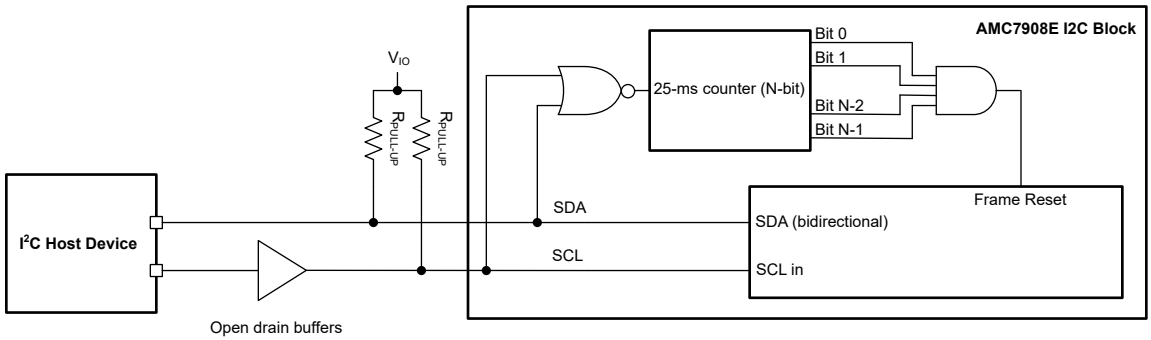


Figure 6-18. I2C Timeout (Logic Diagram)

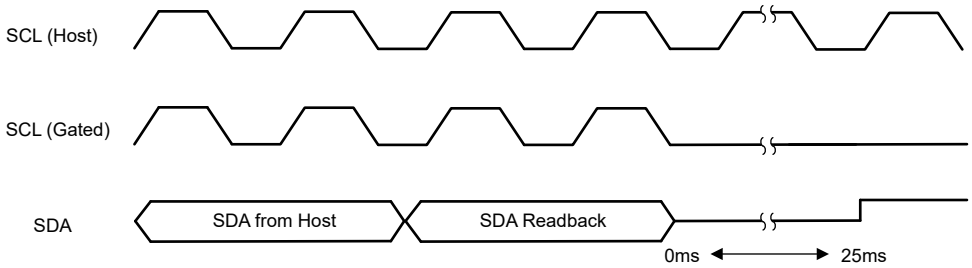


Figure 6-19. I2C Timeout (Timing Diagram)

6.5.1.6 I²C General-Call Reset

The device supports reset using the two-wire general call address 00h (0000 0000b). The device acknowledges the general-call address, and responds to the second byte. If the second byte is 06h (0000 0110b), the device executes a software reset. This software reset initiates a reset event. The device takes no action in response to other values in the second byte.

6.5.2 Serial Peripheral Interface (SPI)

In SPI mode, the device is controlled through a flexible four-wire serial interface that is compatible with SPI-type interfaces used on many microcontrollers and DSP controllers. The interface provides access to the device registers.

6.5.2.1 SPI Bus Overview

A serial interface access cycle is initiated by asserting the $\overline{CS}$ pin low. The serial clock SCLK can be a continuous or gated clock. SDI data are clocked on SCLK falling edges. A regular serial interface access cycle is 24 bits long, thus the $\overline{CS}$ pin must stay low for at least 24 SCLK falling edges. The access cycle ends when the $\overline{CS}$ pin is deasserted high. If the access cycle contains less than the minimum clock edges, the communication is ignored. If the access cycle contains more than the minimum clock edges, only the last 24 bits are used by the device. When $\overline{CS}$ is high, the SCLK and SDI signals are blocked and the SDO pin is in a Hi-Z state.

In a serial interface access cycle, the first byte input to SDI is the instruction cycle that identifies the request as a read or write command, and the 7-bit address to be accessed. The following bits in the cycle form the data cycle, as shown in Table 6-11.

Table 6-11. SPI Serial Interface Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Identifies the communication as a read or write command to the addressed register. RW = 0 sets a write operation. RW = 1 sets a read operation.
22:16	A[6:0]	Register address. Specifies the register to be accessed during the read or write operation.
15:0	DI[15:0]	Data cycle bits. If a write command, the data cycle bits are the values to be written to the register with address A[6:0]. If a read command, the data cycle bits are don't care values.

Read operations require that the SDO pin is first enabled by setting the SDO_EN bit. A read operation is initiated by issuing a read command access cycle. After the read command, a second access cycle must be issued to get the requested data, formatted as shown in Table 6-12. Data are clocked out on the SDO pin on SCLK rising or falling edges, according to the FSDO bit setting.

Table 6-12. SDO Output Access Cycle

BIT	FIELD	DESCRIPTION
23	RW	Echo RW bit from previous access cycle.
22:16	STATUS[6:0]	Lower seven bits of the General Status (GEN_STATUS) register.
15:0	DO[15:0]	Readback data requested on previous access cycle.

7 Register Maps

Table 7-1. Register Section/Block Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

7.1 Global Register Map

Table 7-2. Global Page: Global Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
00	NOP_RESET	R/W	0000	SW_RST/NOP [15:0]															
01	PAGE	R/W	0000	RESERVED											PAGE[4:0]				
03	GEN_STATUS	R	4000	RESERVED				GREF_ALR	GTHERM_ALR	GADC_ALR	GSENSE_ALR	$\overline{\text{ADC\_READY}}$	RESERVED	GVCCVSS_ALR	RESERVED	GALARMIN_ALR	PAON_STS	GTMP_ALR	GALR
04	ALARM_STATUS_0	R	0000	RESERVED							TMP_ALR	RESERVED		ADC1_ALR	ADC0_ALR	RESERVED		SENSE1_ALR	SENSE0_ALR
05	ALARM_STATUS_1	R	0000	RESERVED		ALARMIN_ALR	REF_ALR	THERMERR_ALR	RESERVED					VSSB_ALR	VSSA_ALR	RESERVED		VCCB_ALR	VCCA_ALR
06	PWR_STATUS_0	R	0001	VCCB_STS	VSSB_HIGHRANGE_STS	VSSB_MIDRANGE_STS	VSSB_LOWRANGE_STS	VCCA_STS	VSSA_HIGHRANGE_STS	VSSA_MIDRANGE_STS	VSSA_LOWRANGE_STS	RESERVED							VDDL_STS
07	PWR_STATUS_1	R	0000	DRVEN_DACB3_STS	DRVEN_DACB2_STS	DRVEN_DACB1_STS	DRVEN_DACB0_STS	DRVEN_DACA3_STS	DRVEN_DACA2_STS	DRVEN_DACA1_STS	DRVEN_DACA0_STS	PDACB3_STS	PDACB2_STS	PDACB1_STS	PDACB0_STS	PDACA3_STS	PDACA2_STS	PDACA1_STS	PDACA0_STS
08	PWR_EN	R/W	0200	RESERVED							PAON	PDACB3	PDACB2	PDACB1	PDACB0	PDACA3	PDACA2	PDACA1	PDACA0
10	TRIGGER	W	0000	RESERVED													ALARM_LATCH_CLR	DAC_TRIG	ADC_TRIG
11	GPIO_DATA	R/W	0001	RESERVED															GPIO
12	DRVEN_SW_EN	R/W	00FF	RESERVED								DRVEN_SW_EN_DACB3	DRVEN_SW_EN_DACB2	DRVEN_SW_EN_DACB1	DRVEN_SW_EN_DACB0	DRVEN_SW_EN_DACA3	DRVEN_SW_EN_DACA2	DRVEN_SW_EN_DACA1	DRVEN_SW_EN_DACA0
13	DRVEN	R/W	0000	RESERVED								DRVEN_DACB3	DRVEN_DACB2	DRVEN_DACB1	DRVEN_DACB0	DRVEN_DACA3	DRVEN_DACA2	DRVEN_DACA1	DRVEN_DACA0
14	DAC_BCAST	W	0000	RESERVED			DAC[12:0]												
17	GLOBAL_CFG	R/W	0000	RESERVED														ADC_BYP_EN	ALARM_BYP_EN
18	ADC_SENSE_0	R	0000	ADC[15:0]															
19	ADC_SENSE_1	R	0000	ADC[15:0]															
1A	ADC_ADC_0	R	0000	ADC[15:0]															
1B	ADC_ADC_1	R	0000	ADC[15:0]															
1C	ADC_TMP	R	0000	ADC[15:0]															

7.1.1 Global Registers: Global Page

7.1.1.1 NOP_RESET Register (address = 00h) [reset = 0000h]

Figure 7-1. NOP_RESET Register

15	14	13	12	11	10	9	8
SW_RST[15:8]/NOP							
R/W-0h							
7	6	5	4	3	2	1	0
SW_RST[7:0]/NOP							
R/W-0h							

Table 7-3. NOP_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
0	SW_RST/NOP	R/W	0h	No operation (NOP), unless the data matches a specified value below 0x00AD : Software Reset. Executes a full power-on-reset. Resets the device and all registers to the default power-on-reset state. Auto clears with execution

7.1.1.2 PAGE Register (address = 01h) [reset = 0000h]

Figure 7-2. PAGE Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED			PAGE[4:0]				
R-0h			R/W-0h				

Table 7-4. PAGE Register Field Descriptions

Bit	Field	Type	Reset	Description
4-0	PAGE	R/W	0h	Sets the page value. See the page map for more details. Registers on the Global page are accessible from any page, regardless of the page setting. 0x00: General Configuration Register Page 0x01: ADC Configuration Register Page 0x02: ADC CCS Configuration Register Page 0x03: DAC Configuration Register Page 0x04: DAC Buffer Register Page 0x06: DAC Active Register Page

7.1.1.3 GEN_STATUS Register (address = 03h) [reset = 4000h]

Figure 7-3. GEN_STATUS Register

15	14	13	12	11	10	9	8
RESERVED				GREF_ALR	GTHERM_ALR	GADC_ALR	GSENSE_ALR
R-4h				R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
$\overline{\text{ADC\_READY}}$	RESERVED	GVCCVSS_ALR	RESERVED	GALARMIN_ALR	PAON_STS	GTMP_ALR	GALR
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-5. GEN_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
11	GREF_ALR	R	0h	Global reference status bit. This bit is the OR function of all REF alarm status bits. 0 = No alarm condition 1 = Alarm condition present.
10	GTHERM_ALR	R	0h	Global thermal error status bit. This bit is the OR function of all thermal alarm status bits. 0 = No alarm condition 1 = Alarm condition present.
9	GADC_ALR	R	0h	Global ADC status bit for all ADC inputs. This bit is the OR function of all ADC alarm status bits. 0 = No alarm condition 1 = Alarm condition present.
8	GSENSE_ALR	R	0h	Global sense voltage status bit for all SENSE voltage input pins. This bit is the OR function of all SENSE alarm status bits. 0 = No alarm condition 1 = Alarm condition present.
7	$\overline{\text{ADC\_READY}}$	R	0h	ADC ready indicator (active low). 0 = ADC is ready for trigger to start. 1 = ADC is not ready.
5	GVCCVSS_ALR	R	0h	Global VCC or VSS status bit. This bit is the OR function of all VCC and VSS alarm status bits. 0 = No alarm condition 1 = Alarm condition present.
3	GALARMIN_ALR	R	0h	Global ALARMIN status bit. 0 = No alarm condition 1 = Alarm condition present.
2	PAON_STS	R	0h	PAON status bit. Read to confirm whether PAON is active, or turned off. If any alarm event is configured to turn PAON off, this bit follows the latching behavior of the originating alarm (based on the ALARM_LATCH_DIS setting) 0 = PAON is inactive 1 = PAON is active
1	GTMP_ALR	R	0h	Global temperature sensor status bit. 0 = No alarm condition 1 = Alarm condition present.
0	GALR	R	0h	Global alarm bit. This bit represents the OR function of all individual alarm statuses, and is set to 1 if any alarm condition is present.

7.1.1.4 ALARM_STATUS_0 Register (address = 04h) [reset = 0000h]

Figure 7-4. ALARM_STATUS_0 Register

15	14	13	12	11	10	9	8
RESERVED							TMP_ALR
R-0h							R-0h
7	6	5	4	3	2	1	0
RESERVED		ADC1_ALR	ADC0_ALR	RESERVED		SENSE1_ALR	SENSE_ALR
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 7-6. ALARM_STATUS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
8	TMP_ALR	R	0h	Out-of-range alarm status for temperature sensor, defined by the corresponding threshold registers. 0 = Temperature is in the specified range 1 = Temperature is out-of-range
5	ADC1_ALR	R	0h	Out-of-range alarm status for ADC1, defined by the corresponding threshold registers. 0 = ADC1 channel is in the specified range 1 = ADC1 channel is out-of-range
4	ADC0_ALR	R	0h	Out-of-range alarm status for ADC0, defined by the corresponding threshold registers. 0 = ADC0 channel is in the specified range 1 = ADC0 channel is out-of-range
1	SENSE1_ALR	R	0h	Out-of-range alarm status for SENSE1, defined by the corresponding threshold registers. 0 = SENSE1 channel is in the specified range 1 = SENSE1 channel is out-of-range
0	SENSE0_ALR	R	0h	Out-of-range alarm status for SENSE0, defined by the corresponding threshold registers. 0 = SENSE0 channel is in the specified range 1 = SENSE0 channel is out-of-range

7.1.1.5 ALARM_STATUS_1 Register (address = 05h) [reset = 0000h]

Figure 7-5. ALARM_STATUS_1 Register

15	14	13	12	11	10	9	8
RESERVED		ALARMIN_ALR	REF_ALR	THERMERR_ALR	RESERVED		
R-0h		R-0h	R-0h	R-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		VSSB_ALR	VSSA_ALR	RESERVED		VCCB_ALR	VCCA_ALR
R-0h		R-0h	R-0h	R-0h		R-0h	R-0h

Table 7-7. ALARM_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
13	ALARMIN_ALR	R	0h	$\overline{\text{ALARMIN}}$ alarm status. 0 = $\overline{\text{ALARMIN}}$ has not triggered. 1 = $\overline{\text{ALARMIN}}$ has triggered.
12	REF_ALR	R	0h	Reference alarm status. 0 = Internal reference voltage is valid 1 = Internal reference voltage is less than minimum reference threshold voltage.
11	THERMERR_ALR	R	0h	Thermal error alarm status. 0 = Die temperature is less than 150°C (typical) 1 = Operating temperature greater than or equal to 150°C
5	VSSB_ALR	R	0h	VSSB alarm status. 0 = VSSB is greater than the minimum VSS threshold voltage 1 = VSSB is less than the minimum VSS threshold voltage
4	VSSA_ALR	R	0h	VSSA alarm status. 0 = VSSA is less than the minimum VSS threshold voltage 1 = VSSA is greater than the minimum VSS threshold voltage
1	VCCB_ALR	R	0h	VCCB alarm status. 0 = VCCB is greater than the minimum VCC threshold voltage 1 = VCCB is less than the minimum VCC threshold voltage
0	VCCA_ALR	R	0h	VCCA alarm status. 0 = VCCA is greater than the minimum VCC threshold voltage 1 = VCCA is less than the minimum VCC threshold voltage

7.1.1.6 PWR_STATUS_0 Register (address = 06h) [reset = 0001h]

Figure 7-6. PWR_STATUS_0 Register

15	14	13	12	11	10	9	8
VCCB_STS	VSSB_ HIGHRANGE_ STS	VSSB_ MIDRANGE_ STS	VSSB_ LOWRANGE_ STS	VCCA_STS	VSSA_ HIGHRANGE_ STS	VSSA_ MIDRANGE_ STS	VSSA_ LOWRANGE_ STS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
RESERVED							VDDL_STS
R-0h							R-1h

Table 7-8. PWR_STATUS_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	VCCB_STS	R	0h	Supply detection result for VCCB. 0 = VCCB is less than the minimum VCC threshold voltage 1 = VCCB has exceeded the minimum VCC threshold voltage
14	VSSB_HIGHRANGE_STS	R	0h	Supply detection result for VSSB. 0 = VSSB is between 0V and the high range VSS threshold voltage. 1 = VSSB has exceeded (is more negative than) the high range VSS threshold voltage
13	VSSB_MIDRANGE_STS	R	0h	Supply detection result for VSSB. 0 = VSSB is between 0V and the mid range VSS threshold voltage. 1 = VSSB has exceeded (is more negative than) the mid range VSS threshold voltage
12	VSSB_LOWRANGE_STS	R	0h	Supply detection result for VSSB. 0 = VSSB is between 0V and the low range VSS threshold voltage. 1 = VSSB has exceeded (is more negative than) the low range VSS threshold voltage
11	VCCA_STS	R	0h	Supply detection result for VCCA. 0 = VCCA is less than the minimum VCC threshold voltage 1 = VCCA has exceeded the minimum VCC threshold voltage.
10	VSSA_HIGHRANGE_STS	R	0h	Supply detection result for VSSA. 0 = VSSA is between 0V and the high range VSS threshold voltage. 1 = VSSA has exceeded (is more negative than) the high range VSS threshold voltage
9	VSSA_MIDRANGE_STS	R	0h	Supply detection result for VSSA. 0 = VSSA is between 0V and the mid range VSS threshold voltage. 1 = VSSA has exceeded (is more negative than) the mid range VSS threshold voltage
8	VSSA_LOWRANGE_STS	R	0h	Supply detection result for VSSA. 0 = VSSA is between 0V and the low range VSS threshold voltage. 1 = VSSA has exceeded (is more negative than) the low range VSS threshold voltage
0	VDDL_STS	R	1h	Supply detection result for VDDL. 0 = VDDL is less than the minimum threshold voltage. 1 = VDDL has exceeded the minimum threshold voltage.

7.1.1.7 PWR_STATUS_1 Register (address = 07h) [reset = 0000h]

Figure 7-7. PWR_STATUS_1 Register

15	14	13	12	11	10	9	8
DRVEN_DACB3_STS	DRVEN_DACB2_STS	DRVEN_DACB1_STS	DRVEN_DACB0_STS	DRVEN_DACA3_STS	DRVEN_DACA2_STS	DRVEN_DACA1_STS	DRVEN_DACA0_STS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h
7	6	5	4	3	2	1	0
PDACB3_STS	PDACB2_STS	PDACB1_STS	PDACB0_STS	PDACA3_STS	PDACA2_STS	PDACA1_STS	PDACA0_STS
R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h	R-0h

Table 7-9. PWR_STATUS_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	DRVEN_DACB3_STS	R	0h	DACB3 drive enable status. 0: DRVEN = 0 (DACB3 disabled, outputs forced to VSS). 1: DRVEN = 1.
14	DRVEN_DACB2_STS	R	0h	DACB2 drive enable status. 0: DRVEN = 0 (DACB2 disabled, outputs forced to VSS). 1: DRVEN = 1.
13	DRVEN_DACB1_STS	R	0h	DACB1 drive enable status. 0: DRVEN = 0 (DACB1 disabled, outputs forced to VSS). 1: DRVEN = 1.
12	DRVEN_DACB0_STS	R	0h	DACB0 drive enable status. 0: DRVEN = 0 (DACB0 disabled, outputs forced to VSS). 1: DRVEN = 1.
11	DRVEN_DACA3_STS	R	0h	DACA3 drive enable status. 0: DRVEN = 0 (DACA3 disabled, outputs forced to VSS). 1: DRVEN = 1.
10	DRVEN_DACA2_STS	R	0h	DACA2 drive enable status. 0: DRVEN = 0 (DACA2 disabled, outputs forced to VSS). 1: DRVEN = 1.
9	DRVEN_DACA1_STS	R	0h	DACA1 drive enable status. 0: DRVEN = 0 (DACA1 disabled, outputs forced to VSS). 1: DRVEN = 1.
8	DRVEN_DACA0_STS	R	0h	DACA0 drive enable status. 0: DRVEN = 0 (DACA0 disabled, outputs forced to VSS). 1: DRVEN = 1.
7	PDACB3_STS	R	0h	DACB3 power status. 0: DACB3 disabled in low-power mode. 1: DACB3 is on.
6	PDACB2_STS	R	0h	DACB2 power status. 0: DACB2 disabled in low-power mode. 1: DACB2 is on.
5	PDACB1_STS	R	0h	DACB1 power status. 0: DACB1 disabled in low-power mode. 1: DACB1 is on.
4	PDACB0_STS	R	0h	DACB0 power status. 0: DACB0 disabled in low-power mode. 1: DACB0 is on.
3	PDACA3_STS	R	0h	DACA3 power status. 0: DACA3 disabled in low-power mode. 1: DACA3 is on.
2	PDACA2_STS	R	0h	DACA2 power status. 0: DACA2 disabled in low-power mode. 1: DACA2 is on.
1	PDACA1_STS	R	0h	DACA1 power status. 0: DACA1 disabled in low-power mode. 1: DACA1 is on.
0	PDACA0_STS	R	0h	DACA0 power status. 0: DACA0 disabled in low-power mode. 1: DACA0 is on.

7.1.1.8 PWR_EN Register (address = 08h) [reset = 0200h]

Figure 7-8. PWR_EN Register

15	14	13	12	11	10	9	8
RESERVED							PAON
R-1h							R/W-0h
7	6	5	4	3	2	1	0
PDACB3	PDACB2	PDACB1	PDACB0	PDACA3	PDACA2	PDACA1	PDACA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-10. PWR_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
8	PAON	R/W	0h	PAON power enable bit. 0 : PAON is not enabled 1 : PAON is enabled from power setting (note that this bit remains at 1 if an alarm event turns PAON off; read PAON_STS in the GEN_STATUS register to confirm if PAON is active or not).
7	PDACB3	R/W	0h	DACB3 enabled status. 0: DACB3 disabled. 1: DACB3 is enabled.
6	PDACB2	R/W	0h	DACB2 enabled status. 0: DACB2 disabled. 1: DACB2 is enabled.
5	PDACB1	R/W	0h	DACB1 enabled status. 0: DACB1 disabled. 1: DACB1 is enabled.
4	PDACB0	R/W	0h	DACB0 enabled status. 0: DACB0 disabled. 1: DACB0 is enabled.
3	PDACA3	R/W	0h	DACA3 enabled status. 0: DACA3 disabled. 1: DACA3 is enabled.
2	PDACA2	R/W	0h	DACA2 enabled status. 0: DACA2 disabled. 1: DACA2 is enabled.
1	PDACA1	R/W	0h	DACA1 enabled status. 0: DACA1 disabled. 1: DACA1 is enabled.
0	PDACA0	R/W	0h	DACA0 enabled status. 0: DACA0 disabled. 1: DACA0 is enabled.

7.1.1.9 TRIGGER Register (address = 10h) [reset = 0000h]

Figure 7-9. TRIGGER Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED					ALARM_LATCH_CLR	DAC_TRIG	ADC_TRIG
R-0h					W-0h	W-0h	W-0h

Table 7-11. TRIGGER Register Field Descriptions

Bit	Field	Type	Reset	Description
2	ALARM_LATCH_CLR	W	0h	Manually clear registers which are latching the alarm condition. If an alarm condition is still present, the corresponding alarm latches and alarm state are set again. This bit self-clears 0 = No action. 1 = Clear alarm bits.
1	DAC_TRIG	W	0h	Software LDAC trigger. This bit self-clears. 0 = No action. 1 = Initiate data transfer from DAC buffer registers to active registers.
0	ADC_TRIG	W	0h	ADC conversion trigger. Set this bit to 1 to start the ADC conversions. In direct-mode, this bit self-clears back to 0 after all conversions are completed. In auto-mode, this bit remains set and the ADC continuously converts until the user manually clears the bit back to 0, stopping auto-mode. Before setting ADC_TRIG to 1, confirm the ADC is ready by reading the ADC_READY status bit as 0 twice in succession. 0 = Stop ADC conversions. 1 = Start ADC conversions

7.1.1.10 GPIO_DATA Register (address = 11h) [reset = 0001h]

Figure 7-10. GPIO_DATA Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED							GPIO
R-0h							R/W-1h

Table 7-12. GPIO_DATA Register Field Descriptions

Bit	Field	Type	Reset	Description
0	GPIO	R/W	1h	For read operations the GPIO pin operates as an input. Read to receive the status of the corresponding GPIO pin. For write operations, the GPIO pin operates as an output based on the value written to this register, as follows 0: Set GPIO to logic low. 1: Set GPIO to logic high (when FLEXIO_OUT_ODE = 0) or a high impedance state (when FLEXIO_OUT_ODE = 1)

7.1.1.11 DRVEN_SW_EN Register (address = 12h) [reset = 00FFh]

Figure 7-11. DRVEN_SW_EN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DRVEN_SW_EN_DACB3	DRVEN_SW_EN_DACB2	DRVEN_SW_EN_DACB1	DRVEN_SW_EN_DACB0	DRVEN_SW_EN_DACA3	DRVEN_SW_EN_DACA2	DRVEN_SW_EN_DACA1	DRVEN_SW_EN_DACA0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 7-13. DRVEN_SW_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DRVEN_SW_EN_DACB3	R/W	1h	Enables software operation of DACB3 channel switch (DRVEN). 0: Software control disabled. 1: Software control enabled.
6	DRVEN_SW_EN_DACB2	R/W	1h	Enables software operation of DACB2 channel switch (DRVEN). 0: Software control disabled. 1: Software control enabled.
5	DRVEN_SW_EN_DACB1	R/W	1h	Enables software operation of DACB1 channel switch (DRVEN). 0: Software control disabled. 1: Software control enabled.
4	DRVEN_SW_EN_DACB0	R/W	1h	Enables software operation of DACB0 channel switch (DRVEN). 0: Software control disabled. 1: Software control enabled.
3	DRVEN_SW_EN_DACA3	R/W	1h	Enables software operation of DACA3 channel switch (DRVEN). 0: Software control disabled. 1: Software control enabled.
2	DRVEN_SW_EN_DACA2	R/W	1h	Enables software operation of DACA2 channel switch (DRVEN). 0: Software control disabled. 1: Software control enabled.
1	DRVEN_SW_EN_DACA1	R/W	1h	Enables software operation of DACA1 channel switch (DRVEN). 0: Software control disabled. 1: Software control enabled.
0	DRVEN_SW_EN_DACA0	R/W	1h	Enables software operation of DACA0 channel switch (DRVEN). 0: Software control disabled. 1: Software control enabled.

7.1.1.12 DRVEN Register (address = 13h) [reset = 0000h]

Figure 7-12. DRVEN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DRVEN_DACB3	DRVEN_DACB2	DRVEN_DACB1	DRVEN_DACB0	DRVEN_DACA3	DRVEN_DACA2	DRVEN_DACA1	DRVEN_DACA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-14. DRVEN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DRVEN_DACB3	R/W	0h	Software drive enable value, when software control is enabled on DRVEN_SW_EN_DACB3. 0: DACB3 drive disabled, internally connected to VSSB. 1: DACB3 drive enabled.
6	DRVEN_DACB2	R/W	0h	Software drive enable value, when software control is enabled on DRVEN_SW_EN_DACB2. 0: OUTB2 drive disabled, internally connected to VSSB or DACB3, depending on CLAMP_SEL_OUTB2. 1: OUTB2 drive enabled, connected to DACB2.
5	DRVEN_DACB1	R/W	0h	Software drive enable value, when software control is enabled on DRVEN_SW_EN_DACB1. 0: DACB1 drive disabled, internally connected to VSSB. 1: DACB1 drive enabled.
4	DRVEN_DACB0	R/W	0h	Software drive enable value, when software control is enabled on DRVEN_SW_EN_DACB0. 0: OUTB0 drive disabled, internally connected to VSSB or DACB1, depending on CLAMP_SEL_OUTB0. 1: OUTB0 drive enabled, connected to DACB0.
3	DRVEN_DACA3	R/W	0h	Software drive enable value, when software control is enabled on DRVEN_SW_EN_DACA3. 0: DACA3 drive disabled, internally connected to VSSA. 1: DACA3 drive enabled.
2	DRVEN_DACA2	R/W	0h	Software drive enable value, when software control is enabled on DRVEN_SW_EN_DACA2. 0: OUTA2 drive disabled, internally connected to VSSA or DACA3, depending on CLAMP_SEL_OUTA2. 1: OUTA2 drive enabled, connected to DACA2.
1	DRVEN_DACA1	R/W	0h	Software drive enable value, when software control is enabled on DRVEN_SW_EN_DACA1. 0: DACA1 drive disabled, internally connected to VSSA. 1: DACA1 drive enabled.
0	DRVEN_DACA0	R/W	0h	Software drive enable value, when software control is enabled on DRVEN_SW_EN_DACA0. 0: OUTA0 drive disabled, internally connected to VSSA or DACA1, depending on CLAMP_SEL_OUTA0. 1: OUTA0 drive enabled, connected to DACA0.

7.1.1.13 DAC_BCAST Register (address = 14h) [reset = 0000h]

Figure 7-13. DAC_BCAST Register

15	14	13	12	11	10	9	8
RESERVED			DAC[12:8]				
R-0h			W-0h				
7	6	5	4	3	2	1	0
DAC[7:0]							
W-0h							

Table 7-15. DAC_BCAST Register Field Descriptions

Bit	Field	Type	Reset	Description
12-0	DAC	W	0h	Write to this register sets all DAC buffer and active data register values to the specified code, on channels for which the respective Broadcast Enable (BCEN) bit is set (see Section 7.5.1.2). Otherwise that channel buffer and active registers are unchanged.

7.1.1.14 GLOBAL_CFG Register (address = 17h) [reset = 0000h]

Figure 7-14. GLOBAL_CFG Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						ADC_BYP_EN	ALARM_BYP_EN
R-0h						R/W-0h	R/W-0h

Table 7-16. GLOBAL_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
1	ADC_BYP_EN	R/W	0h	ADC data bypass enable. Bypasses all ADC conversion results. 0: Bypass disabled. 1: All ADC conversion data are bypassed, with data registers forced to the value stored in ADC_BYP (see Section 7.3.1.4).
0	ALARM_BYP_EN	R/W	0h	Internal alarm bypass. 0: Bypass disabled. 1: All alarm condition states and alarm status bits are bypassed.

7.1.1.15 ADC_SENSE0 Register (address = 18h) [reset = 0000h]

Figure 7-15. ADC_SENSE0 Register

15	14	13	12	11	10	9	8
ADC[15:8]							
R-0h							
7	6	5	4	3	2	1	0
ADC[7:0]							
R-0h							

Table 7-17. ADC_SENSE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC	R	0h	Differential voltage measured across the shunt output. 2's complement value. When SHUNT_RANGE = 0, the conversion factor is 5µV/LSB, and when SHUNT_RANGE = 1, the conversion factor is 1.25µV/LSB.

7.1.1.16 ADC_SENSE1 Register (address = 19h) [reset = 0000h]

Figure 7-16. ADC_SENSE1 Register

15	14	13	12	11	10	9	8
ADC[15:8]							
R-0h							
7	6	5	4	3	2	1	0
ADC[7:0]							
R-0h							

Table 7-18. ADC_SENSE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC	R	0h	Differential voltage measured across the shunt output. 2's complement value. When SHUNT_RANGE = 0, the conversion factor is 5µV/LSB, and when SHUNT_RANGE = 1, the conversion factor is 1.25µV/LSB.

7.1.1.17 ADC_ADC0 Register (address = 1Ah) [reset = 0000h]

Figure 7-17. ADC_ADC0 Register

15	14	13	12	11	10	9	8
ADC[15:8]							
R-0h							
7	6	5	4	3	2	1	0
ADC[7:0]							
R-0h							

Table 7-19. ADC_ADC0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC	R	0h	ADCHV voltage output, 2's complement value (always positive). Conversion factor: 3.125mV/LSB.

7.1.1.18 ADC_ADC1 Register (address = 1Bh) [reset = 0000h]

Figure 7-18. ADC_ADC1 Register

15	14	13	12	11	10	9	8
ADC[15:8]							
R-0h							
7	6	5	4	3	2	1	0
ADC[7:0]							
R-0h							

Table 7-20. ADC_ADC1 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC	R	0h	ADCHV voltage output, 2's complement value (always positive). Conversion factor: 3.125mV/LSB.

7.1.1.19 ADC_TMP Register (address = 1Ch) [reset = 0000h]

Figure 7-19. ADC_TMP Register

15	14	13	12	11	10	9	8
ADC[15:8]							
R-0h							
7	6	5	4	3	2	1	0
ADC[7:0]							
R-0h							

Table 7-21. ADC_TMP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC	R	0h	Internal die temperature measurement. 2's complement value. Conversion factor: 7.8125 m°C/LSB.

7.2 General Configuration Register Map

Table 7-22. Page 0: General Configuration Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40	CHIP_ID	R	2480	CHIP_ID[15:0]															
41	CHIP_VER	R	0000	RESERVED												VERSION_ID[3:0]			
42	SDO_EN	R/W	0000	RESERVED														FSDO	SDO_EN
44	GEN_CFG_0	R/W	0010	PAON_POL	PAON_ODE	RESERVED								FLEXIO_OUT_POL	FLEXIO_OUT_ODE	ALARM_LATCH_DIS	RESERVED		
45	GEN_CFG_1	R/W	1101	RESERVED	VSSB_RANGE[2:0]			RESERVED	VSSA_RANGE[2:0]			RESERVED		FLEXIO_FUNC[5:0]					
48	ALARMOUT_SRC_0	R/W	0000	RESERVED							TMP_ALR_OUT	RESERVED		ADC1_ALR_OUT	ADC0_ALR_OUT	RESERVED		SENSE1_ALR_OUT	SENSE0_ALR_OUT
49	ALARMOUT_SRC_1	R/W	1833	RESERVED			REF_ALR_OUT	THERM ERR_ALR_OUT	RESERVED					VSSB_ALR_OUT	VSSA_ALR_OUT	RESERVED		VCCB_ALR_OUT	VCCA_ALR_OUT
4C	ALARM_STATUS_0_BYP	R/W	0000	RESERVED							TMP_ALR_BYP	RESERVED		ADC1_ALR_BYP	ADC0_ALR_BYP	RESERVED		SENSE1_ALR_BYP	SENSE0_ALR_BYP
4D	ALARM_STATUS_1_BYP	R/W	0000	RESERVED			REF_ALR_BYP	THERM ERR_ALR_BYP	RESERVED					VSSB_ALR_BYP	VSSA_ALR_BYP	RESERVED		VCCB_ALR_BYP	VCCA_ALR_BYP
50	PAON_SRC_0	R/W	0000	RESERVED							TMP_PAON_OUT	RESERVED		ADC1_PAON_OUT	ADC0_PAON_OUT	RESERVED		SENSE1_PAON_OUT	SENSE0_PAON_OUT
51	PAON_SRC_1	R/W	1833	RESERVED			REF_PAON_OUT	THERM ERR_PAON_OUT	RESERVED[4:0]					VSSB_PAON_OUT	VSSA_PAON_OUT	RESERVED		VCCB_PAON_OUT	VCCA_PAON_OUT
70	RESET_FLAGS	W	000F	RESERVED												VDD_COLLAPSE_FLAG	RSTPIN_FLAG	VIO_FLAG	PORBASE_FLAG

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7.2.1.1 CHIP_ID Register (address = 40h) [reset = 2480h]

Figure 7-20. CHIP_ID Register

15	14	13	12	11	10	9	8
CHIP_ID[15:8]							
R-24h							
7	6	5	4	3	2	1	0
CHIP_ID[7:0]							
R-80h							

Table 7-23. CHIP_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	CHIP_ID	R	2480h	Chip identification code

7.2.1.2 CHIP_VER Register (address = 41h) [reset = 0000h]

Figure 7-21. CHIP_VER Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				VERSION[3:0]			
R-0h				R-0h			

Table 7-24. CHIP_VER Register Field Descriptions

Bit	Field	Type	Reset	Description
3-0	VERSION[3:0]	R	0h	Chip version ID. 0x0: Rev A. 0x1: Rev B. 0x2: Rev C. 0x3: Rev D.

7.2.1.3 SDO_EN Register (address = 42h) [reset = 0000h]

Figure 7-22. SDO_EN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED						FSDO	SDO_EN
R-0h						R/W-0h	R/W-0h

Table 7-25. SDO_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
1	FSDO	R/W	0h	Enables faster SPI bus speeds by sending the SDO data out one SCLK half-cycle earlier (FSDO mode). Ignored when SDO_EN = 0 0 = FSDO disabled, SDO drives MSB when chip select goes low and then updates on each SCLK rising edge (opposite edge of SDI latching edge) 1 = FSDO enabled, SDO drives MSB when chip select goes low and then updates on each SCLK falling edge (same edge as SDI latching edge)
0	SDO_EN	R/W	0h	SDO Enable. SDO is enabled for read and write operations whenever the SPI $\overline{CS}$ pin is low. SDO is always disabled in I^2C mode regardless of this bit setting. 0 = SDO disabled 1 = SDO enabled during read/write operations

7.2.1.4 GEN_CFG_0 Register (address = 44h) [reset = 0010h]

Table 7-26. GEN_CFG_0 Register

15	14	13	12	11	10	9	8
PAON_POL	PAON_ODE	RESERVED					
R/W-0h	R/W-0h	R-0h					
7	6	5	4	3	2	1	0
RESERVED		FLEXIO_OUT_POL	FLEXIO_OUT_ODE	ALARM_LATCH_DIS	RESERVED		
R-0h		R/W-0h	R/W-1h	R/W-0h	R-0h		

Table 7-27. GEN_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15	PAON_POL	R/W	0h	PAON polarity 0: PAON pin follows PWR_EN PAON bit setting, with high voltage being on and low voltage being off 1: PAON pin is inverted from PWR_EN PAON bit setting, with high voltage being off and low voltage being on.
14	PAON_ODE	R/W	0h	PAON open-drain enable 0: PAON pin is a push-pull output (default) 1: PAON pin is an open-drain output
5	FLEXIO_OUT_POL	R/W	0h	FLEXIO pin polarity, when configured as digital output 0 = FLEXIO is active low 1 = FLEXIO is active high
4	FLEXIO_OUT_ODE	R/W	1h	FLEXIO pin drive mode, when configured as digital output 0 = FLEXIO pin is a push-pull output 1 = FLEXIO pin is an open-drain output
3	ALARM_LATCH_DIS	R/W	0h	Alarm latch status 0 = Alarm state is latched. Global alarm bit GALR and FLEXIO pin (if configured as $\overline{\text{ALARMOUT}}$) only return to default state if the GALR bit is read 0 after corresponding alarm condition subsides 1 = Alarm state is not latched. Global alarm bit and FLEXIO pin (if configured as $\overline{\text{ALARMOUT}}$) return to default state as soon as alarm condition subsides.

7.2.1.5 GEN_CFG_1 Register (address = 45h) [reset = 1101h]

Figure 7-23. GEN_CFG_1 Register

15	14	13	12	11	10	9	8
RESERVED	VSSB_RANGE[2:0]			RESERVED	VSSA_RANGE[2:0]		
R-0h	R/W-1h			R-0h	R/W-1h		
7	6	5	4	3	2	1	0
RESERVED		FLEXIO_FUNC[5:0]					
R-0h		R/W-1h					

Table 7-28. GEN_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
14-12	VSSB_RANGE	R/W	1h	Configure VSS range for DAC group B; at any voltage outside this range, VSSB_ALR is set 001: Low-range VSS (–11V to –3V) 010: Mid-range VSS (–11V to –4.5V) 100: High-range VSS (–11V to –7.5V)
10-8	VSSA_RANGE	R/W	1h	Configure VSS range for DAC group A; at any voltage outside this range, VSSA_ALR is set 001: Low-range VSS (–11V to –3V) 010: Mid-range VSS (–11V to –4.5V) 100: High-range VSS (–11V to –7.5V)
5-0	FLEXIO_FUNC	R/W	1h	Sets function for FLEXIO pin 0x01: $\overline{\text{RESET}}$ 0x02: $\overline{\text{ALARMOUT}}$ 0x04: GPIO pin 0x08: $\overline{\text{LDAC}}$ 0x10: $\overline{\text{ALARMIN}}$ 0x20: DRVEN2

7.2.1.6 ALARMOUT_SRC_0 Register (address = 48h) [reset = 0000h]

Figure 7-24. ALARMOUT_SRC_0 Register

15	14	13	12	11	10	9	8
RESERVED							TMP_ ALR_OUT
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		ADC1_ ALR_OUT	ADC0_ ALR_OUT	RESERVED		SENSE1_ ALR_OUT	SENSE0_ ALR_OUT
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 7-29. ALARMOUT_SRC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
8	TMP_ALR_OUT	R/W	0h	0: Temperature alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: Temperature alarm is a source for $\overline{\text{ALARMOUT}}$ pin assertion.
5	ADC1_ALR_OUT	R/W	0h	0: ADC1 alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: ADC1 alarm is a source for $\overline{\text{ALARMOUT}}$ pin assertion.
4	ADC0_ALR_OUT	R/W	0h	0: ADC0 alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: ADC0 alarm is a source for $\overline{\text{ALARMOUT}}$ pin assertion.
1	SENSE1_ALR_OUT	R/W	0h	0: SENSE1 channel alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: SENSE1 channel is a source for $\overline{\text{ALARMOUT}}$ pin assertion.
0	SENSE0_ALR_OUT	R/W	0h	0: SENSE0 channel alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: SENSE0 channel is a source for $\overline{\text{ALARMOUT}}$ pin assertion.

7.2.1.7 ALARMOUT_SRC_1 Register (address = 49h) [reset = 1833h]

Figure 7-25. ALARMOUT_SRC_1 Register

15	14	13	12	11	10	9	8
RESERVED			REF_ ALR_OUT	THERMERR_ ALR_OUT	RESERVED		
R-0h			R/W-1h	R/W-1h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		VSSB_ ALR_OUT	VSSA_ ALR_OUT	RESERVED		VCCB_ ALR_OUT	VCCA_ ALR_OUT
R-0h		R/W-1h	R/W-1h	R-0h		R/W-1h	R/W-1h

Table 7-30. ALARMOUT_SRC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
12	REF_ALR_OUT	R/W	1h	0: Reference alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: Reference alarm is a source for $\overline{\text{ALARMOUT}}$ pin assertion.
11	THERMERR_ALR_OUT	R/W	1h	0: Thermal alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: Thermal alarm is a source for $\overline{\text{ALARMOUT}}$ pin assertion.
5	VSSB_ALR_OUT	R/W	1h	0: VSSB alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: VSSB alarm is a source for $\overline{\text{ALARMOUT}}$ pin assertion.
4	VSSA_ALR_OUT	R/W	1h	0: VSSA alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: VSSA alarm is a source for $\overline{\text{ALARMOUT}}$ pin assertion.
1	VCCB_ALR_OUT	R/W	1h	0: VCCB alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: VCCB alarm is a source for $\overline{\text{ALARMOUT}}$ pin assertion.
0	VCCA_ALR_OUT	R/W	1h	0: VCCA alarm is not a source for $\overline{\text{ALARMOUT}}$ pin assertion. 1: VCCA alarm is a source for $\overline{\text{ALARMOUT}}$ pin assertion.

7.2.1.8 ALARM_STATUS_0_BYP Register (address = 4Ch) [reset = 0000h]

Figure 7-26. ALARM_STATUS_0_BYP Register

15	14	13	12	11	10	9	8
RESERVED							TMP_ ALR_BYP
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		ADC1_ ALR_BYP	ADC0_ ALR_BYP	RESERVED		SENSE1_ ALR_BYP	SENSE0_ ALR_BYP
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 7-31. ALARM_STATUS_0_BYP Register Field Descriptions

Bit	Field	Type	Reset	Description
8	TMP_ALR_BYP	R/W	0h	Temperature alarm bypass command (when ALARM_BYP_EN = 1) 0: Temperature alarm status is forced to 0 1: Temperature alarm status is forced to 1
5	ADC1_ALR_BYP	R/W	0h	ADC1 alarm bypass command (when ALARM_BYP_EN = 1) 0: ADC1 alarm status is forced to 0 1: ADC1 alarm status is forced to 1
4	ADC0_ALR_BYP	R/W	0h	ADC0 alarm bypass command (when ALARM_BYP_EN = 1) 0: ADC0 alarm status is forced to 0 1: ADC0 alarm status is forced to 1
1	SENSE1_ALR_BYP	R/W	0h	SENSE1 alarm bypass command (when ALARM_BYP_EN = 1) 0: SENSE1 alarm status is forced to 0 1: SENSE1 alarm status is forced to 1
0	SENSE0_ALR_BYP	R/W	0h	SENSE0 alarm bypass command (when ALARM_BYP_EN = 1) 0: SENSE0 alarm status is forced to 0 1: SENSE0 alarm status is forced to 1

7.2.1.9 ALARM_STATUS_1_BYP Register (address = 4Dh) [reset = 0000h]

Figure 7-27. ALARM_STATUS_1_BYP Register

15	14	13	12	11	10	9	8
RESERVED		ALARMIN_ ALR_BYP	REF_ ALR_BYP	THERMERR_ ALR_BYP	RESERVED		
R-0h		R/W-0h	R/W-0h	R/W-0h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		VSSB_ ALR_BYP	VSSA_ ALR_BYP	RESERVED		VCCB_ ALR_BYP	VCCA_ ALR_BYP
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 7-32. ALARM_STATUS_1_BYP Register Field Descriptions

Bit	Field	Type	Reset	Description
13	ALARMIN_ALR_BYP	R/W	0h	ALARMIN bypass command (when ALARM_BYP_EN = 1) 0: ALARMIN alarm status is forced to 0 1: ALARMIN alarm status is forced to 1
12	REF_ALR_BYP	R/W	0h	Reference alarm bypass command (when ALARM_BYP_EN = 1) 0: Reference alarm status is forced to 0 1: Reference alarm status is forced to 1
11	THERMERR_ALR_BYP	R/W	0h	Thermal alarm bypass command (when ALARM_BYP_EN = 1) 0: Thermal alarm status is forced to 0 1: Thermal alarm status is forced to 1
5	VSSB_ALR_BYP	R/W	0h	VSSB alarm bypass command (when ALARM_BYP_EN = 1) 0: VSSB alarm status is forced to 0 1: VSSB alarm status is forced to 1
4	VSSA_ALR_BYP	R/W	0h	VSSA alarm bypass command (when ALARM_BYP_EN = 1) 0: VSSA alarm status is forced to 0 1: VSSA alarm status is forced to 1
1	VCCB_ALR_BYP	R/W	0h	VCCB alarm bypass command (when ALARM_BYP_EN = 1) 0: VCCB alarm status is forced to 0 1: VCCB alarm status is forced to 1
0	VCCA_ALR_BYP	R/W	0h	VCCA alarm bypass command (when ALARM_BYP_EN = 1) 0: VCCA alarm status is forced to 0 1: VCCA alarm status is forced to 1

7.2.1.10 PAON_SRC_0 Register (address = 50h) [reset = 0000h]

Figure 7-28. PAON_SRC_0 Register

15	14	13	12	11	10	9	8
RESERVED							TMP_PAON_OUT
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		ADC1_PAON_OUT	ADC0_PAON_OUT	RESERVED		SENSE1_PAON_OUT	SENSE0_PAON_OUT
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 7-33. PAON_SRC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
8	TMP_PAON_OUT	R/W	0h	0: Temperature alarm event does not affect PAON pin. 1: Temperature alarm event turns off PAON pin.
5	ADC1_PAON_OUT	R/W	0h	0: ADC1 alarm event does not affect PAON pin. 1: ADC1 alarm event turns off PAON pin.
4	ADC0_PAON_OUT	R/W	0h	0: ADC0 alarm event does not affect PAON pin. 1: ADC0 alarm event turns off PAON pin.
1	SENSE1_PAON_OUT	R/W	0h	0: SENSE1 alarm event does not affect PAON pin. 1: SENSE1 alarm event turns off PAON pin.
0	SENSE0_PAON_OUT	R/W	0h	0: SENSE0 alarm event does not affect PAON pin. 1: SENSE0 alarm event turns off PAON pin.

7.2.1.11 PAON_SRC_1 Register (address = 51h) [reset = 1833h]

Figure 7-29. PAON_SRC_1 Register

15	14	13	12	11	10	9	8
RESERVED			REF_PAON_OUT	THERMERR_PAON_OUT	RESERVED		
R-0h			R/W-1h	R/W-1h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		VSSB_PAON_OUT	VSSA_PAON_OUT	RESERVED		VCCB_PAON_OUT	VCCA_PAON_OUT
R-0h		R/W-1h	R/W-1h	R-0h		R/W-1h	R/W-1h

Table 7-34. PAON_SRC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
12	REF_PAON_OUT	R/W	1h	0: Reference alarm event does not affect PAON pin. 1: Reference alarm event turns off PAON pin.
11	THERMERR_PAON_OUT	R/W	1h	0: Thermal error alarm event does not affect PAON pin. 1: Thermal error alarm event turns off PAON pin.
5	VSSB_PAON_OUT	R/W	1h	0: VSSB alarm event does not affect PAON pin. 1: VSSB alarm event turns off PAON pin.
4	VSSA_PAON_OUT	R/W	1h	0: VSSA alarm event does not affect PAON pin. 1: VSSA alarm event turns off PAON pin.
1	VCCB_PAON_OUT	R/W	1h	0: VCCB alarm event does not affect PAON pin. 1: VCCB alarm event turns off PAON pin.
0	VCCA_PAON_OUT	R/W	1h	0: VCCA alarm event does not affect PAON pin. 1: VCCA alarm event turns off PAON pin.

7.2.1.12 RESET_FLAGS Register (Offset = 70h) [Reset = 000Fh]

Figure 7-30. RESET_FLAGS Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
RESERVED				VDD_COLLAPSE_FLAG	RSTPIN_FLAG	VIO_FLAG	PORBASE_FLAG
R-0h				W-1h	W-1h	W-1h	W-1h

Table 7-35. RESET_FLAGS Register Field Descriptions

Bit	Field	Type	Reset	Description
3	VDD_COLLAPSE_FLAG	W	1h	VDD collapse flag. Write to 0 to detect a VDD collapse event, at which time this flag is automatically set to 1. VDD collapse occurs when VDD reaches to within 1V of the VREF voltage.
2	RSTPIN_FLAG	W	1h	RESET pin reset flag. Write to 0 to detect a RESET pin reset event, at which time this flag is automatically set to 1.
1	VIO_FLAG	W	1h	VIO reset flag. Write to 0 to detect a VIO reset event, at which time this flag is automatically set to 1. VIO reset event occurs as a result of VIO dropping below the POR threshold voltage.
0	PORBASE_FLAG	W	1h	POR base flag. Write to 0 to detect a POR-base reset event, at which time this flag is automatically set to 1. POR-base reset event occurs as a result of VDD dropping below the POR threshold voltage.

7.3 ADC Configuration Register Map

Table 7-36. Page 1: ADC Configuration Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40	ADC_GEN_CFG	R/W	3334	RESERVED	FALR_ADC[2:0]			RESERVED	FALR_SENSE[2:0]			RESERVED	FALR_TMP[2:0]			RESERVED	CMODE	SHUNT_RANGE	RESERVED
41	ADC_CONV_CFG_0	R/W	0555	RESERVED					CONV_RATE_TMP[2:0]			RESERVED	CONV_RATE_ADC[2:0]			RESERVED	CONV_RATE_SENSE[2:0]		
42	ADC_CONV_CFG_1	R/W	0000	RESERVED					AVG_TMP[2:0]			RESERVED	AVG_ADC[2:0]			RESERVED	AVG_SENSE[2:0]		
44	ADC_BYP	R/W	0000	ADC_BYP[15:0]															
46	ADC_HYST_0	R/W	0808	HYST_TMP[7:0]									HYST_ADC[7:0]						
47	ADC_HYST_1	R/W	0008	RESERVED									HYST_SENSE[7:0]						
50	SENSE0_UP_THRESH	R/W	7FFF	THRU[15:0]															
51	SENSE0_LO_THRESH	R/W	8000	THRL[15:0]															
52	SENSE1_UP_THRESH	R/W	7FFF	THRU[15:0]															
53	SENSE1_LO_THRESH	R/W	8000	THRL[15:0]															
54	ADC0_UP_THRESH	R/W	7FFF	RESERVED	THRU[14:0]														
55	ADC0_LO_THRESH	R/W	0000	RESERVED	THRL[14:0]														
56	ADC1_UP_THRESH	R/W	7FFF	RESERVED	THRU[14:0]														
57	ADC1_LO_THRESH	R/W	0000	RESERVED	THRL[14:0]														
58	TMP_UP_THRESH	R/W	7FFF	THRU[15:0]															

7.3.1 ADC Configuration Registers: Page 1

7.3.1.1 ADC_GEN_CFG Register (address = 40h) [reset = 3334h]

Figure 7-31. ADC_GEN_CFG Register

15	14	13	12	11	10	9	8
RESERVED	FALR_ADC[2:0]			RESERVED	FALR_SENSE[2:0]		
R-0h	R/W-3h			R-0h	R/W-3h		
7	6	5	4	3	2	1	0
RESERVED	FALR_TMP[2:0]			RESERVED	CMODE	SHUNT_ RANGE	RESERVED
R-0h	R/W-3h			R-0h	R/W-1h	R/W-0h	R-0h

Table 7-37. ADC_GEN_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
14-12	FALR_ADC	R/W	3h	False alarm factor for external input (ADC) channels. 000: 1 out-of-range conversion required to trigger alarm. 001: 4 consecutive out-of-range conversions required to trigger alarm. 010: 8 consecutive out-of-range conversions required to trigger alarm. 011: 16 consecutive out-of-range conversions required to trigger alarm. 100: 32 consecutive out-of-range conversions required to trigger alarm. 101: 64 consecutive out-of-range conversions required to trigger alarm. 110: 128 consecutive out-of-range conversions required to trigger alarm. 111: 256 consecutive out-of-range conversions required to trigger alarm.
10-8	FALR_SENSE	R/W	3h	False alarm factor for SENSE channels. 000: 1 out-of-range conversion required to trigger alarm. 001: 4 consecutive out-of-range conversions required to trigger alarm. 010: 8 consecutive out-of-range conversions required to trigger alarm. 011: 16 consecutive out-of-range conversions required to trigger alarm. 100: 32 consecutive out-of-range conversions required to trigger alarm. 101: 64 consecutive out-of-range conversions required to trigger alarm. 110: 128 consecutive out-of-range conversions required to trigger alarm. 111: 256 consecutive out-of-range conversions required to trigger alarm.
6-4	FALR_TMP	R/W	3h	False alarm factor for temperature measurements. 000: 1 out-of-range conversion required to trigger alarm. 001: 4 consecutive out-of-range conversions required to trigger alarm. 010: 8 consecutive out-of-range conversions required to trigger alarm. 011: 16 consecutive out-of-range conversions required to trigger alarm. 100: 32 consecutive out-of-range conversions required to trigger alarm. 101: 64 consecutive out-of-range conversions required to trigger alarm. 110: 128 consecutive out-of-range conversions required to trigger alarm. 111: 256 consecutive out-of-range conversions required to trigger alarm.
2	CMODE	R/W	1h	ADC conversion mode bit. This bit selects the ADC conversion mode. 0: Direct-mode. The analog inputs specified in the device sequencer are converted sequentially one time. When one set of conversions is complete the ADC is idle and waits for a new trigger. 1: Auto-mode. The analog inputs specified in the device sequencer are converted sequentially and repeatedly. When one set of conversions is complete the ADC sequencer returns to the start index and repeats the sequence.
1	SHUNT_ RANGE	R/W	0h	Shunt voltage range selection bit for SENSE input channels 0: ± 163.84mV range 1: ± 40.96mV range

7.3.1.2 ADC_CONV_CFG_0 Register (address = 41h) [reset = 0555h]

Figure 7-32. ADC_CONV_CFG_0 Register

15	14	13	12	11	10	9	8
RESERVED					CONV_RATE_TMP[2:0]		
R-0h					R/W-5h		
7	6	5	4	3	2	1	0
RESERVED	CONV_RATE_ADC[2:0]			RESERVED	CONV_RATE_SENSE[2:0]		
R-0h	R/W-5h			R-0h	R/W-5h		

Table 7-38. ADC_CONV_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
10-8	CONV_RATE_TMP	R/W	5h	Total acquisition + conversion time for temperature measurements with no averaging. 000: 52µs 001: 86µs 010: 152µs 011: 282µs 100: 542µs 101: 1054µs 110: 2076µs 111: 4122µs
6-4	CONV_RATE_ADC	R/W	5h	Total acquisition + conversion time for ADC voltage measurements with no averaging. 000: 52µs 001: 86µs 010: 152µs 011: 282µs 100: 542µs 101: 1054µs 110: 2076µs 111: 4122µs
2-0	CONV_RATE_SENSE	R/W	5h	Total acquisition + conversion time for SENSE shunt voltage measurements with no averaging. 000: 52µs 001: 86µs 010: 152µs 011: 282µs 100: 542µs 101: 1054µs 110: 2076µs 111: 4122µs

7.3.1.3 ADC_CONV_CFG_1 Register (address = 42h) [reset = 0000h]

Figure 7-33. ADC_CONV_CFG_1 Register

15	14	13	12	11	10	9	8
RESERVED					AVG_TMP[2:0]		
R-0h					R/W-0h		
7	6	5	4	3	2	1	0
RESERVED	AVG_ADC[2:0]			RESERVED	AVG_SENSE[2:0]		
R-0h	R/W-0h			R-0h	R/W-0h		

Table 7-39. ADC_CONV_CFG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
10-8	AVG_TMP	R/W	0h	Averaging setting for temperature measurements. The device reports and acts upon averaged result. 000: 1 sample 001: 4 samples 010: 16 samples 011: 64 samples 100: 128 samples 101: 256 samples 110: 512 samples 111: 1024 samples
6-4	AVG_ADC	R/W	0h	Averaging setting for ADC voltage measurements. The device reports and acts upon averaged result. 000: 1 sample 001: 4 samples 010: 16 samples 011: 64 samples 100: 128 samples 101: 256 samples 110: 512 samples 111: 1024 samples
2-0	AVG_SENSE	R/W	0h	Averaging setting for SENSE shunt voltage measurements. The device reports and acts upon averaged result. 000: 1 sample 001: 4 samples 010: 16 samples 011: 64 samples 100: 128 samples 101: 256 samples 110: 512 samples 111: 1024 samples

7.3.1.4 ADC_BYP Register (address = 44h) [reset = 0000h]

Figure 7-34. ADC_BYP Register

15	14	13	12	11	10	9	8
ADC_BYP[15:8]							
R/W-0h							
7	6	5	4	3	2	1	0
ADC_BYP[7:0]							
R/W-0h							

Table 7-40. ADC_BYP Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	ADC_BYP	R/W	0h	ADC data bypass value. Only used when ADC_BYP_EN is set to 1

7.3.1.5 ADC_HYST_0 Register (address = 46h) [reset = 0808h]

Figure 7-35. ADC_HYST_0 Register

15	14	13	12	11	10	9	8
HYST_TMP[7:0]							
R/W-8h							
7	6	5	4	3	2	1	0
HYST_ADC[7:0]							
R/W-8h							

Table 7-41. ADC_HYST_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
15-8	HYST_TMP	R/W	8h	Hysteresis setting for temperature measurements. 1 LSB per step.
7-0	HYST_ADC	R/W	8h	Hysteresis setting for ADC voltage measurements. 1 LSB per step.

7.3.1.6 ADC_HYST_1 Register (address = 47h) [reset = 0008h]

Figure 7-36. ADC_HYST_1 Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
HYST_SENSE[7:0]							
R/W-8h							

Table 7-42. ADC_HYST_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	HYST_SENSE	R/W	8h	Hysteresis setting for shunt voltage measurements. 1 LSB per step.

7.3.1.7 SENSE0_UP_THRESH Register (address = 50h) [reset = 7FFFh]

Figure 7-37. SENSE0_UP_THRESH Register

15	14	13	12	11	10	9	8
THRU[15:8]							
R/W-7Fh							
7	6	5	4	3	2	1	0
THRU[7:0]							
R/W-FFh							

Table 7-43. SENSE0_UP_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	THRU	R/W	7FFFh	Upper threshold for shunt voltage measurements, 2's complement value. Corresponding alarm status bit is activated if (channel code > UP thresh) or (channel code < LO thresh), and is cleared if (channel code ≤ UP thresh – hyst) and (channel code ≥ LO thresh + hyst). Upper threshold minus hysteresis must always be greater than lower threshold plus hysteresis. When SHUNT_RANGE = 0, the conversion factor is 5µV/LSB, and when SHUNT_RANGE = 1, the conversion factor is 1.25µV/LSB.

7.3.1.8 SENSE0_LO_THRESH Register (address = 51h) [reset = 8000h]

Figure 7-38. SENSE0_LO_THRESH Register

15	14	13	12	11	10	9	8
THRL[15:8]							
R/W-80h							
7	6	5	4	3	2	1	0
THRL[7:0]							
R/W-00h							

Table 7-44. SENSE0_LO_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	THRL	R/W	8000h	Lower threshold for shunt voltage measurements, 2's complement value. Corresponding alarm status bit is activated if (channel code > UP thresh) or (channel code < LO thresh), and is cleared if (channel code ≤ UP thresh – hyst) and (channel code ≥ LO thresh + hyst). Upper threshold minus hysteresis must always be greater than lower threshold plus hysteresis. When SHUNT_RANGE = 0, the conversion factor is 5µV/LSB, and when SHUNT_RANGE = 1, the conversion factor is 1.25µV/LSB.

7.3.1.9 SENSE1_UP_THRESH Register (address = 52h) [reset = 7FFFh]

Figure 7-39. SENSE1_UP_THRESH Register

15	14	13	12	11	10	9	8
THRU[15:8]							
R/W-7Fh							
7	6	5	4	3	2	1	0
THRU[7:0]							
R/W-FFh							

Table 7-45. SENSE1_UP_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	THRU	R/W	7FFFh	Upper threshold for shunt voltage measurements, 2's complement value. Corresponding alarm status bit is activated if (channel code > UP thresh) or (channel code < LO thresh), and is cleared if (channel code ≤ UP thresh – hyst) and (channel code ≥ LO thresh + hyst). Upper threshold minus hysteresis must always be greater than lower threshold plus hysteresis. When SHUNT_RANGE = 0, the conversion factor is 5µV/LSB, and when SHUNT_RANGE = 1, the conversion factor is 1.25µV/LSB.

7.3.1.10 SENSE1_LO_THRESH Register (address = 53h) [reset = 8000h]

Figure 7-40. SENSE1_LO_THRESH Register

15	14	13	12	11	10	9	8
THRL[15:8]							
R/W-80h							
7	6	5	4	3	2	1	0
THRL[7:0]							
R/W-00h							

Table 7-46. SENSE1_LO_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	THRL	R/W	8000h	Lower threshold for shunt voltage measurements, 2's complement value. Corresponding alarm status bit is activated if (channel code > UP thresh) or (channel code < LO thresh), and is cleared if (channel code ≤ UP thresh – hyst) and (channel code ≥ LO thresh + hyst). Upper threshold minus hysteresis must always be greater than lower threshold plus hysteresis. When SHUNT_RANGE = 0, the conversion factor is 5µV/LSB, and when SHUNT_RANGE = 1, the conversion factor is 1.25µV/LSB.

7.3.1.11 ADC0_UP_THRESH Register (address = 54h) [reset = 7FFFh]

Figure 7-41. ADC0_UP_THRESH Register

15	14	13	12	11	10	9	8
RESERVED	THRU[14:8]						
R-0h	R/W-7Fh						
7	6	5	4	3	2	1	0
THRU[7:0]							
R/W-FFh							

Table 7-47. ADC0_UP_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
14-0	THRU	R/W	7FFFh	Upper threshold for ADC voltage measurements, unsigned positive value. Corresponding alarm status bit is activated if (channel code > UP thresh) or (channel code < LO thresh), and is cleared if (channel code ≤ UP thresh – hyst) and (channel code ≥ LO thresh + hyst). Upper threshold minus hysteresis must always be greater than lower threshold plus hysteresis. Conversion factor is 3.125mV/LSB.

7.3.1.12 ADC0_LO_THRESH Register (address = 55h) [reset = 0000h]

Figure 7-42. ADC0_LO_THRESH Register

15	14	13	12	11	10	9	8
RESERVED	THRL[14:8]						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
THRL[7:0]							
R/W-00h							

Table 7-48. ADC0_LO_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
14-0	THRL	R/W	0000h	Lower threshold for ADC voltage measurements, unsigned positive value. Corresponding alarm status bit is activated if (channel code > UP thresh) or (channel code < LO thresh), and is cleared if (channel code ≤ UP thresh – hyst) and (channel code ≥ LO thresh + hyst). Upper threshold minus hysteresis must always be greater than lower threshold plus hysteresis. Conversion factor is 3.125mV/LSB.

7.3.1.13 ADC1_UP_THRESH Register (address = 56h) [reset = 7FFFh]

Figure 7-43. ADC1_UP_THRESH Register

15	14	13	12	11	10	9	8
RESERVED	THRU[14:8]						
R-0h	R/W-7Fh						
7	6	5	4	3	2	1	0
THRU[7:0]							
R/W-FFh							

Table 7-49. ADC1_UP_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
14-0	THRU	R/W	7FFFh	Upper threshold for ADC voltage measurements, unsigned positive value. Corresponding alarm status bit is activated if (channel code > UP thresh) or (channel code < LO thresh), and is cleared if (channel code ≤ UP thresh – hyst) and (channel code ≥ LO thresh + hyst). Upper threshold minus hysteresis must always be greater than lower threshold plus hysteresis. Conversion factor is 3.125mV/LSB.

7.3.1.14 ADC1_LO_THRESH Register (address = 57h) [reset = 0000h]

Figure 7-44. ADC1_LO_THRESH Register

15	14	13	12	11	10	9	8
RESERVED	THRL[14:8]						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
THRL[7:0]							
R/W-00h							

Table 7-50. ADC1_LO_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
14-0	THRL	R/W	0000h	Lower threshold for ADC voltage measurements, unsigned positive value. Corresponding alarm status bit is activated if (channel code > UP thresh) or (channel code < LO thresh), and is cleared if (channel code ≤ UP thresh – hyst) and (channel code ≥ LO thresh + hyst). Upper threshold minus hysteresis must always be greater than lower threshold plus hysteresis. Conversion factor is 3.125mV/LSB.

7.3.1.15 TMP_UP_THRESH Register (address = 58h) [reset = 7FFFh]

Figure 7-45. TMP_UP_THRESH Register

15	14	13	12	11	10	9	8
THRU[15:8]							
R/W-7Fh							
7	6	5	4	3	2	1	0
THRU[7:0]							
R/W-FFh							

Table 7-51. TMP_UP_THRESH Register Field Descriptions

Bit	Field	Type	Reset	Description
15-0	THRU	R/W	7FFFh	Upper threshold for temperature measurements, in 2's complement representation (use positive values only). Corresponding alarm status bit is activated if (channel code > UP thresh), and is cleared if (channel code ≤ UP thresh – hyst). Upper threshold minus hysteresis must always be positive. Conversion factor is 7.8125m°C/LSB.

7.4 ADC Custom Channel Sequencer Configuration Register Map

Table 7-52. Page 2: ADC Custom Channel Sequencer Configuration Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40	ADC_CCS_IDS_0	R/W	0201	RESERVED					CCS_ID_1[2:0]			RESERVED					CCS_ID_0[2:0]		
41	ADC_CCS_IDS_1	R/W	0403	RESERVED					CCS_ID_3[2:0]			RESERVED					CCS_ID_2[2:0]		
42	ADC_CCS_IDS_2	R/W	0005	RESERVED					CCS_ID_5[2:0]			RESERVED					CCS_ID_4[2:0]		
43	ADC_CCS_IDS_3	R/W	0000	RESERVED					CCS_ID_7[2:0]			RESERVED					CCS_ID_6[2:0]		
44	ADC_CCS_IDS_4	R/W	0000	RESERVED					CCS_ID_9[2:0]			RESERVED					CCS_ID_8[2:0]		
45	ADC_CCS_IDS_5	R/W	0000	RESERVED					CCS_ID_11[2:0]			RESERVED					CCS_ID_10[2:0]		
46	ADC_CCS_IDS_6	R/W	0000	RESERVED					CCS_ID_13[2:0]			RESERVED					CCS_ID_12[2:0]		
47	ADC_CCS_IDS_7	R/W	0000	RESERVED					CCS_ID_15[2:0]			RESERVED					CCS_ID_14[2:0]		
48	ADC_CCS_IDS_8	R/W	0000	RESERVED					CCS_ID_17[2:0]			RESERVED					CCS_ID_16[2:0]		
49	ADC_CCS_IDS_9	R/W	0000	RESERVED					CCS_ID_19[2:0]			RESERVED					CCS_ID_18[2:0]		
4A	ADC_CCS_IDS_10	R/W	0000	RESERVED					CCS_ID_21[2:0]			RESERVED					CCS_ID_20[2:0]		
4B	ADC_CCS_IDS_11	R/W	0000	RESERVED					CCS_ID_23[2:0]			RESERVED					CCS_ID_22[2:0]		
4C	ADC_CCS_IDS_12	R/W	0000	RESERVED					CCS_ID_25[2:0]			RESERVED					CCS_ID_24[2:0]		
4D	ADC_CCS_IDS_13	R/W	0000	RESERVED					CCS_ID_27[2:0]			RESERVED					CCS_ID_26[2:0]		
4E	ADC_CCS_IDS_14	R/W	0000	RESERVED					CCS_ID_29[2:0]			RESERVED					CCS_ID_28[2:0]		
4F	ADC_CCS_IDS_15	R/W	0000	RESERVED					CCS_ID_31[2:0]			RESERVED					CCS_ID_30[2:0]		
50	ADC_CCS_IDS_16	R/W	0000	RESERVED					CCS_ID_33[2:0]			RESERVED					CCS_ID_32[2:0]		
51	ADC_CCS_IDS_17	R/W	0000	RESERVED					CCS_ID_35[2:0]			RESERVED					CCS_ID_34[2:0]		
52	ADC_CCS_IDS_18	R/W	0000	RESERVED					CCS_ID_37[2:0]			RESERVED					CCS_ID_36[2:0]		
53	ADC_CCS_IDS_19	R/W	0000	RESERVED					CCS_ID_39[2:0]			RESERVED					CCS_ID_38[2:0]		
54	ADC_CCS_IDS_20	R/W	0000	RESERVED					CCS_ID_41[2:0]			RESERVED					CCS_ID_40[2:0]		
55	ADC_CCS_IDS_21	R/W	0000	RESERVED					CCS_ID_43[2:0]			RESERVED					CCS_ID_42[2:0]		
56	ADC_CCS_IDS_22	R/W	0000	RESERVED					CCS_ID_45[2:0]			RESERVED					CCS_ID_44[2:0]		
57	ADC_CCS_IDS_23	R/W	0000	RESERVED					CCS_ID_47[2:0]			RESERVED					CCS_ID_46[2:0]		
58	ADC_CCS_IDS_24	R/W	0000	RESERVED					CCS_ID_49[2:0]			RESERVED					CCS_ID_48[2:0]		
59	ADC_CCS_IDS_25	R/W	0000	RESERVED					CCS_ID_51[2:0]			RESERVED					CCS_ID_50[2:0]		

Table 7-52. Page 2: ADC Custom Channel Sequencer Configuration Register Map (continued)

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
5A	ADC_CCS_IDS_26	R/W	0000	RESERVED					CCS_ID_53[2:0]			RESERVED					CCS_ID_52[2:0]		
5B	ADC_CCS_IDS_27	R/W	0000	RESERVED					CCS_ID_55[2:0]			RESERVED					CCS_ID_54[2:0]		
5C	ADC_CCS_IDS_28	R/W	0000	RESERVED					CCS_ID_57[2:0]			RESERVED					CCS_ID_56[2:0]		
5D	ADC_CCS_IDS_29	R/W	0000	RESERVED					CCS_ID_59[2:0]			RESERVED					CCS_ID_58[2:0]		
5E	ADC_CCS_IDS_30	R/W	0000	RESERVED					CCS_ID_61[2:0]			RESERVED					CCS_ID_60[2:0]		
5F	ADC_CCS_IDS_31	R/W	0000	RESERVED					CCS_ID_63[2:0]			RESERVED					CCS_ID_62[2:0]		
60	ADC_CCS_IDS_32	R/W	0000	RESERVED					CCS_ID_65[2:0]			RESERVED					CCS_ID_64[2:0]		
61	ADC_CCS_IDS_33	R/W	0000	RESERVED					CCS_ID_67[2:0]			RESERVED					CCS_ID_66[2:0]		
62	ADC_CCS_IDS_34	R/W	0000	RESERVED					CCS_ID_69[2:0]			RESERVED					CCS_ID_68[2:0]		
63	ADC_CCS_IDS_35	R/W	0000	RESERVED					CCS_ID_71[2:0]			RESERVED					CCS_ID_70[2:0]		
64	ADC_CCS_IDS_36	R/W	0000	RESERVED					CCS_ID_73[2:0]			RESERVED					CCS_ID_72[2:0]		
65	ADC_CCS_IDS_37	R/W	0000	RESERVED					CCS_ID_75[2:0]			RESERVED					CCS_ID_74[2:0]		
66	ADC_CCS_IDS_38	R/W	0000	RESERVED					CCS_ID_77[2:0]			RESERVED					CCS_ID_76[2:0]		
67	ADC_CCS_IDS_39	R/W	0000	RESERVED					CCS_ID_79[2:0]			RESERVED					CCS_ID_78[2:0]		
68	ADC_CCS_IDS_40	R/W	0000	RESERVED					CCS_ID_81[2:0]			RESERVED					CCS_ID_80[2:0]		
69	ADC_CCS_IDS_41	R/W	0000	RESERVED					CCS_ID_83[2:0]			RESERVED					CCS_ID_82[2:0]		
6A	ADC_CCS_IDS_42	R/W	0000	RESERVED					CCS_ID_85[2:0]			RESERVED					CCS_ID_84[2:0]		
6B	ADC_CCS_IDS_43	R/W	0000	RESERVED					CCS_ID_87[2:0]			RESERVED					CCS_ID_86[2:0]		
6C	ADC_CCS_IDS_44	R/W	0000	RESERVED					CCS_ID_89[2:0]			RESERVED					CCS_ID_88[2:0]		
6D	ADC_CCS_IDS_45	R/W	0000	RESERVED					CCS_ID_91[2:0]			RESERVED					CCS_ID_90[2:0]		
6E	ADC_CCS_IDS_46	R/W	0000	RESERVED					CCS_ID_93[2:0]			RESERVED					CCS_ID_92[2:0]		
6F	ADC_CCS_IDS_47	R/W	0000	RESERVED					CCS_ID_95[2:0]			RESERVED					CCS_ID_94[2:0]		
70	ADC_CCS_IDS_48	R/W	0000	RESERVED					CCS_ID_97[2:0]			RESERVED					CCS_ID_96[2:0]		

Table 7-52. Page 2: ADC Custom Channel Sequencer Configuration Register Map (continued)

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
71	ADC_CCS_IDS_49	R/W	0000	RESERVED					CCS_ID_99[2:0]			RESERVED					CCS_ID_98[2:0]		
72	ADC_CCS_IDS_50	R/W	0000	RESERVED					CCS_ID_101[2:0]			RESERVED					CCS_ID_100[2:0]		
73	ADC_CCS_IDS_51	R/W	0000	RESERVED					CCS_ID_103[2:0]			RESERVED					CCS_ID_102[2:0]		
74	ADC_CCS_IDS_52	R/W	0000	RESERVED					CCS_ID_105[2:0]			RESERVED					CCS_ID_104[2:0]		
75	ADC_CCS_IDS_53	R/W	0000	RESERVED					CCS_ID_107[2:0]			RESERVED					CCS_ID_106[2:0]		
76	ADC_CCS_IDS_54	R/W	0000	RESERVED					CCS_ID_109[2:0]			RESERVED					CCS_ID_108[2:0]		
77	ADC_CCS_IDS_55	R/W	0000	RESERVED					CCS_ID_111[2:0]			RESERVED					CCS_ID_110[2:0]		
78	ADC_CCS_IDS_56	R/W	0000	RESERVED					CCS_ID_113[2:0]			RESERVED					CCS_ID_112[2:0]		
79	ADC_CCS_IDS_57	R/W	0000	RESERVED					CCS_ID_115[2:0]			RESERVED					CCS_ID_114[2:0]		
7A	ADC_CCS_IDS_58	R/W	0000	RESERVED					CCS_ID_117[2:0]			RESERVED					CCS_ID_116[2:0]		
7B	ADC_CCS_IDS_59	R/W	0000	RESERVED					CCS_ID_119[2:0]			RESERVED					CCS_ID_118[2:0]		
7C	ADC_CCS_IDS_60	R/W	0000	RESERVED					CCS_ID_121[2:0]			RESERVED					CCS_ID_120[2:0]		
7D	ADC_CCS_IDS_61	R/W	0000	RESERVED					CCS_ID_123[2:0]			RESERVED					CCS_ID_122[2:0]		
7E	ADC_CCS_IDS_62	R/W	0000	RESERVED					CCS_ID_125[2:0]			RESERVED					CCS_ID_124[2:0]		
7F	ADC_CCS_CFG_0	R/W	0004	RESERVED	CCS_START_INDEX[6:0]							RESERVED	CCS_STOP_INDEX[6:0]						

7.4.1 ADC CCS Registers: Page 3

7.4.1.1 ADC_CCS_IDS_n Registers (address = 40h to 7Eh) [reset = see Section 7.4]

Figure 7-46. ADC_CCS_IDS_n Register

15	14	13	12	11	10	9	8
RESERVED					CCS_ID_a[2:0]		
R-0h					R/W		
7	6	5	4	3	2	1	0
RESERVED					CCS_ID_b[2:0]		
R-0h					R/W		

Table 7-53. ADC_CCS_IDS_n Register Field Descriptions

Bit	Field	Type	Reset	Description
10-8	CCS_ID_a	R/W	see Section 7.4	ADC custom channel sequence index setting 000: GND 001: SENSE0 010: SENSE1 011: ADC0 100: ADC1 101: TMP
2-0	CCS_ID_b	R/W	see Section 7.4	

Note

CCS_ID_a refers to odd-indexed CCS ID registers, and *CCS_ID_b* refers to even-indexed CCS ID registers.

7.4.1.2 ADC_CCS_CFG_0 Register (address = 7Fh) [reset = 0004h]

Figure 7-47. ADC_CCS_CFG_0 Register

15	14	13	12	11	10	9	8
RESERVED	CCS_START_INDEX[6:0]						
R-0h	R/W-0h						
7	6	5	4	3	2	1	0
RESERVED	CCS_STOP_INDEX[6:0]						
R-0h	R/W-4h						

Table 7-54. ADC_CCS_CFG_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
14-8	CCS_START_INDEX[6:0]	R/W	0h	Starting index pointer
6-0	CCS_STOP_INDEX[6:0]	R/W	4h	Stopping index pointer. Must not be less than the CCS_START_INDEX.

7.5 DAC Configuration Register Map

Table 7-55. Page 3: DAC Configuration Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40	DAC_CURRENT	R/W	0000	DACB3_CURRENT[1:0]		DACB2_CURRENT[1:0]		DACB1_CURRENT[1:0]		DACB0_CURRENT[1:0]		DACA3_CURRENT[1:0]		DACA2_CURRENT[1:0]		DACA1_CURRENT[1:0]		DACA0_CURRENT[1:0]	
41	DAC_SYNC_CFG	R/W	0000	BCEN_DACB3	BCEN_DACB2	BCEN_DACB1	BCEN_DACB0	BCEN_DACA3	BCEN_DACA2	BCEN_DACA1	BCEN_DACA0	SYNCEN_DACB3	SYNCEN_DACB2	SYNCEN_DACB1	SYNCEN_DACB0	SYNCEN_DACA3	SYNCEN_DACA2	SYNCEN_DACA1	SYNCEN_DACA0
42	DAC_CFG	R/W	0000	RESERVED	DACB_BIPOLAR	RESERVED	DACA_BIPOLAR	RESERVED								CLAMP_SEL_OUTB2	CLAMP_SEL_OUTB0	CLAMP_SEL_OUTA2	CLAMP_SEL_OUTA0
43	DAC_APD_EN	R/W	AAFF	APD_EN_OUTB2[1:0]		APD_EN_OUTB0[1:0]		APD_EN_OUTA2[1:0]		APD_EN_OUTA0[1:0]		APD_EN_DACB3	APD_EN_DACB2	APD_EN_DACB1	APD_EN_DACB0	APD_EN_DACA3	APD_EN_DACA2	APD_EN_DACA1	APD_EN_DACA0
44	DACA_APD_SRC_0	R/W	0000	RESERVED							TMP_ALR_APD	RESERVED		ADC1_ALR_APD	ADC0_ALR_APD	RESERVED		SENSE1_ALR_APD	SENSE0_ALR_APD
45	DACA_APD_SRC_1	R/W	1833	RESERVED		ALARMIN_ALR_APD	REF_ALR_APD	THERM ERR_ALR_APD	RESERVED					VSSB_ALR_APD	VSSA_ALR_APD	RESERVED		VCCB_ALR_APD	VCCA_ALR_APD
46	OUTA_APD_SRC_0	R/W	0000	RESERVED							TMP_ALR_APD	RESERVED		ADC1_ALR_APD	ADC0_ALR_APD	RESERVED		SENSE1_ALR_APD	SENSE0_ALR_APD
47	OUTA_APD_SRC_1	R/W	1833	RESERVED		ALARMIN_ALR_APD	REF_ALR_APD	THERM ERR_ALR_APD	RESERVED					VSSB_ALR_APD	VSSA_ALR_APD	RESERVED		VCCB_ALR_APD	VCCA_ALR_APD
48	DACB_APD_SRC_0	R/W	0000	RESERVED							TMP_ALR_APD	RESERVED		ADC1_ALR_APD	ADC0_ALR_APD	RESERVED		SENSE1_ALR_APD	SENSE0_ALR_APD
49	DACB_APD_SRC_1	R/W	1833	RESERVED		ALARMIN_ALR_APD	REF_ALR_APD	THERM ERR_ALR_APD	RESERVED					VSSB_ALR_APD	VSSA_ALR_APD	RESERVED		VCCB_ALR_APD	VCCA_ALR_APD
4A	OUTB_APD_SRC_0	R/W	0000	RESERVED							TMP_ALR_APD	RESERVED		ADC1_ALR_APD	ADC0_ALR_APD	RESERVED		SENSE1_ALR_APD	SENSE0_ALR_APD
4B	OUTB_APD_SRC_1	R/W	1833	RESERVED		ALARMIN_ALR_APD	REF_ALR_APD	THERM ERR_ALR_APD	RESERVED					VSSB_ALR_APD	VSSA_ALR_APD	RESERVED		VCCB_ALR_APD	VCCA_ALR_APD
4C	DAC_CODE_LIMIT_0	R/W	3F3F	RESERVED		DACA1_LIMIT[5:0]						RESERVED		DACA0_LIMIT[5:0]					
4D	DAC_CODE_LIMIT_1	R/W	3F3F	RESERVED		DACA3_LIMIT[5:0]						RESERVED		DACA2_LIMIT[5:0]					
4E	DAC_CODE_LIMIT_2	R/W	3F3F	RESERVED		DACB1_LIMIT[5:0]						RESERVED		DACB0_LIMIT[5:0]					
4F	DAC_CODE_LIMIT_3	R/W	3F3F	RESERVED		DACB3_LIMIT[5:0]						RESERVED		DACB2_LIMIT[5:0]					
50	DRVEN0_EN	R/W	0000	RESERVED								DRVEN0_EN_DACB3	DRVEN0_EN_DACB2	DRVEN0_EN_DACB1	DRVEN0_EN_DACB0	DRVEN0_EN_DACA3	DRVEN0_EN_DACA2	DRVEN0_EN_DACA1	DRVEN0_EN_DACA0
51	DRVEN1_EN	R/W	0000	RESERVED								DRVEN1_EN_DACB3	DRVEN1_EN_DACB2	DRVEN1_EN_DACB1	DRVEN1_EN_DACB0	DRVEN1_EN_DACA3	DRVEN1_EN_DACA2	DRVEN1_EN_DACA1	DRVEN1_EN_DACA0
52	FLEXIO_EN	R/W	0000	RESERVED								FLEXIO_EN_DACB3	FLEXIO_EN_DACB2	FLEXIO_EN_DACB1	FLEXIO_EN_DACB0	FLEXIO_EN_DACA3	FLEXIO_EN_DACA2	FLEXIO_EN_DACA1	FLEXIO_EN_DACA0

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7.5.1.1 DAC_CURRENT Register (address = 40h) [reset = 0000h]

Figure 7-48. DAC_CURRENT Register

15	14	13	12	11	10	9	8
DACB3_CURRENT[1:0]		DACB2_CURRENT[1:0]		DACB1_CURRENT[1:0]		DACB0_CURRENT[1:0]	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	
7	6	5	4	3	2	1	0
DACA3_CURRENT[1:0]		DACA2_CURRENT[1:0]		DACA1_CURRENT[1:0]		DACA0_CURRENT[1:0]	
R/W-0h		R/W-0h		R/W-0h		R/W-0h	

Table 7-56. DAC_CURRENT Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	DACB3_CURRENT	R/W	0h	DAC output current mode selection. 00: Start-up, 15mA 01: Low current mode, 30mA 10: Normal current mode, 90mA 11: High current mode, 120mA
13-12	DACB2_CURRENT	R/W	0h	DAC output current mode selection. 00: Start-up, 15mA 01: Low current mode, 30mA 10: Normal current mode, 90mA 11: High current mode, 120mA
11-10	DACB1_CURRENT	R/W	0h	DAC output current mode selection. 00: Start-up, 15mA 01: Low current mode, 30mA 10: Normal current mode, 90mA 11: High current mode, 120mA
9-8	DACB0_CURRENT	R/W	0h	DAC output current mode selection. 00: Start-up, 15mA 01: Low current mode, 30mA 10: Normal current mode, 90mA 11: High current mode, 120mA
7-6	DACA3_CURRENT	R/W	0h	DAC output current mode selection. 00: Start-up, 15mA 01: Low current mode, 30mA 10: Normal current mode, 90mA 11: High current mode, 120mA
5-4	DACA2_CURRENT	R/W	0h	DAC output current mode selection. 00: Start-up, 15mA 01: Low current mode, 30mA 10: Normal current mode, 90mA 11: High current mode, 120mA
3-2	DACA1_CURRENT	R/W	0h	DAC output current mode selection. 00: Start-up, 15mA 01: Low current mode, 30mA 10: Normal current mode, 90mA 11: High current mode, 120mA
1-0	DACA0_CURRENT	R/W	0h	DAC output current mode selection. 00: Start-up, 15mA 01: Low current mode, 30mA 10: Normal current mode, 90mA 11: High current mode, 120mA

7.5.1.2 DAC_SYNC_CFG Register (address = 41h) [reset = 0000h]

Figure 7-49. DAC_SYNC_CFG Register

15	14	13	12	11	10	9	8
BCEN_DACB3	BCEN_DACB2	BCEN_DACB1	BCEN_DACB0	BCEN_DACA3	BCEN_DACA2	BCEN_DACA1	BCEN_DACA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
SYNCEN_DACB3	SYNCEN_DACB2	SYNCEN_DACB1	SYNCEN_DACB0	SYNCEN_DACA3	SYNCEN_DACA2	SYNCEN_DACA1	SYNCEN_DACA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-57. DAC_SYNC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
15	BCEN_DACB3	R/W	0h	DAC broadcast enable. 0: Ignores broadcast writes on this DAC 1: Allow broadcast writes on this DAC
14	BCEN_DACB2	R/W	0h	
13	BCEN_DACB1	R/W	0h	
12	BCEN_DACB0	R/W	0h	
11	BCEN_DACA3	R/W	0h	
10	BCEN_DACA2	R/W	0h	
9	BCEN_DACA1	R/W	0h	
8	BCEN_DACA0	R/W	0h	
7	SYNCEN_DACB3	R/W	0h	DAC synchronous configuration. 0: Set DAC into asynchronous mode. 1: Set DAC into synchronous mode.
6	SYNCEN_DACB2	R/W	0h	
5	SYNCEN_DACB1	R/W	0h	
4	SYNCEN_DACB0	R/W	0h	
3	SYNCEN_DACA3	R/W	0h	
2	SYNCEN_DACA2	R/W	0h	
1	SYNCEN_DACA1	R/W	0h	
0	SYNCEN_DACA0	R/W	0h	

7.5.1.3 DAC_CFG Register (address = 42h) [reset = 0000h]

Figure 7-50. DAC_CFG Register

15	14	13	12	11	10	9	8
RESERVED	DACB_ BIPOLAR	RESERVED	DACA_ BIPOLAR	RESERVED			
R-0h	R/W-0h	R-0h	R/W-0h	R-0h			
7	6	5	4	3	2	1	0
RESERVED				CLAMP_SEL_ OUTB2	CLAMP_SEL_ OUTB0	CLAMP_SEL_ OUTA2	CLAMP_SEL_ OUTA0
R-0h				R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-58. DAC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
14	DACB_BIPOLAR	R/W	0h	Used to configure DAC group B for bipolar operation. 0: Unipolar operation 1: Bipolar operation
12	DACA_BIPOLAR	R/W	0h	Used to configure DAC group A for bipolar operation. 0: Unipolar operation 1: Bipolar operation
3	CLAMP_SEL_OUTB2	R/W	0h	Clamp voltage selection for OUTB2. 0: Clamp voltage is VSSB 1: Clamp voltage is DACB3
2	CLAMP_SEL_OUTB0	R/W	0h	Clamp voltage selection for OUTB0. 0: Clamp voltage is VSSB 1: Clamp voltage is DACB1
1	CLAMP_SEL_OUTA2	R/W	0h	Clamp voltage selection for OUTA2. 0: Clamp voltage is VSSA 1: Clamp voltage is DACA3
0	CLAMP_SEL_OUTA0	R/W	0h	Clamp voltage selection for OUTA0. 0: Clamp voltage is VSSA 1: Clamp voltage is DACA1

7.5.1.4 DAC_APD_EN Register (address = 43h) [reset = AAFFh]

Figure 7-51. DAC_APD_EN Register

15	14	13	12	11	10	9	8
APD_EN_OUTB2[1:0]		APD_EN_OUTB0[1:0]		APD_EN_OUTA2[1:0]		APD_EN_OUTA0[1:0]	
R/W-2h		R/W-2h		R/W-2h		R/W-2h	
7	6	5	4	3	2	1	0
APD_EN_DACB3	APD_EN_DACB2	APD_EN_DACB1	APD_EN_DACB0	APD_EN_DACA3	APD_EN_DACA2	APD_EN_DACA1	APD_EN_DACA0
R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h	R/W-1h

Table 7-59. DAC_APD_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
15-14	APD_EN_OUTB2	R/W	2h	OUTB pin auto-power-down enable 00: Ignore auto-power-down events on the OUTB pin. 10: Disable OUTB pin drive channel, and connect to VSSB during an auto-power-down event. 11: Disable OUTB pin drive channel, and connect to VSSB or DAC output (depending on clamp setting) during an auto-power-down event.
13-12	APD_EN_OUTB0	R/W	2h	
11-10	APD_EN_OUTA2	R/W	2h	OUTA pin auto-power-down enable 00: Ignore auto-power-down events on the OUTA pin. 10: Disable OUTA pin drive channel, and connect to VSSA during an auto-power-down event. 11: Disable OUTA pin drive channel, and connect to VSSA or DAC output (depending on clamp setting) during an auto-power-down event.
9-8	APD_EN_OUTA0	R/W	2h	
7	APD_EN_DACB3	R/W	1h	DAC pin auto-power-down enable 0: Ignore auto-power-down events on the DAC. 1: Force this DAC to power-down during an auto-power-down event.
6	APD_EN_DACB2	R/W	1h	
5	APD_EN_DACB1	R/W	1h	
4	APD_EN_DACB0	R/W	1h	
3	APD_EN_DACA3	R/W	1h	
2	APD_EN_DACA2	R/W	1h	
1	APD_EN_DACA1	R/W	1h	
0	APD_EN_DACA0	R/W	1h	

7.5.1.5 DACA_APD_SRC_0 Register (address = 44h) [reset = 0000h]

Figure 7-52. DACA_APD_SRC_0 Register

15	14	13	12	11	10	9	8
RESERVED							TMP_ ALR_APD
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		ADC1_ ALR_APD	ADC0_ ALR_APD	RESERVED		SENSE1_ ALR_APD	SENSE0_ ALR_APD
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 7-60. DACA_APD_SRC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
8	TMP_ALR_APD	R/W	0h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: Temperature alarm does not trigger DACA auto-power-down event 1: Temperature alarm triggers DACA auto-power-down event
5	ADC1_ALR_APD	R/W	0h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: ADC1 alarm does not trigger DACA auto-power-down event 1: ADC1 alarm triggers DACA auto-power-down event
4	ADC0_ALR_APD	R/W	0h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: ADC0 alarm does not trigger DACA auto-power-down event 1: ADC0 alarm triggers DACA auto-power-down event
1	SENSE1_ALR_APD	R/W	0h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: SENSE1 alarm does not trigger DACA auto-power-down event 1: SENSE1 alarm triggers DACA auto-power-down event
0	SENSE0_ALR_APD	R/W	0h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: SENSE0 alarm does not trigger DACA auto-power-down event 1: SENSE0 alarm triggers DACA auto-power-down event

7.5.1.6 DACA_APD_SRC_1 Register (address = 45h) [reset = 1833h]

Figure 7-53. DACA_APD_SRC_1 Register

15	14	13	12	11	10	9	8
RESERVED		ALARMIN_ ALR_APD	REF_ ALR_APD	THERMERR_ ALR_APD	RESERVED		
R-0h		R/W-0h	R/W-1h	R/W-1h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		VSSB_ ALR_APD	VSSA_ ALR_APD	RESERVED		VCCB_ ALR_APD	VCCA_ ALR_APD
R-0h		R/W-1h	R/W-1h	R-0h		R/W-1h	R/W-1h

Table 7-61. DACA_APD_SRC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
13	ALARMIN_ALR_APD	R/W	0h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: $\overline{\text{ALARMIN}}$ alarm does not trigger DACA auto-power-down event 1: $\overline{\text{ALARMIN}}$ alarm triggers DACA auto-power-down event
12	REF_ALR_APD	R/W	1h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: Reference alarm does not trigger DACA auto-power-down event 1: Reference alarm triggers DACA auto-power-down event
11	THERMERR_ALR_APD	R/W	1h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: Thermal error alarm does not trigger DACA auto-power-down event 1: Thermal error alarm triggers DACA auto-power-down event
5	VSSB_ALR_APD	R/W	1h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: VSSB alarm does not trigger DACA auto-power-down event 1: VSSB alarm triggers DACA auto-power-down event
4	VSSA_ALR_APD	R/W	1h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: VSSA alarm does not trigger DACA auto-power-down event 1: VSSA alarm triggers DACA auto-power-down event
1	VCCB_ALR_APD	R/W	1h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register.0: VCCB alarm does not trigger DACA auto-power-down event 1: VCCB alarm triggers DACA auto-power-down event
0	VCCA_ALR_APD	R/W	1h	This bit determines if group A DACs are forced into a power-down state by this alarm. The respective DACA channels must be enabled in the DAC_APD_EN register. 0: VCCA alarm does not trigger DACA auto-power-down event 1: VCCA alarm triggers DACA auto-power-down event

7.5.1.7 OUTA_APD_SRC_0 Register (address = 46h) [reset = 0000h]

Figure 7-54. OUTA_APD_SRC_0 Register

15	14	13	12	11	10	9	8
RESERVED							TMP_ALR_APD
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		ADC1_ALR_APD	ADC0_ALR_APD	RESERVED		SENSE1_ALR_APD	SENSE0_ALR_APD
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 7-62. OUTA_APD_SRC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
8	TMP_ALR_APD	R/W	0h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: Temperature alarm does not trigger OUTA pin auto-power-down event 1: Temperature alarm triggers OUTA pin auto-power-down event
5	ADC1_ALR_APD	R/W	0h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: ADC1 alarm does not trigger OUTA pin auto-power-down event 1: ADC1 alarm triggers OUTA pin auto-power-down event
4	ADC0_ALR_APD	R/W	0h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: ADC0 alarm does not trigger OUTA pin auto-power-down event 1: ADC0 alarm triggers OUTA pin auto-power-down event
1	SENSE1_ALR_APD	R/W	0h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: SENSE1 alarm does not trigger OUTA pin auto-power-down event 1: SENSE1 alarm triggers OUTA pin auto-power-down event
0	SENSE0_ALR_APD	R/W	0h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: SENSE0 alarm does not trigger OUTA pin auto-power-down event 1: SENSE0 alarm triggers OUTA pin auto-power-down event

7.5.1.8 OUTA_APD_SRC_1 Register (address = 47h) [reset = 1833h]

Figure 7-55. OUTA_APD_SRC_1 Register

15	14	13	12	11	10	9	8
RESERVED		ALARMIN_ ALR_APD	REF_ ALR_APD	THERMERR_ ALR_APD	RESERVED		
R-0h		R/W-0h	R/W-1h	R/W-1h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		VSSB_ ALR_APD	VSSA_ ALR_APD	RESERVED		VCCB_ ALR_APD	VCCA_ ALR_APD
R-0h		R/W-1h	R/W-1h	R-0h		R/W-1h	R/W-1h

Table 7-63. OUTA_APD_SRC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
13	ALARMIN_ALR_APD	R/W	0h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: $\overline{\text{ALARMIN}}$ alarm does not trigger OUTA pin auto-power-down event 1: $\overline{\text{ALARMIN}}$ alarm triggers OUTA pin auto-power-down event
12	REF_ALR_APD	R/W	1h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: Reference alarm does not trigger OUTA pin auto-power-down event 1: Reference alarm triggers OUTA pin auto-power-down event
11	THERMERR_ALR_APD	R/W	1h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: Thermal error alarm does not trigger OUTA pin auto-power-down event 1: Thermal error alarm triggers OUTA pin auto-power-down event
5	VSSB_ALR_APD	R/W	1h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: VSSB alarm does not trigger OUTA pin auto-power-down event 1: VSSB alarm triggers OUTA pin auto-power-down event
4	VSSA_ALR_APD	R/W	1h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: VSSA alarm does not trigger OUTA pin auto-power-down event 1: VSSA alarm triggers OUTA pin auto-power-down event
1	VCCB_ALR_APD	R/W	1h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: VCCB alarm does not trigger OUTA pin auto-power-down event 1: VCCB alarm triggers OUTA pin auto-power-down event
0	VCCA_ALR_APD	R/W	1h	This bit determines if group A OUT pins are forced into a power-down state by this alarm. The respective OUTA pins must be enabled in the DAC_APD_EN register. 0: VCCA alarm does not trigger OUTA pin auto-power-down event 1: VCCA alarm triggers OUTA pin auto-power-down event

7.5.1.9 DACB_APD_SRC_0 Register (address = 48h) [reset = 0000h]

Figure 7-56. DACB_APD_SRC_0 Register

15	14	13	12	11	10	9	8
RESERVED							TMP_ ALR_APD
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		ADC1_ ALR_APD	ADC0_ ALR_APD	RESERVED		SENSE1_ ALR_APD	SENSE0_ ALR_APD
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 7-64. DACB_APD_SRC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
8	TMP_ALR_APD	R/W	0h	This bit determines if group B DAC pins are forced into a power-down state by this alarm. The respective DACB pins must be enabled in the DAC_APD_EN register. 0: Temperature alarm does not trigger DACB auto-power-down event 1: Temperature alarm triggers DACB auto-power-down event
5	ADC1_ALR_APD	R/W	0h	This bit determines if group B DAC pins are forced into a power-down state by this alarm. The respective DACB pins must be enabled in the DAC_APD_EN register. 0: ADC1 alarm does not trigger DACB auto-power-down event 1: ADC1 alarm triggers DACB auto-power-down event
4	ADC0_ALR_APD	R/W	0h	This bit determines if group B DAC pins are forced into a power-down state by this alarm. The respective DACB pins must be enabled in the DAC_APD_EN register. 0: ADC0 alarm does not trigger DACB auto-power-down event 1: ADC0 alarm triggers DACB auto-power-down event
1	SENSE1_ALR_APD	R/W	0h	This bit determines if group B DAC pins are forced into a power-down state by this alarm. The respective DACB pins must be enabled in the DAC_APD_EN register. 0: SENSE1 alarm does not trigger DACB auto-power-down event 1: SENSE1 alarm triggers DACB auto-power-down event
0	SENSE0_ALR_APD	R/W	0h	This bit determines if group B DAC pins are forced into a power-down state by this alarm. The respective DACB pins must be enabled in the DAC_APD_EN register. 0: SENSE0 alarm does not trigger DACB auto-power-down event 1: SENSE0 alarm triggers DACB auto-power-down event

7.5.1.10 DACB_APD_SRC_1 Register (address = 49h) [reset = 1833h]

Figure 7-57. DACB_APD_SRC_1 Register

15	14	13	12	11	10	9	8
RESERVED		ALARMIN_ ALR_APD	REF_ ALR_APD	THERMERR_ ALR_APD	RESERVED		
R-0h		R/W-0h	R/W-1h	R/W-1h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		VSSB_ ALR_APD	VSSA_ ALR_APD	RESERVED		VCCB_ ALR_APD	VCCA_ ALR_APD
R-0h		R/W-1h	R/W-1h	R-0h		R/W-1h	R/W-1h

Table 7-65. DACB_APD_SRC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
13	ALARMIN_ALR_APD	R/W	0h	This bit determines if group B DACs are forced into a power-down state by this alarm. The respective DACB channels must be enabled in the DAC_APD_EN register. 0: $\overline{\text{ALARMIN}}$ alarm does not trigger DACB auto-power-down event 1: $\overline{\text{ALARMIN}}$ alarm triggers DACB auto-power-down event
12	REF_ALR_APD	R/W	1h	This bit determines if group B DACs are forced into a power-down state by this alarm. The respective DACB channels must be enabled in the DAC_APD_EN register. 0: Reference alarm does not trigger DACB auto-power-down event 1: Reference alarm triggers DACB auto-power-down event
11	THERMERR_ALR_APD	R/W	1h	This bit determines if group B DACs are forced into a power-down state by this alarm. The respective DACB channels must be enabled in the DAC_APD_EN register. 0: Thermal error alarm does not trigger DACB auto-power-down event 1: Thermal error alarm triggers DACB auto-power-down event
5	VSSB_ALR_APD	R/W	1h	This bit determines if group B DACs are forced into a power-down state by this alarm. The respective DACB channels must be enabled in the DAC_APD_EN register. 0: VSSB alarm does not trigger DACB auto-power-down event 1: VSSB alarm triggers DACB auto-power-down event
4	VSSA_ALR_APD	R/W	1h	This bit determines if group B DACs are forced into a power-down state by this alarm. The respective DACB channels must be enabled in the DAC_APD_EN register. 0: VSSA alarm does not trigger DACB auto-power-down event 1: VSSA alarm triggers DACB auto-power-down event
1	VCCB_ALR_APD	R/W	1h	This bit determines if group B DACs are forced into a power-down state by this alarm. The respective DACB channels must be enabled in the DAC_APD_EN register. 0: VCCB alarm does not trigger DACB auto-power-down event 1: VCCB alarm triggers DACB auto-power-down event
0	VCCA_ALR_APD	R/W	1h	This bit determines if group B DACs are forced into a power-down state by this alarm. The respective DACB channels must be enabled in the DAC_APD_EN register. 0: VCCA alarm does not trigger DACB auto-power-down event 1: VCCA alarm triggers DACB auto-power-down event

7.5.1.11 OUTB_APD_SRC_0 Register (address = 4Ah) [reset = 0000h]

Figure 7-58. OUTB_APD_SRC_0 Register

15	14	13	12	11	10	9	8
RESERVED							TMP_ALR_APD
R-0h							R/W-0h
7	6	5	4	3	2	1	0
RESERVED		ADC1_ALR_APD	ADC0_ALR_APD	RESERVED		SENSE1_ALR_APD	SENSE0_ALR_APD
R-0h		R/W-0h	R/W-0h	R-0h		R/W-0h	R/W-0h

Table 7-66. OUTB_APD_SRC_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
8	TMP_ALR_APD	R/W	0h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: Temperature alarm does not trigger OUTB pin auto-power-down event 1: Temperature alarm triggers OUTB pin auto-power-down event
5	ADC1_ALR_APD	R/W	0h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: ADC1 alarm does not trigger OUTB pin auto-power-down event 1: ADC1 alarm triggers OUTB pin auto-power-down event
4	ADC0_ALR_APD	R/W	0h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: ADC0 alarm does not trigger OUTB pin auto-power-down event 1: ADC0 alarm triggers OUTB pin auto-power-down event
1	SENSE1_ALR_APD	R/W	0h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: SENSE1 alarm does not trigger OUTB pin auto-power-down event 1: SENSE1 alarm triggers OUTB pin auto-power-down event
0	SENSE0_ALR_APD	R/W	0h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: SENSE0 alarm does not trigger OUTB pin auto-power-down event 1: SENSE0 alarm triggers OUTB pin auto-power-down event

7.5.1.12 OUTB_APD_SRC_1 Register (address = 4Bh) [reset = 1833h]

Figure 7-59. OUTB_APD_SRC_1 Register

15	14	13	12	11	10	9	8
RESERVED		ALARMIN_ ALR_APD	REF_ ALR_APD	THERMERR_ ALR_APD	RESERVED		
R-0h		R/W-0h	R/W-1h	R/W-1h	R-0h		
7	6	5	4	3	2	1	0
RESERVED		VSSB_ ALR_APD	VSSA_ ALR_APD	RESERVED		VCCB_ ALR_APD	VCCA_ ALR_APD
R-0h		R/W-1h	R/W-1h	R-0h		R/W-1h	R/W-1h

Table 7-67. OUTB_APD_SRC_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
13	ALARMIN_ALR_APD	R/W	0h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: $\overline{\text{ALARMIN}}$ alarm does not trigger OUTB pin auto-power-down event 1: $\overline{\text{ALARMIN}}$ alarm triggers OUTB pin auto-power-down event
12	REF_ALR_APD	R/W	1h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: Reference alarm does not trigger OUTB pin auto-power-down event 1: Reference alarm triggers OUTB pin auto-power-down event
11	THERMERR_ALR_APD	R/W	1h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: Thermal error alarm does not trigger OUTB pin auto-power-down event 1: Thermal error alarm triggers OUTB pin auto-power-down event
5	VSSB_ALR_APD	R/W	1h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: VSSB alarm does not trigger OUTB pin auto-power-down event 1: VSSB alarm triggers OUTB pin auto-power-down event
4	VSSA_ALR_APD	R/W	1h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: VSSA alarm does not trigger OUTB pin auto-power-down event 1: VSSA alarm triggers OUTB pin auto-power-down event
1	VCCB_ALR_APD	R/W	1h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: VCCB alarm does not trigger OUTB pin auto-power-down event 1: VCCB alarm triggers OUTB pin auto-power-down event
0	VCCA_ALR_APD	R/W	1h	This bit determines if group B OUT pins are forced into a power-down state by this alarm. The respective OUTB pins must be enabled in the DAC_APD_EN register. 0: VCCA alarm does not trigger OUTB pin auto-power-down event 1: VCCA alarm triggers OUTB pin auto-power-down event

7.5.1.13 DAC_CODE_LIMIT_0 Register (address = 4Ch) [reset = 3F3Fh]

Figure 7-60. DAC_CODE_LIMIT_0 Register

15	14	13	12	11	10	9	8
RESERVED		DACA1_LIMITS[5:0]					
R-0h		R/W-3Fh					
7	6	5	4	3	2	1	0
RESERVED		DACA0_LIMITS[5:0]					
R-0h		R/W-3Fh					

Table 7-68. DAC_CODE_LIMIT_0 Register Field Descriptions

Bit	Field	Type	Reset	Description
13-8	DACA1_LIMITS	R/W	3Fh	DAC active register latch code limit; off by default. Program these bits with the following values to achieve the limit specified for the upper six MSBs of the DAC codes. 00h: 007Fh 01h: 00FFh 02h: 017Fh 03h: 01FFh 04h: 027Fh 05h: 02FFh 06h: 037Fh 07h: 03FFh 08h: 047Fh 09h: 04FFh 0Ah: 057Fh 0Bh: 05FFh 0Ch: 067Fh 0Dh: 06FFh 0Eh: 077Fh 0Fh: 07FFh 10h: 087Fh 11h: 08FFh 12h: 097Fh 13h: 09FFh 14h: 0A7Fh 15h: 0AFFh 16h: 0B7Fh 17h: 0BFFh 18h: 0C7Fh 19h: 0CFFh 1Ah: 0D7Fh 1Bh: 0DFFh 1Ch: 0E7Fh 1Dh: 0EFFh 1Eh: 0F7Fh 1Fh: 0FFFh 20h: 107Fh 21h: 10FFh 22h: 117Fh 23h: 11FFh 24h: 127Fh 25h: 12FFh 26h: 137Fh 27h: 13FFh 28h: 147Fh 29h: 14FFh 2Ah: 157Fh 2Bh: 15FFh 2Ch: 167Fh 2Dh: 16FFh 2Eh: 177Fh 2Fh: 17FFh 30h: 187Fh 31h: 18FFh 32h: 197Fh 33h: 19FFh 34h: 1A7Fh 35h: 1AFFh 36h: 1B7Fh 37h: 1BFFh 38h: 1C7Fh 39h: 1CFFh 3Ah: 1D7Fh 3Bh: 1DFFh 3Ch: 1E7Fh 3Dh: 1EFFh 3Eh: 1F7Fh 3Fh: 1FFFh
5-0	DACA0_LIMITS	R/W	3Fh	

7.5.1.14 DAC_CODE_LIMIT_1 Register (address = 4Dh) [reset = 3F3Fh]

Figure 7-61. DAC_CODE_LIMIT_1 Register

15	14	13	12	11	10	9	8
RESERVED		DACA3_LIMITS[5:0]					
R-0h		R/W-3Fh					
7	6	5	4	3	2	1	0
RESERVED		DACA2_LIMITS[5:0]					
R-0h		R/W-3Fh					

Table 7-69. DAC_CODE_LIMIT_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
13-8	DACA3_LIMITS	R/W	3Fh	DAC active register latch code limit; off by default. Program these bits with the following values to achieve the limit specified for the upper six MSBs of the DAC codes. 00h: 007Fh 01h: 00FFh 02h: 017Fh 03h: 01FFh 04h: 027Fh 05h: 02FFh 06h: 037Fh 07h: 03FFh 08h: 047Fh 09h: 04FFh 0Ah: 057Fh 0Bh: 05FFh 0Ch: 067Fh 0Dh: 06FFh 0Eh: 077Fh 0Fh: 07FFh 10h: 087Fh 11h: 08FFh 12h: 097Fh 13h: 09FFh 14h: 0A7Fh 15h: 0AFFh 16h: 0B7Fh 17h: 0BFFh 18h: 0C7Fh 19h: 0CFFh 1Ah: 0D7Fh 1Bh: 0DFFh 1Ch: 0E7Fh 1Dh: 0EFFh 1Eh: 0F7Fh 1Fh: 0FFFh 20h: 107Fh 21h: 10FFh 22h: 117Fh 23h: 11FFh 24h: 127Fh 25h: 12FFh 26h: 137Fh 27h: 13FFh 28h: 147Fh 29h: 14FFh 2Ah: 157Fh 2Bh: 15FFh 2Ch: 167Fh 2Dh: 16FFh 2Eh: 177Fh 2Fh: 17FFh 30h: 187Fh 31h: 18FFh 32h: 197Fh 33h: 19FFh 34h: 1A7Fh 35h: 1AFFh 36h: 1B7Fh 37h: 1BFFh 38h: 1C7Fh 39h: 1CFFh 3Ah: 1D7Fh 3Bh: 1DFFh 3Ch: 1E7Fh 3Dh: 1EFFh 3Eh: 1F7Fh 3Fh: 1FFFh
5-0	DACA2_LIMITS	R/W	3Fh	

7.5.1.15 DAC_CODE_LIMIT_2 Register (address = 4Eh) [reset = 3F3Fh]

Figure 7-62. DAC_CODE_LIMIT_2 Register

15	14	13	12	11	10	9	8
RESERVED		DACB1_LIMITS[5:0]					
R-0h		R/W-3Fh					
7	6	5	4	3	2	1	0
RESERVED		DACB0_LIMITS[5:0]					
R-0h		R/W-3Fh					

Table 7-70. DAC_CODE_LIMIT_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
13-8	DACB1_LIMITS	R/W	3Fh	DAC active register latch code limit; off by default. Program these bits with the following values to achieve the limit specified for the upper six MSBs of the DAC codes. 00h: 007Fh 01h: 00FFh 02h: 017Fh 03h: 01FFh 04h: 027Fh 05h: 02FFh 06h: 037Fh 07h: 03FFh 08h: 047Fh 09h: 04FFh 0Ah: 057Fh 0Bh: 05FFh 0Ch: 067Fh 0Dh: 06FFh 0Eh: 077Fh 0Fh: 07FFh 10h: 087Fh 11h: 08FFh 12h: 097Fh 13h: 09FFh 14h: 0A7Fh 15h: 0AFFh 16h: 0B7Fh 17h: 0BFFh 18h: 0C7Fh 19h: 0CFFh 1Ah: 0D7Fh 1Bh: 0DFFh 1Ch: 0E7Fh 1Dh: 0EFFh 1Eh: 0F7Fh 1Fh: 0FFFh 20h: 107Fh 21h: 10FFh 22h: 117Fh 23h: 11FFh 24h: 127Fh 25h: 12FFh 26h: 137Fh 27h: 13FFh 28h: 147Fh 29h: 14FFh 2Ah: 157Fh 2Bh: 15FFh 2Ch: 167Fh 2Dh: 16FFh 2Eh: 177Fh 2Fh: 17FFh 30h: 187Fh 31h: 18FFh 32h: 197Fh 33h: 19FFh 34h: 1A7Fh 35h: 1AFFh 36h: 1B7Fh 37h: 1BFFh 38h: 1C7Fh 39h: 1CFFh 3Ah: 1D7Fh 3Bh: 1DFFh 3Ch: 1E7Fh 3Dh: 1EFFh 3Eh: 1F7Fh 3Fh: 1FFFh
5-0	DACB0_LIMITS	R/W	3Fh	

7.5.1.16 DAC_CODE_LIMIT_3 Register (address = 4Fh) [reset = 3F3Fh]

Figure 7-63. DAC_CODE_LIMIT_3 Register

15	14	13	12	11	10	9	8
RESERVED		DACB3_LIMITS[5:0]					
R-0h		R/W-3Fh					
7	6	5	4	3	2	1	0
RESERVED		DACB2_LIMITS[5:0]					
R-0h		R/W-3Fh					

Table 7-71. DAC_CODE_LIMIT_3 Register Field Descriptions

Bit	Field	Type	Reset	Description
13-8	DACB3_LIMITS	R/W	3Fh	DAC active register latch code limit; off by default. Program these bits with the following values to achieve the limit specified for the upper six MSBs of the DAC codes. 00h: 007Fh 01h: 00FFh 02h: 017Fh 03h: 01FFh 04h: 027Fh 05h: 02FFh 06h: 037Fh 07h: 03FFh 08h: 047Fh 09h: 04FFh 0Ah: 057Fh 0Bh: 05FFh 0Ch: 067Fh 0Dh: 06FFh 0Eh: 077Fh 0Fh: 07FFh 10h: 087Fh 11h: 08FFh 12h: 097Fh 13h: 09FFh 14h: 0A7Fh 15h: 0AFFh 16h: 0B7Fh 17h: 0BFFh 18h: 0C7Fh 19h: 0CFFh 1Ah: 0D7Fh 1Bh: 0DFFh 1Ch: 0E7Fh 1Dh: 0EFFh 1Eh: 0F7Fh 1Fh: 0FFFh 20h: 107Fh 21h: 10FFh 22h: 117Fh 23h: 11FFh 24h: 127Fh 25h: 12FFh 26h: 137Fh 27h: 13FFh 28h: 147Fh 29h: 14FFh 2Ah: 157Fh 2Bh: 15FFh 2Ch: 167Fh 2Dh: 16FFh 2Eh: 177Fh 2Fh: 17FFh 30h: 187Fh 31h: 18FFh 32h: 197Fh 33h: 19FFh 34h: 1A7Fh 35h: 1AFFh 36h: 1B7Fh 37h: 1BFFh 38h: 1C7Fh 39h: 1CFFh 3Ah: 1D7Fh 3Bh: 1DFFh 3Ch: 1E7Fh 3Dh: 1EFFh 3Eh: 1F7Fh 3Fh: 1FFFh
5-0	DACB2_LIMITS	R/W	3Fh	

7.5.1.17 DRVEN0_EN Register (address = 50h) [reset = 0000h]

Figure 7-64. DRVEN0_EN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DRVEN0_EN_DACB3	DRVEN0_EN_DACB2	DRVEN0_EN_DACB1	DRVEN0_EN_DACB0	DRVEN0_EN_DACA3	DRVEN0_EN_DACA2	DRVEN0_EN_DACA1	DRVEN0_EN_DACA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-72. DRVEN0_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DRVEN0_EN_DACB3	R/W	0h	0: Ignore DRVEN0 on DACB3 1: DRVEN0 enabled for DACB3
6	DRVEN0_EN_DACB2	R/W	0h	0: Ignore DRVEN0 on DACB2 1: DRVEN0 enabled for DACB2
5	DRVEN0_EN_DACB1	R/W	0h	0: Ignore DRVEN0 on DACB1 1: DRVEN0 enabled for DACB1
4	DRVEN0_EN_DACB0	R/W	0h	0: Ignore DRVEN0 on DACB0 1: DRVEN0 enabled for DACB0
3	DRVEN0_EN_DACA3	R/W	0h	0: Ignore DRVEN0 on DACA3 1: DRVEN0 enabled for DACA3
2	DRVEN0_EN_DACA2	R/W	0h	0: Ignore DRVEN0 on DACA2 1: DRVEN0 enabled for DACA2
1	DRVEN0_EN_DACA1	R/W	0h	0: Ignore DRVEN0 on DACA1 1: DRVEN0 enabled for DACA1
0	DRVEN0_EN_DACA0	R/W	0h	0: Ignore DRVEN0 on DACA0 1: DRVEN0 enabled for DACA0

7.5.1.18 DRVEN1_EN Register (address = 51h) [reset = 0000h]

Figure 7-65. DRVEN1_EN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
DRVEN1_EN_DACB3	DRVEN1_EN_DACB2	DRVEN1_EN_DACB1	DRVEN1_EN_DACB0	DRVEN1_EN_DACA3	DRVEN1_EN_DACA2	DRVEN1_EN_DACA1	DRVEN1_EN_DACA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-73. DRVEN1_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DRVEN1_EN_DACB3	R/W	0h	0: Ignore DRVEN1 on DACB3 1: DRVEN1 enabled for DACB3
6	DRVEN1_EN_DACB2	R/W	0h	0: Ignore DRVEN1 on DACB2 1: DRVEN1 enabled for DACB2
5	DRVEN1_EN_DACB1	R/W	0h	0: Ignore DRVEN1 on DACB1 1: DRVEN1 enabled for DACB1
4	DRVEN1_EN_DACB0	R/W	0h	0: Ignore DRVEN1 on DACB0 1: DRVEN1 enabled for DACB0
3	DRVEN1_EN_DACA3	R/W	0h	0: Ignore DRVEN1 on DACA3 1: DRVEN1 enabled for DACA3
2	DRVEN1_EN_DACA2	R/W	0h	0: Ignore DRVEN1 on DACA2 1: DRVEN1 enabled for DACA2
1	DRVEN1_EN_DACA1	R/W	0h	0: Ignore DRVEN1 on DACA1 1: DRVEN1 enabled for DACA1
0	DRVEN1_EN_DACA0	R/W	0h	0: Ignore DRVEN1 on DACA0 1: DRVEN1 enabled for DACA0

7.5.1.19 FLEXIO_EN Register (address = 52h) [reset = 0000h]

Figure 7-66. FLEXIO_EN Register

15	14	13	12	11	10	9	8
RESERVED							
R-0h							
7	6	5	4	3	2	1	0
FLEXIO_EN_DACB3	FLEXIO_EN_DACB2	FLEXIO_EN_DACB1	FLEXIO_EN_DACB0	FLEXIO_EN_DACA3	FLEXIO_EN_DACA2	FLEXIO_EN_DACA1	FLEXIO_EN_DACA0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h

Table 7-74. FLEXIO_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FLEXIO_EN_DACB3	R/W	0h	0: Ignore FLEXIO on DACB3 1: FLEXIO enabled for DACB3
6	FLEXIO_EN_DACB2	R/W	0h	0: Ignore FLEXIO on DACB2 1: FLEXIO enabled for DACB2
5	FLEXIO_EN_DACB1	R/W	0h	0: Ignore FLEXIO on DACB1 1: FLEXIO enabled for DACB1
4	FLEXIO_EN_DACB0	R/W	0h	0: Ignore FLEXIO on DACB0 1: FLEXIO enabled for DACB0
3	FLEXIO_EN_DACA3	R/W	0h	0: Ignore FLEXIO on DACA3 1: FLEXIO enabled for DACA3
2	FLEXIO_EN_DACA2	R/W	0h	0: Ignore FLEXIO on DACA2 1: FLEXIO enabled for DACA2
1	FLEXIO_EN_DACA1	R/W	0h	0: Ignore FLEXIO on DACA1 1: FLEXIO enabled for DACA1
0	FLEXIO_EN_DACA0	R/W	0h	0: Ignore FLEXIO on DACA0 1: FLEXIO enabled for DACA0

7.6 DAC Buffer Register Map

Table 7-75. Page 4: DAC Buffer Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40	DACA0	R/W	0000	RESERVED			DAC[12:0]												
41	DACA1	R/W	0000	RESERVED			DAC[12:0]												
42	DACA2	R/W	0000	RESERVED			DAC[12:0]												
43	DACA3	R/W	0000	RESERVED			DAC[12:0]												
44	DACB0	R/W	0000	RESERVED			DAC[12:0]												
45	DACB1	R/W	0000	RESERVED			DAC[12:0]												
46	DACB2	R/W	0000	RESERVED			DAC[12:0]												
47	DACB3	R/W	0000	RESERVED			DAC[12:0]												

7.6.1 DAC Buffer Data Registers: Page 4

7.6.1.1 DACA/Bn Buffer Registers (address = 40h to 47h) [reset = 0000h]

Figure 7-67. DACA/B*n* Buffer Register

15	14	13	12	11	10	9	8
RESERVED			DAC[12:8]				
R-0h			R/W-0h				
7	6	5	4	3	2	1	0
DAC[7:0]							
R/W-0h							

Table 7-76. DACA/B*n* Buffer Register Field Descriptions

Bit	Field	Type	Reset	Description
12-0	DAC	R/W	0h	Stores 13-bit data to be loaded to DACn active register, in MSB-aligned, unipolar binary format.

7.7 DAC Active Register Map

Table 7-77. Page 6: DAC Active Register Map

ADDR (HEX)	REGISTER	TYPE	RESET (HEX)	BIT DESCRIPTION															
				15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
40	DACA0	R	0000	RESERVED			DAC[12:0]												
41	DACA1	R	0000	RESERVED			DAC[12:0]												
42	DACA2	R	0000	RESERVED			DAC[12:0]												
43	DACA3	R	0000	RESERVED			DAC[12:0]												
44	DACB0	R	0000	RESERVED			DAC[12:0]												
45	DACB1	R	0000	RESERVED			DAC[12:0]												
46	DACB2	R	0000	RESERVED			DAC[12:0]												
47	DACB3	R	0000	RESERVED			DAC[12:0]												

7.7.1 DAC Active Data Registers: Page 4

7.7.1.1 DACA/Bn Active Register (address = 40h to 47h) [reset = 0000h]

Figure 7-68. DACA/B*n* Active Registers

15	14	13	12	11	10	9	8
RESERVED			DAC[12:8]				
R-0h			R-0h				
7	6	5	4	3	2	1	0
DAC[7:0]							
R-0h							

Table 7-78. DACA/B*n* Active Register Field Descriptions

Bit	Field	Type	Reset	Description
12-0	DAC	R	0h	Stores 13-bit data to be loaded to DACn channel in MSB-aligned, unipolar binary format.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The primary application of the AFE20408 device is to provide power amplifier (PA) gate-bias control. The integrated switches allow the gate bias to be switched between a temperature-adjusted *on voltage* and a static, lower-potential *off voltage*.

In addition, the AFE20408 has features to detect alarm conditions, and in response, lower the gate voltages and turn off the PA during these events.

8.1.1 Output Switching Timing

The externally applied output capacitors allow for noise filtering, and enable fast switching on the output channels of the device. Large capacitors can be connected to the output of the static channels: DACA0, DACA1, DACA2, DACA3 on group A, and DACB0, DACB1, DACB2, DACB3 on group B. Capacitors of lower values can be connected to the dynamic channels, OUTA0, OUTA2, OUTB0, and OUTB2. This capacitor arrangement means that the larger capacitors can quickly charge the smaller capacitors instead of relying on the DAC output buffers.

Figure 8-1 shows a simplified model of switch arrangement for the OUTA0 channel. The on-resistance of the switches are represented by R_{SW1} and R_{SW2}. These resistors primarily serve to limit the settling time of V_{OUTA1} after a switching event, as the settling time is essentially an RC function.

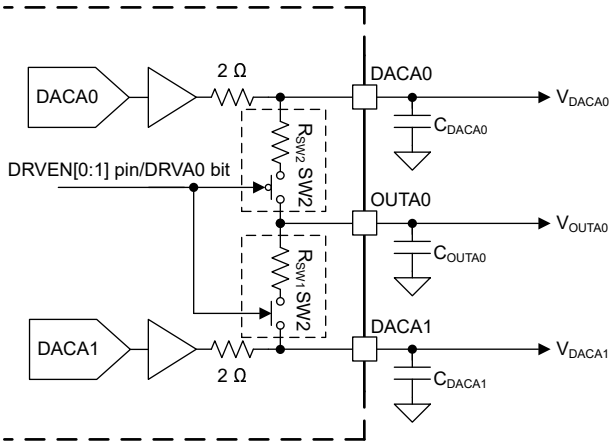


Figure 8-1. Switching Transients

For example, consider the case where DRVEN0 changes from a low-state to a high-state. The steady-state of V_{DACA0} is equal to V_{DACA1} before the switch event. After the DRVEN pin goes high, SW2 closes, connecting C_{OUTA1} and C_{DACA0} to each other. As these capacitors are now in parallel, the voltages across each equalize to a new voltage. This voltage, described as $V_{CDAC||COUT}$ in the following equation, can be calculated by finding the charge stored in each capacitor. The total charge on the two capacitors in parallel is equal to the sum of the charge of each capacitor.

$$Q_{CDAC||COUT} = Q_{CDAC} + Q_{COUT} \tag{2}$$

$$V_{CDAC||COUT}(C_{DACA1} + C_{OUTA0}) = V_{DACA1} \times C_{DACA1} + V_{OUTA0} \times C_{OUTA0} \tag{3}$$

$$V_{CDAC||COUT} = \frac{V_{DACA1} \times C_{DACA1} + V_{OUTA0} \times C_{OUTA0}}{(C_{DACA1} + C_{OUTA0})} \tag{4}$$

The time required for the two output to equalize, described as the *Capacitive Settling Period*, is calculated using the equation below. As DACA0 is lower potential than DACA1, V_{OUTA0} can be expressed as a charging function.

$$V_{OUTA0}(t) = \left(V_{CDAC||COUT} - V_{OUTA0}(t_0)\right)\left(1 - e^{\frac{-t}{R_{SW1} \times C_{OUTA0}}}\right) + V_{OUTA0}(t_0) \tag{5}$$

During the capacitive settling period, V_{DACA1} is expressed as a discharging RC function.

$$V_{DACA1}(t) = V_{DACA1}(t_0) - \left(V_{DACA1}(t_0) - V_{CDAC||COUT}\right)\left(1 - e^{\frac{-t}{R_{SW1} \times C_{OUTA0}}}\right) \tag{6}$$

Connecting the capacitors together allows the output to change to $V_{CDAC||COUT}$ quickly, but after that period, the DAC output buffer continues to charge C_{OUTA1} to the V_{DACA0} value. The settling time for that final transition depends on the RC function formed by the series resistance on the DAC output, the switch resistance, and the capacitive load on the DAC. In addition, the output current of the DAC is limited.

Figure 8-2 shows the switch response for the OUTA0 pin when switching from a static DAC channel to VSS, while Figure 8-3 shows the switch response of the OUTA0 signal when switching between static DAC outputs.

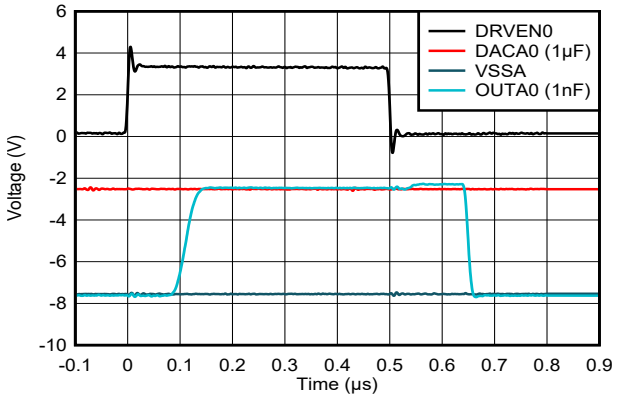


Figure 8-2. DAC-to-VSS Switch Response

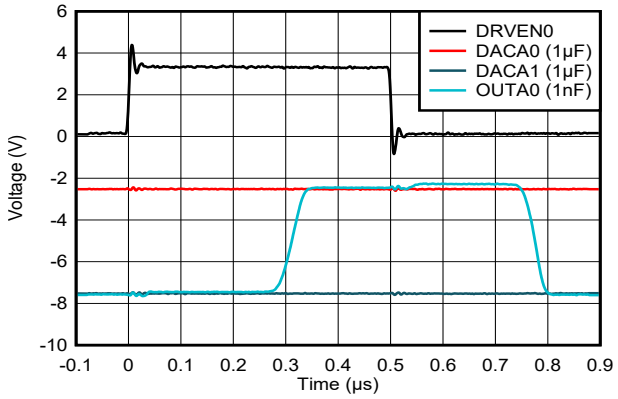


Figure 8-3. DAC-to-DAC Switch Response

8.2 Typical Application

Figure 8-4 shows an example schematic for PA biasing applications, using a single AFE20408 device to bias GaN and LDMOS PAs simultaneously. In this application, DAC group A is configured in a negative output range, while DAC group B is configured in positive output range.

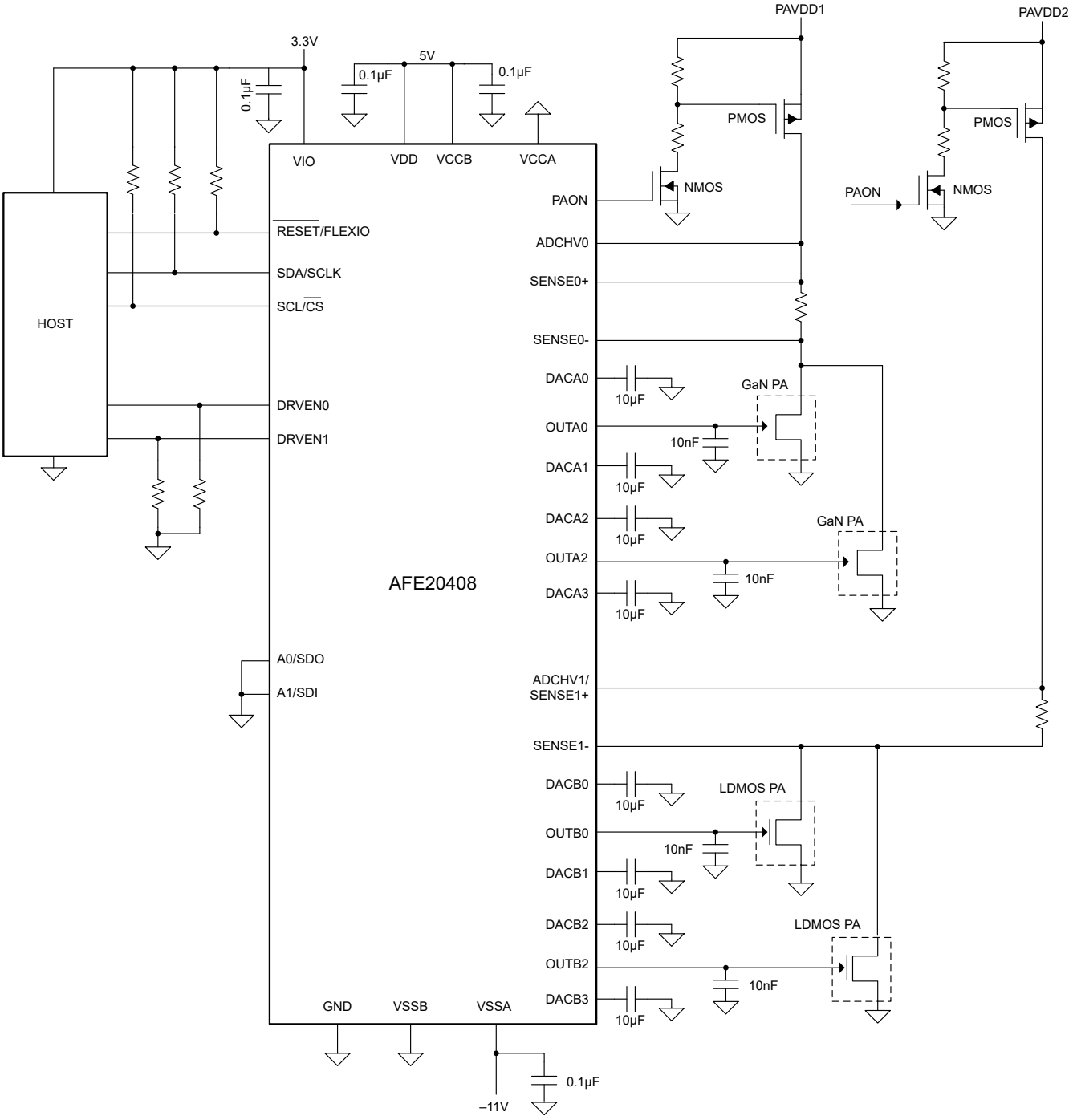


Figure 8-4. Power Amplifier Biasing Application

8.2.1 Design Requirements

The example schematic uses the majority of the design parameters listed in Table 8-1. The power supplies and DAC outputs are configured for the mixed output range.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CCA}	Grounded
V_{CCB}	11V
V_{SSA}	–11V
V_{SSB}	Grounded
V_{DD}	5V
V_{IO}	1.8V
DAC outputs	Group A selectable ranges: –10V to 0V
	Group B selectable ranges: 0V to 10V

8.2.2 Detailed Design Procedure

8.2.2.1 ADC Input Conditioning

The ADC inputs feature an input range that can be configured as either 0V to 2.5V or 0V to 5V.

To reduce ADC sample glitch, place a 470pF capacitor on the ADC input. By adding small series resistors (in series with the ADC inputs) a low-pass noise filter can be implemented, as shown in Figure 8-5.

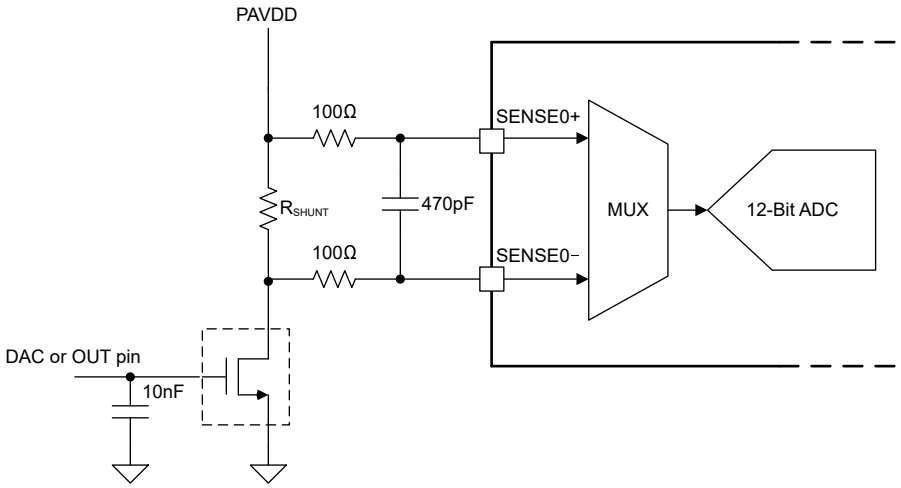


Figure 8-5. ADC Input Conditioning

8.2.2.2 Quiescent Current and Total Power Consumption

Calculating the total power consumption of the device requires all of the supply inputs and DAC loads to be known. Equation 7 calculates the total power, Each component is the power contributed by a supply or DAC loads.

$$P_{TOTAL} = P_{IO} + P_{DD} + P_{CC} + P_{SS} + P_{DAC-LOAD} \quad (7)$$

where

- P_{IO} is the power consumed by the device from the V_{IO} supply:

$$P_{IO} = V_{IO} \times I_{IO-quiescent} \quad (8)$$

- P_{DD} is the power consumed by the device from the V_{DD} supply:

$$P_{DD} = V_{DD} \times I_{DD-quiescent} \quad (9)$$

- P_{CC} is the power consumed by the device from the V_{CC} supply:

$$P_{CC} = V_{CC} \times I_{CC-quiescent} \quad (10)$$

- P_{SS} is the power consumed by the device from the V_{SS} supply:

$$P_{SS} = V_{SS} \times I_{SS-quiescent} \quad (11)$$

- $P_{DAC-LOAD}$ is the power consumed by the device as a result of the DAC loads from the sourcing or sinking supply. The power of each DAC channel can be calculated separately, then summed to find the total power of the DAC loads. The power depends not only on the voltage of the DAC output, but also on the difference between the current sourcing or sinking supply and the DAC output voltage. The following equation shows how to calculate $P_{DAC-LOAD}$:

$$P_{DAC-LOAD} = \sum_{channel\ n=0}^{n} V_{SUPPLY-LOAD} \times I_{LOAD} \quad (12)$$

Figure 8-6 shows the load configuration in both the positive output range and negative output range.

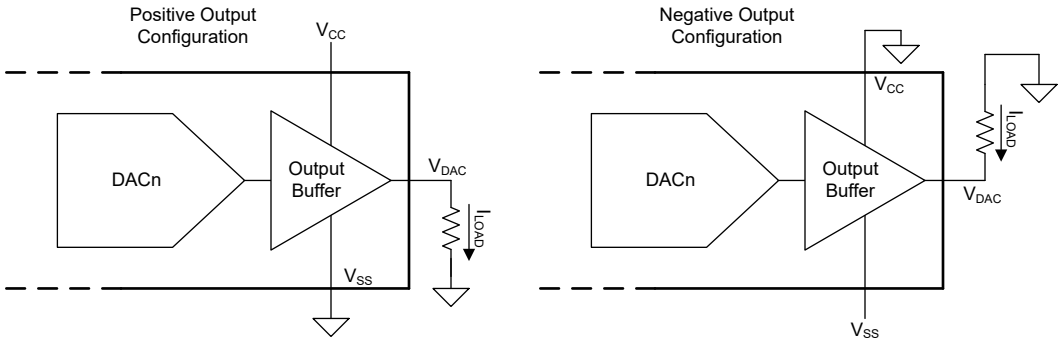


Figure 8-6. DAC Output Load

When the device is in the positive output range, the device is likely sourcing current. While in the negative range, the device is likely sinking current. The difference between the supply voltage and the DAC output voltage is $V_{SUPPLY-LOAD}$, as shown in the following equations.

When the device is in the positive output range, $V_{SUPPLY-LOAD}$ can be calculated as:

$$V_{SUPPLY-LOAD} = V_{CC} - V_{DAC} \quad (13)$$

When the device is in the negative output range, $V_{SUPPLY-LOAD}$ can be calculated as:

$$V_{SUPPLY-LOAD} = V_{SS} - V_{DAC} \quad (14)$$

8.2.2.2.1 Maximum VCC/VSS Supply Current Transients

In many applications, the DAC outputs of the device have a capacitive load. When the DAC outputs transition from one output voltage to another, the short-circuit limit protection can be triggered. If the DAC output buffer reaches the short-circuit current limit of the amplifier, significant current is drawn from the output amplifier supply. Equation 15 shows how to calculate the estimated maximum current that is demanded of the supply during the transition.

$$I_{VCC-MAX} = I_{VCC-quiescent} + \sum_{channel\,n=0}^{n} I_{SHORT-CIRCUIT-LIMIT} \quad (15)$$

8.2.2.2.2 DAC Load Stability

Figure 8-7 shows the required configuration when capacitive loads are present on the DAC output. No series resistor is required on the DAC output, as the DAC is able to prevent oscillation issues on the output amplifier.

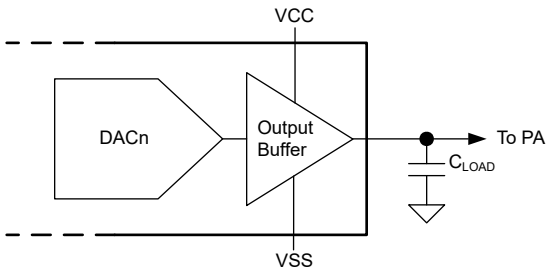


Figure 8-7. DAC Output Load

8.2.2.3 Disabling PA Drain Voltage

The PAVDD voltage is separated from the drain voltage of the power amplifier with a series PMOS transistor. The activation of the PMOS transistor connects the PAVDD voltage supply to the drain pin of the power amplifier. The PMOS transistor is driven with a voltage divider that swings from PAVDD to PAVDD(R2 / (R1 + R2)). The NMOS transistor shown in Figure 8-4 is connected to the PAON output of the AFE20408. When PAON is low, the PMOS gate is equal to the PAVDD voltage, disconnecting the PAVDD voltage from the PA. When PAON is high, the voltage divider turns on and enables the PMOS, connecting the PAVDD voltage to the PA.

8.2.2.4 PAON External Circuit

During start-up, the AFE20408 PAON is Hi-Z until all power supplies are established. When operating in push-pull mode, a pull-down resistor to ground is recommended to keep the PAON output from floating. When operating in open-drain mode, the PAON output is to be isolated from the pullup resistor to V_{DD}, until all power has been applied. Figure 8-8 shows a dual NMOS circuit that grounds the PAON output until both V_{DD} and V_{IO} are powered to an operating voltage, after which the PAON output operates as a pullup to V_{DD}.

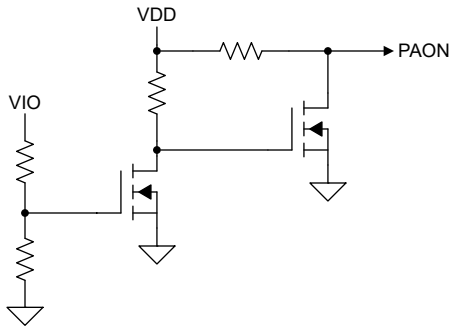
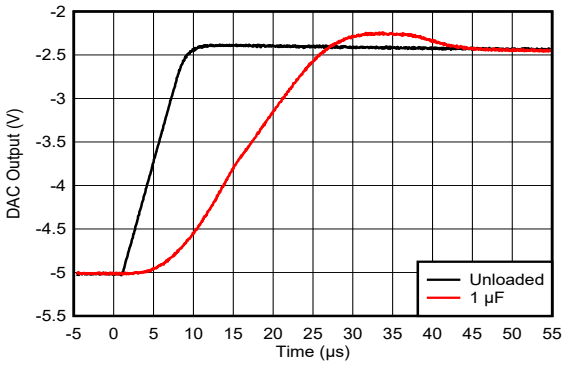


Figure 8-8. PAON Open-Drain Circuit

8.2.3 Application Curves

8.2.3.1 DAC Load Stability

Figure 8-9 shows the DAC output response when the DAC is unloaded, and when the DAC is loaded with a capacitor, respectively.



DAC step size: –5V to –2.5V

Figure 8-9. DAC Settling Time vs Load Capacitance

8.2.3.2 Start-Up Behavior

The AFE20408 is designed to minimize DAC output glitch during power supply transients at power-on and power-down. Figure 8-10 to Figure 8-13 detail this behavior.

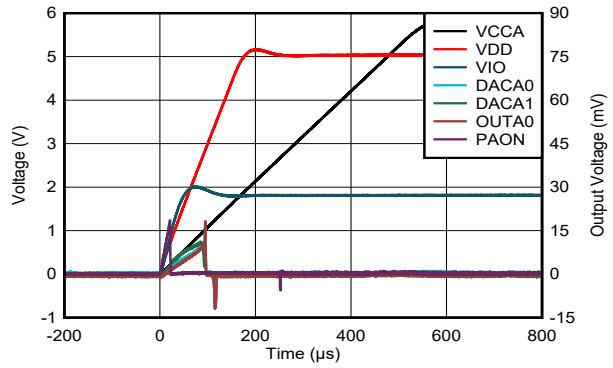


Figure 8-10. DAC Output During V_{CC} Power-On Transient

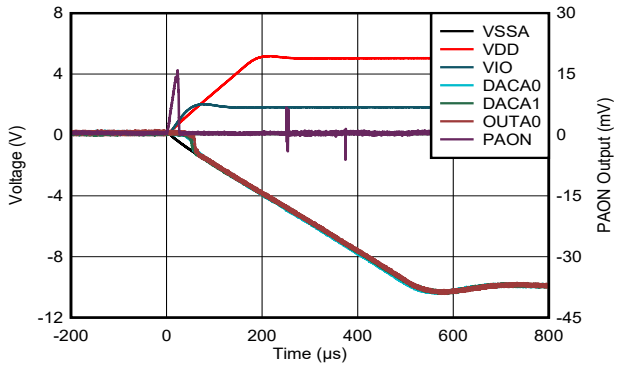


Figure 8-11. DAC Output During V_{SS} Power-On Transient

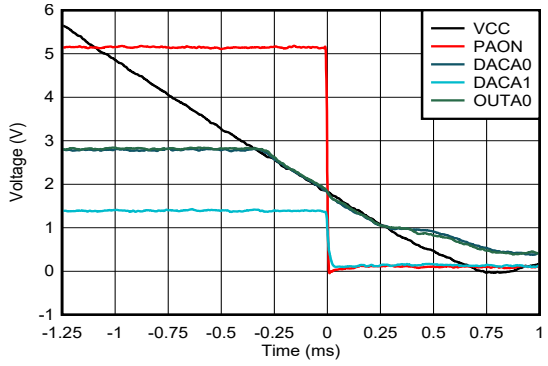


Figure 8-12. DAC Output During V_{CC} Power-Down Transient

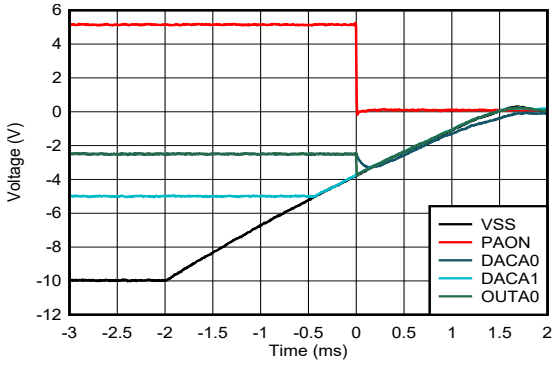


Figure 8-13. DAC Output During V_{SS} Power-Down Transient

8.3 Initialization Setup

After power-up, the device can be configured over the serial interface. The following steps can be used in a typical configuration.

1. After the supplies have ramped to the final output voltage, issue a hardware or software reset to make sure the device is in a known state. Allow approximately 5ms for the device registers to initialize after the reset event
2. Write to the ADC_CONV_CFG_0 and ADC_GEN_CFG registers (in the ADC configuration register page) to set the ADC conversion rate, conversion mode, and shunt range.
3. Configure the ADC inputs and custom channel sequencer (CCS), by writing to the ADC_CCS_IDS registers and the ADC_CCS_CFG_0 register (located in the ADC CCS Configuration register page).
4. Set the DAC current limits by writing to the DAC_CURRENT register in the DAC Configuration register page.
5. Initialize the DACs by configuring the DAC_APD_SRC registers, the OUT_APD_SRC registers, the ALARMOUT_SRC registers, the DAC DRVEN_EN registers, and the DAC_CODE_LIMIT registers (all located in the DAC Configuration register page).
6. Set the ADC and temperature sensor alarm limits by writing to the ADCn_UP_THRESH, ADCn_LOW_THRESH and TMP_UP_THRESH registers in the ADC Configuration register page (where n = 0,1).
7. Write the initial DAC output values by writing to the DACAn or DACBn data registers (where n = 0,1,2,3).
8. Enable the DACs by writing to the power enable (PWR_EN) register in the global register page.
9. Initiate a single (or multiple) ADC conversion by writing to the ADC_TRIG bit in the TRIGGER register (located in the global register page).
10. Update the DAC output values by writing to the DAC_TRIG bit in the TRIGGER register, if using synchronous mode on the respective DAC.

8.4 Power Supply Recommendations

There is no required supply sequence, but be aware that the device stays in the reset state until all supplies reach the power-good threshold. Also, a hardware or software reset to the device is recommended after the supplies reach the power-good threshold, so that the device can initialize in a known state. Following this reset (or any reset event) wait at least 5ms so that the device registers can properly initialize.

In applications where a negative voltage is applied to V_{SS} first, some small negative voltages can be present at other supply pins, such as the V_{IO} and V_{DD}. The negative voltages at the supply pins can exceed the values listed in *Section 5.1*, but because these voltages are created from intrinsic circuitry, the voltage levels are safe for operation.

8.5 Layout

8.5.1 Layout Guidelines

- Bypass all power supply pins to ground with a low-ESR ceramic bypass capacitor. Bypass capacitors on the V_{CCx} and V_{SSx} inputs are recommended to be three to four times the total capacitance on the respective group DAC outputs to make sure the inrush current does not cause localized supply collapse when the outputs transition to different voltage output. The typical recommended bypass capacitor has a value of 1µF and is ceramic with X7R or NP0 dielectric.
- Place capacitors on the DAC[0:3], OUT0, and OUT2 pins as close to the device as possible. This placement reduces the impact of parasitic inductance and resistance from the switching path. Parasitic inductance and resistance delays the output settling time.
- Connect the thermal pad on the device to a large copper area, preferably a ground plane.
- When using the local temperature sensor for the output bias voltage temperature compensations, place the device geographically close to the PA, preferably sharing a solid ground plane for thermal conduction.

8.5.2 Layout Diagram

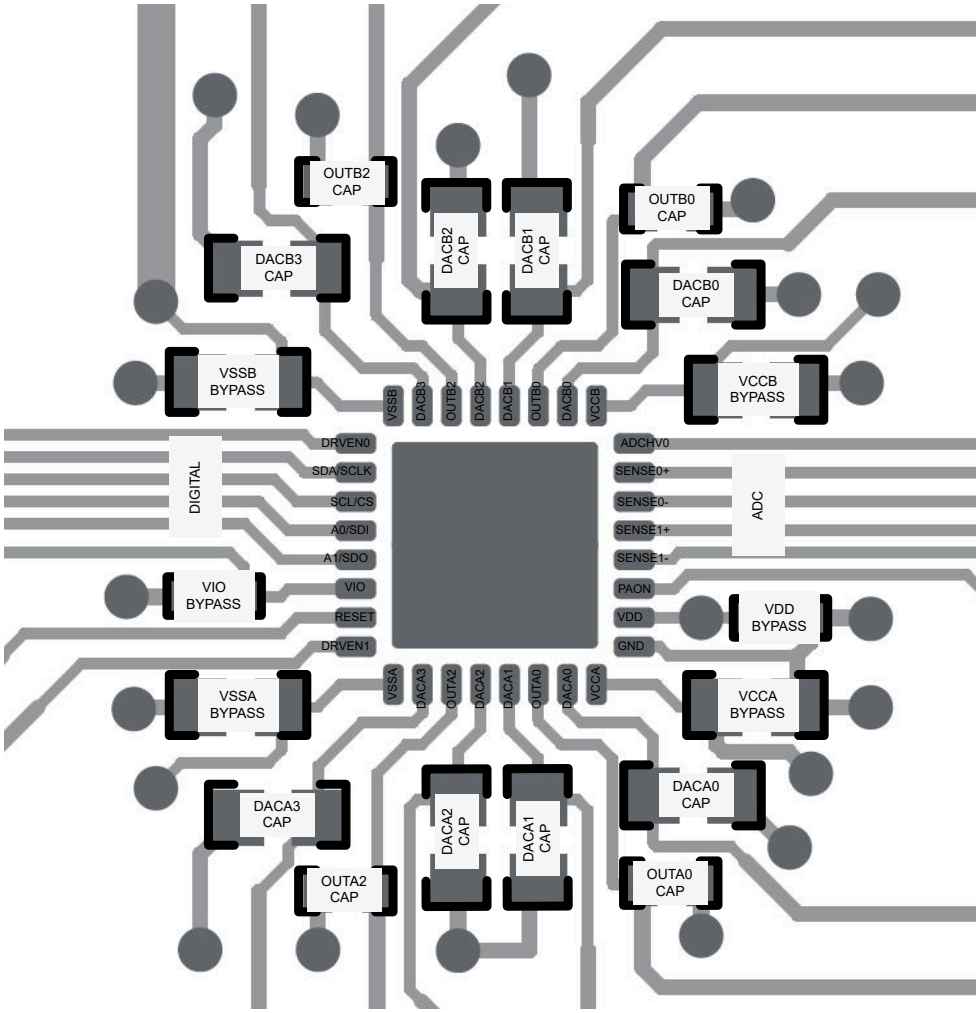


Figure 8-14. AMC20408 Layout

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, AFE20408EVM user's guide

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.

9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
April 2024	*	Initial release.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated device(s). These data are subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AFE20408RHBT	ACTIVE	VQFN	RHB	32	250	RoHS & Green	NIPDAUAG	Level-3-260C-168 HR	-40 to 125	AFE 20408	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

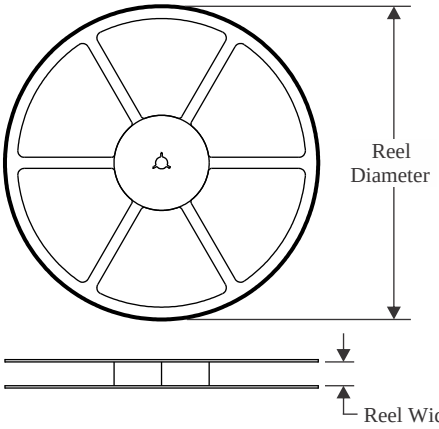
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

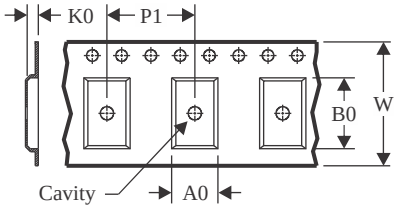
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

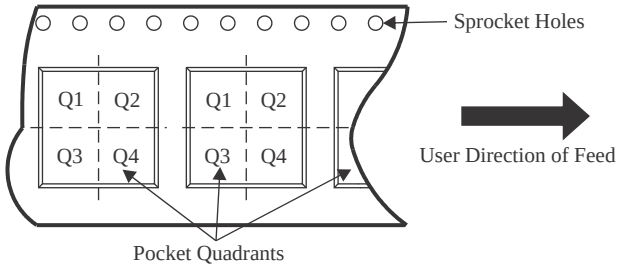


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

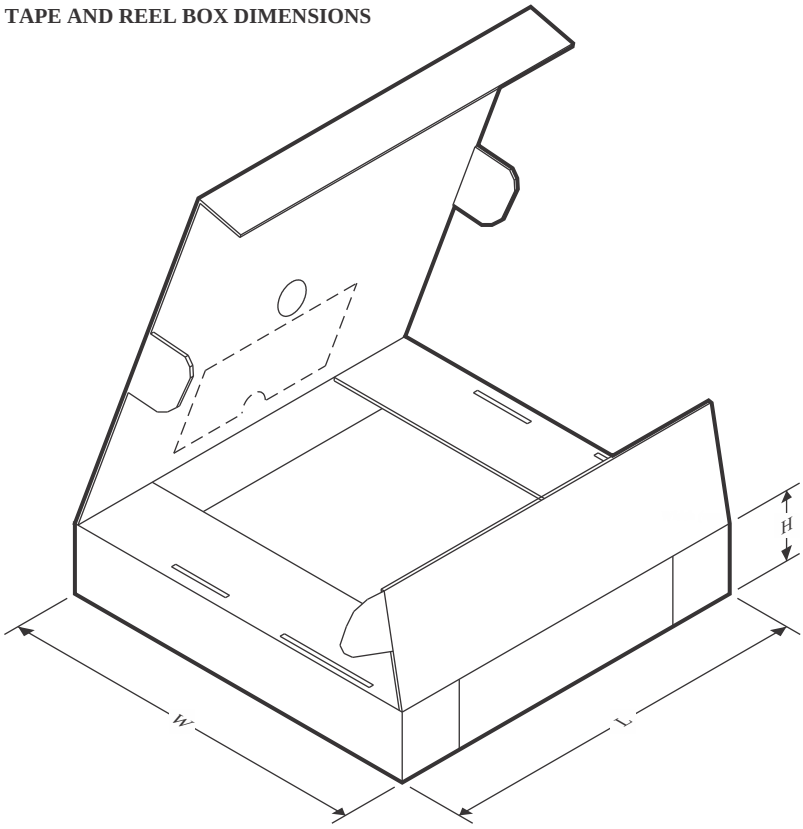
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AFE20408RHBT	VQFN	RHB	32	250	180.0	12.4	5.25	5.25	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AFE20408RHBT	VQFN	RHB	32	250	213.0	191.0	35.0

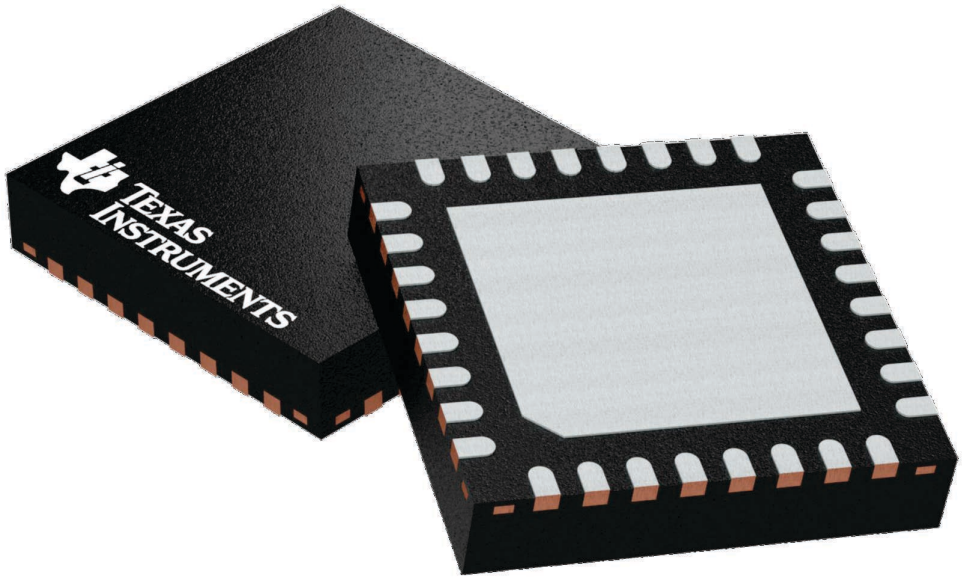
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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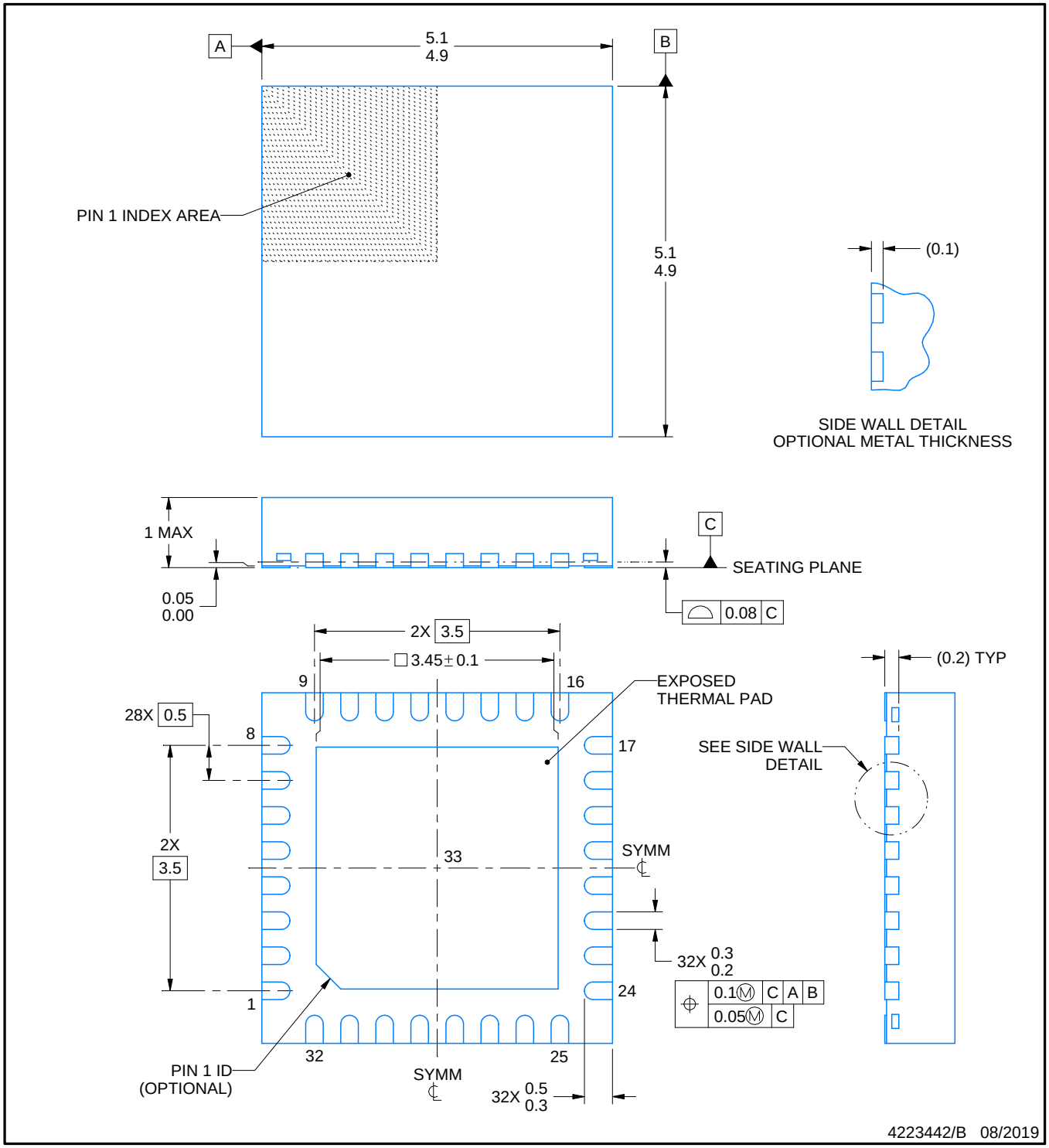
RHB0032E

PACKAGE OUTLINE

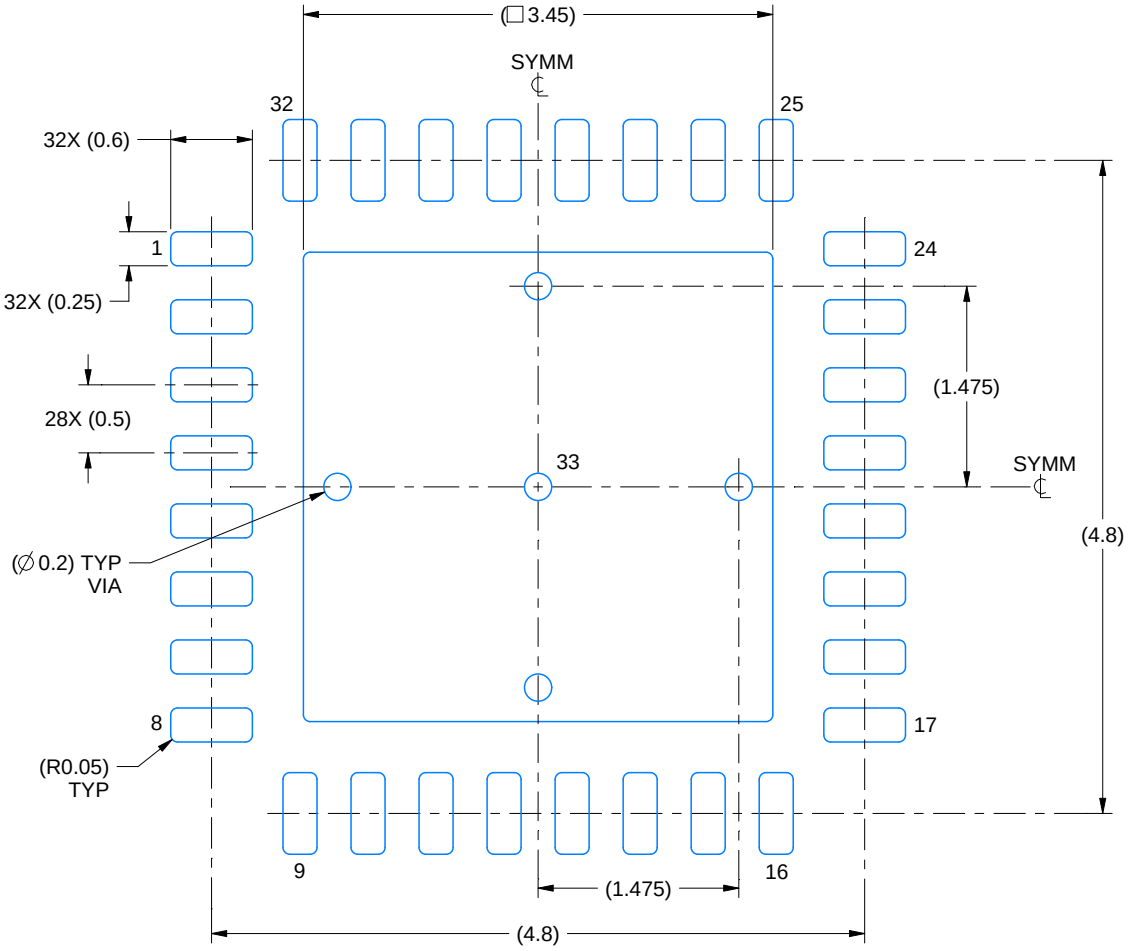
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

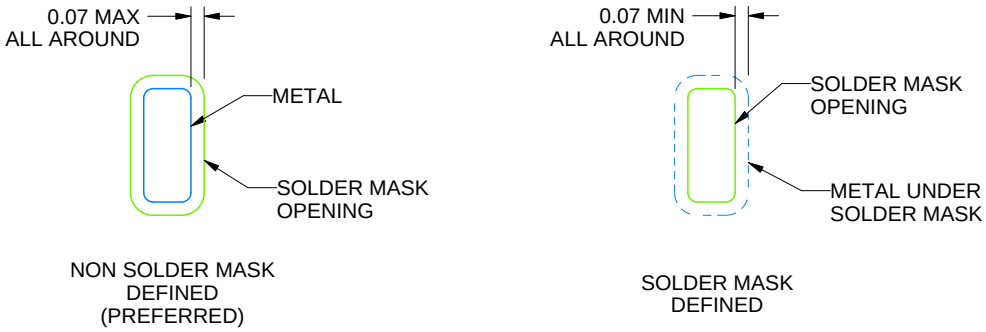


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X



SOLDER MASK DETAILS

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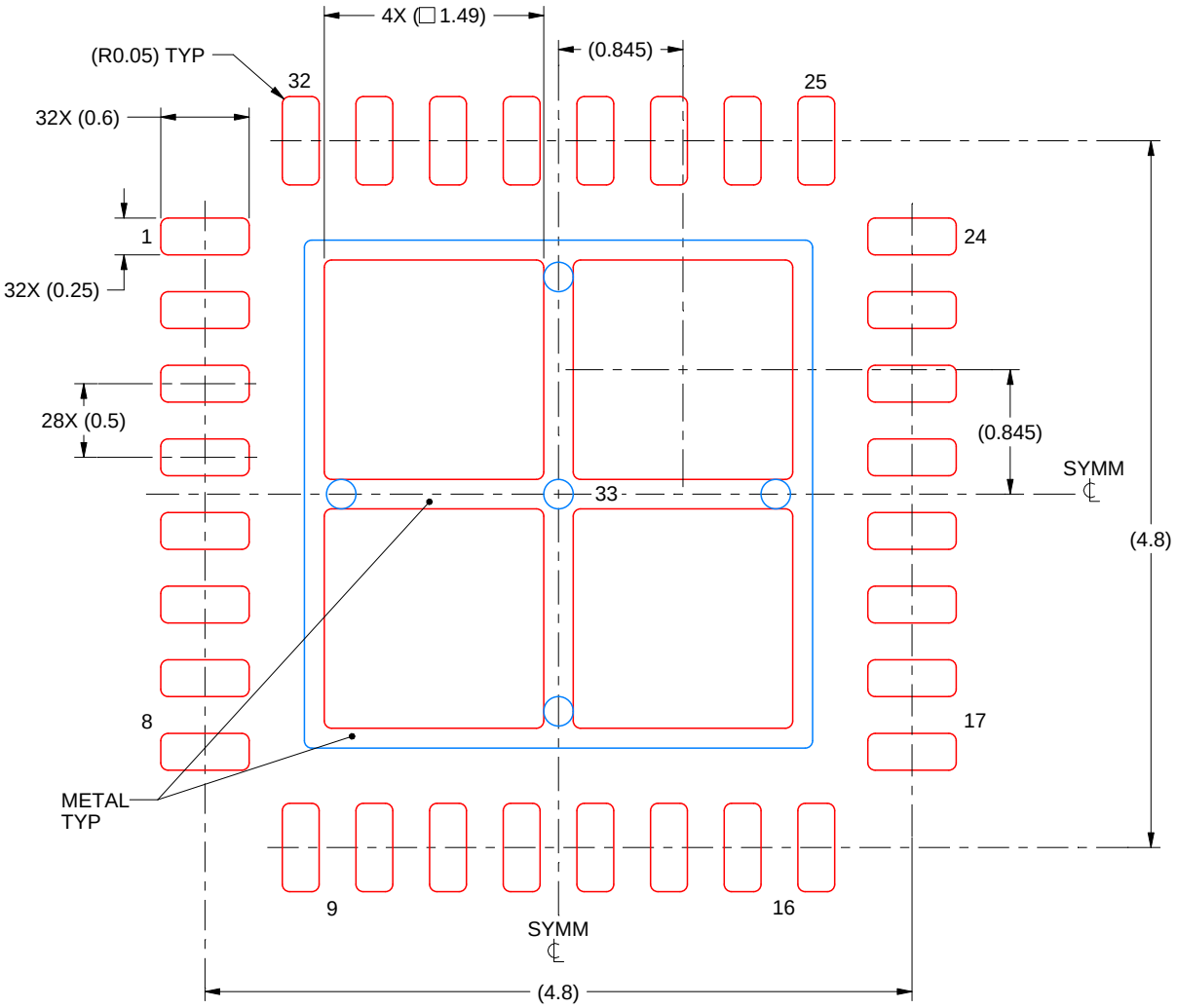
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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