







AFE7769D, AFE7728D, AFE7768D SBASAG3A - JULY 2023 - REVISED OCTOBER 2023

AFE77xxD Quad/Dual-Channel RF Transceiver With Dual Feedback Paths Integrating CFR/DPD

1 Features

- Quad (AFE776xD) / Dual (AFE7728D) transmitters based on 0-IF up-conversion architecture:
 - Up to 650 MHz (AFE77x8D) / 730 MHz (AFE7769D) of RF transmitted DPD expansion bandwidth per chain
- Quad (AFE776xD) / Dual (AFE7728D) receivers based on 0-IF down-conversion architecture:
 - Up to 200 MHz (AFE77x8D) / 300 MHz (AFE7769D) of RF received bandwidth per
- Feedback chain based on direct RF sampling architecture:
 - Up to 650 MHz (AFE77x8D) / 730 MHz (AFE7769D) of RF observed DPD expansion bandwidth
- Integrated CFR/DPD for PA linearization
 - Up to 200MHz (AFE77x8D) / 300MHz (AFE7769D) instantaneous bandwidth
 - Up to 650MHz (AFE77x8D) / 730MHz (AFE7769D) DPD expansion bandwidth
- Integrated CFR/DPD for PA linearization
 - Multistage CFR with configurable cancelling
 - Hardware accelerated DPD estimation engine
 - Signal Dynamics based corrector for GaN PA linearization
 - Smart data capture
- RF frequency range: 600 MHz to 6 GHz
- Four wideband fractional-N PLL, VCO for TX and RX LO
- Dedicated integer-N PLL, VCO for data converters clock generation
- JESD204B and JESD204C SerDes interface support:
 - 4 SerDes transceivers up to 29.5 Gbps
 - 8b/10b and 64b/66b encoding
 - 16-bit, 12-bit, 24-bit and 32-bit formatting
 - Subclass 1 multi-device synchronization
- Package: 17-mm × 17-mm FCBGA, 0.8-mm pitch

2 Applications

- Macro remote radio unit (RRU)
- Small cell base station
- Active antenna system mMIMO (AAS)
- Distributed Antenna Systems (DAS)
- Repeater

3 Description

The AFE77xxD is a pin-compatible family of highperformance, multichannel transceivers, integrating four (AFE7768D/AFE7769D) or two (AFE7728D) up-conversion transmitter chains, (AFE7768D/AFE7769D) or two (AFE7728D) direct down-conversion receiver chains, two wideband RF sampling digitizing auxiliary chains (feedback paths) and low-power Digital Pre-Distortion (DPD) engine for Power Amplifier (PA) linearization. The high dynamic range of the transmitter and receiver chains enables wireless base stations to transmit and receive 2G, 3G, 4G, and 5G signals. The integrated Crest Factor Reduction (CFR) unit helps reduce the Peakto-Average Ratio (PAR) of the input signal for more efficient transmission through the Power Amplifier. The integrated hardware accelerated DPD estimator and corrector provides flexible and efficient DPD solution for PA linearization. The integrated DPD engine corrects the distortion due to PA nonlinearity for signals up to 200MHz (AFE77x8D) / 300MHz (AFE7769D) instantaneous bandwidth, and within up to 650MHz (AFE77x8D) / 730MHz (AFE7769D) DPD expanded bandwidth. A dedicated GaN corrector addresses the long-term nonlinear memory effects due to charge trapping of GaN PAs.

The low power dissipation and high density channel integration of the AFE77xxD allow the device to address the power and size constraints of 4G and 5G base stations. The wideband and high dynamic range feedback path can assist the DPD of the power amplifiers in the transmitter chain through smart data capture at various intercepting points. The available 29.5Gbps SerDes speed can help reduce the number of lanes required to transfer the data in and out of the device.

Package Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE ⁽²⁾
AFE77xxD	ABJ (FCBGA, 400)	17.00 mm × 17.00 mm

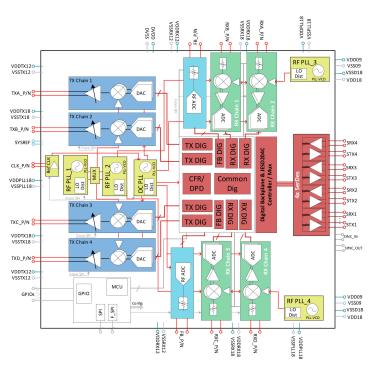
- For all available packages, see the orderable addendum at the end of the data sheet.
- The package size (length × width) is a nominal value and includes pins, where applicable.

Each receiver chain of the AFE77xxD includes a 28-dB range digital step attenuator (DSA), followed by a wideband passive IQ demodulator, and a baseband amplifier with integrated antialiasing low pass filters with programmable bandwidth, driving continuous-time sigma-delta ADCs. The RX chain can receive an instantaneous bandwidth (IBW) up to 200 MHz (AFE77x8D) / 300 MHz (AFE7769D). Each receiver channel has two analog peak power detectors and various digital power detectors to assist an external or internal autonomous AGC control for receiver channels, and a RF overload detector for device reliability protection. The integrated QMC (quadrature mismatch compensation) algorithm is capable to continuously monitor and correct for the RX chain I and Q imbalance mismatch without the need to inject any specific signals or perform offline calibration.

Each transmitter chain includes two 14-bit, 3.3-Gsps IQ DACs, followed by a programmable reconstruction and DAC image rejection filter, an IQ modulator driving a wideband RF amplifier with 39-dB range gain control. The TX chain integrated QMC and LO leakage cancellation algorithms, leveraging the FB path can constantly track and correct for the TX chain IQ mismatch and LO leakage.

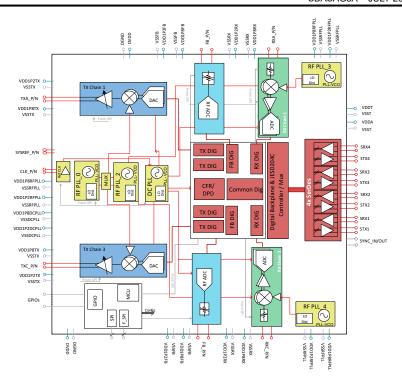
Each FB path is based on RF sampling architecture, and includes an input RF DSA driving a 14-bit, 3.3-Gsps RF ADC. The direct sampling architecture provides an inherently wideband receiver chain and simplifies the calibration of the TX chains impairments. The FB path integrates two independent NCOs, which allow for a fast switching between two observed RF input bands.

The synthesizer section integrates four fractional-N RF PLLs that can generate four different RF LOs, allowing the device to support up to two different bands, each one configured as two transmitters, two receivers, and one feedback path (with AFE7768D/AFE7769D), or one transmitter, one receiver, and one feedback path (with AFE7728D).



AFE7768D/AFE7769D Block Diagram





AFE7728D Block Diagram



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.



5 Device and Documentation Support

5.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.2 Support Resources

TI E2E[™] support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.3 Trademarks

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5.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.5 Glossary

TI Glossary

This glossary lists and explains terms, acronyms, and definitions.

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead finish/ Ball material	MSL Peak Temp	Op Temp (°C)	Device Marking (4/5)	Samples
							(6)				
AFE7728DIABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7728D	Samples
AFE7768DIABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7768D	Samples
AFE7769DIABJ	ACTIVE	FCBGA	ABJ	400	90	RoHS & Green	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7769D	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (CI) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- (3) MSL, Peak Temp. The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
- (4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.
- (5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
- (6) Lead finish/Ball material Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

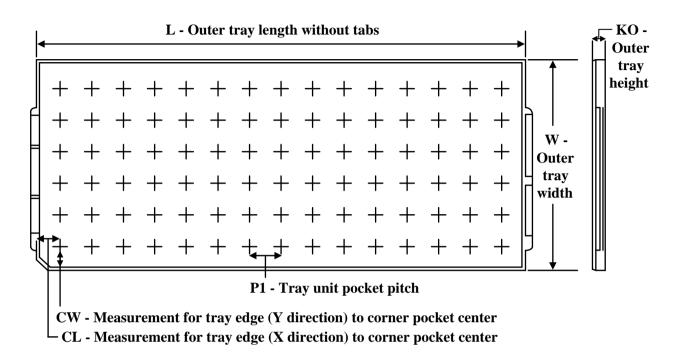
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TRAY



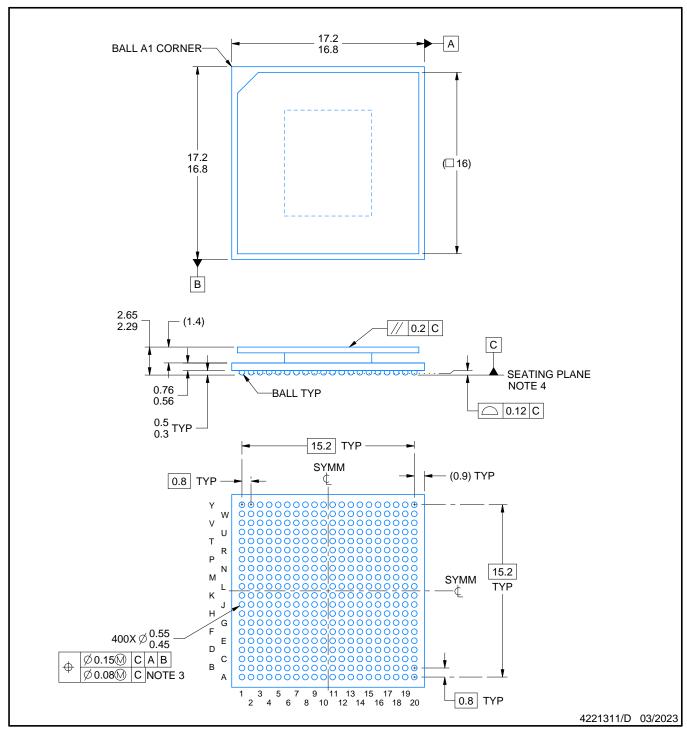
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	Κ0 (μm)	P1 (mm)	CL (mm)	CW (mm)
AFE7728DIABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7768DIABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7769DIABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2



BALL GRID ARRAY

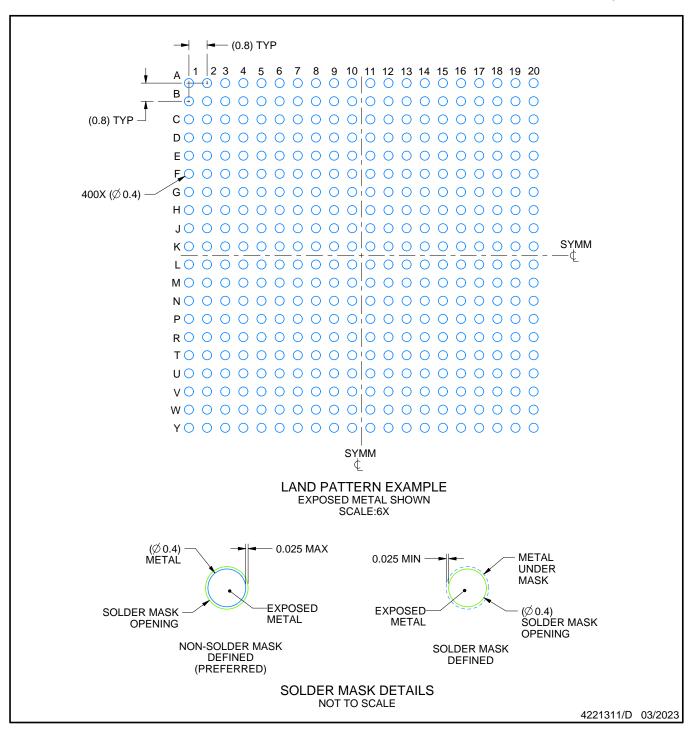


NOTES:

- 1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- 2. This drawing is subject to change without notice.
- 3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
- 4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
- 5. The lids are electrically floating (e.g. not tied to GND).



BALL GRID ARRAY

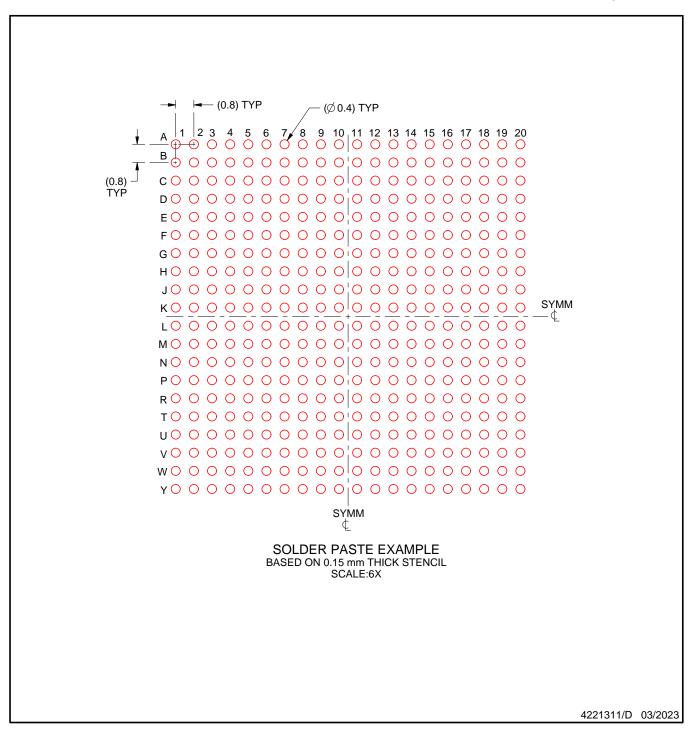


NOTES: (continued)

Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints.For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



BALL GRID ARRAY



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.



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