AFE7960: 4-Transmit, 6-Receive RF-Sampling Transceiver, 8GHz to 18GHz, Maximum 1200MHz IBW

1 Features

- Request full data sheet
- Four RF sampling 12GSPS DACs
- Six RF sampling 3GSPS ADCs
- Maximum RF signal bandwidth:
- – 4TX: 1200MHz; 2TX: 2400MHz
  – 4RX: 1200MHz; 6RX: 600MHz
- RF frequency range:
- – TX: 8GHz to 18GHz
  – RX: 8GHz to 18GHz
- Digital Up-Converters (DUC) and Digital Down-Converters (DDC): Fast frequency hopping using 16 pre-configurable Numerically Controlled Oscillators (NCOs) in DDC and DUC
- Flexible clocking options:
- – External RF clock
  – Internal PLL mode with low speed input clock
- SerDes data interface:
- – JESD204B 8b/10b and JESD204C 64b/66b
  – TX: 8 lanes, RX/FB: 8 lanes, up to 29.5Gbps
  – Subclass 1 multi-device synchronization
  – SYSREF alignment detector
- Package: 17mm × 17mm FCBGA, 0.8mm pitch

2 Applications

- Radar
- Seeker front end
- Defense radio
- Tactical communications infrastructure
- Wireless communications test
- Satellite constellation ground-stations

3 Description

The AFE7960 is a high performance, wide bandwidth multi-channel transceiver, integrating four (4T) RF sampling transmitter (TX) chains and a total of six (6R) RF sampling receivers. Out of the six receivers, four have full functionality and can be used as receive (RX) signal chains in a radio application. The other two receivers can optionally be configured as feedback (FB) receivers in a Digital pre-distortion (DPD) signal chain. Alternatively, all six can be used as receive signal chains. With operation up to 18 GHz, the AFE enables direct RF sampling in the Ku band without the need for additional frequency conversions stages. This high density and configurability enables high-channel-count, multi-mission systems.

The TX and RX interface data rates can be chosen based on signal bandwidths, and is limited by the JESD204B/C interface speed. The data streams are matched to the DAC update rate or to the ADC conversion rate using interpolation in the DUC or decimation in the DDC.

The DAC runs at a maximum rate of 12GSPS and operates in the 2nd and 3rd Nyquist, enabling the generation of RF signals up to 18GHz.

Each receive chain has a 3GSPS ADC which can convert higher Nyquist zones to digitize RF signals up to a maximum of 18GHz. Digital power detectors at the ADC output can be configured to assist an external Automatic Gain control (AGC) loop to control the RF front-end gain.

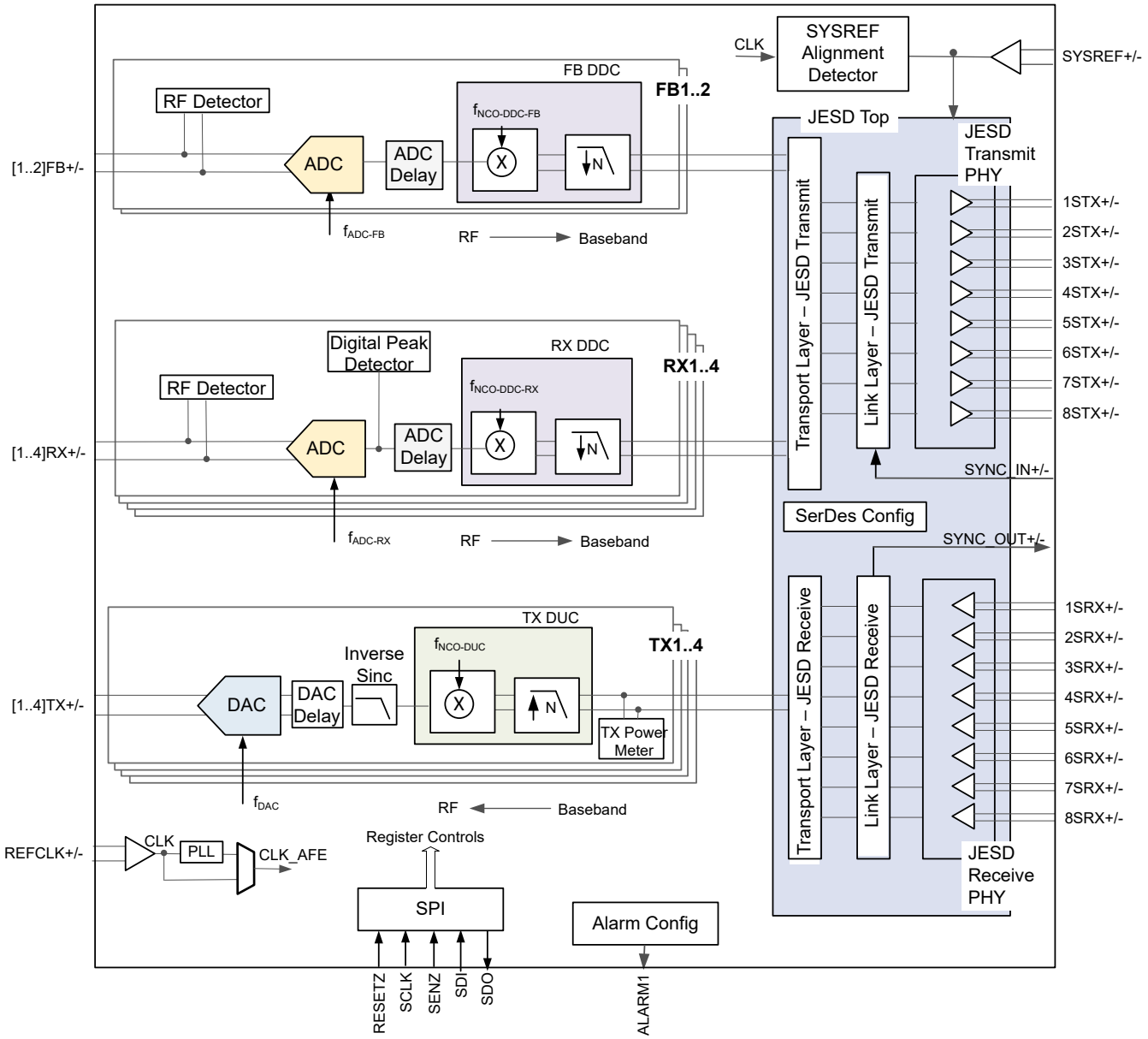
The AFE7960 can be programmed using the SPI interface. The device has programmable GPIOs that can be configured to various functions like interrupt generation, fast frequency hopping, and so forth.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AFE7960	ABJ (FC-BGA 400)	17mm × 17mm
	ALK (FC-BGA 400)	17mm × 17mm

(1) For more information, see Mechanical, Packaging, and Orderable Information section at the end of the data sheet..
(2) The package size (length × width) is a nominal value and includes pins, where applicable.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.



Functional Block Diagram

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4 Device and Documentation Support

4.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.2 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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4.3 Trademarks

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4.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2026	*	Initial Release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AFE7960IABJ	Active	Production	FCBGA (ABJ) | 400	90 | JEDEC TRAY (5+1)	Yes	SNAGCU	Level-3-260C-168 HR	-40 to 85	AFE7960
AFE7960IALK	Active	Production	FCBGA (ALK) | 400	90 | JEDEC TRAY (5+1)	No	SNPB	Level-3-220C-168 HR	-40 to 85	AFE7960 SNPB

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

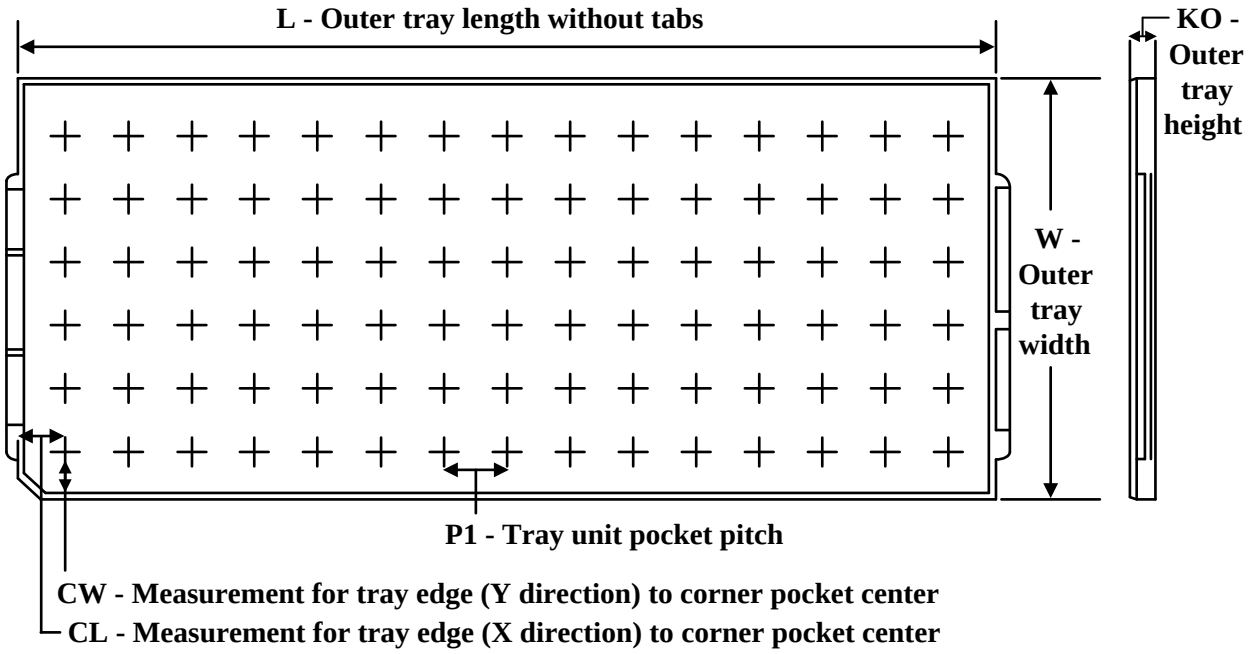
(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

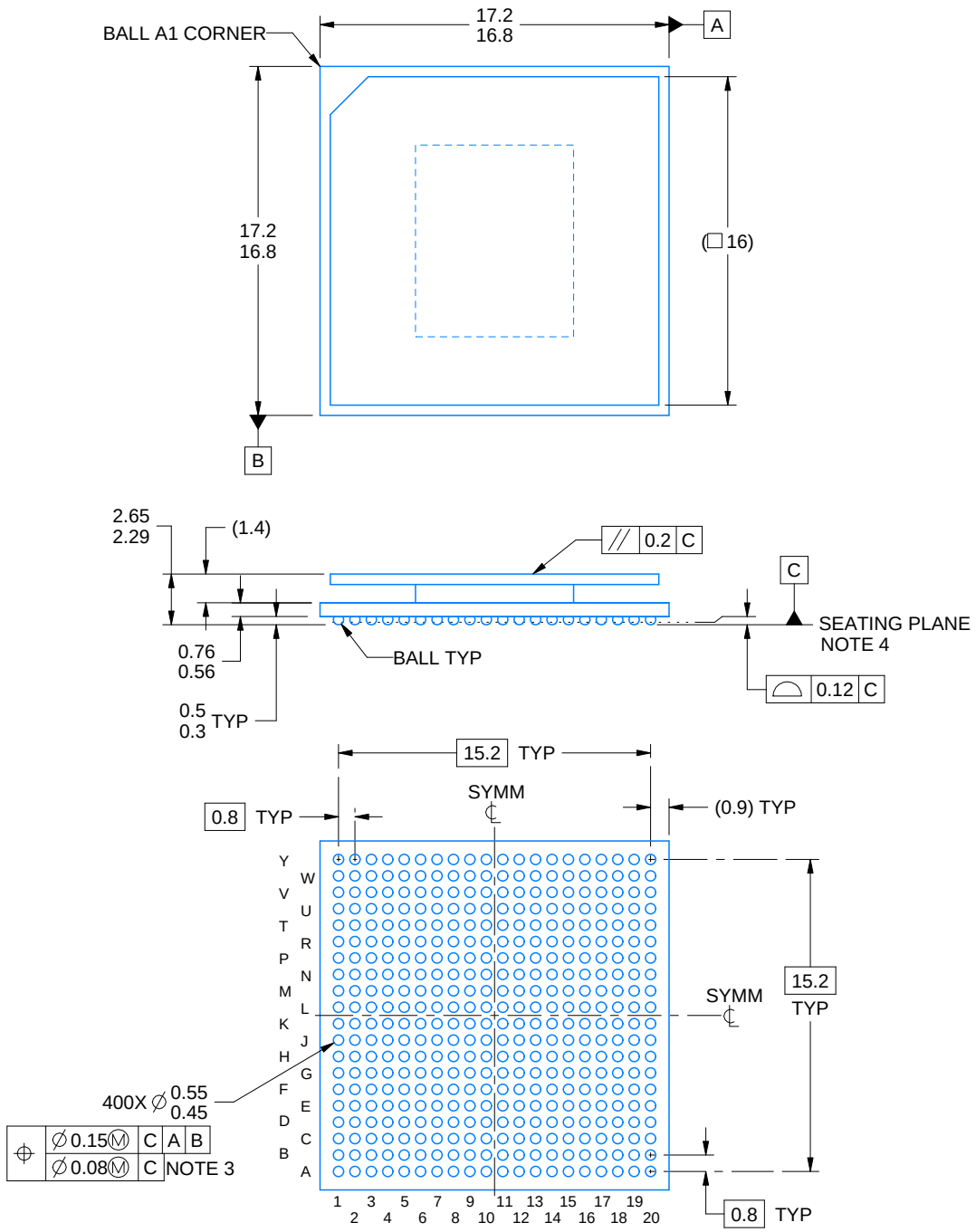
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
AFE7960IABJ	ABJ	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2
AFE7960IALK	ALK	FCBGA	400	90	6 x 15	150	315	135.9	7620	19.5	21	19.2

PACKAGE OUTLINE

ABJ0400A

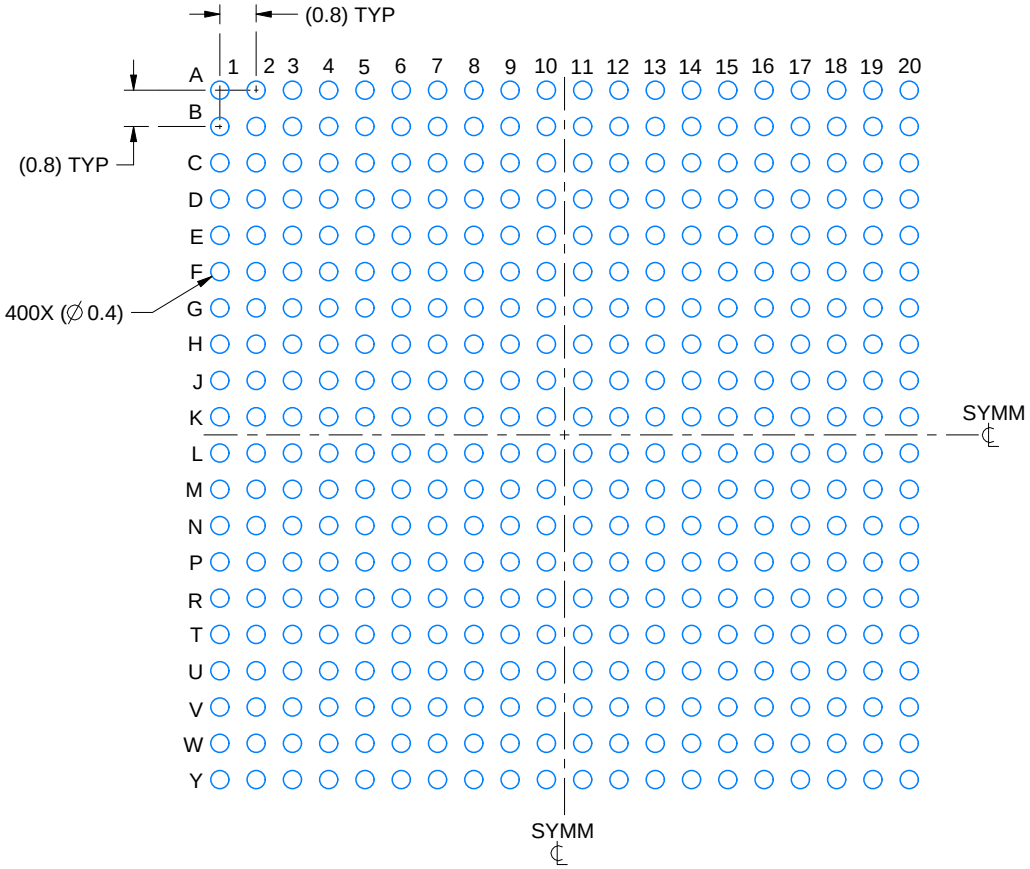
FCBGA - 2.65 mm max height

BALL GRID ARRAY

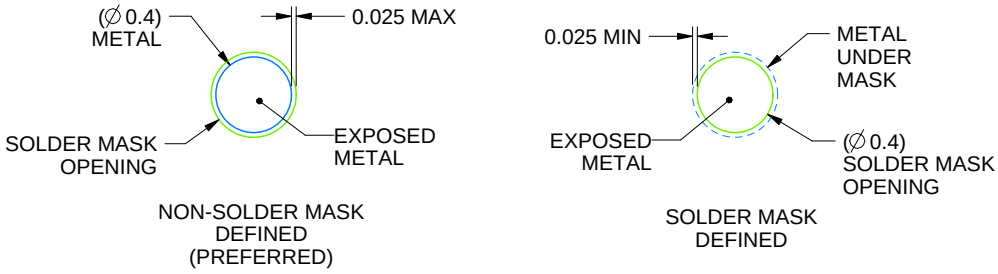


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

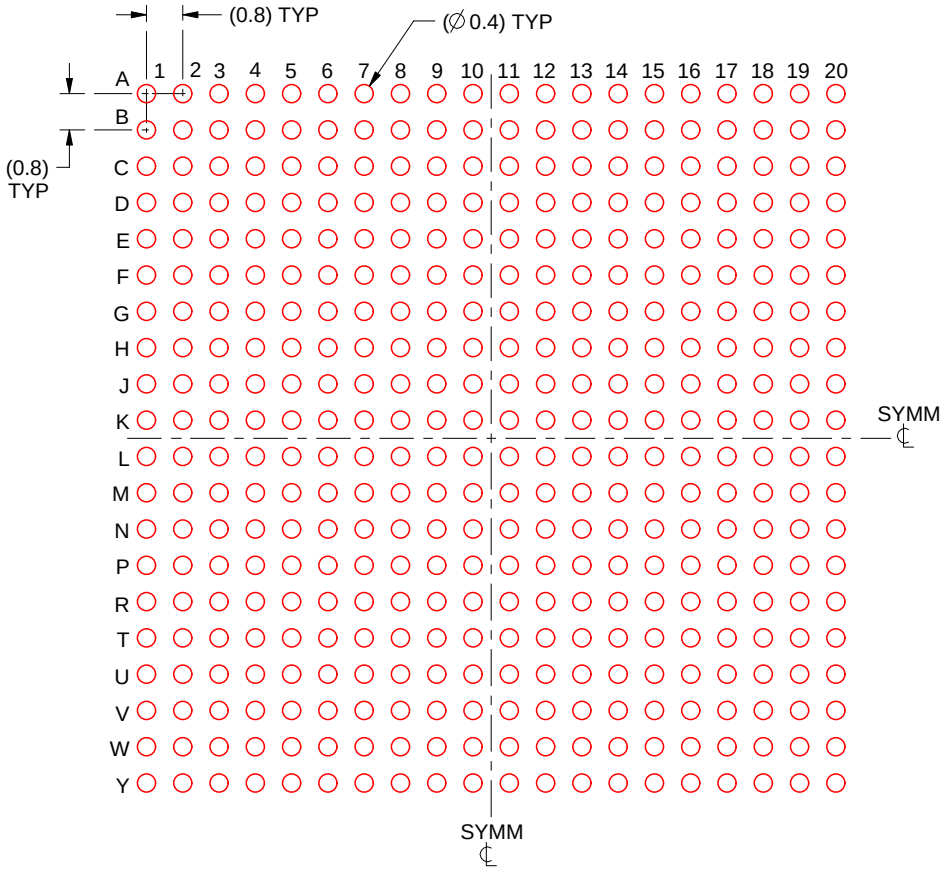


SOLDER MASK DETAILS
NOT TO SCALE

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NOTES: (continued)

6. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

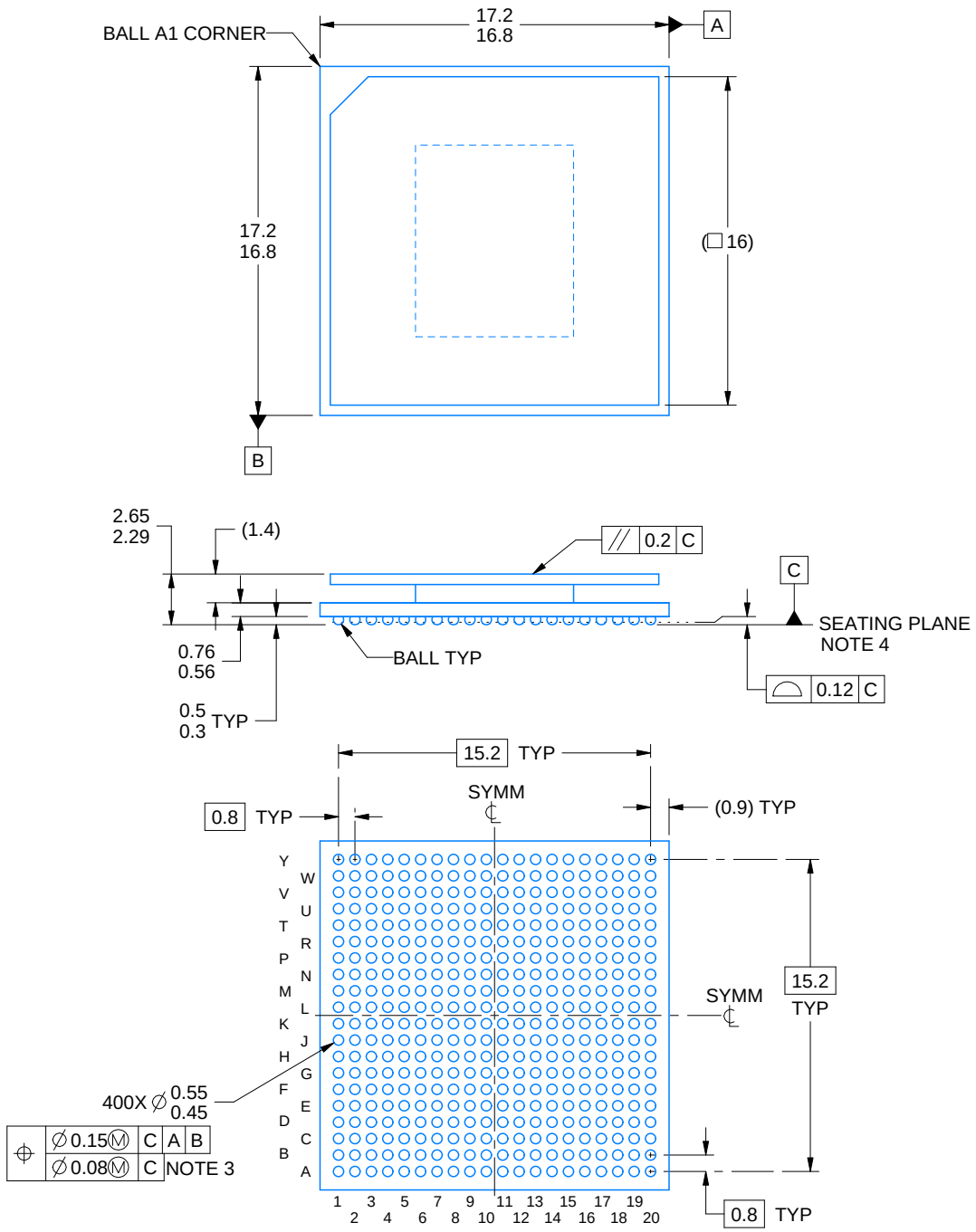
7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

ALK0400A

PACKAGE OUTLINE

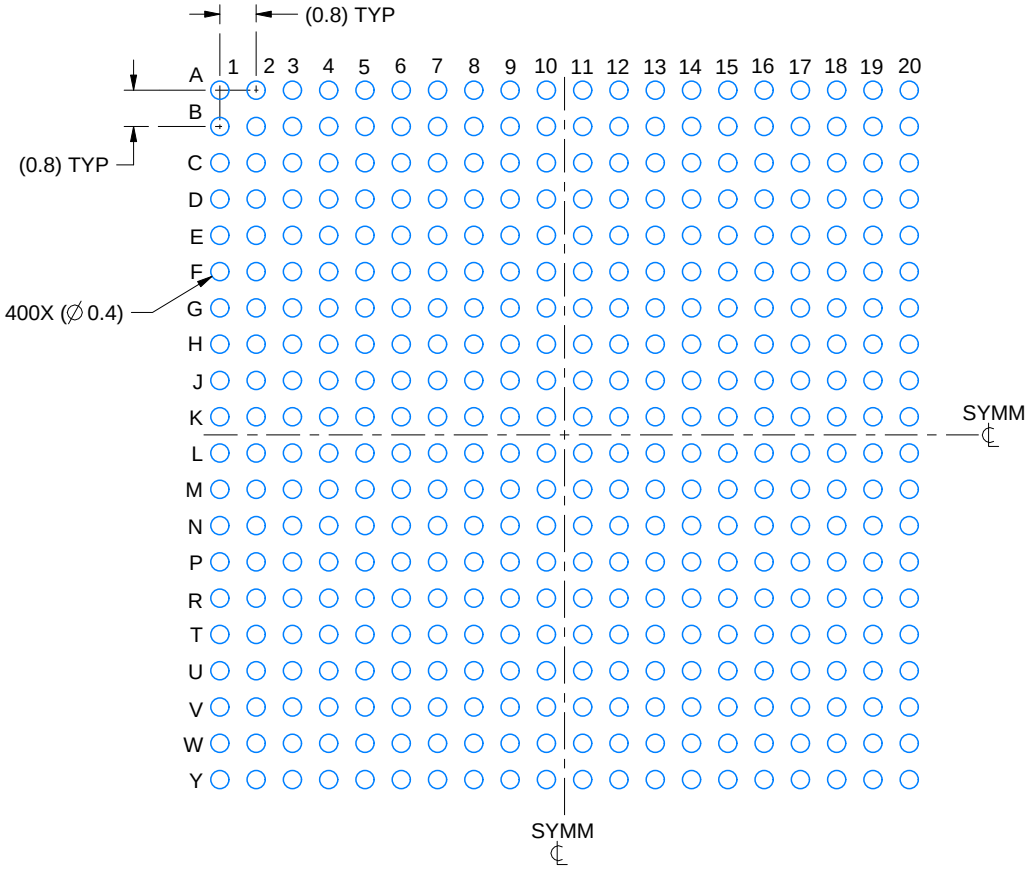
FCBGA - 2.65 mm max height

BALL GRID ARRAY

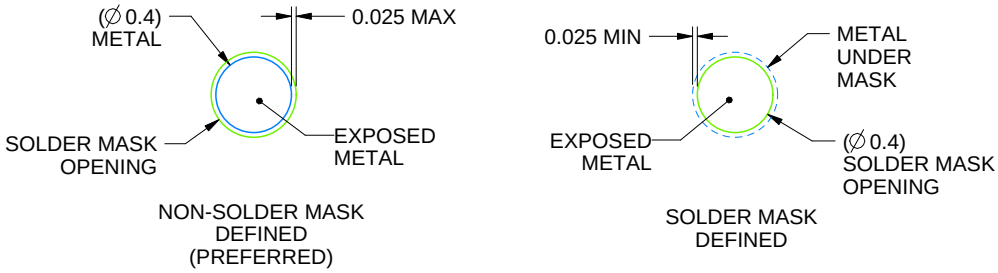


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
4. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
5. Pb-Free die bump and SnPb solder ball.
6. The lids are electrically floating (e.g. not tied to GND).



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:6X

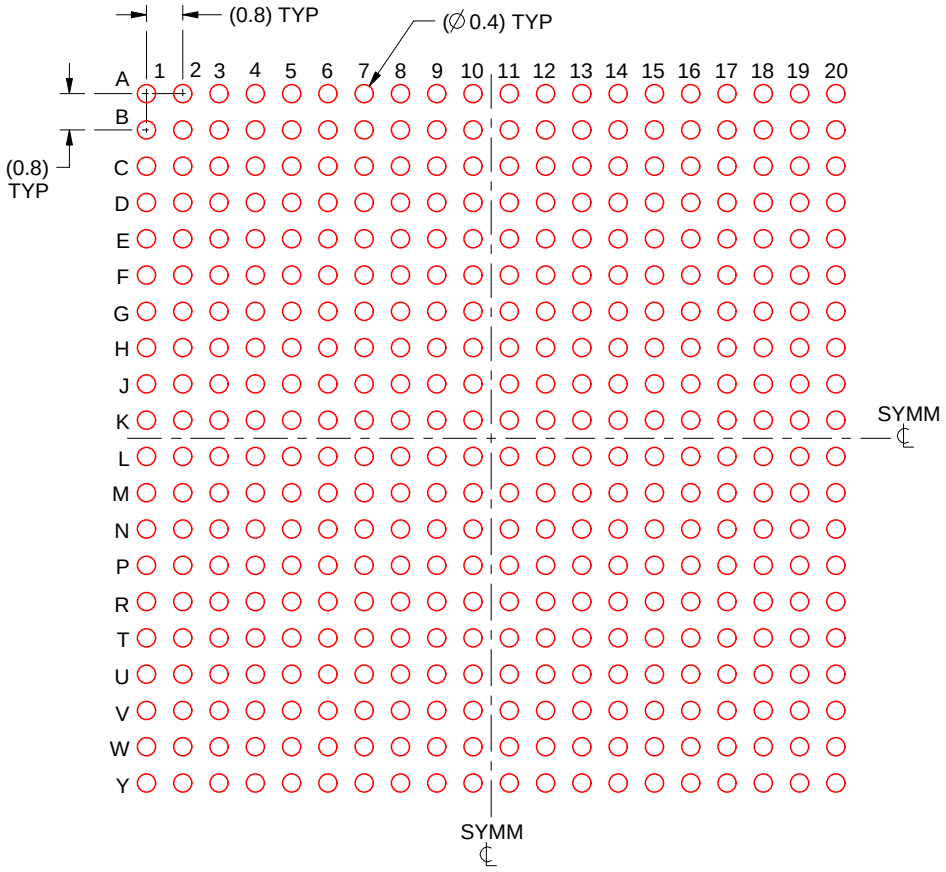


SOLDER MASK DETAILS
NOT TO SCALE

4225930/C 03/2023

NOTES: (continued)

7. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For more information, see Texas Instruments literature number SPRU811 (www.ti.com/lit/spru811).



SOLDER PASTE EXAMPLE
BASED ON 0.15 mm THICK STENCIL
SCALE:6X

4225930/C 03/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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