AMC0x02R-Q1 Automotive, Precision, ±50-mV Input, Basic and Reinforced Isolated Amplifiers With Single-Ended, Ratiometric Output

1 Features

- AEC-Q100 qualified for automotive applications:
  - Temperature grade 1: –40°C to +125°C, T_A
- Linear input voltage range: ±50mV
- Supply voltage range:
  - High-side (VDD1): 3.0V to 5.5V
  - Low-side (VDD2): 3.0V to 5.5V
- Single-ended, ratiometric output
  - Reference Input: 2.7V to 5.5V
- Low DC errors:
  - Offset error: ±50µV (maximum)
  - Offset drift: ±1µV/°C (maximum)
  - Gain error: ±0.2% (maximum)
  - Gain drift: ±45ppm/°C (maximum)
  - Nonlinearity: 0.04% (maximum)
- High CMTI: 150V/ns (minimum)
- Low EMI: Meets CISPR-11 and CISPR-25 standards
- Isolation ratings:
  - AMC0202R-Q1: Basic isolation
  - AMC0302R-Q1: Reinforced Isolation
- Safety-related certifications:
  - DIN EN IEC 60747-17 (VDE 0884-17)
  - UL1577

2 Applications

- Traction inverters
- Onboard chargers
- DC/DC converters

3 Description

The AMC0x02R-Q1 is a precision, galvanically isolated amplifier with a ±50mV, differential input and single-ended, ratiometric output. The input is optimized for direct connection to a shunt resistor or other low-impedance signal source.

The isolation barrier separates parts of the system that operate on different common-mode voltage levels. The isolation barrier is highly resistant to magnetic interference. This barrier is certified to provide reinforced isolation up to $5kV_{RMS}$ (DWV package) and basic isolation up to $3kV_{RMS}$ (D package) (60s).

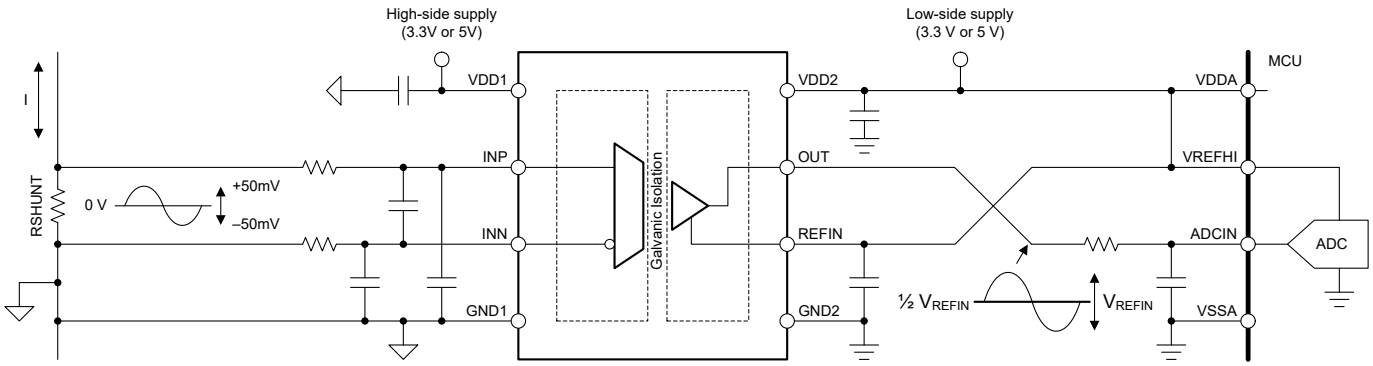
The AMC0x02R-Q1 outputs a single-ended signal proportional to the input voltage. The full-scale output is set by the voltage applied to the REFIN pin. The output of the AMC0x02R-Q1 is designed to connect directly to the input of an ADC. Connect REFIN to the same reference voltage as the ADC to match the dynamic input voltage range of the ADC.

The AMC0x02R-Q1 comes in 8-pin, wide- and narrow-body SOIC packages, and is fully specified over the temperature range from –40°C to +125°C.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)
AMC0202R-Q1	D (SOIC, 8)	4.9mm × 6mm
AMC0302R-Q1	DWV (SOIC, 8)	5.85mm × 11.5mm

(1) For more information, see the *Mechanical, Packaging, and Orderable Information*.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.



Typical Application

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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4 Device Comparison Table

PARAMETER	AMC0202R-Q1	AMC0302R-Q1
Isolation rating per VDE 0884-17	Basic	Reinforced
Package	Narrow-body SOIC (D)	Wide-body SOIC (DWV)

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5 Pin Configuration and Functions

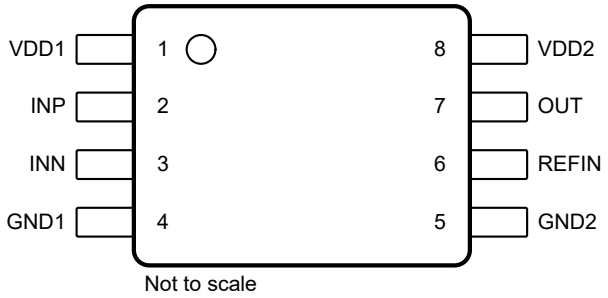

Figure 5-1. DWV and D Packages, 8-Pin SOIC (Top View)

Table 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD1	High-side power	High-side power supply(1)
2	INP	Analog input	Noninverting analog input(2)
3	INN	Analog Input	Inverting analog input(2)
4	GND1	High-side ground	High-side analog ground
5	GND2	Low-side ground	Low-side analog ground
6	REFIN	Analog input	The voltage applied to this pin sets the full-scale output of the device. Connect REFIN to a low-impedance source as described in the *Connecting the REFIN Pin* section.
7	OUT	Analog output	Analog output
8	VDD2	Low-side power	Low-side power supply(1)

(1) See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
(2) See the *Input Filter Design* section for input filter design recommendations.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power-supply voltage	High-side VDD1 to GND1	–0.3	6.5	V
	Low-side VDD2 to GND2	–0.3	6.5	
Analog input voltage	INP, INN to GND1	GND1 – 4	VDD1 + 0.5	V
Reference input voltage	REFIN to GND2	GND2 – 0.5	VDD2 + 0.5	V
Analog output voltage	OUT to GND2	GND2 – 0.5	VDD2 + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1), HBM ESD classification level 2	±2000	V
		Charged-device model (CDM), per AEC Q100-011, CDM ESD classification level C6	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD1	High-side power supply	VDD1 to GND1	3	5.0	5.5	V
VDD2	Low-side power supply	VDD2 to GND2	3	3.3	5.5	V
ANALOG INPUT						
$V_{Clipping}$	Nominal differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$	–64		64	mV
V_{FSR}	Specified linear differential input voltage	$V_{IN} = V_{INP} – V_{INN}$	–50		50	mV
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to GND1	–0.032		1	V
$C_{IN, EXT}$	Minimum external capacitance connected to the input	from INP to INN		10		nF
REFERENCE INPUT						
V_{REFIN}	Reference input voltage	REFIN to GND2	2.7		VDD2	V
ANALOG OUTPUT						
C_{LOAD}	Capacitive load	OUT to GND2			500	pF
R_{LOAD}	Resistive load	OUT to GND2		10	1	kΩ
TEMPERATURE RANGE						
T_A	Specified ambient temperature		–40		125	°C

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6.4 Thermal Information (D Package)

THERMAL METRIC(1)		D (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	58.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	19.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	58.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

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6.5 Thermal Information (DWV Package)

THERMAL METRIC(1)		DWV (SOIC)	UNIT
		8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.0	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	14.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	61.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

6.6 Power Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5V	80	mW
P_{D1}	Maximum power dissipation (high-side)	VDD1 = 5.5V	38	mW
P_{D2}	Maximum power dissipation (low-side)	VDD2 = 5.5V	42	mW

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6.7 Insulation Specifications (Basic Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 4	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 4	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 600V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	1130	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	800	V_{RMS}
		At DC voltage	1130	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	4250	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	5000	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.3 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.5 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7), $V_{pd(ini)} = V_{IOTM} = V_{pd(m)}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5V_{PP} at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	3000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried out in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

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6.8 Insulation Specifications (Reinforced Isolation)

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance(1)	Shortest pin-to-pin distance through air	≥ 8.5	mm
CPG	External creepage(1)	Shortest pin-to-pin distance across the package surface	≥ 8.5	mm
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the double insulation	≥ 15.4	µm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300V_{RMS}	I-IV	
		Rated mains voltage ≤ 6000V_{RMS}	I-III	
DIN EN IEC 60747-17 (VDE 0884-17)(2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage	2120	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave)	1500	V_{RMS}
		At DC voltage	2120	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1s (100% production test)	7000	V_{PK}
V_{IMP}	Maximum impulse voltage(3)	Tested in air, 1.2/50µs waveform per IEC 62368-1	7700	V_{PK}
V_{IOSM}	Maximum surge isolation voltage(4)	Tested in oil (qualification test), 1.2/50µs waveform per IEC 62368-1	10000	V_{PK}
q_{pd}	Apparent charge(5)	Method a, after input/output safety test subgroups 2 and 3, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{pd(ini)} = V_{IOTM}$, t_{ini} = 60s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10s	≤ 5	
		Method b1, at preconditioning (type test) and routine test, $V_{pd(ini)} = 1.2 \times V_{IOTM}$, t_{ini} = 1s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1s	≤ 5	
		Method b2, at routine test (100% production)(7) $V_{pd(ini)} = V_{pd(m)} = 1.2 \times V_{IOTM}$, $t_{ini} = t_m$ = 1s	≤ 5	
C_{IO}	Barrier capacitance, input to output(6)	V_{IO} = 0.5V_{PP} at 1MHz	≅1.5	pF
R_{IO}	Insulation resistance, input to output(6)	V_{IO} = 500V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO}$, t = 60s (qualification test), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Maintain the creepage and clearance distance of a board design to make sure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air to determine the surge immunity of the package.
(4) Testing is carried in oil to determine the intrinsic surge immunity of the isolation barrier.
(5) Apparent charge is electrical discharge caused by a partial discharge (pd).
(6) All pins on each side of the barrier are tied together, creating a two-pin device.
(7) Either method b1 or b2 is used in production.

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6.9 Safety-Related Certifications (Basic Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN 61010-1 (VDE 0411-1) Clause : 6.4.3 ; 6.7.1.3 ; 6.7.2.1 ; 6.7.2.2 ; 6.7.3.4.2 ; 6.8.3.1	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Basic insulation	Single protection
Certificate number: Pending	File number: Pending

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6.10 Safety-Related Certifications (Reinforced Isolation)

VDE	UL
DIN EN IEC 60747-17 (VDE 0884-17), EN IEC 60747-17, DIN EN IEC 62368-1 (VDE 0868-1), EN IEC 62368-1, IEC 62368-1 Clause : 5.4.3 ; 5.4.4.4 ; 5.4.9	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate number: Pending	File number: Pending

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6.11 Safety Limiting Values (D Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 116.5°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			195	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 116.5°C/W, T_J = 150°C, T_A = 25°C			1070	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

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6.12 Safety Limiting Values (DWV Package)

Safety limiting(1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to over-heat the die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 102.8°C/W, VDDx = 5.5V, T_J = 150°C, T_A = 25°C			220	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 102.8°C/W, T_J = 150°C, T_A = 25°C			1210	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the Thermal Information table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum supply voltage for high-side and low-side.

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6.13 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0V to 5.5V, VDD2 = 3.0V to 5.5V, V_{REFIN} = 3.3V, V_{INP} = –50mV to +50mV, and V_{INN} = 0V; typical specifications are at T_A = 25°C, VDD1 = 5V, VDD2 = 3.3V, and V_{REFIN} = 1.65V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
C_{IN}	Effective input sampling capacitance			8		pF
R_{IN}	Input impedance		5.3	6.3	7.3	kΩ
I_{INP}	Input current	$V_{IN} = (V_{INP} – V_{INN}) = V_{FSR, MAX}$		8		µA
I_{INN}	Input current	$V_{IN} = (V_{INP} – V_{INN}) = V_{FSR, MAX}$		–8		µA
CMTI	Common-mode transient immunity	|GND1 – GND2| = 1kV	150			V/ns
REFERENCE INPUT						
R_{REFIN}	Input Impedance	REFIN to GND2, V_{REFIN} = 3.3V, T_A = 25°C	65.3	76.8	88.3	kΩ
		REFIN to GND2, V_{REFIN} = 5V, T_A = 25°C	62	72.9	83.9	
TCR_{REFIN}	Input Impedance thermal drift			–235		ppm/°C
ANALOG OUTPUT						
	Nominal Gain			V_{REFIN} / 2 / |$V_{Clipping}$|		V/V
R_{OUT}	Output resistance			<0.2		Ω
	Output short-circuit current	OUT pin, sourcing or sinking, INN = INP = GND1 or VDD1, output shorted to either GND2 or VDD2		11		mA
DC ACCURACY						
V_{OS}	Offset voltage(1) (2)	T_A = 25°C, INP = INN = GND1	–50	±4	50	µV
TCV_{OS}	Offset drift(1) (2) (4)		–1	±0.15	1	µV/°C
E_G	Gain error(1)	T_A = 25°C	–0.2%	±0.04	0.2%	
TCE_G	Gain drift(1) (5)		–45	±5	45	ppm/°C
	Nonlinearity(1)		–0.04%		0.04%	
	Nonlinearity(1)		–0.04		0.04	%
	Output noise	INP = INN = GND1, f_{IN} = 0Hz, BW = 100kHz brickwall filter		270		$µV_{RMS}$
CMRR	Common-mode rejection ratio	f_{IN} = 0Hz, $V_{CM\ min} ≤ V_{CM} ≤ V_{CM\ max}$		–100		dB
		f_{IN} = 10kHz, $V_{CM\ min} ≤ V_{CM} ≤ V_{CM\ max}$		–97		
PSRR	Power-supply rejection ratio(2)	VDD1 DC PSRR, INP = INN = GND1, VDD1 from 3V to 5.5V		–113		dB
		VDD1 AC PSRR, INP = INN = GND1, VDD1 with 10kHz / 100mV ripple		–94		
		VDD2 DC PSRR, INP = INN = GND1, VDD2 from 3V to 5.5V		–116		
		VDD2 AC PSRR, INP = INN = GND1, VDD2 with 10kHz / 100mV ripple		–94		
AC ACCURACY						
BW	Output bandwidth		220	295		kHz
THD	Total harmonic distortion(3)	f_{IN} = 10kHz		–80		dB
SNR	Signal-to-noise ratio	f_{IN} = 1 kHz, BW = 10kHz	80	84		dB
	Signal-to-noise ratio	f_{IN} = 10kHz, BW = 100kHz		75		
POWER SUPPLY						

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minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD1 = 3.0V to 5.5V, VDD2 = 3.0V to 5.5V, V_{REFIN} = 3.3V, V_{INP} = –50mV to +50mV, and V_{INN} = 0V; typical specifications are at T_A = 25°C, VDD1 = 5V, VDD2 = 3.3V, and V_{REFIN} = 1.65V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
IDD1	High-side supply current			5.6	6.9	mA
IDD2	Low-side supply current			5.0	7.6	mA
$VDD1_{UV}$	High-side undervoltage detection threshold	VDD1 rising	2.5	2.6	2.7	V
		VDD1 falling	1.9	2.0	2.1	
$VDD2_{UV}$	Low-side undervoltage detection threshold	VDD2 rising	2.3	2.5	2.7	V
		VDD2 falling	1.9	2.05	2.2	

(1) The typical value includes one standard deviation (*sigma*) at nominal operating conditions.
(2) This parameter is input referred.
(3) THD is the ratio of the rms sum of the amplitues of first five higher harmonics to the amplitude of the fundamental.
(4) Offset error temperature drift is calculated using the box method, as described by the following equation: $TCV_{OS} = (V_{OS,MAX} - V_{OS,MIN}) / TempRange$ where $V_{OS,MAX}$ and $V_{OS,MIN}$ refer to the maximum and minimum V_{OS} values measured within the temperature range (–40 to 125°C).
(5) Gain error temperature drift is calculated using the box method, as described by the following equation: $TCE_G\ (ppm) = ((E_{G,MAX} - E_{G,MIN}) / TempRange) \times 10^4$ where $E_{G,MAX}$ and $E_{G,MIN}$ refer to the maximum and minimum E_G values (in %) measured within the temperature range (–40 to 125°C).

6.14 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time			1.7		µs
t_f	Output signal fall time			1.7		µs
	V_{INx} to V_{OUTx} signal delay (50% - 10%)	Unfiltered output		0.8	1.3	µs
	V_{INx} to V_{OUTx} signal delay (50% - 50%)	Unfiltered output		1.6	2.1	µs
	V_{INx} to V_{OUTx} signal delay (50% - 90%)	Unfiltered output		2.5	3	µs
t_{AS}	Analog settling time	VDD1 step to 3.0V with VDD2 ≥ 3.0V, V_{REFIN} = 3.3V, to V_{OUT} valid, 0.1% settling		30	100	µs

6.15 Timing Diagram

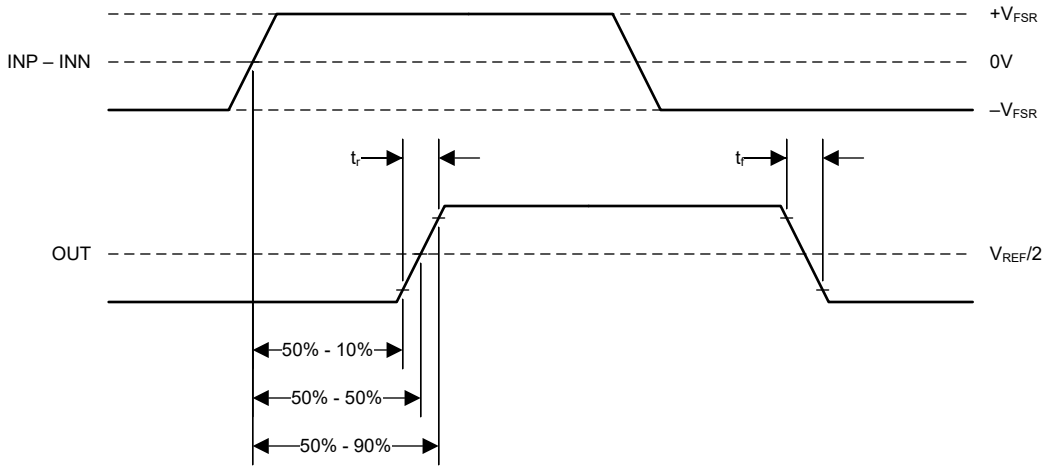


Figure 6-1. Rise, Fall, and Delay Time Waveforms

6.16 Insulation Characteristics Curves

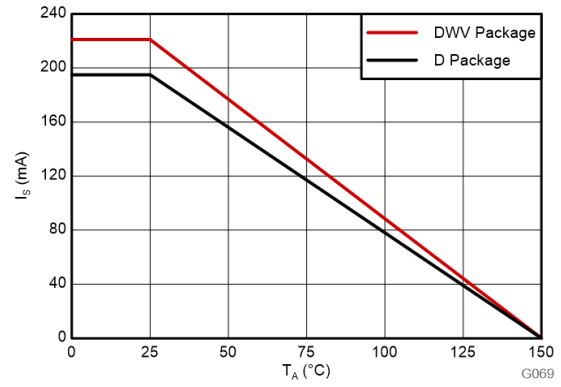


Figure 6-2. Thermal Derating Curve for Safety-Limiting Current per VDE

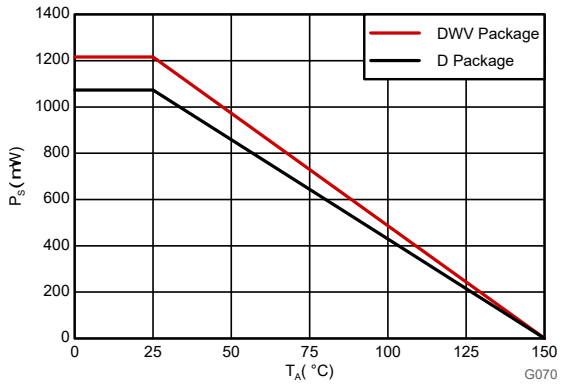
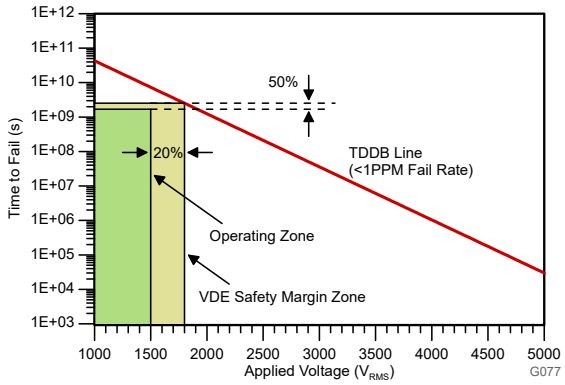
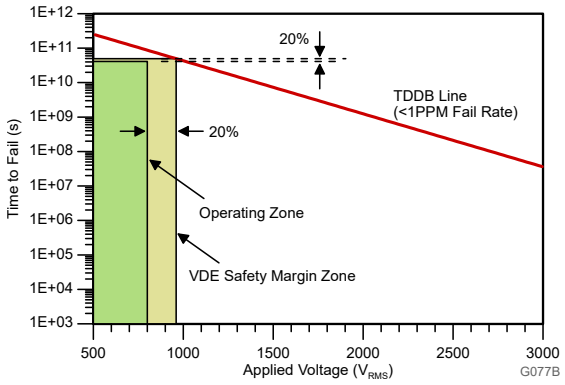


Figure 6-3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 1500V_{RMS}, projected operating lifetime ≥50 years

Figure 6-4. Isolation Capacitor Lifetime Projection (Reinforced Isolation)



T_A up to 150°C, stress-voltage frequency = 60Hz, isolation working voltage = 800V_{RMS}, projected operating lifetime >>100 years

Figure 6-5. Isolation Capacitor Lifetime Projection (Basic Isolation)

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6.17 Typical Characteristics

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

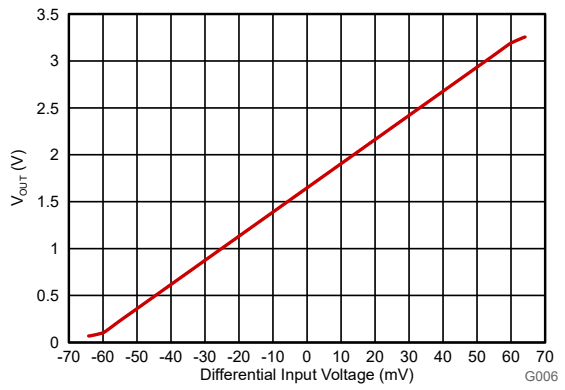
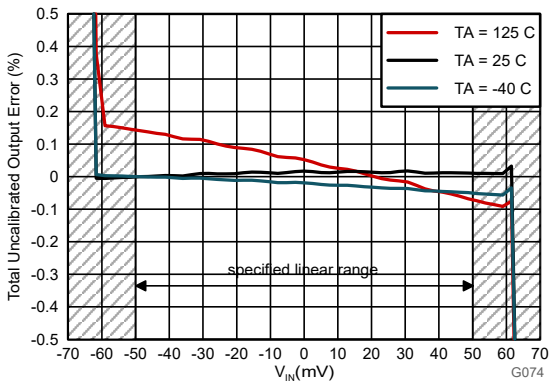


Figure 6-6. Output Voltage vs Input Voltage



Total uncalibrated output error is defined as:(($V_{OUT_Measured}$ – $V_{OUT_Expected}$) / V_{REFIN}) x 100 , where $V_{OUT_Expected}$ = V_{IN} / $V_{Clipping}$ x V_{REFIN} / 2 + V_{REFIN} / 2, V_{REFIN} = 3.3V and $V_{Clipping}$ = 0.064V

Figure 6-7. Unadjusted Error vs Input Voltage

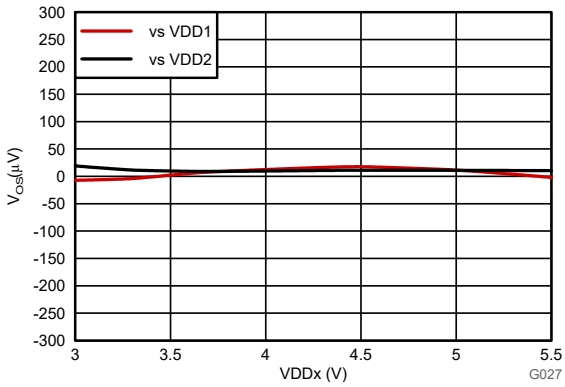


Figure 6-8. Input Offset Voltage vs Supply Voltage

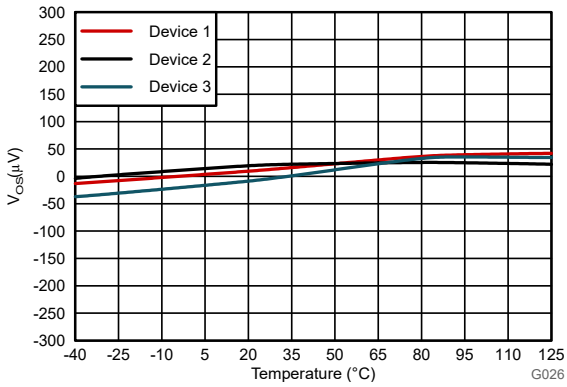
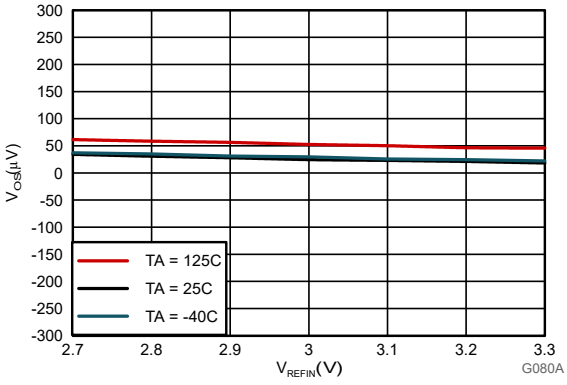
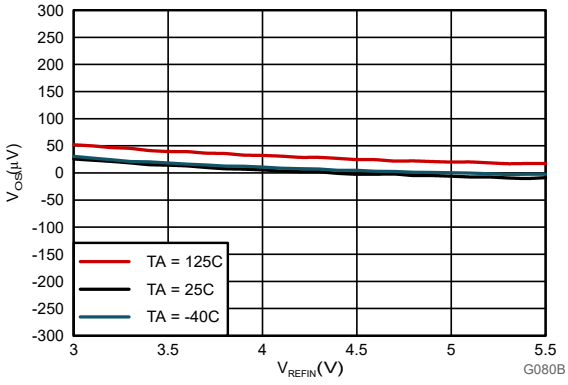


Figure 6-9. Input Offset Voltage vs Temperature



VDD2 = 3.3V

Figure 6-10. Input Offset Voltage vs VREFIN



VDD2 = 5.5V

Figure 6-11. Input Offset Voltage vs VREFIN

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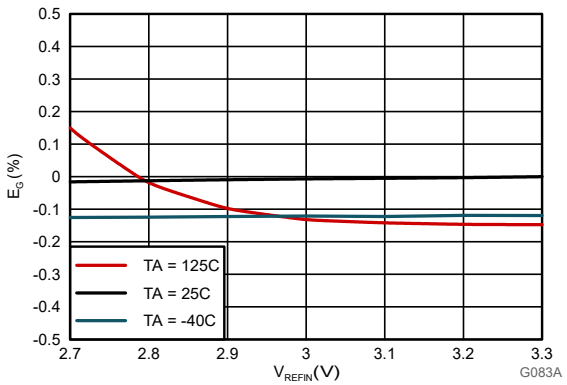
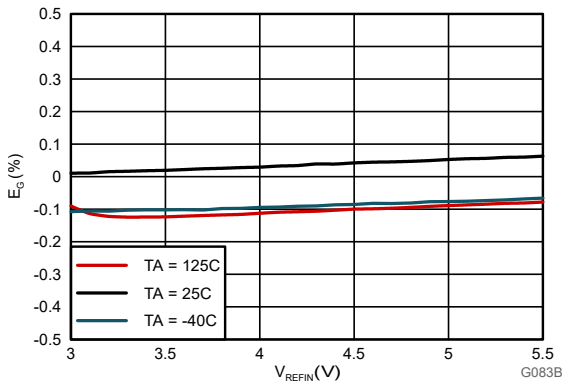
6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)



VDD2 = 3.3V

Figure 6-12. Gain Error vs VREFIN



VDD2 = 5.5V

Figure 6-13. Gain Error vs VREFIN

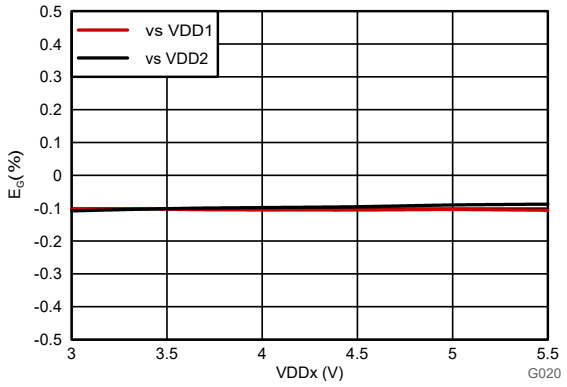


Figure 6-14. Gain Error vs Supply Voltage

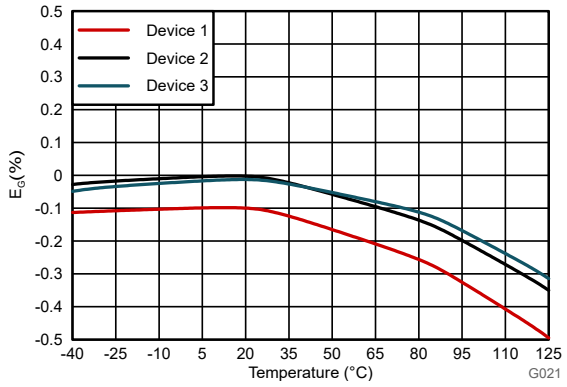


Figure 6-15. Gain Error vs Temperature

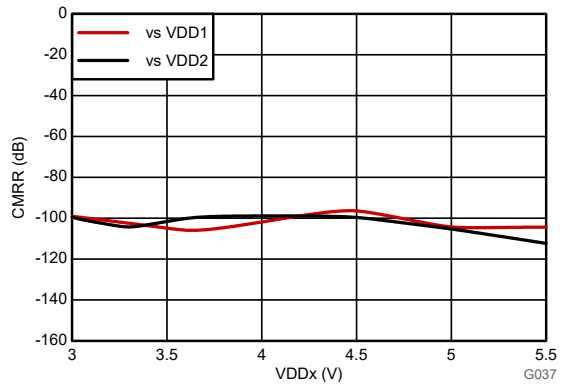


Figure 6-16. Common-Mode Rejection Ratio vs Supply Voltage

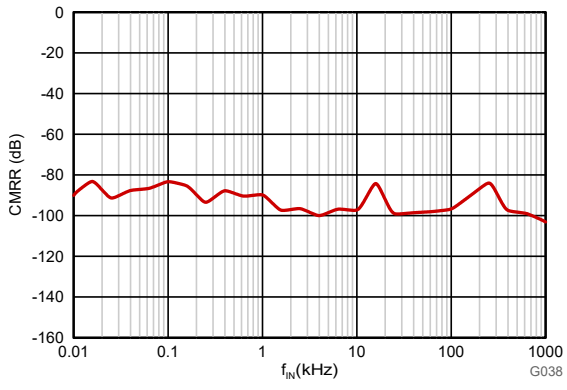


Figure 6-17. Common-Mode Rejection Ratio vs Input Frequency

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6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

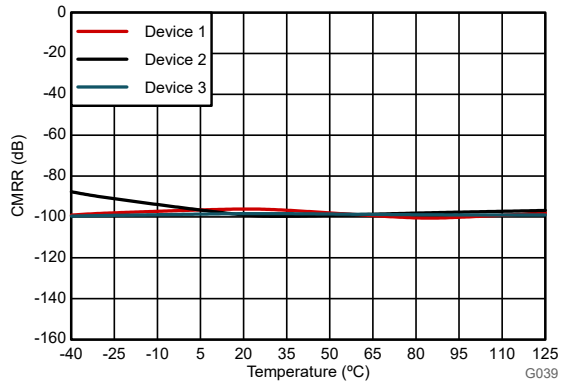

Figure 6-18. Common-Mode Rejection Ratio vs Temperature

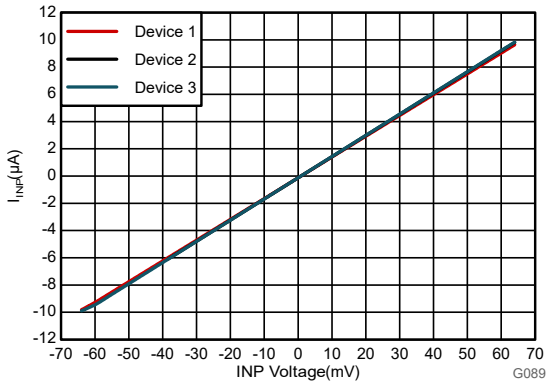

Figure 6-19. Input Current vs Input Voltage

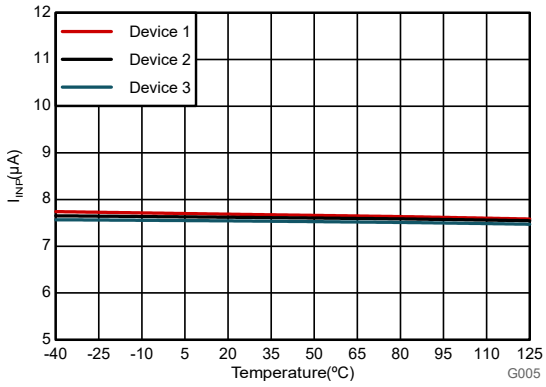

Figure 6-20. Input Current vs Temperature

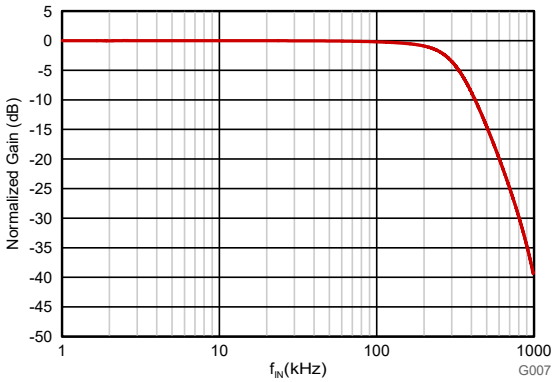

Figure 6-21. Normalized Gain vs Input Frequency

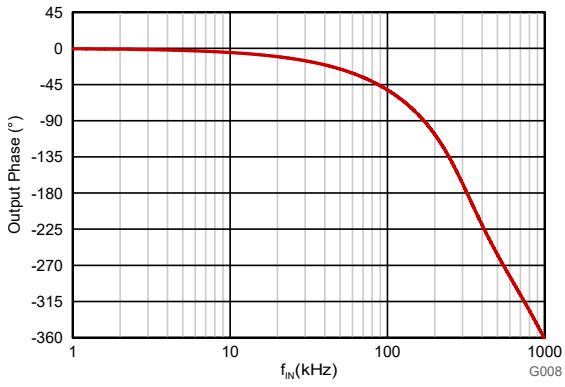

Figure 6-22. Output Phase vs Input Frequency

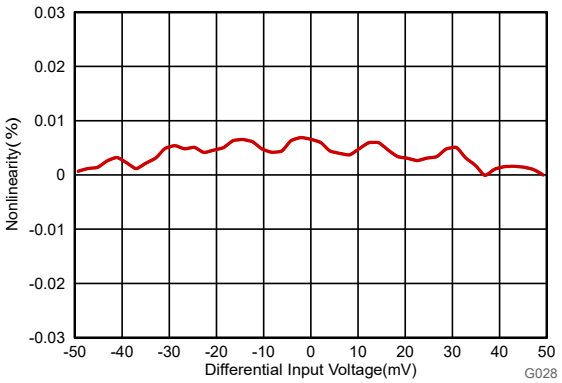

Figure 6-23. Nonlinearity vs Input Voltage

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6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

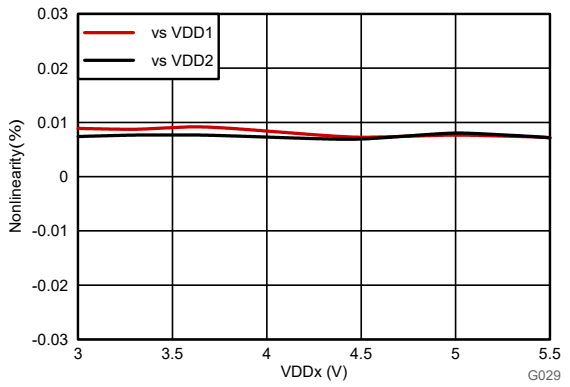

Figure 6-24. Nonlinearity vs Supply Voltage

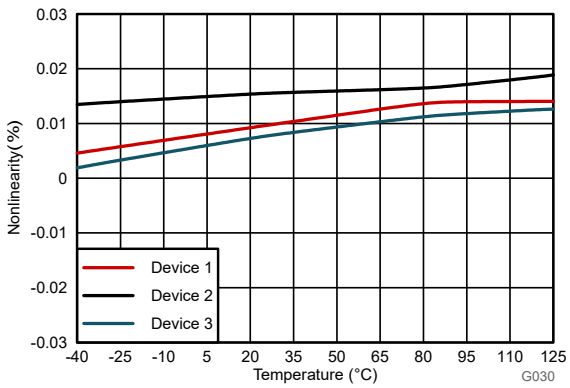

Figure 6-25. Nonlinearity vs Temperature

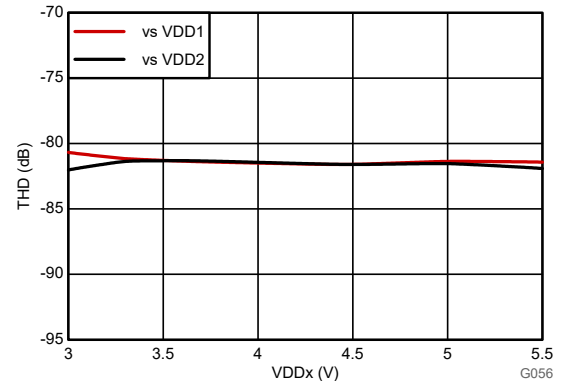

Figure 6-26. Total Harmonic Distortion vs Supply Voltage

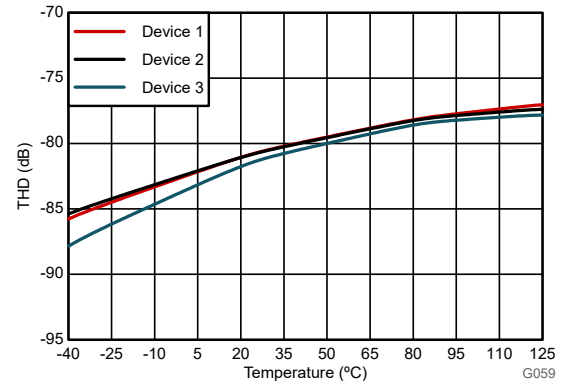

Figure 6-27. Total Harmonic Distortion vs Temperature

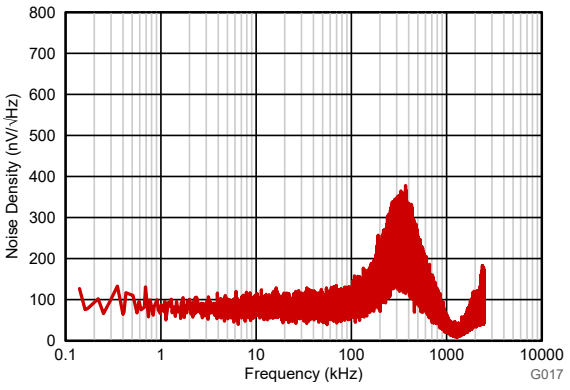

Figure 6-28. Input-Referred Noise Density vs Frequency

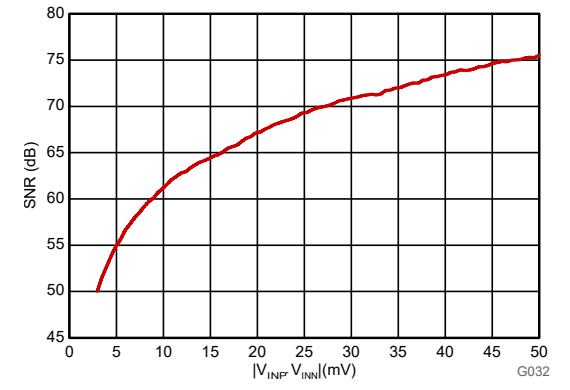

Figure 6-29. Signal-to-Noise Ratio vs Input Voltage

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6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

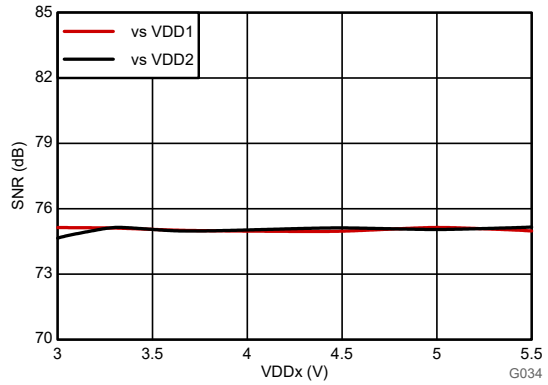

Figure 6-30. Signal-to-Noise Ratio vs Supply Voltage

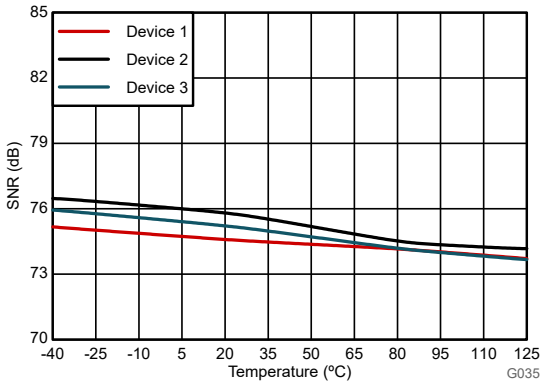

Figure 6-31. Signal-to-Noise Ratio vs Temperature

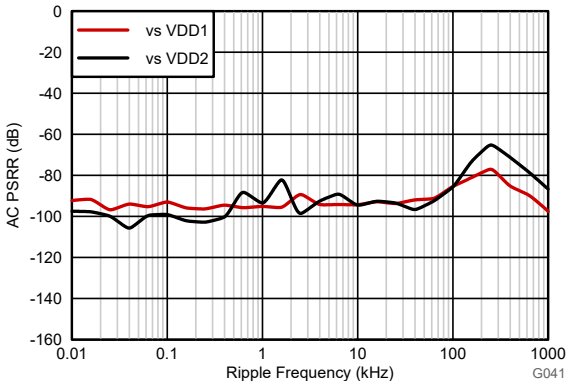

Figure 6-32. Power-Supply Rejection Ratio vs Ripple Frequency

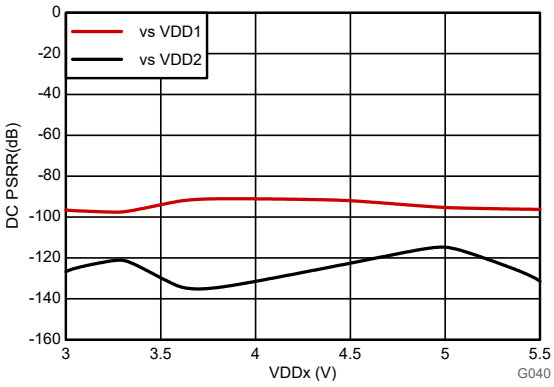

Figure 6-33. Power-Supply Rejection Ratio vs Supply Voltage

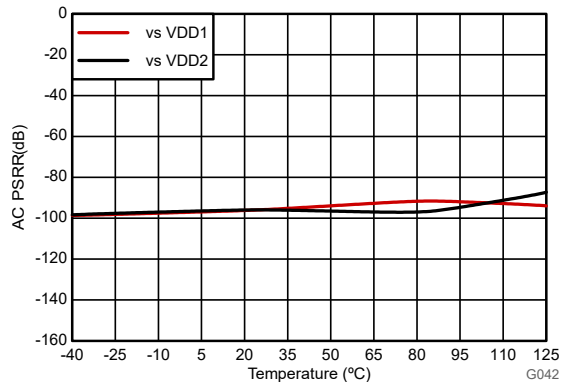

Figure 6-34. Power-Supply Rejection Ratio vs Temperature

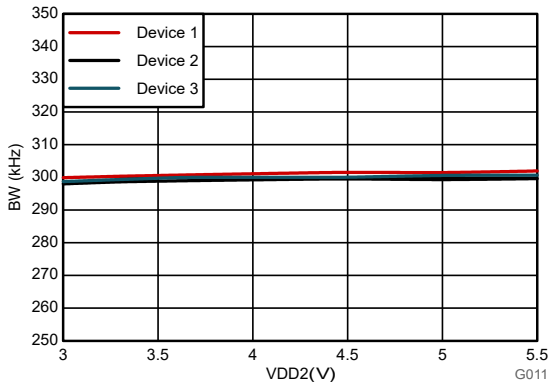

Figure 6-35. Output Bandwidth vs Low-Side Supply Voltage

6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

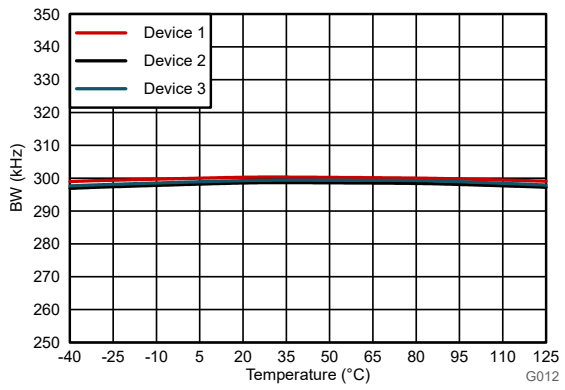

Figure 6-36. Output Bandwidth vs Temperature

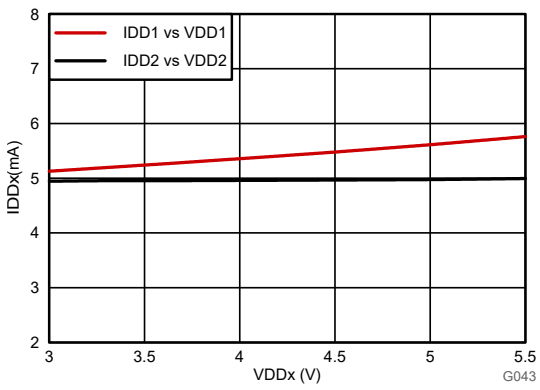

Figure 6-37. Supply Current vs Supply Voltage

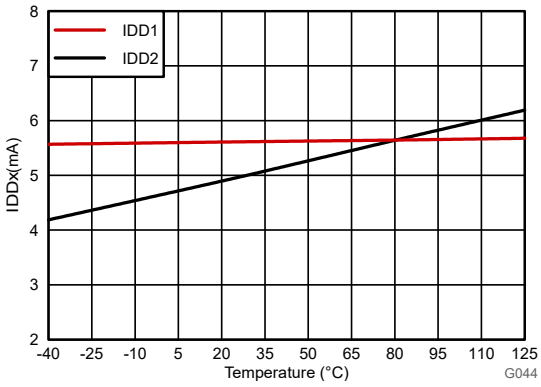

Figure 6-38. Supply Current vs Temperature

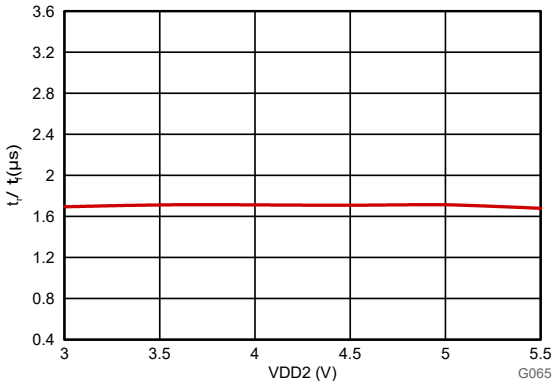

Figure 6-39. Output Rise and Fall Time vs Low-Side Supply

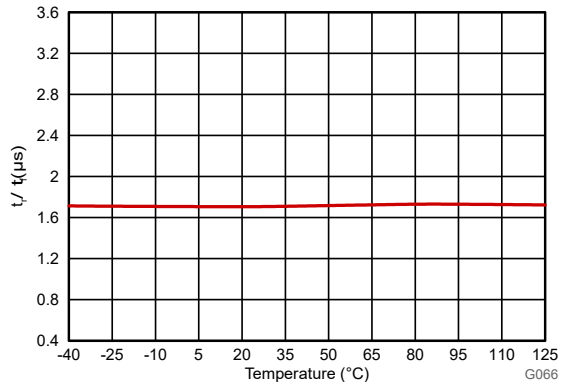

Figure 6-40. Output Rise and Fall Time vs Temperature

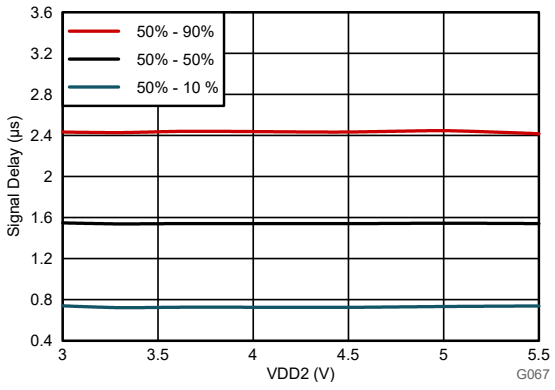

Figure 6-41. V_{IN} to V_{OUT} Signal Delay vs Low-Side Supply Voltage

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6.17 Typical Characteristics (continued)

at VDD1 = 5V, VDD2 = 3.3V, VREFIN = 3.3V, VINP = –50mV to 50mV, VINN = 0V, and f_{IN} = 10kHz (unless otherwise noted)

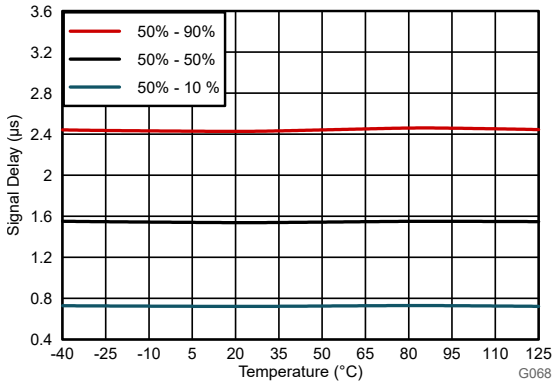


Figure 6-42. V_{IN} to V_{OUT} Signal Delay vs Temperature

7 Detailed Description

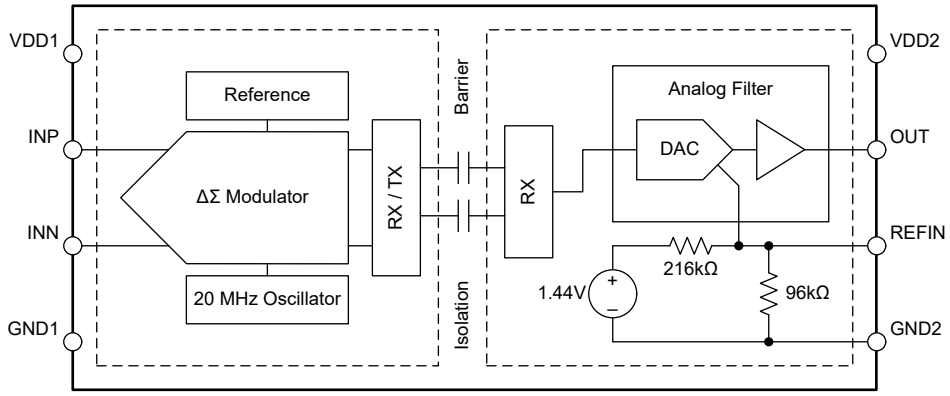
7.1 Overview

The AMC0x02R-Q1 is a precision, galvanically isolated amplifier with a ±50mV, differential input and single-ended, ratiometric output. The input stage of the device drives a second-order, delta-sigma (ΔΣ) modulator. The modulator converts the analog input signal into a digital bitstream that is transferred across the isolation barrier that separates the high-side from the low-side.

On the low-side, the received bitstream is processed by an analog filter that outputs a GND2-referenced, single-ended signal at the OUT pin. This single-ended output signal is proportional to the input signal. The full-scale output voltage of the isolated amplifier is equal to the voltage applied to the REFIN pin.

The SiO_2-based, capacitive isolation barrier supports a high level of magnetic field immunity, as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application note. The digital modulation used in the AMC0x02R-Q1 transmits data across the isolation barrier. This modulation, and the isolation barrier characteristics, result in high reliability and high common-mode transient immunity.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

As shown in Figure 7-1, input of the AMC0x02R-Q1 has a fully differential, switched-capacitor circuit with a dynamic input impedance of 6.3kΩ.

The sampling capacitor is continuously charged and discharged with a frequency of 20MHz. With the S1 switches closed, C_{IND} charges to the voltage difference across V_{INP} and V_{INN}. For the discharge phase, both S1 switches open first and then both S2 switches close. C_{IND} discharges to approximately AGND + 0.8V during this phase.

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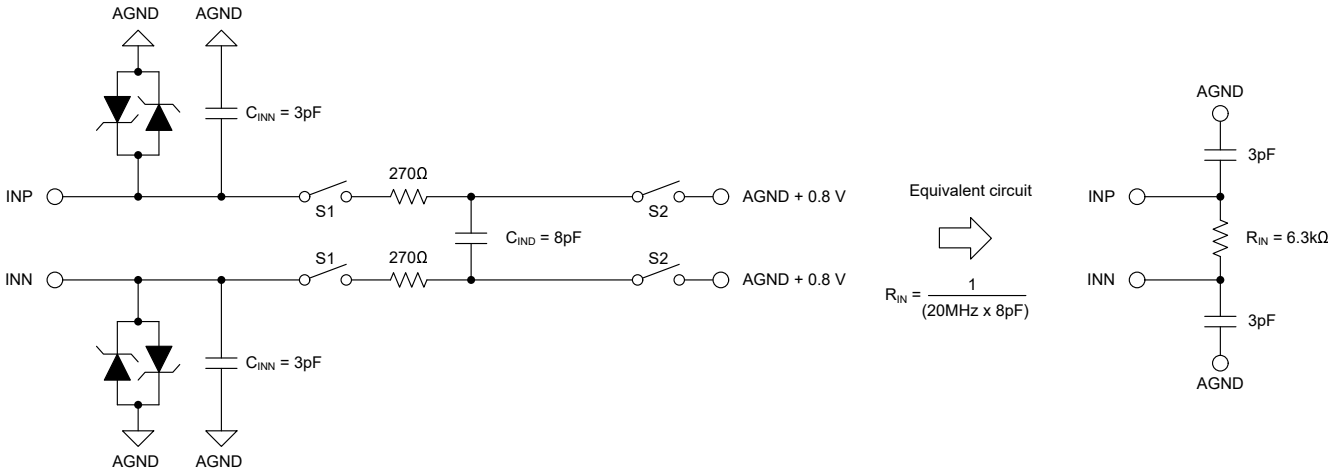

Figure 7-1. Equivalent Input Circuit

The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. There are two restrictions on the analog input signals (INP and INN).

- First, if the input voltage exceeds the input range specified in the *Absolute Maximum Ratings* table, limit the input current to the absolute maximum value. This is to prevent device input electrostatic discharge (ESD) diode damage due to high current.
- Second, keep the differential analog input voltage within the specified full-scale range (V_{FSR}) and input common-mode voltage range (V_{CM}) ranges. V_{FSR} and $V_{CM}$are specified in the *Recommended Operating Conditions* table. The device noise and linearilty performance is guaranteed only in this range.

7.3.2 Isolation Channel Signal Transmission

As shown in OOK-Based Modulation Scheme, the AMC0x02R-Q1 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. The transmit driver (TX) is illustrated in the *Functional Block Diagram* . TX transmits an internally generated, high-frequency carrier across the isolation barrier to represent a digital *one*. However, TX does not send a signal to represent a digital *zero*. The nominal frequency of the carrier used inside the AMC0x02R-Q1 is 480MHz.

The receiver (RX) on the other side of the isolation barrier recovers and demodulates the signal and provides the input to the analog filter. The AMC0x02R-Q1 transmission channel is optimized to achieve the highest level of common-mode transient immunity (CMTI) and the lowest level of radiated emissions. The high-frequency carrier and RX/TX buffer switching cause these emissions.

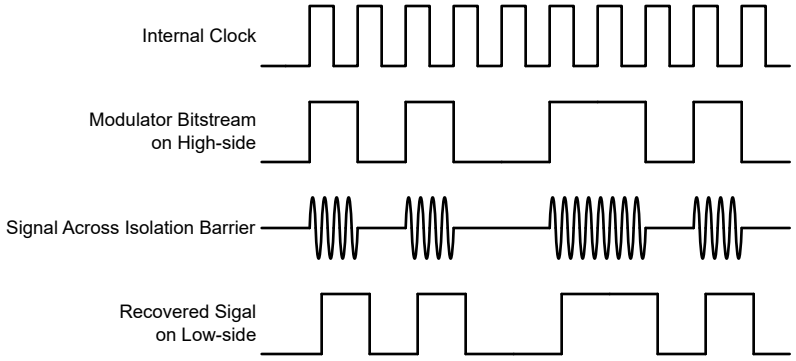

Figure 7-2. OOK-Based Modulation Scheme

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7.3.3 Analog Output

The AMC0x02R-Q1 provides a single-ended analog output voltage proportional to the input voltage. The output is referred to GND2 and is galvanically isolated from the input of the device. The output is designed to connect directly to the input of an ADC.

The full-scale output voltage is set by the REFIN pin. For any input voltage within the specified linear input range, the device outputs a voltage equal to:

$$V_{OUT} = V_{IN} / V_{Clipping} \times V_{REFIN} / 2 + V_{REFIN} / 2 = (V_{INP} – V_{INN}) / V_{Clipping} \times V_{REFIN} / 2 + V_{REFIN} / 2 \quad (1)$$

Connect REFIN to the same reference voltage as a downstream ADC to match the ADC dynamic input voltage range. With a shared reference voltage, the ADC outputs a negative full-scale code when the negative clipping voltage is applied to the input of the AMC0x02R-Q1. The ADC outputs the mid-range code when 0V is applied to the input of the AMC0x02R-Q1. The ADC outputs a positive full-scale code when the positive clipping voltage is applied to the input of the AMC0x02R-Q1.

The device is linear within the specified linear full-scale range. Beyond the linear full-scale range, the output continues to follow the input, but with reduced linearity performance. The output clips when the input voltage reaches the clipping voltage. Figure 7-3 shows the input-to-output transfer characteristic.

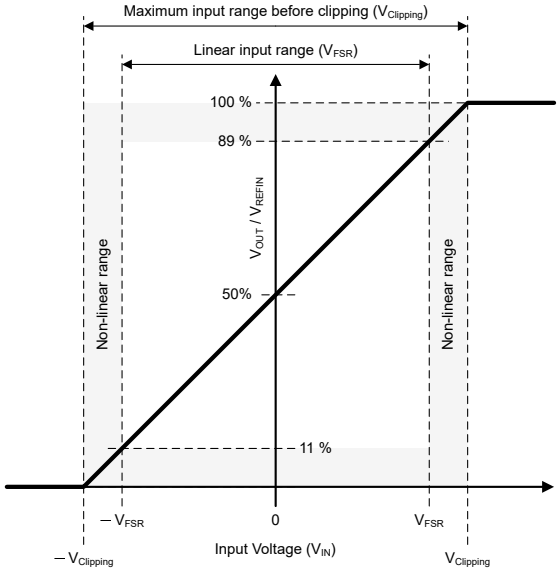

Figure 7-3. Input-to-Output Transfer Curve of the AMC0x02R-Q1

7.4 Device Functional Modes

The AMC0x02R-Q1 operates in one of the following states:

- Off-state: The low-side supply (VDD2) is below the $VDD2_{UV}$ threshold. The device is not responsive. OUT is in Hi-Z state. Internally, OUT is clamped to VDD2 and GND2 by ESD protection diodes.
- Missing high-side supply: The low-side of the device (VDD2) is supplied and within recommended operating conditions. The high-side supply (VDD1) is below the $VDD1_{UV}$ threshold. The OUT pin is driven to V_{REFIN} / 2.
- Analog input overrange (positive full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is above the maximum clipping voltage $V_{Clipping, MAX}$. The device outputs V_{REFIN} at the OUT pin.
- Analog input underrange (negative full-scale input): VDD1 and VDD2 are within recommended operating conditions but the analog input voltage V_{IN} is below the minimum clipping voltage $V_{Clipping, MIN}$. The OUT pin is driven to GND2.
- Normal operation: VDD1, VDD2, and V_{IN} are within the recommended operating conditions. The device outputs a voltage that is proportional to the input voltage.

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Table 7-1 lists the operating modes.

Table 7-1. Device Operational Modes

OPERATING CONDITION	VDD1	VDD2	V_{IN}	DEVICE RESPONSE
Off	Don't care	VDD2 < $VDD2_{UV}$	Don't care	OUT is in Hi-Z state. Internally, OUT is clamped to VDD2 and GND2 by ESD protection diodes.
Missing high-side supply	VDD1 < $VDD1_{UV}$	Valid(1)	Don't care	The OUT pin is driven to V_{REFIN} / 2.
Input overrange	Valid(1)	Valid(1)	V_{IN} > $V_{Clipping, MAX}$	The device outputs V_{REFIN} at the OUT pin.
Input underrange	Valid(1)	Valid(1)	V_{IN} < $V_{Clipping, MIN}$	The OUT pin is driven to GND2.
Normal operation	Valid(1)	Valid(1)	Valid(1)	The device outputs a voltage that is proportional to the input voltage.

(1) *Valid* denotes operation within the recommended operating conditions.

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The AMC0x02R-Q1 has low analog input voltage range, high accuracy, low temperature drift, and high common-mode transient immunity. The AMC0x02R-Q1 is primarily designed for shunt-based current-sensing applications where accurate current monitoring is required in the presence of high common-mode voltages. The AMC0x02R-Q1 is preferred for isolated current sensing in HEV/EV charging piles, HEV/EV onboard chargers (OBC), HEV/EV DC/DC converters, and HEV/EV traction inverters applications.

8.2 Typical Application

The following image shows the AMC0x02R-Q1 in a typical application. The load current flowing through an external shunt resistor RSHUNT produces a voltage drop. The AMC0x02R-Q1 high-side circuitry senses the voltage drop across the shunt resistor, then digitizes and transfers data across the isolation barrier to the low side. Low-side circuitry reconstructs the digitized data into an analog signal and provides the signal as single-ended ratiometric voltage on the output pin.

The differential input, single-ended ratiometric output, and high common-mode transient immunity (CMTI) of the AMC0x02R-Q1 provide reliable and accurate operation even in high-noise environments.

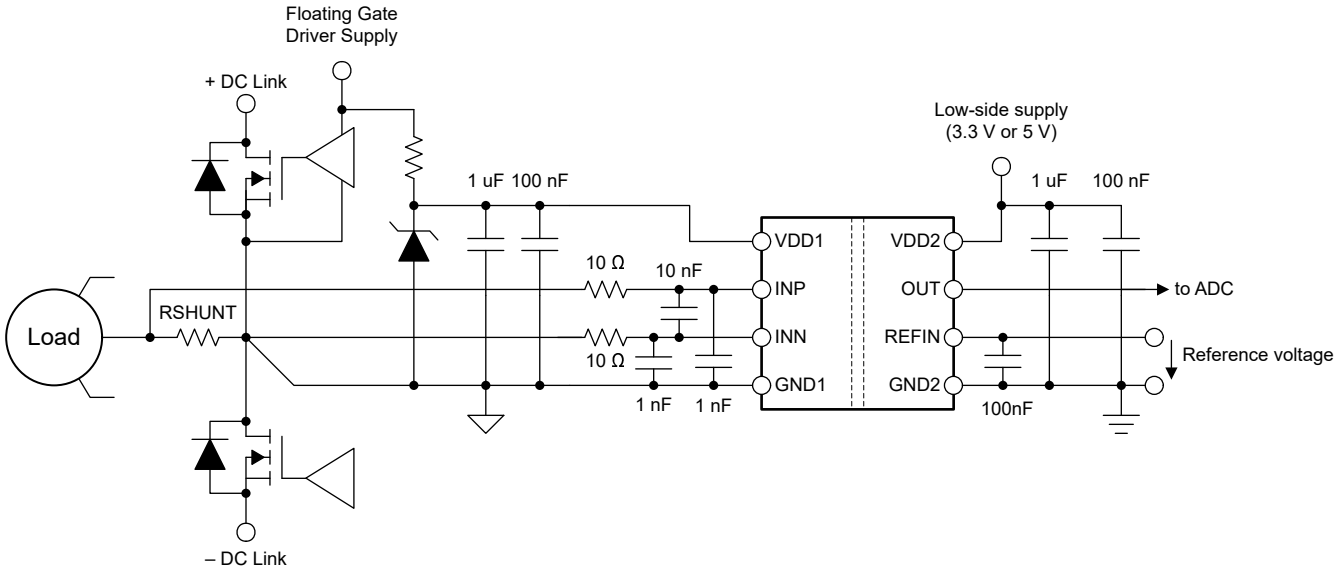

Figure 8-1. Using the AMC0x02R-Q1 for Current Sensing in a Typical Application

8.2.1 Design Requirements

Table 8-1 lists the parameters for this typical application.

Table 8-1. Design Requirements

PARAMETER	VALUE
High-side supply voltage	3.3V or 5V
Low-side supply voltage	3.3V or 5V
Voltage drop across RSHUNT for a linear response	±50mV(maximum)

8.2.2 Detailed Design Procedure

In the *Typical Application* figure, the high-side power supply (VDD1) for the AMC0x02R-Q1 is derived from the floating power supply of the upper gate driver.

The floating ground reference (GND1) is derived from the end of the shunt resistor that is connected to the negative input of the AMC0x02R-Q1 (INN). If a four-pin shunt is used, the inputs of the AMC0x02R-Q1 are connected to the inner leads. GND1 is then connected to the outer lead on the INN-side of the shunt. To minimize offset and improve accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. Do not short GND1 to INN directly at the device input; see the *Layout Example* section for more details.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current:

$$V_{SHUNT} = I \times RSHUNT \quad (2)$$

Select a RSHUNT value to satisfy the following two conditions:

- First, the voltage drop caused by the nominal current range does not exceed the recommended differential input voltage range of $V_{SHUNT} \leq \pm 50mV$.
- Secondly, the voltage drop caused by the maximum allowed overcurrent does not exceed the input voltage that causes a clipping output. Keep $V_{SHUNT} \leq V_{Clipping}$.

8.2.2.1 Input Filter Design

Place a differential RC filter (R1, R2, C5) in front of the isolated amplifier to improve signal-to-noise performance of the signal path. Design the input filter such that:

- The cutoff frequency of the filter is at least one order of magnitude lower than the sampling frequency (20MHz) of the ΔΣ modulator
- The input bias current does not generate significant voltage drop across the DC impedance of the input filter
- The impedances measured from the analog inputs are equal

Place capacitors C6 and C7 to improve common-mode rejection at high frequencies (>1MHz) and to improve offset voltage performance. For best performance, verify C6 matches the value of C7 and that both capacitors are 10 to 20 times lower in value than C5. NP0-type capacitors offer low temperature drift and low voltage coefficients, and are preferred for common-mode filtering.

For most applications, the structure shown in Figure 8-2 achieves excellent performance.

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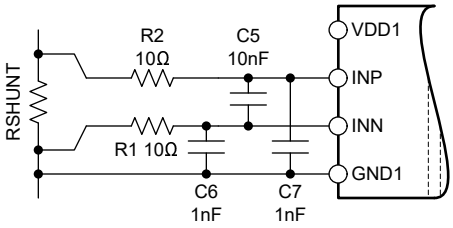

Figure 8-2. Input Filter

8.2.2.2 Connecting the REFIN Pin

The reference input has a finite input impedance as shown in the *Functional Block Diagram* . Consider this impedance when driving the REFIN pin from a high-impedance source. Connect a 100nF capacitor from REFIN to GND2 to filter out high-frequency noise at the reference input. Figure 8-3 shows different options for connecting the REFIN pin.

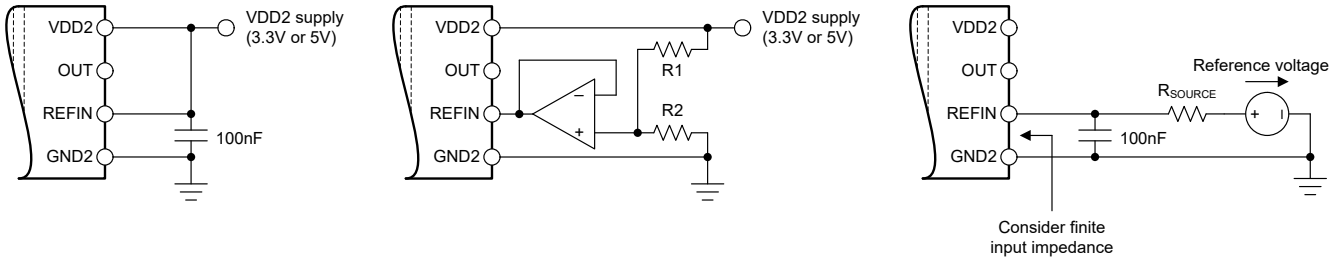

Figure 8-3. Connecting the REFIN Pin

In the first example, REFIN is shorted to VDD2. In the second example, V_{REFIN} is derived from VDD2 through a buffered resistive divider. In the third example, an external voltage source drives the reference input pin.

8.2.3 Application Curves

One important aspect of power-stage design is the effective detection of an overcurrent condition to protect the switching devices and passive components from damage. To power off the system quickly in the event of an overcurrent condition, a low delay caused by the isolated amplifier is required. Figure 8-4 shows the typical full-scale step response of the AMC0x02R-Q1.

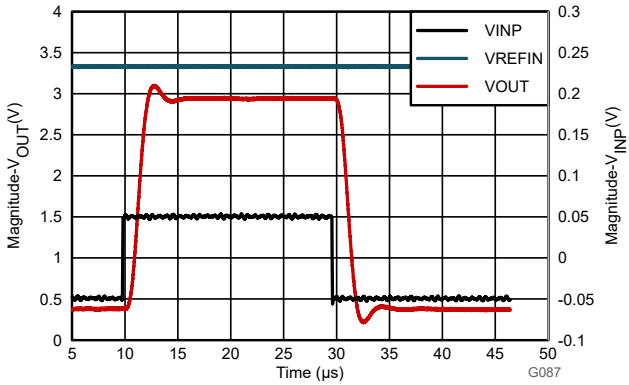

Figure 8-4. Output Step Response of the AMC0x02R-Q1

Figure 8-5 shows the typical step response of the AMC0x02R-Q1 when a transient step is applied on its reference input pin with INP and INN connected to GND1.

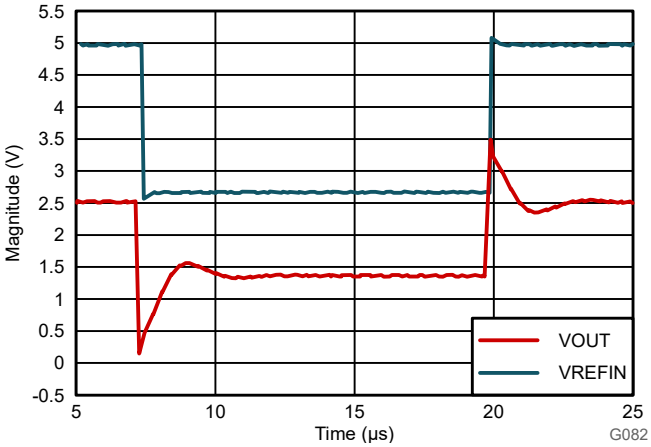

Figure 8-5. Reference Input Step Response of the AMC0x02R-Q1

8.3 Best Design Practices

Place a minimum 10nF capacitor at the device input (from INP to INN). This capacitor helps avoid voltage droop at the input during the sampling period of the switched-capacitor input stage.

Do not short GND1 to INN directly at the device input. For best accuracy, route the ground connection as a separate trace that connects directly to the shunt resistor. See the *Layout Example* section for more details.

Do not leave the inputs of the AMC0x02R-Q1 unconnected (floating) when the device is powered up. If the device inputs are left floating, the input bias current potentially drives the inputs to a positive value that exceeds the operating common-mode input voltage. This condition causes the device to output the fail-safe voltage described in the *Analog Output* section.

Connect the high-side ground (GND1) to INN, either by a hard short or through a resistive path. A DC current path between INN and GND1 is required to define the input common-mode voltage. Do not exceed the input common-mode range specified in the *Recommended Operating Conditions* table.

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8.4 Power Supply Recommendations

In a typical application, the high-side power supply (VDD1) for the AMC0x02R-Q1 is generated from the low-side supply (VDD2) by an isolated DC/DC converter. A low-cost option is based on the push-pull driver SN6501-Q1 and a transformer that supports the desired isolation voltage ratings.

The AMC0x02R-Q1 does not require any specific power-up sequencing. The high-side power supply (VDD1) is decoupled with a low-ESR, 100nF capacitor (C1) parallel to a low-ESR, 1µF capacitor (C2). The low-side power supply (VDD2) is equally decoupled with a low-ESR, 100nF capacitor (C3) parallel to a low-ESR, 1µF capacitor (C4). Place all four capacitors (C1, C2, C3, and C4) as close to the device as possible. Figure 8-6 shows a decoupling diagram for the AMC0x02R-Q1.

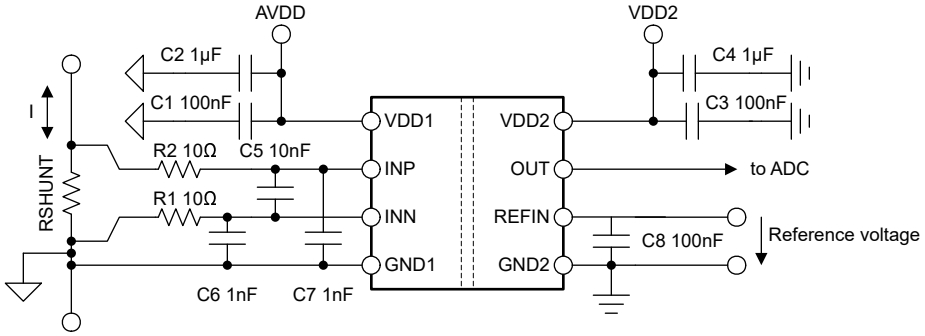


Figure 8-6. Decoupling of the AMC0x02R-Q1

Verify capacitors provide adequate *effective* capacitance under the applicable DC bias conditions experienced in the application. Multilayer ceramic capacitors (MLCC) typically exhibit only a fraction of the nominal capacitance under real-world conditions. Consider this factor when selecting these capacitors. This issue is especially acute in low-profile capacitors, where the dielectric field strength is higher than in taller components. Reputable capacitor manufacturers provide capacitance versus DC bias curves that greatly simplify component selection.

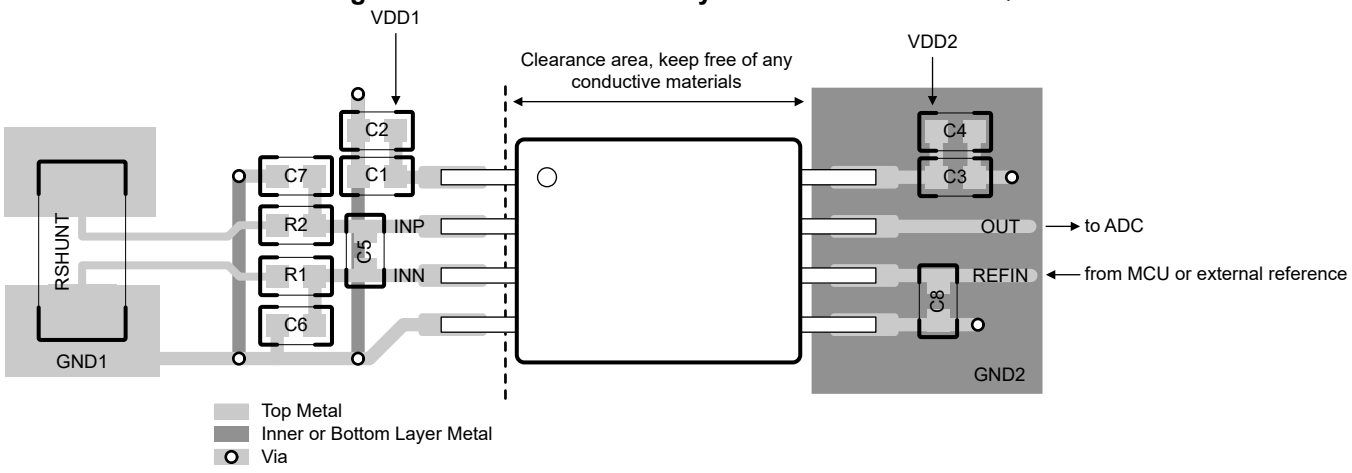
8.5 Layout

8.5.1 Layout Guidelines

The *Layout Example* section details a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC0x02R-Q1 supply pins). This example also depicts the placement of other components required by the device.

8.5.2 Layout Example

Figure 8-7. Recommended Layout of the AMC0x02R-Q1



9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *ISO72x Digital Isolator Magnetic-Field Immunity* application report
- Texas Instrument, *SN6501-Q1 Transformer Driver for Isolated Power Supplies* data sheet
- Texas Instruments, *Isolated Amplifier Voltage Sensing Excel Calculator* design tool

9.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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9.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
December 2025	*	Initial Release

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
AMC0302RQDWVRQ1	Active	Production	SOIC (DWV) | 8	1000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C0302R-Q

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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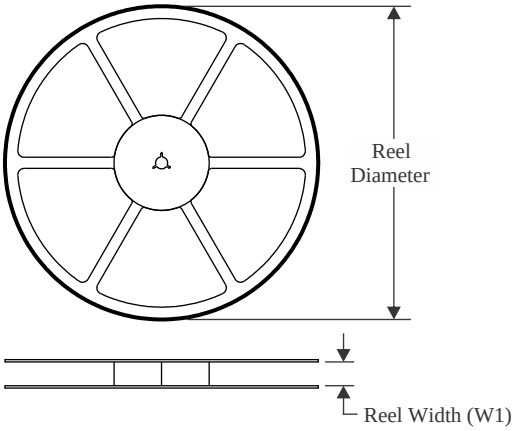
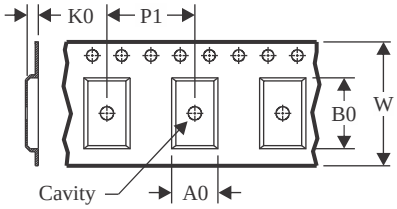
TAPE AND REEL INFORMATION

REEL DIMENSIONS

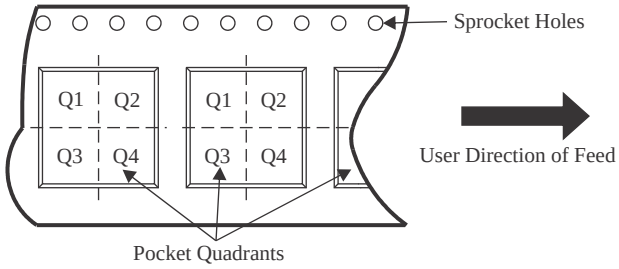


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

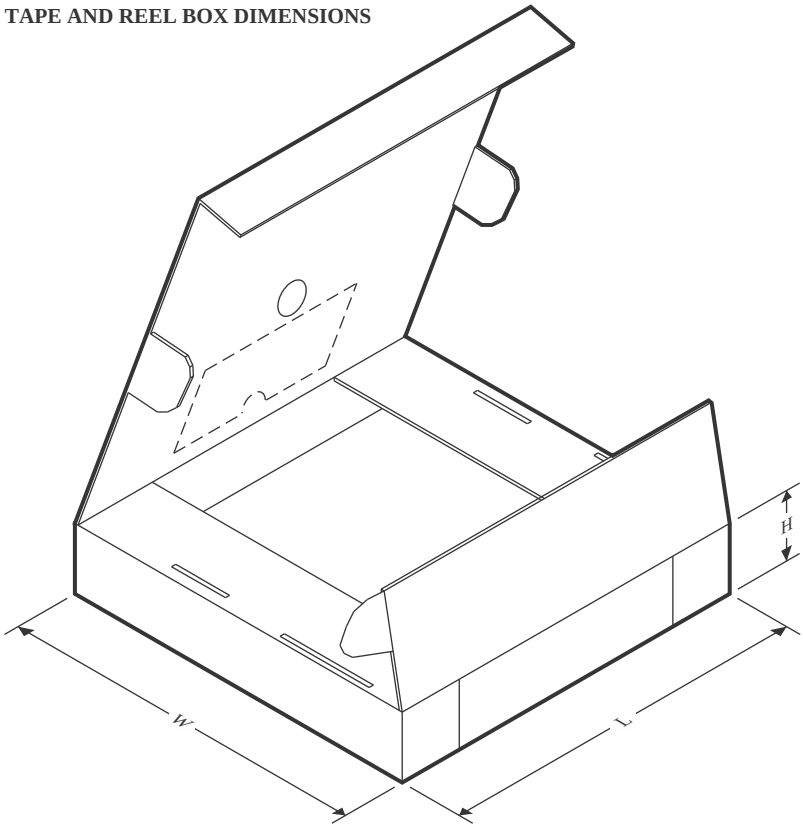
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

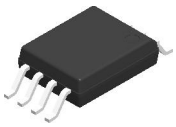
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC0302RQDWVRQ1	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

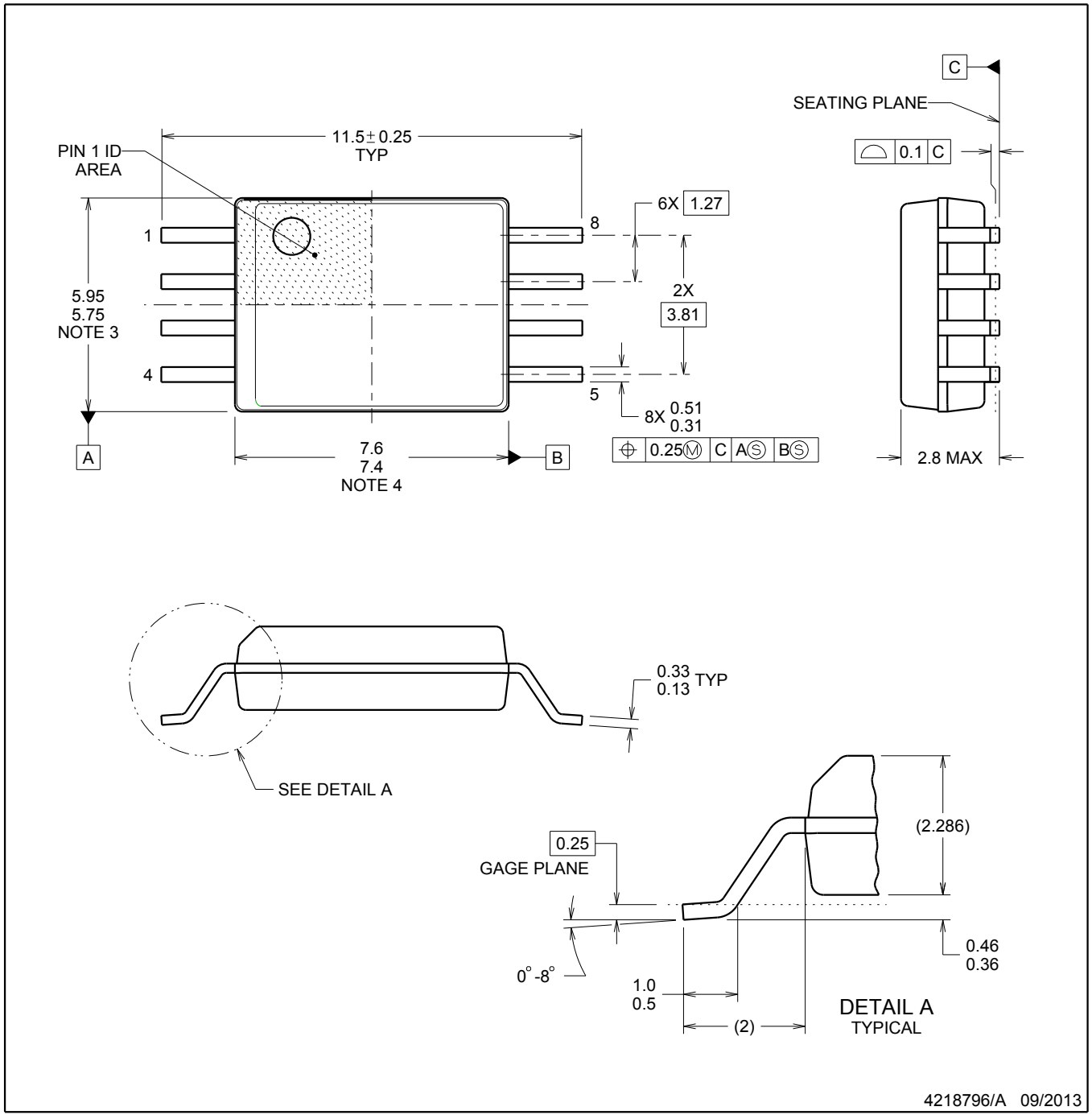
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC0302RQDWVRQ1	SOIC	DWV	8	1000	353.0	353.0	32.0



DWV0008A

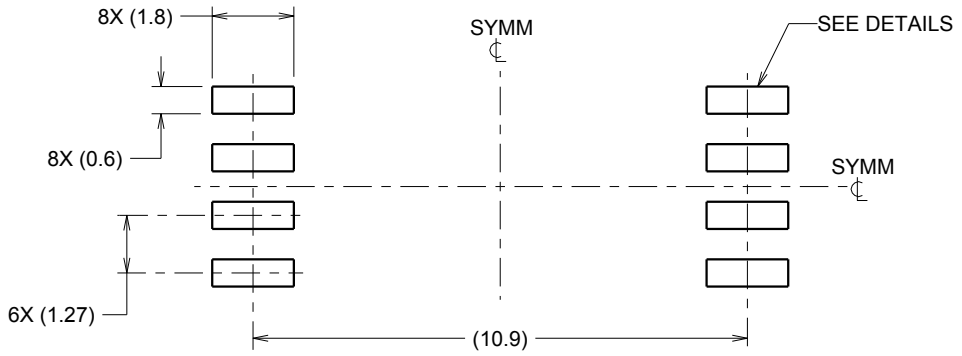
SOIC - 2.8 mm max height

SOIC

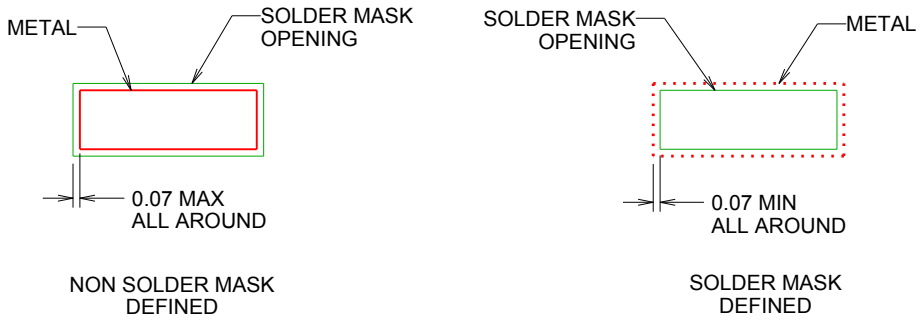


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X



SOLDER MASK DETAILS

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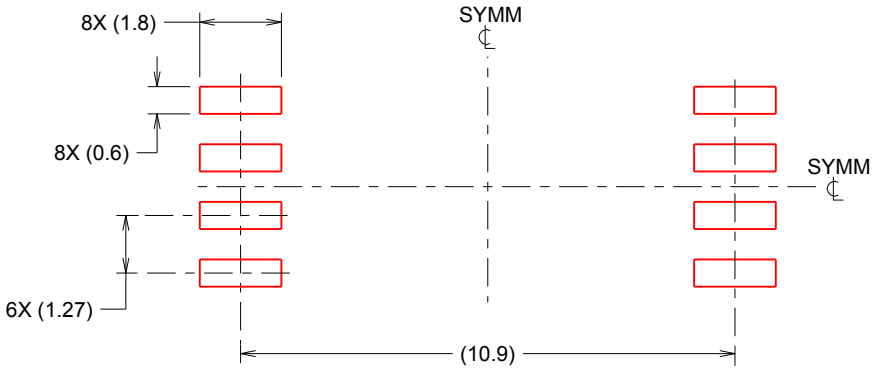
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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