AMC3301 Precision, ±250-mV Input, Reinforced Isolated Amplifier With Integrated DC/DC Converter

1 Features

- 3.3-V or 5-V single supply, CISPR11-compliant operation with integrated DC/DC converter
- ±250-mV input voltage range optimized for current measurement using shunt resistors
- Fixed gain: 8.2
- Low DC errors:
  - Initial offset voltage: ±0.2 mV (max)
  - Offset drift: ±5 µV/°C (max)
  - Initial gain error: ±0.4% (max)
  - Gain drift: ±60 ppm/°C (max)
  - Initial nonlinearity: ±0.075% (max)
- System-level diagnostic features
- Safety-related certifications:
  - 7071-V_{PK} reinforced isolation per DIN VDE V 0884-11 (VDE V 0884-11): 2017-01
  - 5000-V_{RMS} isolation for 1 minute per UL1577
- High CMTI: 75 kV/µs (min)

2 Applications

- Compact, isolated shunt-based current sensing in:
  - Photovoltaic inverters
  - Uninterruptible power supplies
  - Charging piles
  - Power delivery systems
  - Industrial robots
  - Compact frequency inverters

3 Description

The AMC3301 is a precision, isolated amplifier with a fully integrated, isolated DC/DC converter that allows single-supply operation from the low-side of the device. The reinforced capacitive isolation barrier is certified according to VDE V 0884-11 and UL1577 and separates parts of the system that operate on different common-mode voltage levels and protects lower-voltage parts from damage.

The input of the AMC3301 is optimized for direct connection to shunt resistors or other low voltage-level signal sources. The integrated isolated DC/DC converter allows flexible placement of the shunt and the AMC3301, and makes the device a unique solution for space-constrained applications.

The excellent performance of the device supports accurate current monitoring and control, resulting in system-level power savings and, especially in motor control applications, low torque ripple. The integrated input common-mode overvoltage and DC/DC converter operation fault detection features of the AMC3301 simplify system-level design and diagnostics.

The AMC3301 is specified over the extended industrial temperature range of –40°C to +125°C.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
AMC3301	SOIC (16)	10.30 mm × 7.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

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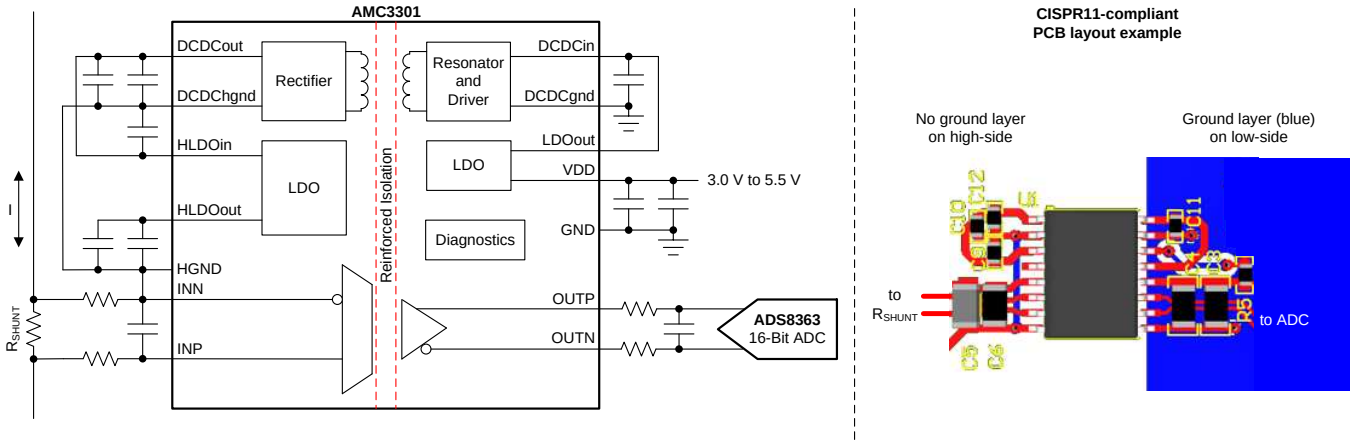
Application Example



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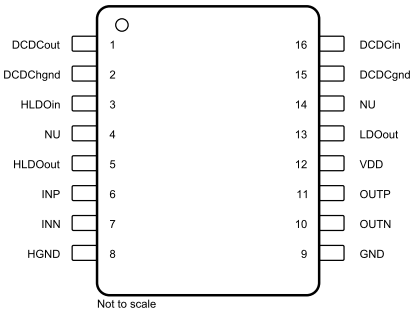
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
August 2019	*	Initial release.

5 Pin Configuration and Functions

DWE Package
16-Pin SOIC
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	DCDCout	—	Secondary-side output of the isolated DC/DC converter, connect to HLDOin. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
2	DCDChgnd	—	Secondary-side ground reference for the isolated DC/DC converter. Connect to HGND pin.
3	HLDOin	—	Input of the secondary-side LDO, connect to DCDCout. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
4, 14	NU	—	Leave these terminals unconnected (floating)
5	HLDOout	—	Output of the secondary-side LDO. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
6	INP	I	Noninverting analog input
7	INN	I	Inverting analog input
8	HGND	—	High-side analog ground. Connect to one of analog input pins close to avoid common-mode input voltage range violations.
9	GND	—	Low-side analog ground. Connect to DCDCgnd pin.
10	OUTN	O	Inverting analog output
11	OUTP	O	Noninverting analog output
12	VDD	—	Low-side power supply, 3.0 V to 5.5 V. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
13	LDOout	—	Output of the primary-side LDO, connect to DCDCin. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.
15	DCDCgnd	—	Primary-side ground reference for the isolated DC/DC converter. Connect to GND pin.
16	DCDCin	—	Primary-side input of the isolated dc/dc converter, connect to LDOout. See the *Power Supply Recommendations* section for power-supply decoupling recommendations.

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6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
Power-supply voltage	VDD to GND	–0.3	6.5	V
Analog input voltage	INP, INN	HGND – 6	HLDOout + 0.5	V
Output voltage	OUTP, OUTN	GND – 0.5	VDD + 0.5	V
Input current	Continuous, any pin except power-supply pins	–10	10	mA
Temperature	Junction, T_J		150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Low-side power supply	VDD to GND	3	3.3	5.5	V
$V_{Clipping}$	Differential input voltage before clipping output	$V_{IN} = V_{INP} – V_{INN}$		±320		mV
V_{FSR}	Specified linear differential full-scale voltage	$V_{IN} = V_{INP} – V_{INN}$	–250		250	mV
	Absolute common-mode input voltage (1)	$(V_{INP} + V_{INN}) / 2$ to HGND	–2		HLDOout	V
V_{CM}	Operating common-mode input voltage	$(V_{INP} + V_{INN}) / 2$ to HGND	–0.16		1	V
T_A	Specified ambient temperature		–40		125	°C

(1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the *Absolute Maximum Ratings* table.

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6.4 Thermal Information

THERMAL METRIC(1)		AMC3301 DWL (SOIC) 16 PINS	UNIT
R_{qJA}	Junction-to-ambient thermal resistance	73.5	°C/W
$R_{qJC(top)}$	Junction-to-case (top) thermal resistance	31	°C/W
R_{qJB}	Junction-to-board thermal resistance	44	°C/W
Y_{JT}	Junction-to-top characterization parameter	16.7	°C/W
Y_{JB}	Junction-to-board characterization parameter	42.8	°C/W
$R_{qJC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation	VDD = 5.5 V			170.5	mW
		VDD = 3.6 V			108	

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6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance (1)	Shortest pin-to-pin distance through air	≥ 8	mm
CPG	External creepage (1)	Shortest pin-to-pin distance across the package surface	≥ 8	mm
DTI	Distance through the insulation	Minimum internal gap (internal clearance - capacitive signal isolation)	≥ 21	µm
		Minimum internal gap (internal clearance - transformer power isolation)	≥ 120	
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112	≥ 600	V
	Material group	According to IEC 60664-1	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 600 V_{RMS}	I-IV	
		Rated mains voltage ≤ 1000 V_{RMS}	I-III	
DIN VDE V 0884-11 (VDE V 0884-11): 2017-01 (2)				
V_{IORM}	Maximum repetitive peak isolation voltage	At AC voltage (bipolar)	1414	V_{PK}
V_{IOWM}	Maximum-rated isolation working voltage	At AC voltage (sine wave); time-dependent dielectric breakdown (TDDB) test; see *Figure 4*	1000	V_{RMS}
		At DC voltage	1414	V_{DC}
V_{IOTM}	Maximum transient isolation voltage	$V_{TEST} = V_{IOTM}$, t = 60 s (qualification test)	7071	V_{PK}
		$V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test)	8485	
V_{IOSM}	Maximum surge isolation voltage (3)	Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.6 \times V_{IOSM} = 10000\ V_{PK}$ (qualification)	6250	V_{PK}
q_{pd}	Apparent charge (4)	Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.2 \times V_{IORM}$, t_m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, t_{ini} = 60 s, $V_{pd(m)} = 1.6 \times V_{IORM}$, t_m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, t_{ini} = 1 s, $V_{pd(m)} = 1.875 \times V_{IORM}$, t_m = 1 s	≤ 5	
C_{IO}	Barrier capacitance, input to output (5)	V_{IO} = 0.5 V_{PP} at 1 MHz	~3.5	pF
R_{IO}	Insulation resistance, input to output (5)	V_{IO} = 500 V at T_A = 25°C	> 10^{12}	Ω
		V_{IO} = 500 V at 100°C ≤ T_A ≤ 125°C	> 10^{11}	
		V_{IO} = 500 V at T_S = 150°C	> 10^9	
	Pollution degree		2	
	Climatic category		55/125/21	
UL1577				
V_{ISO}	Withstand isolation voltage	$V_{TEST} = V_{ISO} = 5000\ V_{RMS}$ or 7071 V_{DC}, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO}$, t = 1 s (100% production test)	5000	V_{RMS}

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves, ribs, or both on a PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings must be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.

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6.7 Safety-Related Certifications

VDE	UL
Certified according to DIN VDE V 0884-11 (VDE V 0884-11): 2017-01, DIN EN 60950-1 (VDE 0805 Teil 1): 2014-08, and DIN EN 60065 (VDE 0860): 2005-11	Recognized under 1577 component recognition and CSA component acceptance NO 5 programs
Reinforced insulation	Single protection
Certificate planned	Certificate planned

6.8 Safety Limiting Values

Safety limiting (1) intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry. A failure ofthe I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheatthe die and damage the isolation barrier potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 73.5°C/W, VDD = 5.5 V, T_J = 150°C, T_A = 25°C, see *Figure 2*			309	mA
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 73.5°C/W, VDD = 3.6 V, T_J = 150°C, T_A = 25°C, see *Figure 2*			472	mA
P_S	Safety input, output, or total power	$R_{\theta JA}$ = 73.5°C/W, T_J = 150°C, T_A = 25°C, see *Figure 3*			1700	mW
T_S	Maximum safety temperature				150	°C

(1) The maximum safety temperature, T_S, has the same value as the maximum junction temperature, T_J, specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S. These limits vary with the ambient temperature, T_A.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times VDD_{max}$, where VDD_{max} is the maximum low-side voltage.

6.9 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = HGND = 0V; typical specifications are at TA = 25°C, and VDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT						
V_{CMov}	Common-mode overvoltage detection level	(V_{INP} + V_{INN}) / 2 to HGND	1			V
	Hysteresis of common-mode overvoltage detection level			94		mV
V_{OS}	Input offset voltage (1)	Initial, at T_A = 25°C, INP = INN = HGND (2)	–0.2	±0.03	0.2	mV
TCV_{OS}	Input offset drift (1)		–5	±1.5	5	uV/°C
CMRR	Common-mode rejection ratio	f_{IN} = 0 Hz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–100		dB
		f_{IN} = 10 kHz, $V_{CM\ min} \le V_{CM} \le V_{CM\ max}$		–98		
PSRR	Power-supply rejection ratio	At dc		–103		dB
		100-mV and 10-kHz ripple		–86		
C_{IN}	Single-ended input capacitance (3)	INN = HGND, f_{IN} = 310 kHz		2		pF
C_{IND}	Differential input capacitance (3)	f_{IN} = 310 kHz		1		
R_{IN}	Single-ended input resistance (3)	INN = HGND		18		kΩ
R_{IND}	Differential input resistance (3)			21		
I_{IB}	Input bias current	INP = INN = HGND; I_{IB} = (I_{IBP} + I_{IBN}) / 2	–41	–30	–24	uA
TCI_{IB}	Input bias current drift			±1		nA/°C
I_{IO}	Input offset current	I_{IO} = I_{IBP} – I_{IBN}		±5		nA

(1) The typical value includes one sigma statistical variation.
(2) The typical value is at VDD1 = 3.3 V.
(3) Also see the Analog Input section for more details.

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Electrical Characteristics (continued)

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, INP = –250 mV to +250 mV, and INN = HGND = 0V; typical specifications are at TA = 25°C, and VDD = 3.3 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG OUTPUT						
	Nominal gain			8.2		
E_G	Gain error (1)	Initial, at T_A = 25°C	–0.4	±0.1	0.4	%
TCE_G	Gain error drift(1)		–60	±20	60	ppm/°C
	Nonlinearity(1)		–0.075	±0.03	0.075	%
	Nonlinearity drift			±1		ppm/°C
THD	Total harmonic distortion	V_{IN} = 0.5 Vpp, f_{IN} = 10 kHz, BW = 100 kHz		–85		dB
	Output noise	INP = INN = HGND, f_{IN} = 0 Hz, BW = 100 kHz		220		mV_{RMS}
SNR	Signal-to-noise ratio	V_{IN} = 0.5 V_{PP}, f_{IN} = 1 kHz, BW = 10 kHz	80	85		dB
		V_{IN} = 0.5 V_{PP}, f_{IN} = 10 kHz, BW = 100 kHz		72		
V_{CMout}	Common-mode output voltage		1.39	1.44	1.49	V
$V_{Failsafe}$	Failsafe differential output voltage	$V_{CM} \geq V_{CMov}$, or $V_{DCDCout} \leq V_{DCDCoutUV}$, or $V_{HLDOout} \leq V_{HLDOoutUV}$		–2.6	–2.5	V
BW_{OUT}	Output bandwidth		250	310		kHz
R_{OUT}	Output resistance	On OUTP or OUTN		< 0.2		Ω
	Output short-circuit current	On OUTP or OUTN		±14		mA
CMTI	Common-mode transient immunity	|HGND – GND| = 2 kV	75	140		kV/µs
POWER SUPPLY						
IDD	Low-side supply current	4.5 V ≤ VDD ≤ 5.5 V		28.5	31	mA
		3.0 V ≤ VDD ≤ 3.6 V		27.5	30	mA
$V_{DCDCout}$	DCDC output voltage	DCDCout to HGND	3.3	3.6	4.2	V
V_{DCDCUV}	DCDC output undervoltage detection threshold voltage	DCDC output falling	2	2.25		V
$V_{HLDOout}$	High-side LDO output voltage	HLDO to HGND	3	3.2	3.4	V
V_{HLDOUV}	High-side LDO output undervoltage detection threshold voltage	HLDO output falling	2.4	2.6		V
I_H	High-side supply current for auxiliary circuitry	additional current available on DCDCout or HLDOout to HGND			1	mA

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6.10 Switching Characteristics

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_r	Output signal rise time	See *Figure 1*		1.3		µs
t_f	Output signal fall time	See *Figure 1*		1.3		µs
	V_{INx} to V_{OUTx} signal delay (50% - 10%)	Unfiltered output, see *Figure 1*		1	1.5	µs
	V_{INx} to V_{OUTx} signal delay (50% - 50%)	Unfiltered output, see *Figure 1*		1.6	2.1	µs
	V_{INx} to V_{OUTx} signal delay (50% - 90%)	Unfiltered output, see *Figure 1*		2.5	3	µs

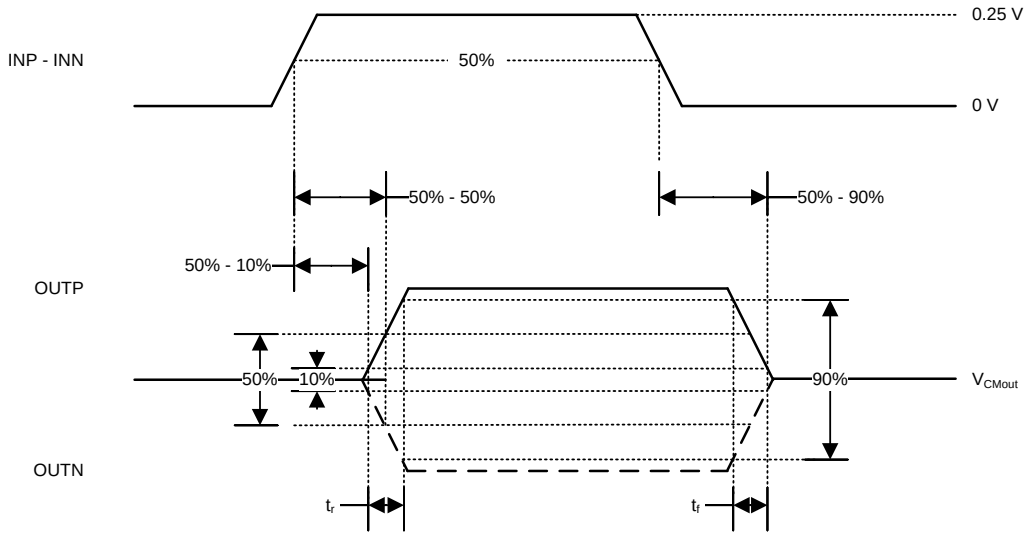

Figure 1. Rise, Fall, and Delay Time Waveforms

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6.11 Insulation Characteristics Curves

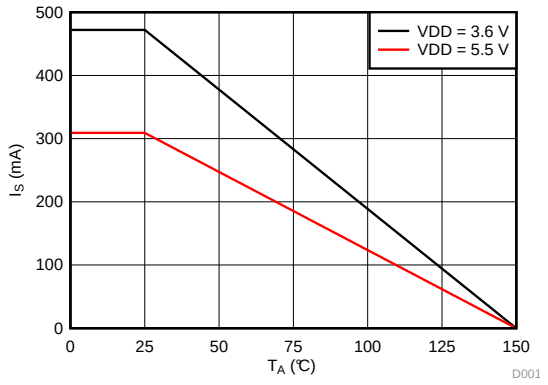


Figure 2. Thermal Derating Curve for Safety-Limiting Current per VDE

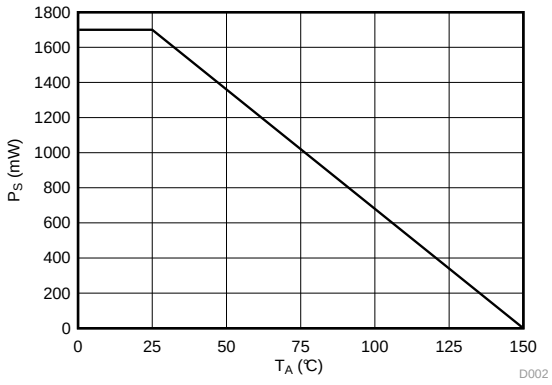
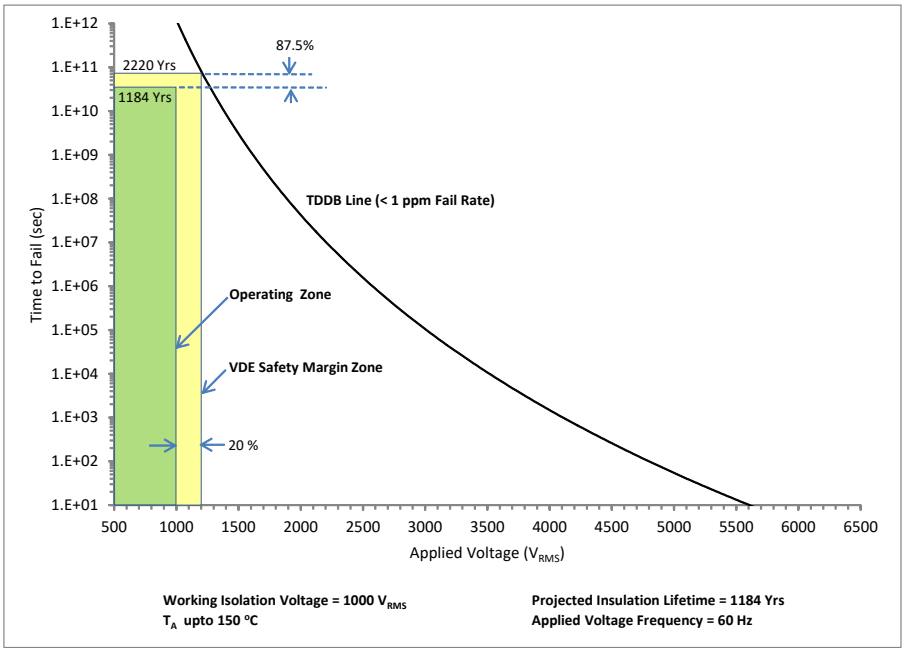


Figure 3. Thermal Derating Curve for Safety-Limiting Power per VDE



T_A up to 150°C, stress-voltage frequency = 60 Hz,
isolation working voltage = 1000 V_{RMS}, operating lifetime = 1184 years

Figure 4. Reinforced Isolation Capacitor Lifetime Projection

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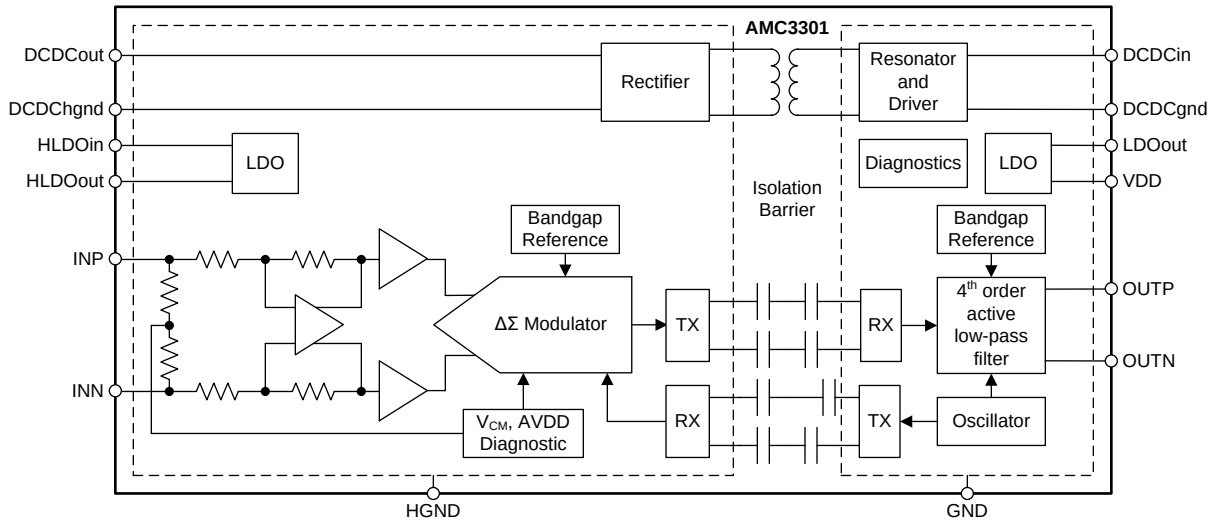
7 Detailed Description

7.1 Overview

The AMC3301 is a fully-differential, precision, isolated amplifier with fully integrated DC/DC converter that allows to supply the device from a single 3.3-V or 5-V voltage supply source on the low-side. The input stage of the device consists of a fully-differential amplifier that drives a second-order, delta-sigma (ΔΣ) modulator. The modulator uses the internal voltage reference and clock generator to convert the analog input signal to a digital bitstream. The drivers (called *TX* in the *Functional Block Diagram*) transfer the output of the modulator across the isolation barrier that separates the high-side and low-side voltage domains. The received bitstream and clock are synchronized and processed by a fourth-order analog filter on the low-side and presented as a differential output of the device, as shown in the *Functional Block Diagram*.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The differential amplifier input stage of the AMC3301 feeds a second-order, switched-capacitor, feed-forward ΔΣ modulator. The gain of the differential amplifier is set by internal precision resistors to a factor of 4 with a differential input impedance of 22 kΩ. The modulator converts the analog signal into a bitstream that is transferred over the isolation barrier, as described in the *Data Isolation Channel Signal Transmission* section.

There are two restrictions on the analog input signals (INP and INN). First, if the input voltage exceeds the range HGND – 6 V to HLDOout + 0.5 V, the input current must be limited to 10 mA because the device input electrostatic discharge (ESD) diodes turns on. In addition, the linearity and noise performance of the device are ensured only when the analog input voltage remains within the specified linear full-scale range (FSR) and within the specified common-mode input voltage range.

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Feature Description (continued)

7.3.2 Data Isolation Channel Signal Transmission

The AMC3301 uses an on-off keying (OOK) modulation scheme to transmit the modulator output bitstream across the SiO_2-based isolation barrier. As shown in Figure 5, the transmitter modulates the bitstream at TX IN with an internally-generated, high-frequency carrier across the isolation barrier to represent a digital *one* and does not send a signal to represent the digital *zero*. The nominal frequency of the carrier used inside the AMC3301 is 480 MHz.

The receiver demodulates the signal after advanced signal conditioning and produces the output. The AMC3301 also incorporates advanced circuit techniques to maximize the CMTI performance and minimize the radiated emissions caused by the high-frequency carrier and IO buffer switching.

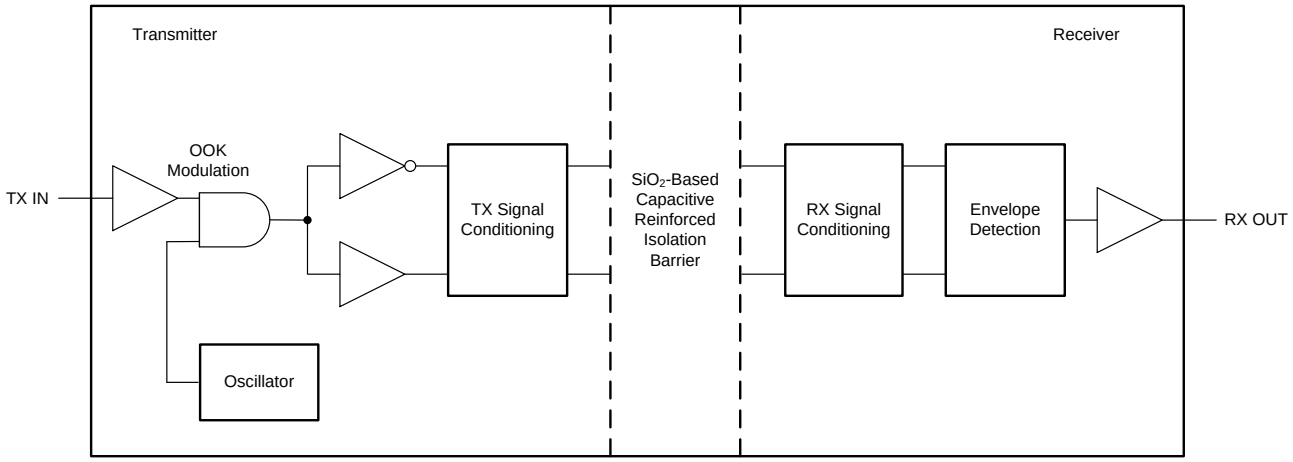


Figure 5. Block Diagram of a Data Isolation Channel

Figure 6 shows the concept of the OOK scheme.

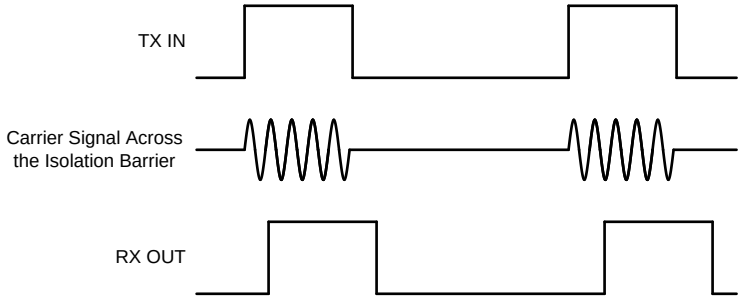


Figure 6. OOK-Based Modulation Scheme

Feature Description (continued)

7.3.3 Isolated DC/DC Converter

The AMC3301 offers a fully integrated isolated DC/DC converter stage that includes following components that are shown in the *Functional Block Diagram* section:

- A low-dropout regulator (LDO) on the primary side to stabilize the supply voltage VDD that drives the primary side of the converter
- Primary full-bridge inverter and drivers
- Laminate-based, air-core transformer for high immunity to magnetic fields
- Secondary full-bridge rectifier
- Secondary LDO to stabilize the output voltage of the DC/DC converter for high analog performance of the signal path

The DC/DC converter utilizes spread-spectrum clock generation technique to reduce the spectral density of the electromagnetic radiation. The resonator frequency is synchronous to the operation of the ΔΣ modulator to minimize the interference and support the high analog performance of the device.

The architecture of the DC/DC converter is optimized to drive the high-side circuitry of the AMC3301 (fully-differential gain stage, modulator etc.) and to offer additional current for optional auxiliary circuit (i.e. active fllter or pre-amplifier) called I_H as specified in the *Electrical Characteristics* table.

7.3.4 Fail-Safe Output

The AMC3301 offers a fail-safe output that simplifies diagnostics on system level. The fail-safe output is active in two cases:

- When the integrated DC/DC converter doesn't deliver the required supply voltage on the secondary side of the device, or
- When the common-mode input voltage, that is V_{CM} = (INP + INN) / 2, exceeds the minimum common-mode over-voltage detection level V_{CMov}.

Figure 7 and Figure 8 show the fail-safe output of the AMC3301 that is a negative differential output voltage value that does not occur under normal device operation. As a reference value for the fail-safe detection on a system level, use the $V_{FAILSAFE}$ voltage as specified in the *Electrical Characteristics*.

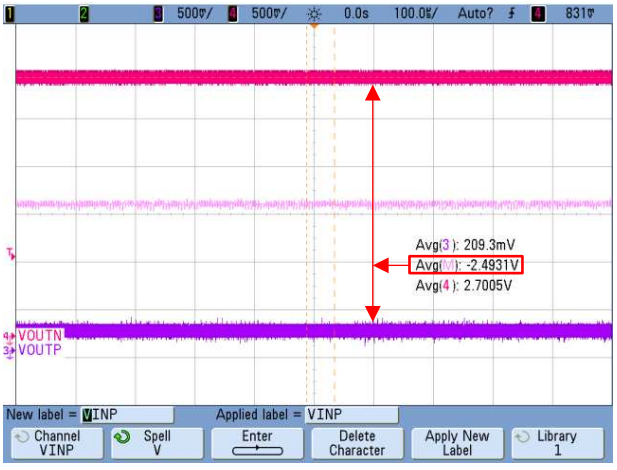


Figure 7. Typical Negative Clipping Output of the AMC3301

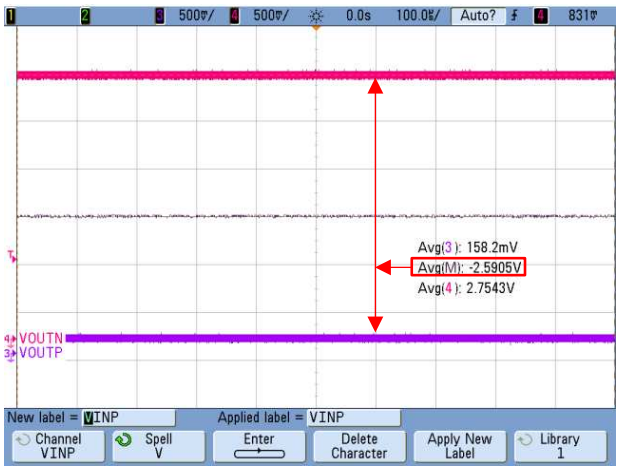


Figure 8. Typical Failsafe Output of the AMC3301

7.4 Device Functional Modes

The AMC3301 is operational when the power supply VDD is applied, as specified in *Recommended Operating Conditions* table.

ADVANCE INFORMATION

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The low input voltage range, very low nonlinearity, and temperature drift make the AMC3301 a high-performance solution for industrial applications where shunt-based current sensing with high common-mode voltage levels is required. The integrated isolated DC/DC converter offers additional flexibility for placement of the shunt and the AMC3301, system layout optimization, and results in smaller PCB size comparing to solutions based on discrete components.

8.2 Typical Application

Isolated amplifiers are widely used in frequency inverters that are critical parts of industrial motor drives, photovoltaic inverters, uninterruptible power supplies, and other industrial applications. The input structure of the AMC3301 is optimized for use with low-value shunt resistors in current sensing applications.

Figure 9 shows a typical operation of the AMC3301 for current sensing in a frequency inverter application. This simplified schematics ommits the required power supply and decoupling details. Phase current measurement is accomplished through the shunt resistors, R_{SHUNT} (in this case, a two-pin shunts). The differential input and the high common-mode transient immunity of the AMC3301 ensure reliable and accurate operation even in high-noise environments (such as the power stage of the motor drive). The high-impedance input and wide input voltage range make the AMC1311 suitable for dc bus voltage sensing.

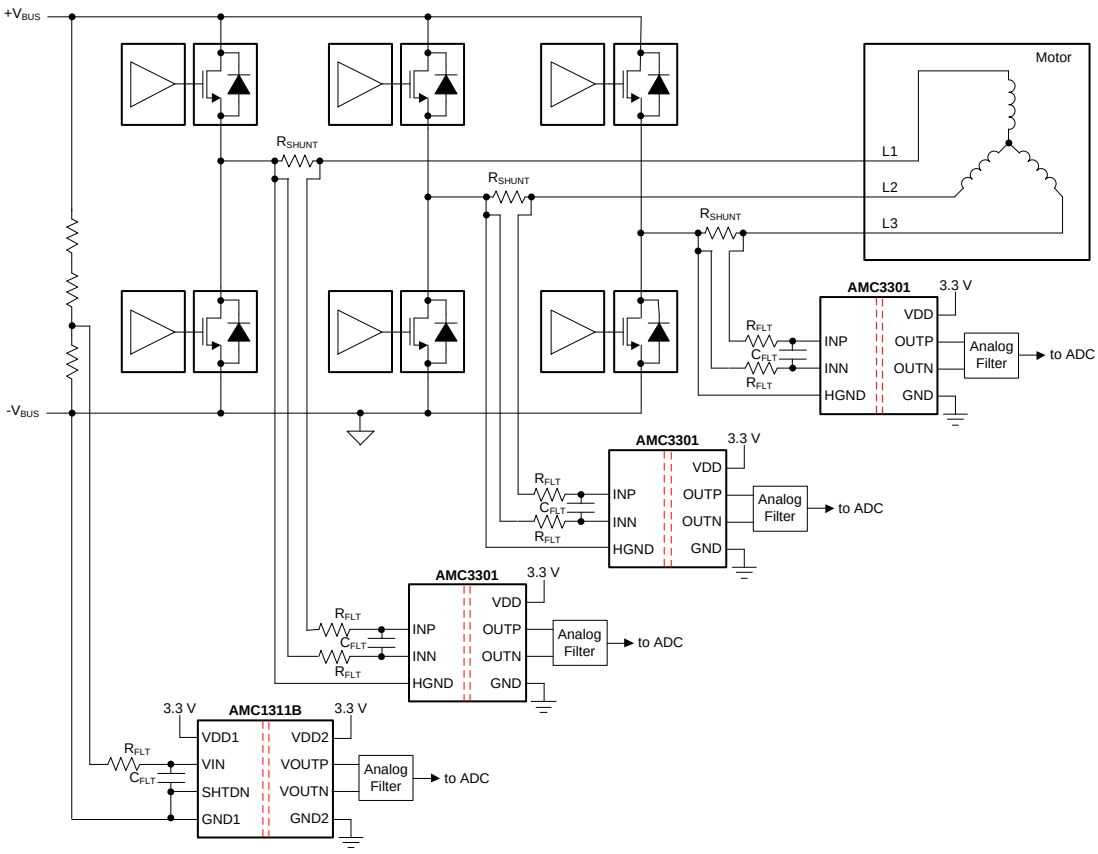


Figure 9. Using the AMC3301 for Current Sensing in Frequency Inverters

Typical Application (continued)

8.2.1 Design Requirements

Table 1 table lists the parameters for this typical application.

Table 1. Design Requirements

PARAMETER	VALUE
Supply voltage	3.3 V or 5 V
Voltage drop across the shunt for a linear response	± 250 mV (maximum)
Signal delay (50% VIN to 90% OUTP, OUTN)	3 µs (maximum)

8.2.2 Detailed Design Procedure

The AMC3301 is powered from the low-side power supply (VDD). Further details are provided in the *Power Supply Recommendations* section.

The floating ground reference (HGND) is derived from one of the ends of the shunt resistor that is connected to the negative input of the AMC3301 (INN). If a four-pin shunt is used, the inputs of the AMC3301 device are connected to the inner leads and HGND is connected to one of the outer shunt leads.

Use Ohm's Law to calculate the voltage drop across the shunt resistor (V_{SHUNT}) for the desired measured current: $V_{SHUNT} = I \times R_{SHUNT}$.

Consider the following two restrictions to choose the proper value of the shunt resistor R_{SHUNT}:

- The voltage drop caused by the nominal current range must not exceed the recommended differential input voltage range: $V_{SHUNT} \leq \pm 250$ mV
- The voltage drop caused by the maximum allowed overcurrent must not exceed the input voltage that causes a clipping output: $V_{SHUNT} \leq V_{Clipping}$

For systems using single-ended input ADCs, Figure 10 shows an example of a TLV6001-based signal conversion and filter circuit as used on the AMC1311EVM. Tailor the bandwidth of this filter stage to the bandwidth requirement of the system and use NP0-type capacitors for best performance.

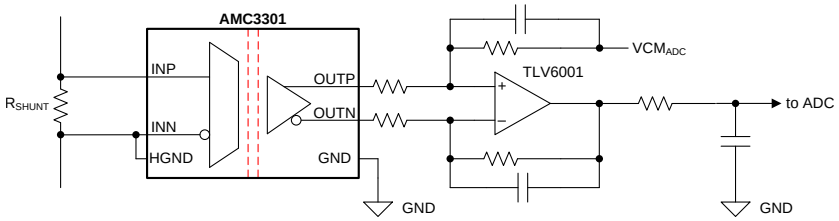


Figure 10. Connecting the AMC3301 Output to Single-Ended Input ADC

For more information on the general procedure to design the filtering and driving stages of SAR ADCs, see *18-Bit, 1MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* and *18-Bit Data Acquisition Block (DAQ) Optimized for Lowest Power*, available for download at www.ti.com.

8.3 What to Do and What Not to Do

Do not leave the inputs of the AMC3301 unconnected (floating) when the device is powered up. If both device inputs are left floating, the input bias current drives these inputs to the output common-mode of the analog front-end of approximately 2 V. As result, the internal common-mode overvoltage detector turns on and the output functions as described in the *Fail-Safe Output* section, which may lead to an undesired reaction on the system level.

ADVANCE INFORMATION

9 Power Supply Recommendations

The AMC3301 is powered from the low-side power supply (VDD) with a nominal value of 3.3 V (or 5 V) ± 10%. TI recommends a low-ESR decoupling capacitor of 1 nF (C4 in Figure 11) placed as close as possible to the VDD pin, followed by a 1-µF capacitor (C3) to filter this power-supply path.

The primary-side of the DC/DC converter is decoupled with low-ESR 0.1-µF capacitor (C11) positioned close to the device between pins DCDCin and DCDCgnd. Use a combination of low-ESR, 100-nF capacitor (C12) placed as close as possible to the DCDCout and DCDChgnd pins, followed by a 1-µFcapacitor (C10) for decoupling of the secondary side. The secondary-side ground reference DCDChgnd and HGND pins are connected to one end of the shunt resistor, that is also connected to the negative input (INN) of the device. If a four-pin shunt is used, the device inputs are connected to the inner leads, while HGND and DCDChgnd are connected to one of the outer leads of the shunt.

For the secondary-side LDO, use low-ESR capacitors of 1nF (C9), placed as close as possible to the HLDOin pin and a combination of low-ESR 1-nF (C6) and 100-nF (C5) decoupling capacitors. Place C6 as close as possible to the HLDOout pin.
See the *Layout Guidelines* section for the corresponding layout recommendation.

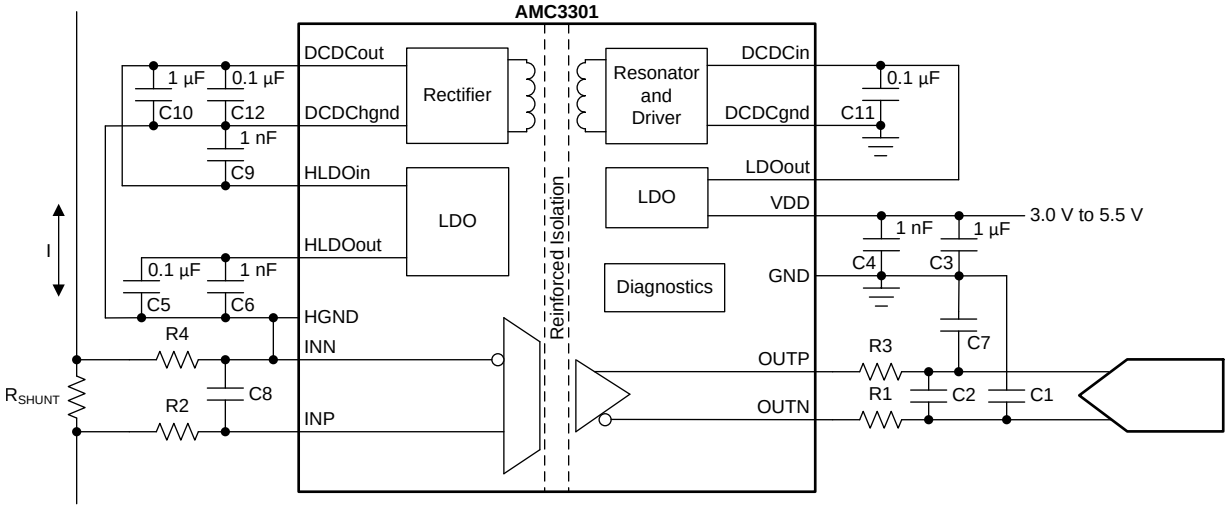


Figure 11. AMC3301 Power Supply Decoupling Scheme

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

Figure 12 shows a layout recommendation with the critical placement of the decoupling capacitors (as close as possible to the AMC3301 supply pins) and uses the same reference designators as used in the *Power Supply Recommendations* section. For best performance, place the shunt resistor close to the INP and INN inputs of the AMC3301 and keep the layout of both connections symmetrical.

To avoid violation of the operating common-mode input voltage specification and reduce the electromagnetic radiation, connect one of the analog inputs (INN or INP) to high-side analog ground reference (HGND) as close as possible to the AMC3301.

This layout is used on the AMC3301EVM and supports CISPR-11 compliant electromagnetic radiation levels.

10.2 Layout Example

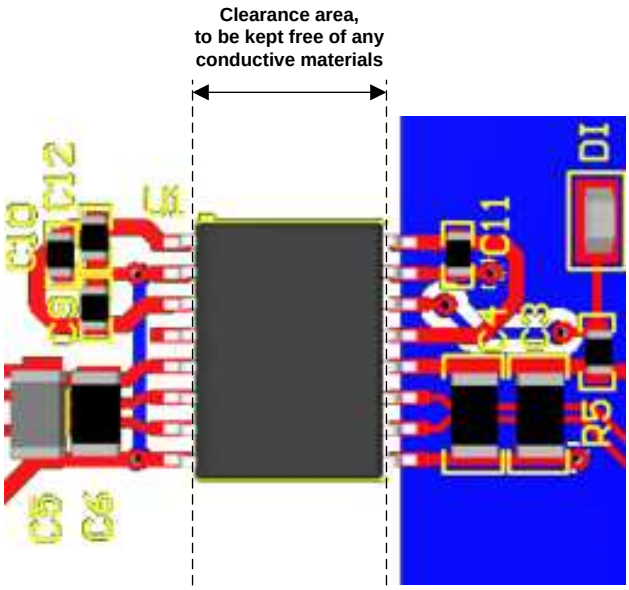


Figure 12. Recommended Layout of the AMC3301

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Isolation Glossary* application report
- Texas Instruments, *Dual, 1MSPS, 16-/14-/12-Bit, 4×2 or 2×2 Channel, Simultaneous Sampling Analog-to-Digital Converter* data sheet
- Texas Instruments, *Semiconductor and IC Package Thermal Metrics* application report
- Texas Instruments, *AMC1311x High-Impedance, 2-V Input, Reinforced Isolated Amplifier* data sheet
- Texas Instruments, *TLV600x Low-Power, Rail-to-Rail In/Out, 1-MHz Operational Amplifier for Cost-Sensitive Systems* data sheet
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Distortion and Noise* reference guide
- Texas Instruments, *18-Bit, 1-MSPS Data Acquisition Block (DAQ) Optimized for Lowest Power* reference guide

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC3301DWE	PREVIEW	SOIC	DWE	16	40	TBD	Call TI	Call TI	-40 to 125		
AMC3301DWER	PREVIEW	SOIC	DWE	16	2000	TBD	Call TI	Call TI	-40 to 125		
PAMC3301DWER	ACTIVE	SOIC	DWE	16	2000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

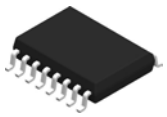
(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

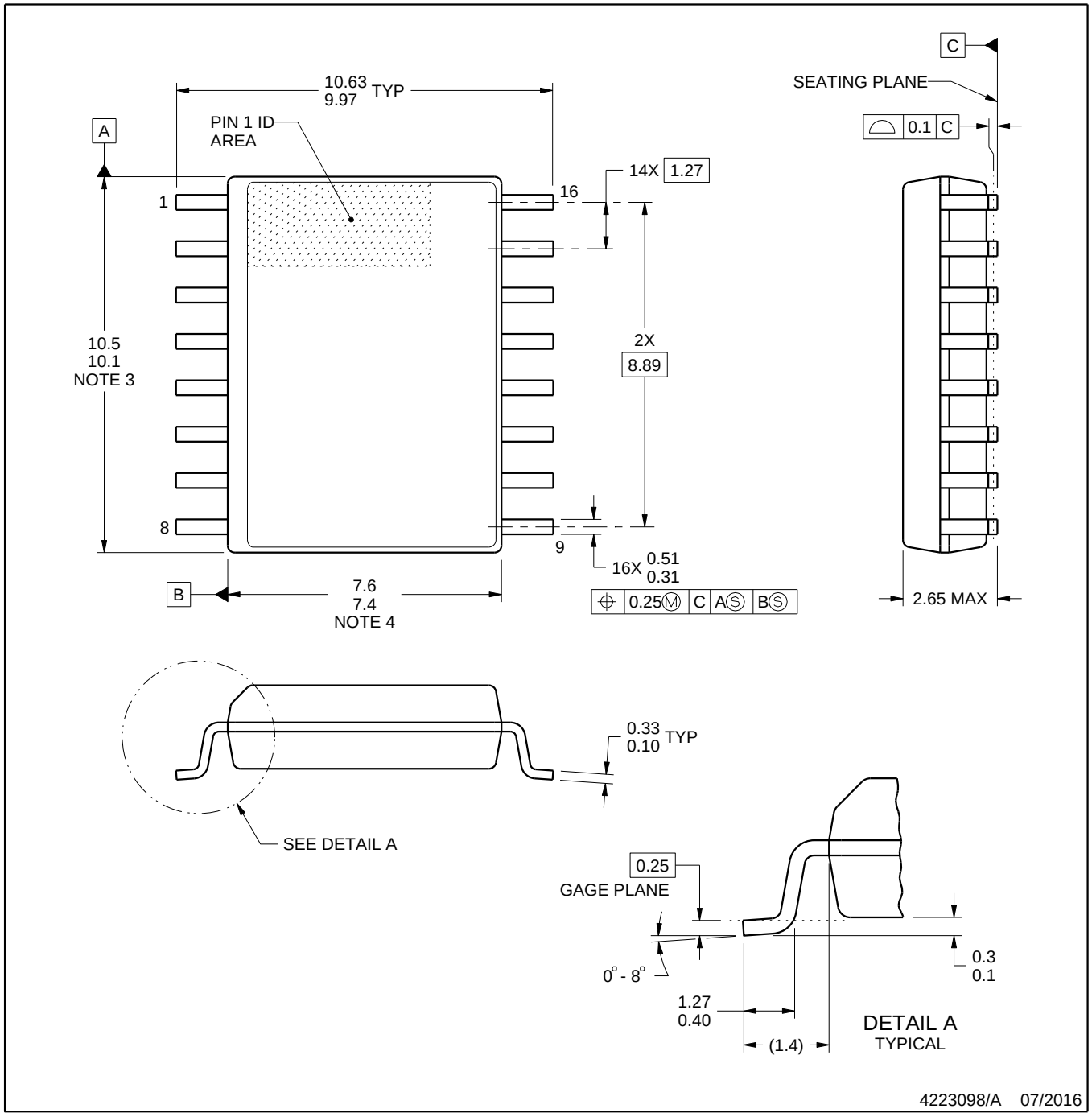


PACKAGE OUTLINE

DWE0016A

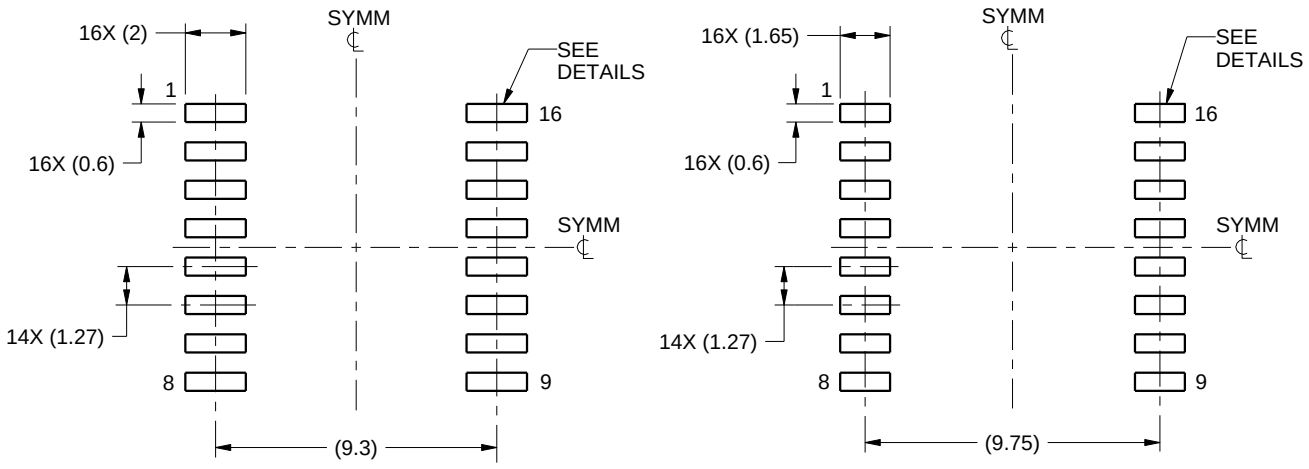
SOIC - 2.65 mm max height

SOIC



NOTES:

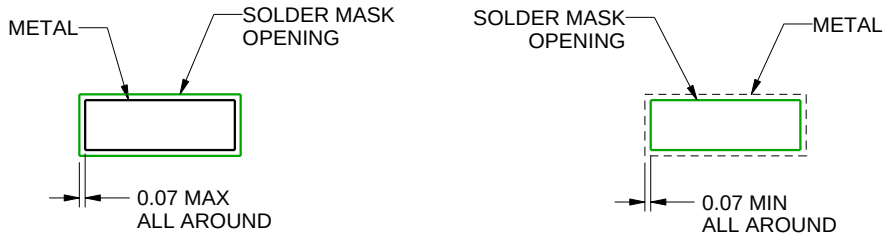
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X



NON SOLDER MASK DEFINED

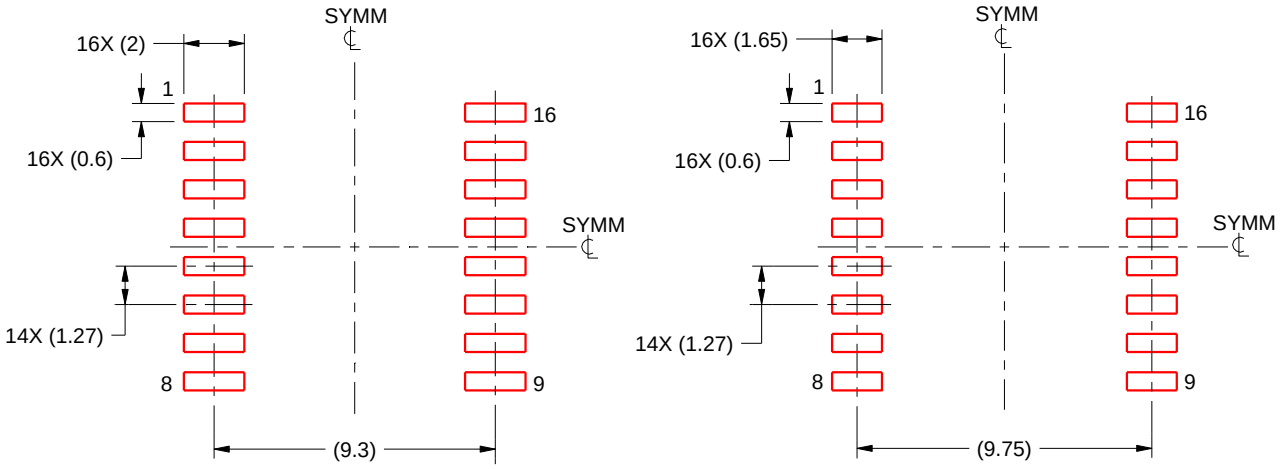
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4223098/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4223098/A 07/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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