BQ25886 Standalone 2-Cell, 2-A Boost-Mode Battery Charger With PowerPath, USB BC1.2 Detection, and USB On-The-Go Boost (OTG)

1 Features

- High-efficiency 2-A, 1.5-MHz switch mode boost charger
  - 93.4% Charge efficiency at 5-V adapter, 7.6-V battery, 1-A charge
  - Optimized for USB input and 2-cell Li-Ion battery
- Single input to support USB input adapters
  - Supports 4.3-V to 6.2-V input voltage range with 20-V absolute maximum input voltage rating
  - Input current limit (500 mA to 3.3 A) to support USB2.0, USB3.0 standard adapters
  - Integrated USB D+/D- auto-detect USB SDP, CDP, DCP, and non-standard adapters
- Standalone function with PowerPath management
  - Highest battery discharge efficiency with 17-mΩ battery discharge MOSFET
  - Narrow VDC (NVDC) PowerPath management
    - Instant-on works with no battery or deeply discharged battery
    - Ideal diode operation in battery supplement mode
  - Adjustable charge voltage with VSET pin supports 8.2 V, 8.4 V, 8.7 V, and 8.8 V
  - Adjustable charge current with ICHGSET pin supports 100 to 2200 mA
  - Adjustable input current limit with ILIM pin
- Input current optimizer (ICO) to maximize input power without overloading adapters
- High integration includes all MOSFETs, current sensing and loop compensation
- High accuracy
  - ±0.5% Charge voltage regulation
  - ±5% Charge current regulation
  - ±7.5% Input current regulation
- Safety
  - Battery temperature sensing in charge
  - Thermal regulation and thermal shutdown

2 Applications

- Wireless speaker
- Smart Speaker
- EPOS Printer
- Portable POS
- IP network camera

3 Description

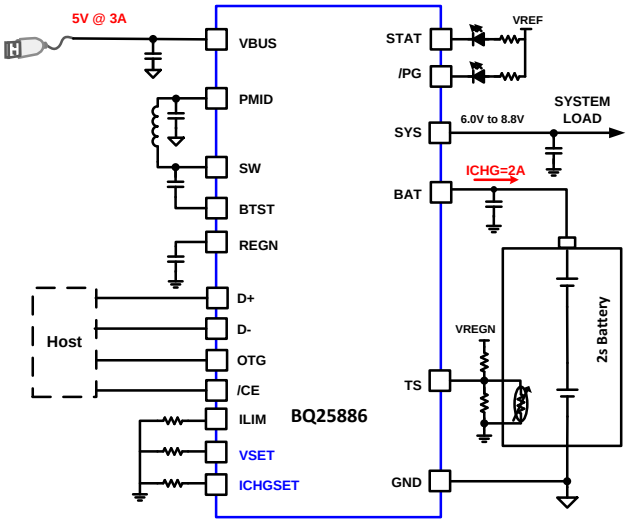
The BQ25886 is a highly-integrated 2-A boost switch-mode battery charge management and system PowerPath management which enables instant power on and provides accurate termination control device for 2-cell (2s) Li-Ion and Li-polymer battery. The BQ25886 is a standalone solution with PowerPath and OTG.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ25886	VQFN (24)	4.00 mm x 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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4 Revision History

Changes from Original (March 2019) to Revision A	Page
• Changed from Advance Information to Production Data	1

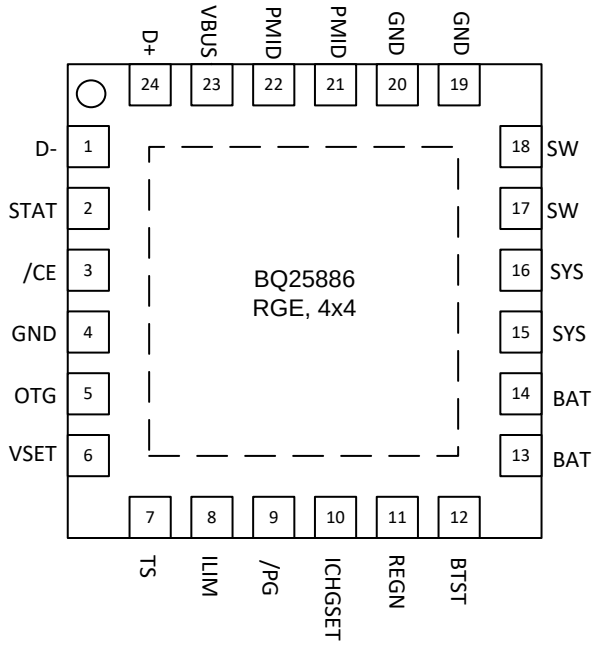
5 Device Comparison Table

Table 1. Device Comparison

PART NUMBER	BQ25882	BQ25883	BQ25886	BQ25887
VBUS Operating Range	3.9 to 6.2 V	3.9 to 6.2 V	4.3 to 6.2 V	3.9 to 6.2 V
USB Detection	D+/D-	D+/D-	D+/D-	PSEL
PowerPath	Yes	Yes	Yes	No
Cell Balancing	No	No	No	Yes
OTG	Up to 2 A	Up to 2 A	Up to 2 A	No OTG
16 bit ADC	Yes	Yes	No	Yes
Control Interface	I2C	I2C	Standalone	I2C
Status Pin	/PG	STAT, /PG	STAT, /PG	STAT, /PG
Package	2.1x2.1 WCSP-25	4x4 QFN-24	4x4 QFN-24	4x4 QFN-24

6 Pin Configuration and Functions

RGE Package (Standalone)
24-Pin VQFN
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D+	24	AIO	**Positive USB data line –** D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and secondary detection in BC1.2.
D–	1	AIO	**Negative USB data line –** D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD) and secondary detection in BC1.2.
STAT	2	DO	**Open drain charge status indicator –** Connect to the pull-up rail via 10-kΩ resistor. LOW indicates charge in progress. HIGH indicates charge complete or charge disabled. When any fault occurs, the STAT pin blinks at 1Hz.
$\overline{CE}$	3	DI	**Active Low Charge Enable Pin –** Battery charging is enabled when $\overline{CE}$ pin is LOW. $\overline{CE}$ pin is internally pulled low with 900k-Ω resistor.
OTG	5	DI	**OTG –** USB On-The-Go Enable input. Pull high to enable OTG function. Pull low to disable OTG function.
VSET	6	AI	**Battery Charge Voltage Limit –** VSET pin sets battery charge voltage. Program battery regulation voltage with a resistor pull-down from VSET to GND as follows: R_{VSET}< 18kΩ (short to GND) = 8.2 V R_{VSET}= 39kΩ (±10%) = 8.8 V R_{VSET}= 75kΩ (±10%) = 8.7 V R_{VSET}> 150kΩ (floating) = 8.4 V
TS	7	AI	**Temperature Qualification Voltage –** Connect a negative temperature coefficient thermistor. Program temperature window with a resistor divider from REGN to TS to GND. Charge suspends when TS pin is out of range. Recommend 103AT-2 thermistor.
ILIM	8	AI	**Input Current Limit (IINDPM) –** ILIM pin sets the maximum input current and can be used to monitor input current. IINDPM loop regulates ILIM pin voltage at 0.8V. When ILIM pin is less than 0.8V, the input current can be calculated by IIN = KILIM x VILIM / (RILIM x 0.8V). A resistor connected from ILIM pin to ground sets the input current limit as maximum (IINMAX = KILIM / RILIM). When ILIM pin is short to GND, the input current limit is set to maximum by ILIM. Input current limit less than 500mA is not supported on ILIM pin. Do not float this pin.

Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
$\overline{PG}$	9	DO	**Open drain active low power good indicator –** Connect to the pull up rail via 10-kΩ resistor. LOW indicates a good input source if the input voltage is within VVBUS_OP (3.9 V), and can provide more than IPOORSRC (30 mA).
ICHGSET	10	AI	**Charge Current Limit –** A resistor from ICHGSET to GND is used to program the charge current. The acceptable programming range on ICHGSET pin is 30mA (114Ω) – 2.2A (8kΩ). Pre-charge and termination current is 1/10 of the fast charge current. The minimum pre-charge current is clamped at 30mA (typ). Minimum termination current is clamped at 10mA (typ). ICHGSET short to GND clamps charge current to minimum setting 30mA (typ). Floating ICHGSET disables charge.
REGN	11	P	**Gate Drive Supply –** Bias supply for internal MOSFETs driver and IC. Bypass REGN to GND with a 4.7-µF ceramic capacitor. REGN current limit is 50 mA.
BTST	12	P	**PWM High-side Driver Supply –** Internally, BTST is connected to the cathode of the boot-strap diode. Connect a 47nF bootstrap capacitor from SW to BTST.
BAT	13, 14	P	**Battery Power Connection –** Connect minimum recommended 10-µF capacitance after derating closely to the BAT pin and GND.
SYS	15, 16	P	**System Connection –** The internal BATFET is connected between SYS and BAT. When the battery falls below the minimum system voltage, the switch-mode converter keeps SYS above the minimum system voltage. Connect a 2x22-µF capacitance after derating closely to the SYS pin and PGND.
SW	17, 18	P	**Inductor Connection –** Connect to the switched side of the external inductor.
GND	19, 20, 4	–	**Ground Return**
PMID	21, 22	P	**Blocking MOSFET Connection –** The minimum recommended total input low-ESR capacitance on VBUS and PMID, after applied derating, is 10 uF. At least 1-uF is recommended at VBUS with the remainder at PMID. Typical value for PMID is 10 uF.
VBUS	23	P	**Input Supply –** VBUS is connected to the external DC supply. Bypass VBUS to GND with at least 1-µF ceramic capacitor, placed as close to the IC as possible.
NC	1	–	**No Connect –** Leave these pins floating or tie to ground.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Voltage Range (with respect to GND unless otherwise specified)	VBUS (converter not switching)	-0.3	20	V
	PMID (converter not switching)	-0.3	8.5	V
	BAT, SYS (converter not switching)	-0.3	12	V
	SW	-0.3 (2)	13	V
	BTST	-0.3	19	V
	REGN, STAT, /PG, TS	-0.3	6	V
	ILIM	-0.3	5	V
	BTST to SW	-0.3	6	V
	D+, D-, ICHGSET, VSET, /CE	-0.3	6	V
Output Sink Current	STAT, /PG		6	mA
Junction Temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Theseare stress ratings only, which do not imply functional operation of the device at these or anyother conditions beyond those indicated under *Recommended OperatingConditions*. Exposure to absolute-maximum-rated conditions for extended periods mayaffect device reliability.
(2) -2V for 50ns

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input Voltage	4.3		6.2	V
I_{VBUS}	Average input current (VBUS)			3.3	A
I_{BAT}	Average charge current (IBAT)			2.2	A
I_{BAT_RMS}	RMS discharging current with internal MOSFET			5	A
I_{BAT_PK}	Peak discharging current with internal MOSFET			9 (up to 1us)	A
V_{BAT}	Battery Voltage			9.2 (1)	V
T_A	Operating free-air temperature range	-40		85	°C

(1) The inherent switching noise voltage spikes should not exceed the absolute maximum rating on SW pin. A tight layout minimizes switching noise.

7.4 Thermal Information

over operating free-air temperature range (unless otherwise noted)

THERMAL METRIC(1)		BQ25886 RGE (VQFN) 24-PIN	UNIT
$R_{\Theta JA}$	Junction-to-ambient thermal resistance (EVM(2))	18	°C/W
$R_{\Theta JA}$	Junction-to-ambient thermal resistance (JEDEC (1))	32.4	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	26.7	°C/W
$R_{\Theta JB}$	Junction-to-board thermal resistance	10.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.6	°C/W
$R_{\Theta\ JC(bot)}$	Junction-to-case (bottom) thermal resistance	3.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953.
(2) Measured on 35µm thick copper, 4-layer board

7.5 Electrical Characteristics

$V_{VBUS\_UVLO\_RISING}$< V_{VBUS} < V_{VBUS_OV}, T_J = -40°C to+125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{BAT}	Battery discharge current (BAT)	VBAT = 9 V, No VBUS, SCL, SDA = 0 V or 1.8 V, T_J=25C, ADC Disabled		12	14	µA
		VBAT = 9 V, No VBUS, SCL, SDA = 0 V or 1.8 V, T_J < 85C, ADC Disabled		12	20	µA
I_{VBUS_HIZ}	Input supply current (VBUS) in HIZ	VBUS = 5 V, High-Z Mode, no battery, 25℃		30	48	µA
		VBUS = 5 V, High-Z Mode, no battery, <85℃		30	55.2	µA
I_{VBUS}	Input supply current (VBUS)	VBUS = 5 V, V_{BAT} = 7.6 V, converter not switching		1.5	3	mA
		VBUS = 5 V, V_{BAT} = 7.6 V, converter switching, I_{SYS} = 0A		3		mA
VBUS/VBAT POWER UP						
V_{VBUS_OP}	VBUS operating range		4.3		6.2	V
$V_{VBUS\_UVLO\_RISING}$	VBUS rising, no battery	VBUS rising		3.3	3.68	V
V_{VBUS_OV}	VBUS over-voltage rising threshold	VBUS rising	6.2		6.6	V
	VBUS over-voltage falling threshold	VBUS falling	5.9		6.4	V
$V_{POORSRC\_FALLING}$	Bad adapter detection threshold	VBUS falling below $V_{POORSRC\_FALLING}$		3.7		V
$I_{POORSRC}$	Bad adapter detection current source			15		mA
POWER-PATH						
V_{SYS}	Typical System Regulation Voltage	ISYS = 0A, VBAT = 8.80 V > SYS_MIN, Charge Disabled		100		mV
		ISYS = 0A, VBAT < SYS_MIN, Charge Disabled		200		mV
V_{SYS_MIN}	System Regulation Voltage	VBAT < SYS_MIN, Charge Disabled	6.2	6.4		V
BATTERY CHARGER						
V_{REG_ACC}	Charge voltage	RVSET < 18 kΩ, VREG = 8.20 V, T_J = -40℃ - 85℃	8.159	8.2	8.241	V
V_{REG_ACC}	Charge voltage	RVSET = 39 kΩ (±10%), VREG = 8.80 V, T_J = -40℃ - 85℃	8.756	8.8	8.844	V
V_{REG_ACC}	Charge voltage	RVSET = 75 kΩ (±10%), VREG = 8.70 V, T_J = -40℃ - 85℃	8.656	8.7	8.744	V
V_{REG_ACC}	Charge voltage	RSET > 150kΩ,VREG = 8.40 V, T_J = -40℃ to 85℃	8.358	8.4	8.442	V

Electrical Characteristics (continued)

$V_{VBUS\_UVLO\_RISING}$< V_{VBUS} < V_{VBUS_OV}, T_J = -40°C to+125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$K_{ICHGSET}$	Charge current regulation setting ratio	ICHG = $R_{ICHGSET}/K_{ICHGSET}$. ICHG = 1000 mA		3810		Ω/A
I_{CHG_RANGE}	Charge current regulation range		30		2200	mA
I_{CHG_ACC}	Fast Charge current regulation accuracy	ICHG = 1000 mA, VBAT = 6.2 V or 7.6 V, T_J = 0°C to 85°C	-7.5		7.5	%
I_{CHG_ACC}	Fast Charge current regulation accuracy	ICHG = 500mA, VBAT = 6.2 V or 7.6 V, T_J = 0°C to 85°C	-15		15	%
I_{CHG_ACC}	Fast Charge current regulation accuracy	ICHG = 250 mA, VBAT = 6.2 V or 7.6 V, T_J = 0°C to 85°C	-25		25	%
I_{PRECHG_RANGE}	Precharge current range		30		800	mA
I_{PRECHG_ACC}	Precharge current accuracy	VBAT = 5.2 V, IPRECHG = 200 mA, T_J = 25°C	170		237	mA
		VBAT = 5.2 V, IPRECHG = 200 mA, T_J = 0°C to 85°C	150		245	mA
I_{TERM_RANGE}	Termination current range		10		800	mA
I_{TERM_ACC}	Termination current accuracy	ICHG = 1.5A, ITERM = 150 mA, T_J = 25°C	143		159	mA
I_{TERM_ACC}		ICHG = 1.5A, ITERM = 150 mA, T_J = 0°C to 85°C	120		180	mA
I_{TERM_ACC}		ICHG = 1.5A, ITERM = 50 mA, T_J = 25°C	42		60	mA
I_{TERM_ACC}		ICHG = 1.5A, ITERM = 50 mA, T_J = 0°C to 85°C	18		75	mA
$V_{BAT\_SHORT\_RISING}$	Short Battery Voltage rising threshold to start pre-charging	VBAT rising	4.1	4.4	4.7	V
$V_{BAT\_SHORT\_FALLING}$	Short Battery Voltage falling threshold to stop pre-charging	VBAT falling	3.7	4	4.3	V
I_{BAT_SHORT}	Low Battery Voltage trickle charging current	VBAT < 4.4 V		100		mA
$V_{BAT\_LOWV\_RISING}$	VBAT LOWV Rising threshold to start fast-charging	VBAT rising, VBATLOWV = 6.0 V	5.7	6	6.3	V
$V_{BAT\_LOWV\_FALLING}$	VBAT LOWV Falling threshold to stop fast-charging	VBAT falling, VBATLOWV = 6.0 V	5.3	5.6	5.9	V
V_{RECHG}	Recharge threshold below V_{REG}	VBAT falling		200		mV
R_{ON_QHS} (Q2)	High-side switching MOSFET on-resistance between SW and SYS (Q2)	T_J = 25°C		32	35	mΩ
		T_J = – 40°C to 125°C		32	47	mΩ
R_{ON_QLS} (Q3)	Low-side switching MOSFET on-resistance between SW and GND (Q3)	T_J = 25°C		42	46	mΩ
		T_J = – 40°C to 125°C		42	63	mΩ
R_{ON_QBAT} (Q4)	MOSFET on-resistance between SYS and BAT (Q4)	T_J = 25°C		18	19	mΩ
R_{ON_QBAT} (Q4)	MOSFET on-resistance between SYS and BAT (Q4)	T_J = – 40°C - 85°C		18	23	mΩ
I_{BAT_DISCHG}	BAT Discharge current source	VBAT = 8V, EN_BAT_DISCHG = 1	8	11.5	16	mA
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM}	Input voltage regulation range		4.171	4.3	4.429	V
K_{ILIM}	I_{INMAX} = K_{ILIM}/R_{ILIM}	Input Current regulation by ILIM pin		1110		A x Ω
I_{INDPM}	Input current regulation limit, I_{INMAX} = K_{ILIM}/R_{ILIM}	Input Current regulation by ILIM pin = 0.5A	457	505	553	mA
		Input Current regulation by ILIM pin = 0.9A	839	909	980	mA
		Input Current regulation by ILIM pin = 1.5A	1413	1518	1624	mA
R_{ON_QBLK} (Q1)	Blocking MOSFET on-resistance between VBUS and PMID (QBLK)	T_J = 25°C		33	37	mΩ
		T_J = – 40°C to 125°C		33	51	mΩ

Electrical Characteristics (continued)

$V_{VBUS\_UVLO\_RISING} < V_{VBUS} < V_{VBUS\_OV}$, T_J = -40°C to+125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
D + /D- DETECTION						
$V_{D+D-\_600MVSRC}$	D+/D- Voltage Source (600 mV)		500	600	700	mV
$I_{D+\_10UASRC}$	D+ Current Source (10 µA)		7	10	14	µA
$I_{D+D-\_100UASNK}$	D+/D- Current Sink (100 µA)		50	100	150	µA
V_{D+D-_0P325}	D+/D- Comparator Threshold for Secondary Detection		250		400	mV
R_{D-_19K}	D- Resistor to Ground (19 kΩ)		14.25		24.8	kΩ
V_{D+_0P8}	D+ Comparator Threshold for Data Contact Detection				800	mV
V_{D+D-_1P2}	D+/D- Threshold for Non-standard adapter		1.05		1.35	V
V_{D+D-_2P0}	D+/D- Comparator Threshold for Non-standard adapter		1.85		2.15	V
V_{D+D-_2P8}	D+/D- Threshold for Non-standard adapter		2.55		2.85	V
I_{D+D-_LKG}	D+/D- Leakage Current	HiZ	-1		1	µA
BATTERY OVER-VOLTAGE PROTECTION						
$V_{BAT\_OVP\_RISING}$	Battery over-voltage rising threshold	VBAT rising, as percentage of VREG	102.5	104	105	%
$V_{BAT\_OVP\_FALLING}$	Battery over-voltage falling threshold	VBAT falling, as percentage of VREG	101	102	103.3	%
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 120°C		120		°C
T_{SHUT_RISING}	Thermal Shutdown Rising threshold	Temperature Increasing		150		°C
	Thermal Shutdown Falling threshold	Temperature Decreasing		120		°C
JEITA THERMISTOR COMPARATOR (BOOST MODE)						
V_{T1}	TS pin voltage rising. T1 (0°C) threshold, Charge suspended below this temperature.	As Percentage to REGN	72.75	73.25	73.75	%
V_{T1_HYS}	TS pin voltage falling. Charge re-enabled to ICHG/2 and VREG above this temperature	As Percentage to REGN		1.3		%
V_{T2}	TS pin voltage rising. T2 (10°C) threshold, charge set to ICHG/2 and VREG below this temperature	As Percentage to REGN	67.75	68.25	68.75	%
V_{T2_HYS}	TS pin voltage falling. Charge set to ICHG and VREG above this temperature	As Percentage to REGN		1.2		%
V_{T3}	TS pin voltage falling. T3 (45°C) threshold, charge set to ICHG and 8.1 V above this temperature.	As Percentage to REGN	44.25	44.75	45.25	%
V_{T3_HYS}	TS pin voltage rising. Charge set to ICHG and VREG below this temperature	As Percentage to REGN		1		%
V_{T5}	TS pin voltage falling. T5 (60°C) threshold, charge suspended above this temperature.	As Percentage to REGN	33.875	34.375	34.875	%
V_{T5_HYS}	TS pin voltage rising. Charge set to ICHG and 8.1 V below this temperature	As Percentage to REGN		1.35		%
COLD/HOT THERMISTOR COMPARATOR (OTG BUCK MODE)						
V_{BCOLD0}	Cold Temperature Threshold, TS pin Voltage Rising Threshold	As Percentage to REGN (Approx. – 10°C w/ 103AT)	76.5	77	77.5	%
V_{BCOLD0_HYS}	Cold Temperature Threshold, TS pin Voltage Falling Threshold	As Percentage to REGN		1		%

Electrical Characteristics (continued)

$V_{VBUS\_UVLO\_RISING}$< V_{VBUS} < V_{VBUS_OV}, T_J = -40°C to+125°C, and T_J = 25°C for typical values (unless otherwise noted)

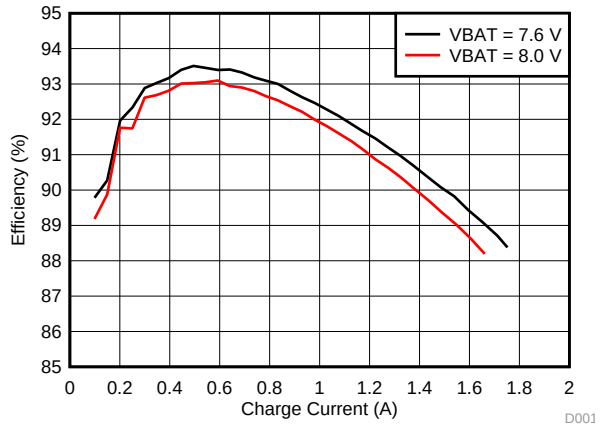
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BHOT1}	Hot Temperature Threshold, TS pin Voltage falling Threshold	As Percentage to REGN (Approx. 60°C w/ 103AT)	33.875	34.375	34.875	%
V_{BHOT1_HYS}	Hot Temperature Threshold, TS pin Voltage rising Threshold	As Percentage to REGN		3		%
BOOST MODE CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency	1.35	1.5	1.65	MHz
OTG BUCK MODE CONVERTER						
V_{OTG_ACC}	OTG Buck mode voltage regulation accuracy	IVBUS = 0A, OTG_VLIM = 5.1V	4.947	5.1	5.253	V
V_{OTG_ACC}	OTG Buck mode voltage regulation accuracy	IVBUS = 0A, OTG_VLIM = 5.1 V	-3		3	%
I_{OTG_ACC}	OTG Buck mode current regulation accuracy	OTG_ILIM = 2A	-15	-7.5	0	%
V_{OTG_OVP}	OTG Buck mode over-voltage threshold		5.8	6		V
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5 V, I_{REGN} = 20 mA	4.7	4.8	5.15	V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5 V, V_{REGN} = 3.8 V	50			mA
LOGIC I/O PIN (/CE)						
V_{IH_CEZ}	Input high threshold level, /CE		1.3			V
V_{IL_CEZ}	Input low threshold level, /CE				0.4	V
$I_{IN\_BIAS\_CEZ}$	High level leakage current, /CE	Pull-up rail 1.8 V			2.5	uA
LOGIC O PIN (/INT, /PG, STAT)						
V_{OL}	Output low threshold level	Sink current = 5 mA			0.4	V
I_{OUT_BIAS}	High level leakage current	Pull-up rail 1.8 V			1	µA

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
VBUS/BAT POWER UP						
t_{VBUS_OV}	VBUS OVP reaction time	VBUS rising above V_{BUS_OV} threshold to converter turn off		200		ns
$t_{POORSRC}$	Bad adapter detection duration			30		ms
BATTERY CHARGER						
t_{TERM_DGL}	Deglitch time for charge termination	Charge current falling below I_{TERM}		250		ms
t_{RECGH_DGL}	Deglitch time for recharge threshold	BAT voltage falling below V_{RECHG} = 100 mV		250		ms
$t_{BAT\_OVP\_DGL}$	Deglitch time for battery over-voltage to disable charge			1		µs
t_{SAFETY}	Charge Safety Timer Accuracy	CHG_TIMER = 12 hours	10.8	12	13.2	hr
DIGITAL CLOCK AND WATCHDOG TIMER						
f_{LPDIG}	Digital low power clock	REGN LDO disabled	18	30	45	kHZ
f_{DIG}	Digital clock	REGN LDO enabled	1.35	1.5	1.65	MHz

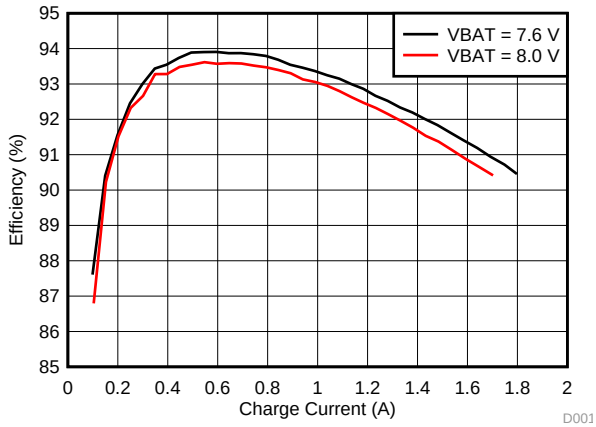
7.7 Typical Characteristics

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS}= 44µF, C_{BAT} = 10µF, L = 1µH (DFE252012F-1R0) (unless otherwise specified)



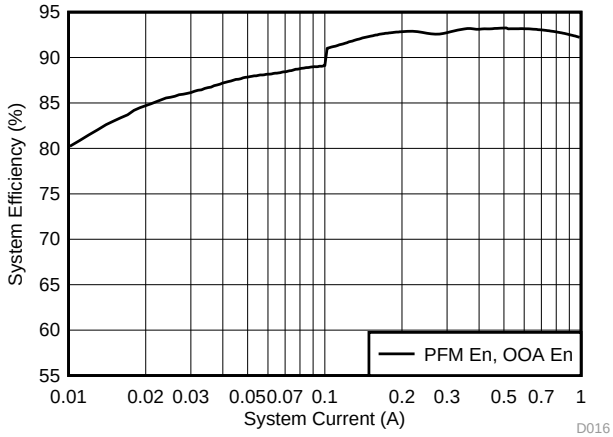
VBUS = 5V

Figure 1. Charge Efficiency vs. Charge Current



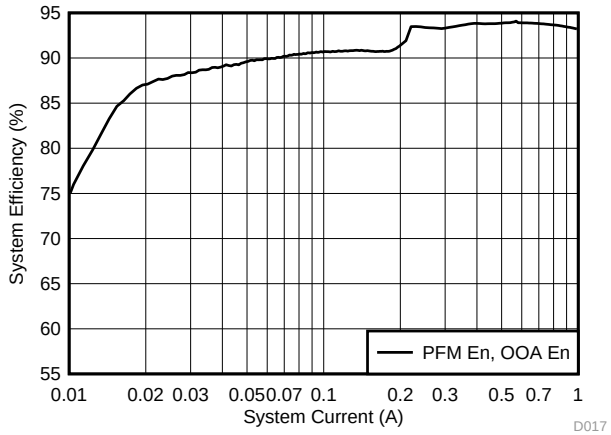
VBUS = 5V L = 1µH (IHLP2525CZER1R0k01)

Figure 2. Charge Efficiency vs. Charge Current



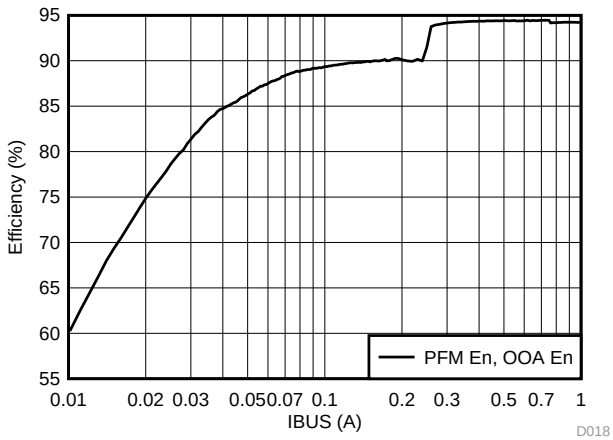
VBUS = 5V VBAT = 8.4V

Figure 3. System Efficiency vs. System Current



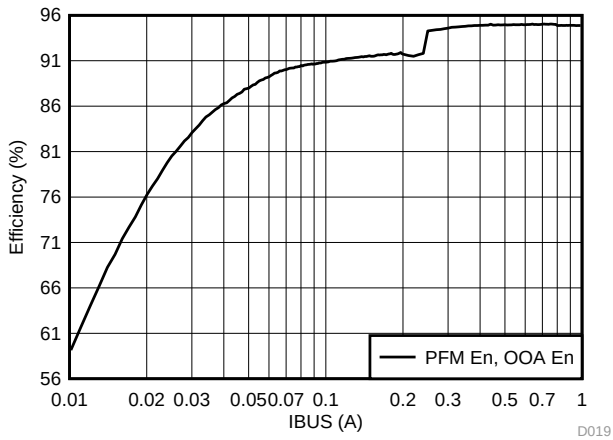
VBUS = 5V VBAT = 8.4V L = 1µH (IHLP2525CZER1R0k01)

Figure 4. System Efficiency vs. System Current



VBUS = 5V VBAT = 7.6V

Figure 5. OTG Efficiency vs. VBUS Output Current

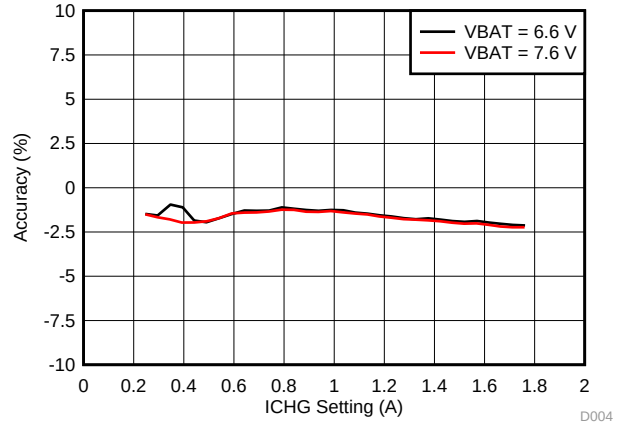


VBUS = 5V VBAT = 7.6V L = 1µH (IHLP2525CZER1R0k01)

Figure 6. OTG Efficiency vs. VBUS Output Current

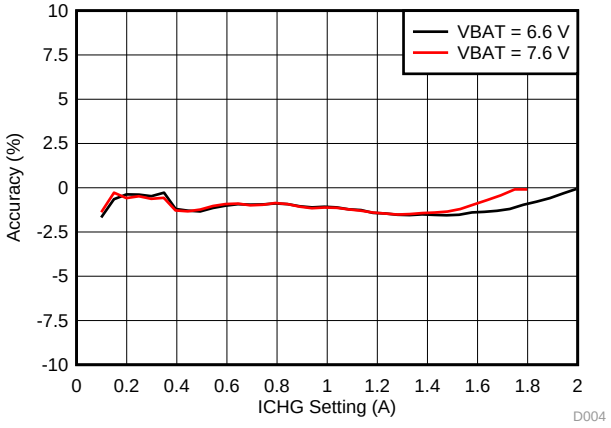
Typical Characteristics (continued)

C_{VBUS} = 1µF, C_{PMID}= 10µF, C_{SYS}= 44µF, C_{BAT} = 10µF, L = 1µH (DFE252012F-1R0) (unless otherwise specified)



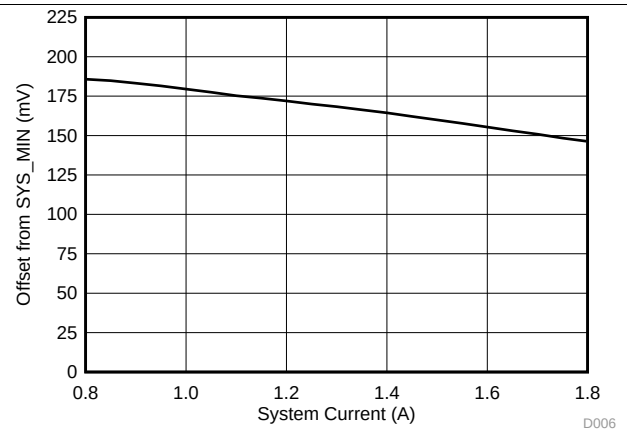
VBUS = 5V

Figure 7. Charge Current Accuracy vs. ICHG Setting



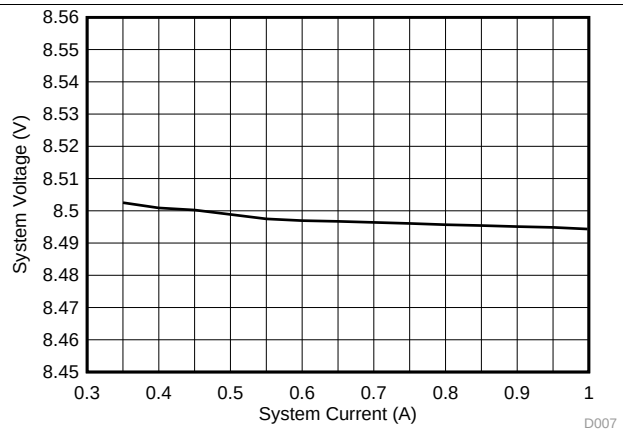
VBUS = 5V L = 1µH (IHLP2525CZER1R0k01)

Figure 8. Charge Current Accuracy vs. ICHG Setting



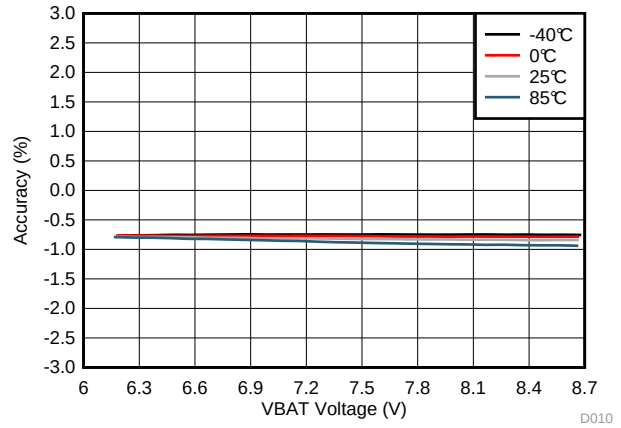
VBUS = 5V VBAT = 6V, EN_CHG = 0 SYSMIN = 7V

Figure 9. SYSMIN Load Regulation



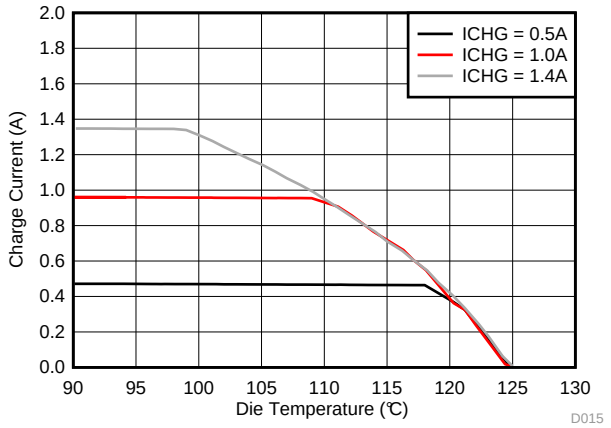
VBUS = 5V VBAT = 8.4V EN_CHG = 0

Figure 10. System Load Regulation After Charge Done



VBUS = 5.1V IBUS = 1A

Figure 11. OTG Voltage Regulation vs. VBAT Voltage



VBUS = 5V VBAT = 7.6V ICHG = 0.5A, 1.0A, 1.4A
Measured on 35-µm thick copper, 4-layer board

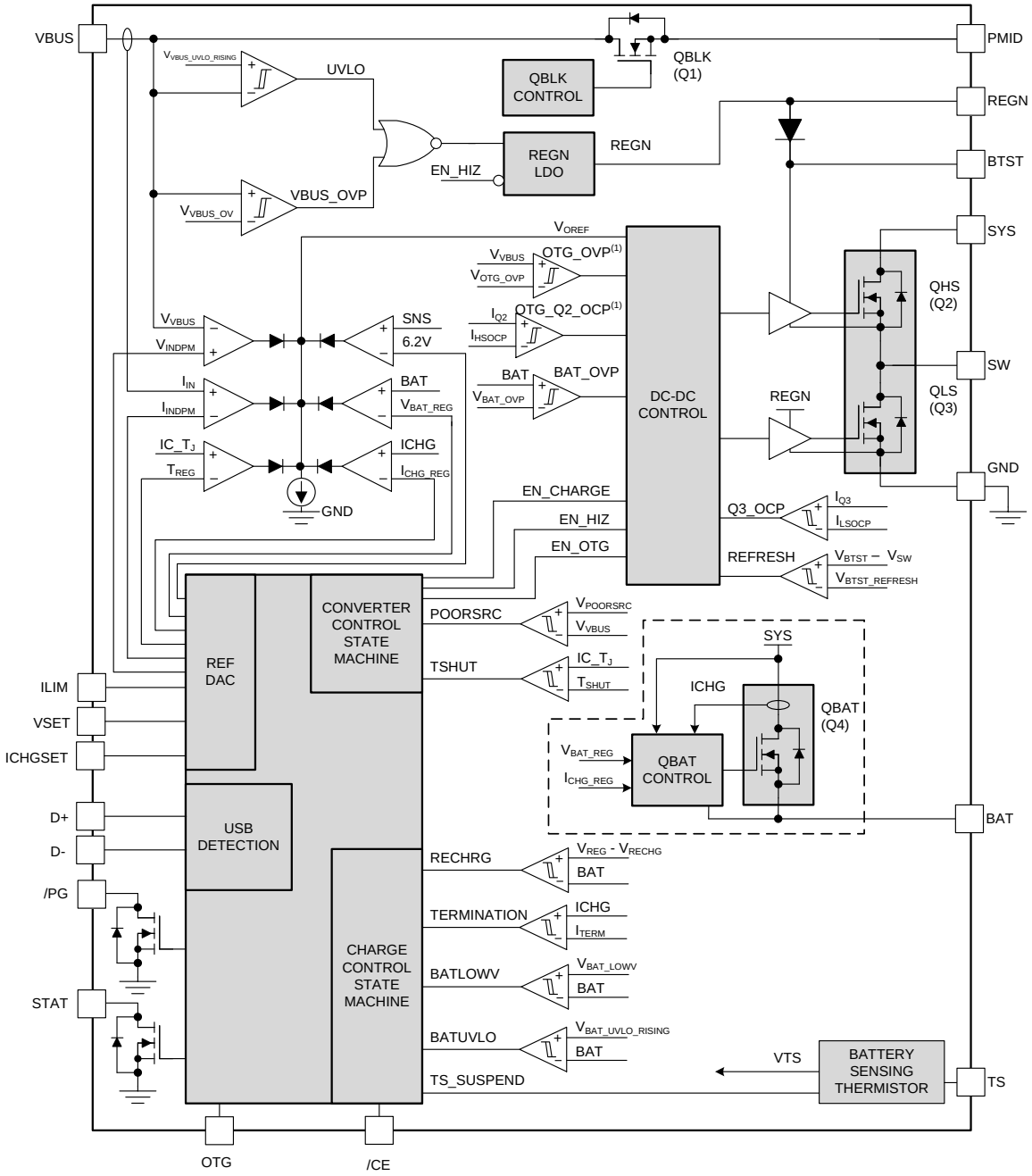
Figure 12. Max Current Temperature Profile

8 Detailed Description

8.1 Overview

The BQ25886 device is a highly integrated 2-A switch-mode battery charger for 2s Li-Ion and Li-polymer battery. It integrates the input blocking FET (Q1, QBLK), high-side switching FET (Q2, QHS), low-side switching FET (Q3, QLS), and battery FET (Q4, QBAT). The device also integrates the boot-strap diode for high-side gate drive.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Device Power-On-Reset

The internal bias circuits are powered from either VBAT or VBUS when it rises above $V_{VBUS\_UVLO\_RISING}$ or $V_{BAT\_UVLO\_RISING}$. When VBUS rises above $V_{VBUS\_UVLO\_RISING}$ or BAT rises above $V_{BAT\_UVLO\_RISING}$, the BATFET driver is active.

8.3.2 Device Power Up from Battery without Input Source

If only the battery is present and the voltage is above UVLO threshold ($V_{BAT\_UVLO\_RISING}$), the BATFET turns on and connects battery to system. The REGN LDO stays off to minimize the quiescent current. The low $R_{DS(ON)}$ of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

8.3.3 Device Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on REGN LDO and all the bias circuits. It detects and sets the input current limit before the boost converter is started. The power up sequence from input source is as listed:

1. Poor Source Qualification
2. Input Source Type Detection based on D+/D- to set default Input Current Limit (IINDPM) and input source type
3. Power Up REGN LDO
4. Converter Power-up

8.3.3.1 Poor Source Qualification

After REGN LDO powers up, the device checks the current capability of the input source. The input source has to meet the following requirements in order to start the boost converter.

1. VBUS voltage below V_{VBUS_OVP}
2. VBUS voltage above $V_{POORSRC}$ when pulling $I_{POORSRC}$ (typical 15mA)

If V_{BUS_OVP} is detected (condition 1 above), the device automatically retries detection once the over-voltage fault goes away. If a poor source is detected (condition 2 above), the device repeats poor source qualification routine every 2 seconds. After 7 consecutive failures, the device goes to HIZ mode. The battery powers up the system when the device is in HIZ. On BQ25886, adapter re-plugin is required to restart device operation. If the fault is not removed, the part will enter HIZ mode again after the 7 consecutive failures.

8.3.3.2 Input Source Type Detection

After input source is qualified, the charger device runs input source type detection.

The BQ25886 sets input current limit through D+/D- pin. After input source type detection, /PG pin is pulled LOW. The charger input current is always limited by the lower of ILIM pin or input source detection (500mA or 900mA), Input Current Optimizer (ICO) setting if a DCP is detected.

8.3.3.2.1 D+/D– Detection Sets Input Current Limit

The BQ25886 contains a D+/D- based input source detection to program the input current limit. The D+/D- detection has three major steps: Data Contact Detect (DCD), Primary Detection, and Secondary Detection.

Feature Description (continued)

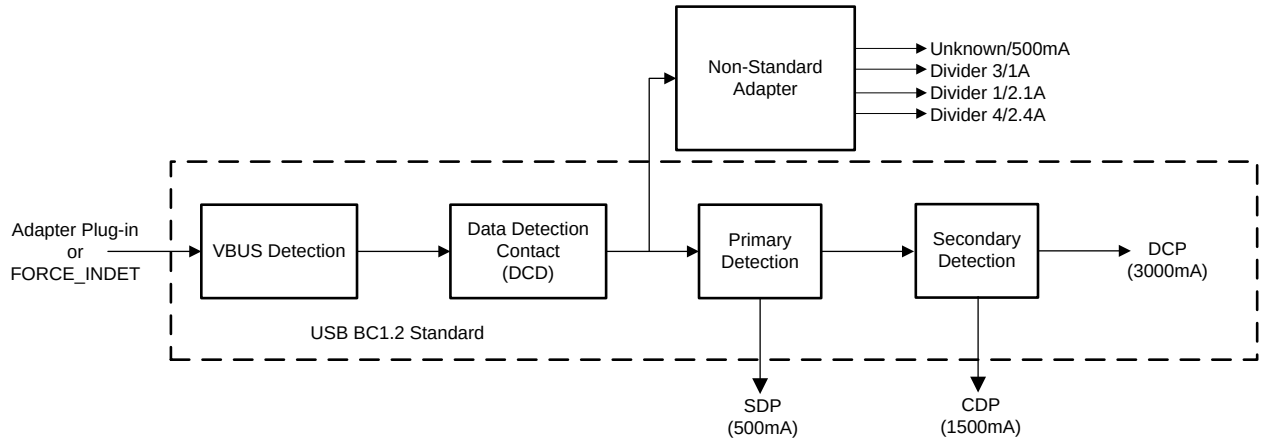


Figure 13. D+/D- Detection Flow

Table 2. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT
Divider 1	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P0_VTH}	2.1 A
Divider 3	V_{D+} within V_{2P0_VTH}	V_{D-} within V_{2P8_VTH}	1 A
Divider 4	V_{D+} within V_{2P8_VTH}	V_{D-} within V_{2P8_VTH}	2.4 A

Table 3. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINDPM)
USB SDP (USB500)	500 mA
USB CDP	1.5 A
USB DCP	3.0 A
Divider 3	1 A
Divider 1	2.1 A
Divider 4	2.4 A
Unknown 5V Adapter	500 mA

8.3.3.3 Power Up REGN Regulator (LDO)

The REGN LDO supplies internal bias circuits as well as the QHS and QLS gate drive. The LDO also provides bias rail to TS external resistors. The pull-up rail of STAT and PG can be connected to REGN as well. The REGN is enabled when all the below conditions are valid.

1. VBUS above $V_{VBUS\_UVLO\_RISING}$ in boost mode or VBUS below $V_{VBUS\_UVLO\_RISING}$ in buck mode
2. Poor Source Qualification detects a valid input source
3. Input Source Type Detection completes and sets appropriate input current limit
4. After 220-ms delay is complete

If one of the above conditions is not valid, the device is in high impedance mode (HIZ) with REGN LDO off. The device draws less than I_{VBUS_HIZ} from VBUS during HIZ state. The battery powers up the system when the device is in HIZ.

8.3.3.4 Converter Power Up

After the input current limit is set, the $\overline{PG}$ pin is pulled LOW, and the converter is enabled, allowing the QHS and QLS to start switching.Before charging begins, the battery discharge source (IBAT_DISCHG) is enabled automatically to detect the presence of battery. BATFET stays on to charge the battery. The device provides soft-start when system rail is ramped up.

As a battery charger, the device deploys a highly efficient 1.5-MHz boost switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature, simplifying output filter design.

In order to improve light-load efficiency, the device switches to PFM (Pulse Frequency Modulation) control at light load when battery is below minimum system voltage setting or charging is disabled. During the PFM operation, the switching duty cycle is set by the ratio of SYS and VBUS.

8.3.4 Input Current Optimizer (ICO)

The device provides innovative Input Current Optimizer (ICO) to identify maximum power point without overloading the input source. The algorithm automatically identifies maximum input current limit of a power source without staying in VINDPM to avoid input source overload.

On BQ25886, ICO starts automatically when DCP type of input source is detected. When other input source typs are detected, ICO is disabled. The actual input current limit used by the Dynamic Power Management circuitry is limited by the lower value of current limit identified by the ICO algorithm or the current limit set by the ILIM pin. When the algorithm is enabled, it runs continuously to adjust input current limit of Dynamic Power Management (IINDPM) using ICO algorithm. When optimal input current is identified, the input current limit set by ICO will not be changed until the algorithm is forced to run by the following event:

1. A new input source is plugged-in
2. VINDPM is entered
3. VBUS_OVP event

Table 4. Input Current Optimizer Automatic Operation

DEVICE	INPUT SOURCE	INPUT CURRENT LIMIT (IINDPM)	AUTOMATIC START ICO ALGORITHM
BQ25886 (D+/D–)	USB SDP (USB500)	500 mA	Disable
	USB CDP	1.5 A	Disable
	USB DCP	3.0 A	Enable
	Divider 3	1 A	Disable
	Divider 1	2.1 A	Disable
	Divider 4	2.4 A	Disable
	Unknown 5V Adapter	500 mA	Disable

8.3.5 Buck Mode Operation from Battery (OTG)

The device supports buck converter operation to deliver power from the battery to other portable devices through USB port. The buck mode output current rating meets the USB On-The-Go 500-mA output requirement. The maximum output is 2.0 A. The buck operation is enabled when the following conditions are valid:

1. BAT above V_{OTG_BAT}
2. VBUS less than $V_{VBUS\_PRESENT}$
3. Buck mode operation is enabled (OTG pin is pulled high)
4. Voltage at TS (thermistor) pin is within range BHOT and BCOLD
5. After 30-ms delay from buck mode enable

8.3.6 PowerPath Management

The device accommodates a wide range of input sources from USB, to wall adapter, to power bank. The device provides automatic power path selection to supply the system (SYS) from input source (VBUS), battery (BAT), or both.

8.3.6.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. Even with a fully depleted battery, the system is regulated above the minimum system voltage (fixed 6.2 V (typ)).

When the battery is below minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 200 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the the BATFET's drain to source voltage drop.

When the battery charging is disabled and VBAT is above minimum system voltage setting or charging is terminated, the system is always regulated at typically 50mV above battery voltage.

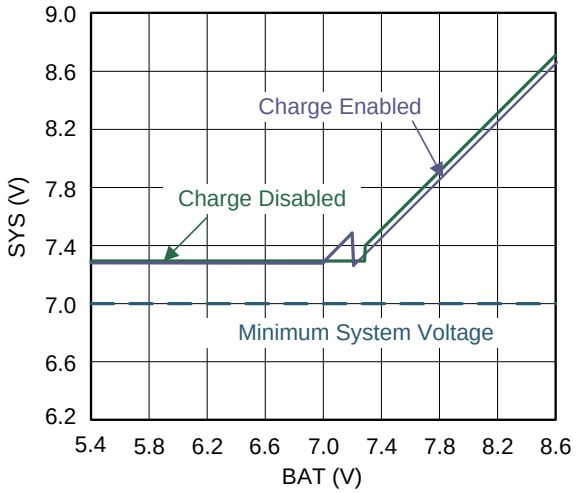


Figure 14. System Voltage vs. Battery Voltage

8.3.6.2 Dynamic Power Management

To meet the maximum current limit in the USB spec and avoid over loading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. As the charger's system load plus charge current increases with constant input voltage, the charger's input current must increase. If this current exceeds the charger's preset input current limit or causes the input source voltage to droop near the input voltage limit (VINDPM fixed at 4.3 V typical), the device then reduces the charge current until the input current is regulated to the input current limit or the input voltage is regulated to the VINDPM threshold.Note that if the D+/D- algorithm detected a DCP port and VINDPM triggered, the ICO algorithm lowers the input current limit.

If the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the Supplement Mode where the BATFET turns on and battery starts discharging so that the system is supported from both the input source and battery.

The figure shows the DPM response with 5-V/3-A adapter, 6.4-V battery, 1.5-A charge current and 6.8 V minimum system voltage setting.

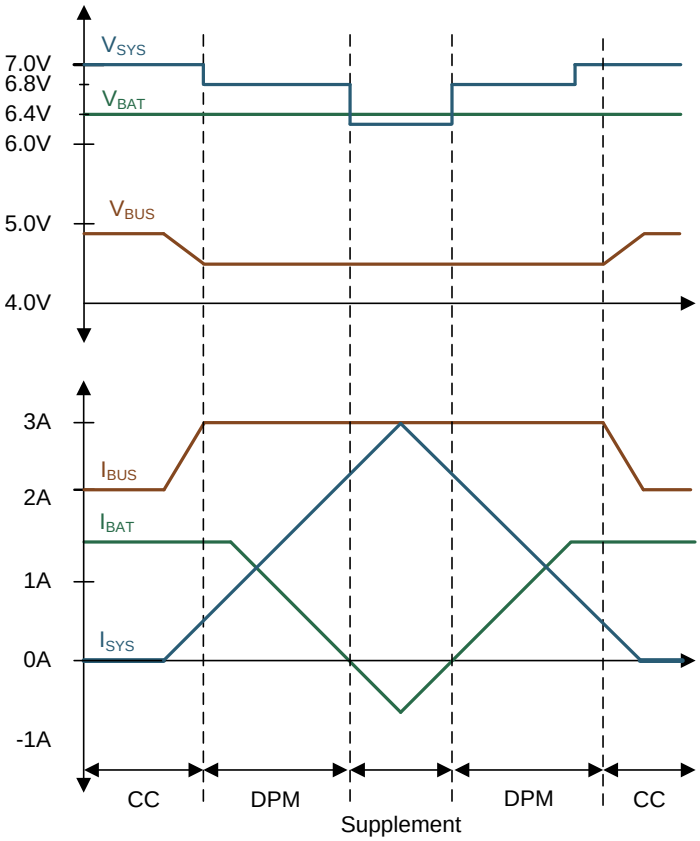


Figure 15. DPM Response

8.3.6.3 Supplement Mode

When the voltage falls below the battery voltage, the BATFET turns on.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. The figure shows the V-I curve of the BATFET gate regulation operation. BATFET turns off to exit Supplement Mode when the battery is below battery depletion threshold ($V_{BAT\_UVLO\_RISING}$).

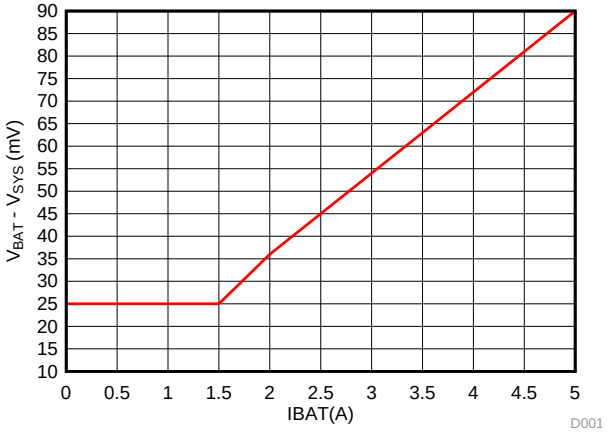


Figure 16. BATFET I-V Curve

8.3.7 Battery Charging Management

The BQ25886 charges 2-cell Li-Ion battery with up to 2.2-A charge current for high capacity battery. The low $R_{DS(ON)}$ BATFET improves charging efficiency and minimize the voltage drop during discharging.

8.3.7.1 Autonomous Charging Cycle

When battery charging is enabled ($\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 5 below.

Table 5. Charging Parameter Default Settings

DEFAULT MODE	BQ25886
Charging Voltage	Set by VSET
Charging Current	Set by ICHGSET
Pre-Charge Current	1/10 of ICHG
Termination Current	1/10 of ICHG
Temperature Profile	JEITA
Safety Timer	12 hours

A new charge cycle starts when the following conditions are valid:

1. Converter starts
2. No thermistor fault on TS
3. No safety timer fault

The charger automatically terminates the charging cycle when the charging current is below termination threshold, charge voltage is above recharge threshold, and device is not in DPM mode or thermal regulation. When a full battery voltage is discharged below recharge threshold (threshold fixed at 200 mV for BQ25886), the device automatically starts a new charging cycle. After the charge is done, toggle $\overline{CE}$ pin can initiate a new charging cycle.

The STAT output indicates the charging status of: charging (LOW), charging complete or charge disable (HIGH) or charging fault (Blinking). If no battery is connected, the STAT pin blinks as capacitance connected at BAT charges, discharges, then recharges.

8.3.7.2 Battery Charging Profile

The device charges the battery in five phases: trickle charge, pre-charge, constant current, constant voltage, and top-off timer charging. At the beginning of a charging cycle, the device checks the battery voltage and regulates current/voltage accordingly.

If the charger device is in DPM regulation or thermal regulation during charging, the actual charging current will be less than the programmed value. In this case, termination is temporarily disabled and the charging safety timer is counted at half the clock rate, as explained in the Charging Safety Timer section.

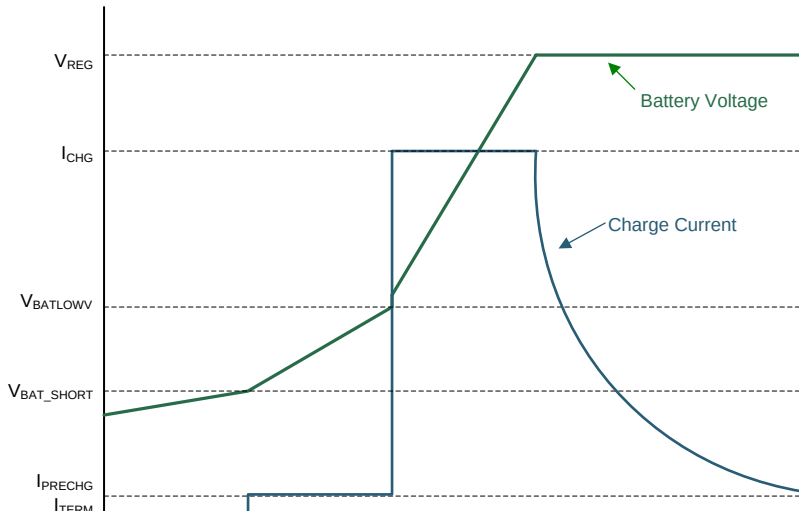


Figure 17. Battery Charging Profile

8.3.7.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

When termination occurs, the STAT pin goes HIGH. Termination is temporarily disabled when the charger device is in input current, voltage or thermal regulation. On the BQ25886, termination threshold is 1/10 of the fast charge current setting.

8.3.7.4 Thermistor Qualification

The charger device provides a single thermistor input for battery temperature monitor.

8.3.7.4.1 JEITA Guideline Compliance in Charge Mode

To improve the safety of charging Li-ion batteries, JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin must be within the VT1 to VT5 thresholds. If TS voltage exceeds the T1-T5 range, the controller suspends charging and waits until the battery temperature is within the T1 to T5 range. At cool temperature (T1-T2), JEITA recommends the charge current to be reduced to half of the charge current or lower. At warm temperature (T3-T5), JEITA recommends charge voltage less than 4.1 V / cell.

On the BQ25886, at cool temperature (T1-T2), the charge current is reduced to 20% of the fast charge current, ICHG. At warm temperature (T3 - T5), the charge voltage is set to 8.0 V. Whenever the charger detectes "warm" or "cool" temperature, termination is automatically disabled.

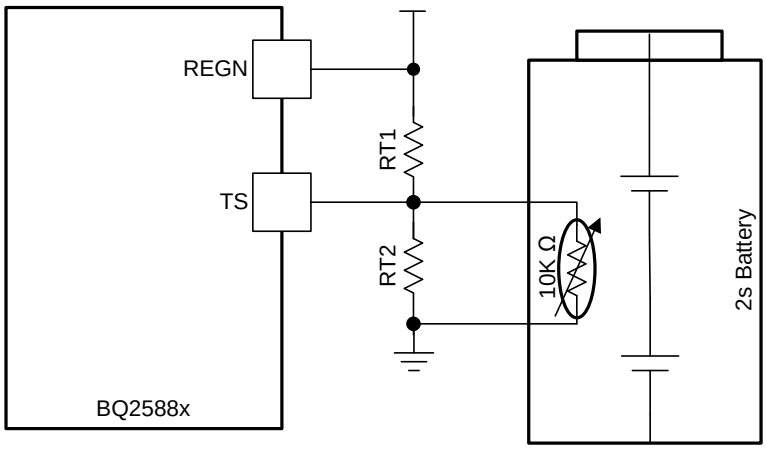


Figure 18. TS Resistor Network

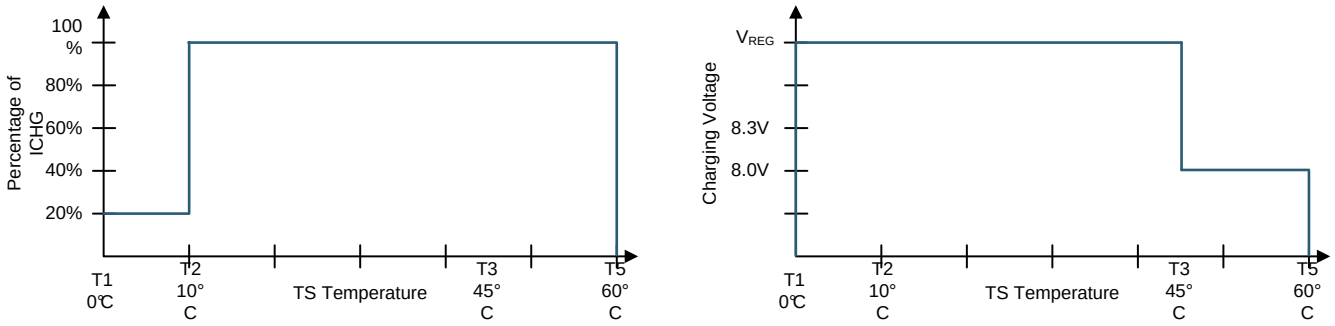


Figure 19. TS Charging Values

Assuming a 103AT NTC (Negative Temperature Coefficient) thermistor on the battery pack as shown above, the value of RT1 and RT2 can be determined by:

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - \frac{1}{V_{T1}}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}} - 1\right) - R_{NTC,T5} \times \left(\frac{1}{V_{T5}} - 1\right)} \quad (1)$$

$$RT1 = \frac{\frac{1}{V_{T1}} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \quad (2)$$

Select 0°C to 60°C range for Li-ion or Li-polymer battery:

$R_{NTC,T1}$ = 27.28 kΩ

$R_{NTC,T5}$ = 3.02 kΩ

RT1 = 5.24 kΩ

RT2 = 30.31 kΩ

8.3.7.5 Charging Safety Timer

The device has built-in safety timer to prevent extended charging cycle due to abnormal battery conditions.

During input voltage, current or thermal regulation, the safety timer counts at half clock rate as the actual charge current is likely to be below the setting. For example, if the charger is in input current regulation throughout the whole charging cycle, and the safety timer is set to 12 hours, then the timer will expire in 24 hours.

During faults which disable charging, or supplement mode, timer is suspended. Once the fault goes away, safety timer resumes. If the charging cycle is stopped and started again, the timer gets reset.

The safety timer is reset for the following events:

1. Charging cycle stop and restart (toggle $\overline{CE}$ pin, or charged battery falls below recharge threshold).
2. BAT voltage changes from pre-charge to fast-charge or vice versa.

The precharge safety timer (fixed 2hr counter that runs when VBAT < V_{BAT_LOWV}), follows the same rules as the fast-charge safety timer in terms of getting suspended, reset, and counting at half-rate.

8.3.8 Status Outputs

8.3.8.1 Power Good Indicator ($\overline{PG}$)

The open drain $\overline{PG}$ pin goes low to indicate a good input source when:

1. VBUS above $V_{VBUS\_UVLO\_RISING}$
2. VBUS below V_{VBUS_OV} threshold
3. VBUS above $V_{POORSRC}$ (typ. 3.7 V) when $I_{POORSRC}$ (typ. 30 mA) current is applied (not a poor source)
4. Input Source Type Detection is completed

8.3.8.2 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED.

Table 6. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including trickle charge, pre-charge, fast-charge, recharge)	LOW
Charging complete	HIGH
Sleep mode, charge disable	HIGH
Charge suspend (Input over-voltage, TS fault, timer fault or battery over-voltage) OTG Buck Mode suspend (due to TS fault)	Blinking at 1Hz

8.3.9 Input Current Limit on ILIM Pin

For safe operation, the BQ2588x has an additional hardware pin on ILIM to limit maximum input current. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (3)$$

The actual input current limit is the lower value between ILIM pin setting and current limit set by D+/D- detection. The device regulates ILIM pin at 0.8 V. If ILIM voltage exceeds 0.8 V, the device enters input current regulation (refer to Dynamic Power Management section).

The ILIM pin can also be used to monitor input current. The voltage on ILIM pin is proportional to the input current. ILIM can be used to monitor input current with the following relationship:

$$I_{IN} = \frac{K_{ILIM} \times V_{ILIM}}{R_{ILIM} \times 0.8V} \quad (4)$$

For example, if ILIM pin is set with 820-Ω resistor, and the ILIM voltage 0.5V, the actual input current is 0.795 A to 0.973 A. If ILIM pin is open, the input current is limited to zero since ILIM voltage floats above 0.8 V.

8.3.10 Voltage and Current Monitoring

The device closely monitors the input voltage, as well as internal FET currents for safe boost and buck mode operation.

8.3.10.1 Voltage and Current Monitoring in Boost Mode

8.3.10.1.1 Input Over-Voltage Protection

The valid input voltage range for boost mode operation is V_{VBUS_OP}. If VBUS voltage exceeds V_{VBUS_OV}, the device stops switching immediately to protect the power FETs. The device automatically starts switching again when the over-voltage condition goes away.

8.3.10.1.2 Input Under-Voltage Protection

The valid input voltage range for boost mode operation is V_{VBUS_OP}. If VBUS voltage falls below $V_{POORSRC}$ during operation, the device stops switching. The device automatically attempts to restart switching when the under-voltage condition goes away.

8.3.10.1.3 System Over-Voltage Protection

The charger device clamps the system voltage during load transient so that the components connect to system would not be damaged due to high voltage. SYSOVP threshold is 350 mV above system regulation voltage. Upon SYSOVP, converter stops immediately to clamp the overshoot.

8.3.10.1.4 System Over-Current Protection

The charger device continually monitors and compares VBUS to VSYS to protect against a system short-circuit event. In the event that VSYS drops to within 250 mV of VBUS during operation, a short circuit event is flagged and the converter stops switching. The device attempts to recover from this condition automatically.

8.3.10.2 Voltage and Current Monitoring in OTG Buck Mode

The device closely monitors the VBUS voltage, as well as RBFET (Q1, QBLK) and LSFET (Q3, QLS) current to ensure safe buck mode operation.

8.3.10.2.1 VBUS Over-voltage Protection

When the VBUS voltage rises above regulation target and exceeds V_{OTG_OVP}, the device enters over-voltage protection which stops switching, and exits buck mode.

8.3.10.2.2 VBUS Over-Current Protection

The device monitors output current to provide output short protection. The OTG buck mode has built-in constant current regulation to allow OTG to adapt to various types of loads. If short circuit is detected on VBUS, the OTG turns off and retries 7 times. If the retries are not successful, OTG is disabled.

8.3.11 Thermal Regulation and Thermal Shutdown

8.3.11.1 Thermal Protection in Boost Mode

The device monitors internal junction temperature, T_J, to avoid overheating and limits the IC surface temperature in boost mode. When the internal junction temperature exceeds the thermal regulation limit (120°C), the device reduces charge current.

During thermal regulation, the actual charging current is usually below the programmed value. Therefore, termination is disabled, and the safety timer runs at half the clock rate.

Additionally, the device has thermal shutdown to turn off the converter when IC surface temperature exceeds T_{SHUT}. The converter turns back on when IC temperature is below T_{SHUT_HYS}.

8.3.11.2 Thermal Protection in OTG Buck Mode

The BQ2588x monitors the internal junction temperature to provide thermal shutdown during OTG buck mode.

8.3.12 Battery Protection

8.3.12.1 Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage while charging. When battery over-voltage occurs, the charger device immediately disables charge.

8.4 Device Functional Modes

The BQ25886 is a standalone device and therefore does not include any functional modes for I^2C operations.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

A typical application consists of the BQ25886 configured as a standalone device and a 2s battery charger for Li-Ion and Li-Polymer batteries used in a wide range of portable devices. It integrates an input blocking FET (QBLK, Q1), high-side switching FET (QHS, Q2), and low-side switching FET (QLS, Q3). The device also integrates a bootstrap diode for the high-side gate drive.

9.2 Typical Application

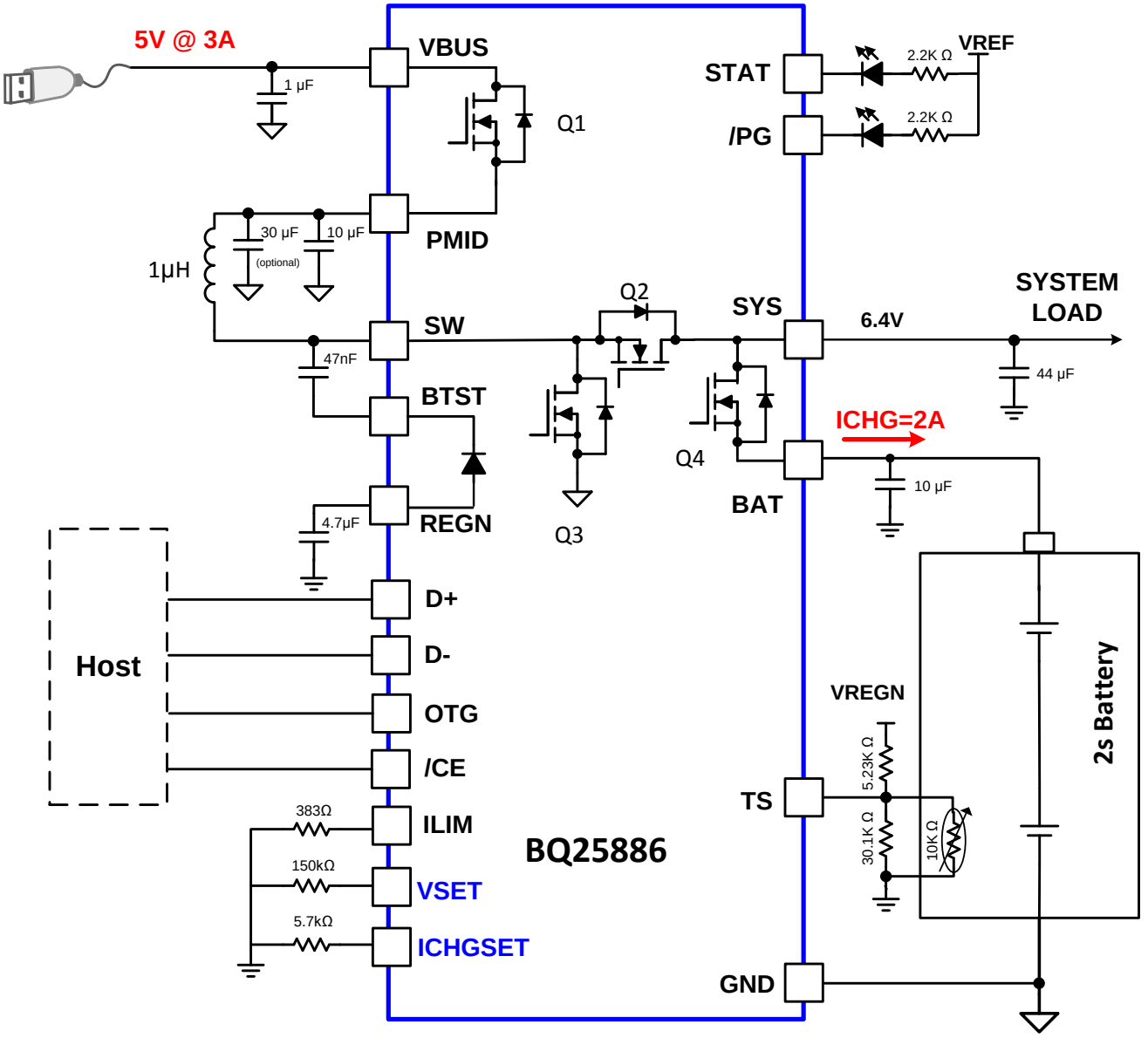


Figure 20. BQ25886 (Stand-Alone) Typical Application Diagram

Typical Application (continued)

9.2.1 Design Requirements

For this design example, use the parameters shown in Table 7 below.

Table 7. Design Parameters

PARAMETER	VALUE
VBUS voltage range	4.3 V to 6.2 V
Input current limit (ILIM)	2.4 A
Fast charge current limit (ICHGSET)	1.5 A
Minimum System Voltage	6.2 V
Battery Regulation Voltage (VSET)	8.4 V

9.2.2 Detailed Design Procedure

9.2.2.1 Inductor Selection

The device has 1.5-MHz switching frequency to allow the use of small inductor and capacitor values. The inductor saturation current should be higher than the input current (I_{IN}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{IN} + \frac{I_{RIPPLE}}{2} \tag{5}$$

The inductor ripple current (I_{RIPPLE}) depends on input voltage (V_{VBUS}), duty cycle (D = V_{BAT}/V_{BUS}), switching frequency (f_{SW}) and inductance (L):

$$I_{RIPPLE} = \frac{V_{BUS} \times (V_{SYS} - V_{BUS})}{V_{SYS} \times f_{SW} \times L} \tag{6}$$

The maximum inductor ripple current happens in the vicinity of D = 0.5. Usually inductor ripple is designed in the range of (20 – 40%) maximum charging current as a trade-off between inductor size and efficiency for a practical design.

9.2.2.2 Input (VBUS / PMID) Capacitor

The input capacitor should have enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current occurs when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{PMID} occurs where the duty cycle is closest to 50% and can be estimated by

$$I_{PMID} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{7}$$

A low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed close to the PMID and GND pins of the IC. Voltage rating of the capacitor must be higher than normal input voltage level. 25-V rating or higher capacitor is preferred for up to 5-V input voltage. A minimum 10-µF capacitor is suggested for up to 3.3-A input current. Keep in mind, long impedance cable would cause significant voltage drop with higher inrush current. For optimal performance, 44-uF cap on PMID is recommended. In addition, a minimum 1-µF capacitor is suggested at VBUS pin.

9.2.2.3 Output (VSYS) Capacitor

The SYS capacitor is the boost converter output capacitor and should also have enough ripple current rating to absorb output switching ripple current. The output capacitor RMS current I_{COUT} is given:

$$I_{CSYS,\,rms} = I_{OUT} \times \sqrt{\frac{D}{1-D}} \tag{8}$$

The output capacitor voltage ripple is a function of the boost output current (I_{OUT}), and can be calculated as follows:

$$\Delta V_{SYS} = \frac{I_{OUT} \times D}{f_{SW} \times C_{SYS}} \quad (9)$$

A low ESR ceramic capacitor such as X7R or X5R is preferred for SYS decoupling capacitor and should be placed close to the SYS and GND pins of the IC. Voltage rating of the capacitor must be higher than normal output voltage level. 16-V rating or higher capacitor is preferred. Minimum 44-μF capacitor is suggested for up to 2.2-A boost converter output current.

9.2.2.4 ILIM resistor

The ILIM resistor sets the maximum input current limit and can be used to monitor input current. The maximum input current is set by a resistor from ILIM pin to ground as:

$$I_{INMAX} = \frac{K_{ILIM}}{R_{ILIM}} \quad (10)$$

Using maximum input current limit 900mA as an example. The KLIM is 1110. If the maximum input current limit cannot exceed 900mA, then IINMAX used in the calculation should be 819.9mA as regulation accuracy at 900mA (typ) setting is around +/-8.9%. Resistor accuracy should also be taken into consideration when setting input current limit. When ILIM pin is short to GND, the input current limit is set to maximum by ILIM. Input current limit less than 500mA is not supported on ILIM pin. Do not float this pin.

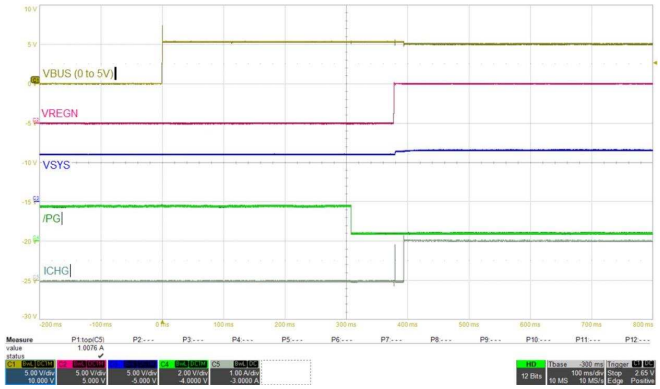
9.2.2.5 ICHGSET resistor

A resistor from ICHGSET to GND is used to program the charge current. Pre-charge and termination current is 1/10 of the fast charge current. The minimum pre-charge current is clamped at 30mA (typ). Minimum termination current is clamped at 10mA (typ). ICHGSET short to GND clamps charge current to minimum setting 30mA (typ). Floating ICHGSET disables charge. RICHGSET can be calculated as:

$$I_{CHGSET} = \frac{R_{ICHGSET}}{K_{ICHGSET}} \quad (11)$$

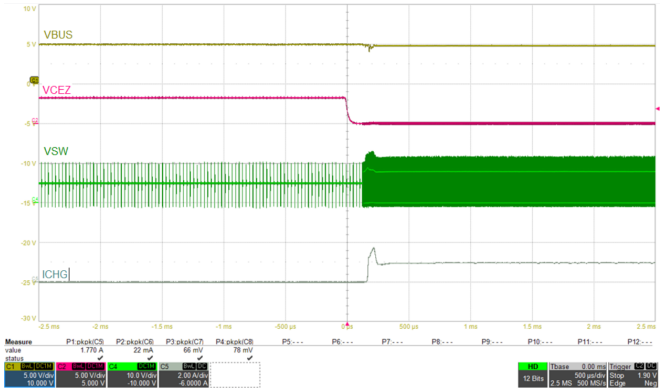
9.2.3 Application Curves

C_{VBUS} = 1 µF, C_{PMID}= 10 µF, C_{BAT} = 10 µF, C_{SYS} = 44 µF, L = DFE252012F-1R0 (1 µH) (unless otherwise specified)



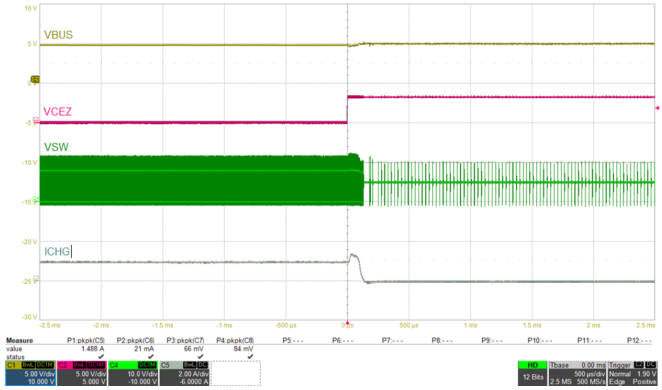
VBUS = 5 V VBAT = 6.0 V ICHG = 1 A

Figure 21. Adapter Power Up with Charge Enabled



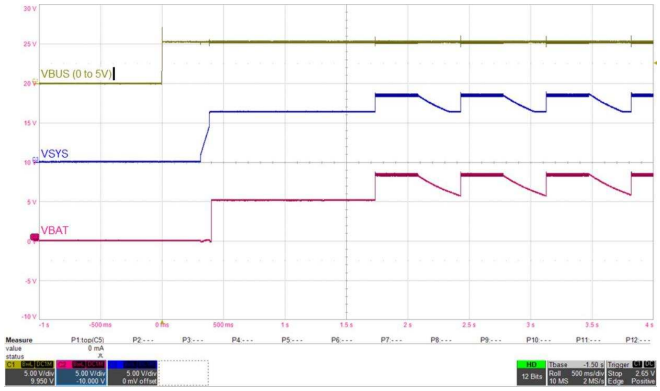
VBUS = 5 V VBAT = 7.4 V ICHG = 1 A

Figure 22. Charge Enable



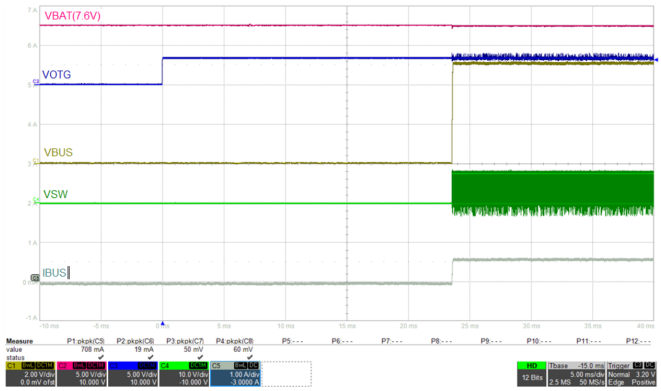
VBUS = 5 V VBAT = 7.4 V ICHG = 1 A

Figure 23. Charge Disabled



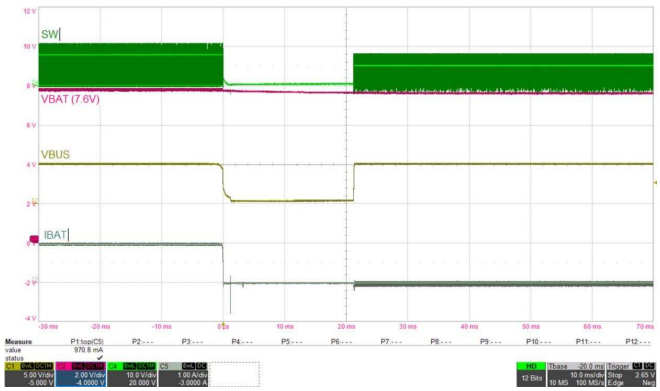
VBUS = 5 V VBAT = Open Charge enabled

Figure 24. Adapter Plug-in with No Battery



VBAT = 7.6 V VBUS = 5.1 V No IBUS load

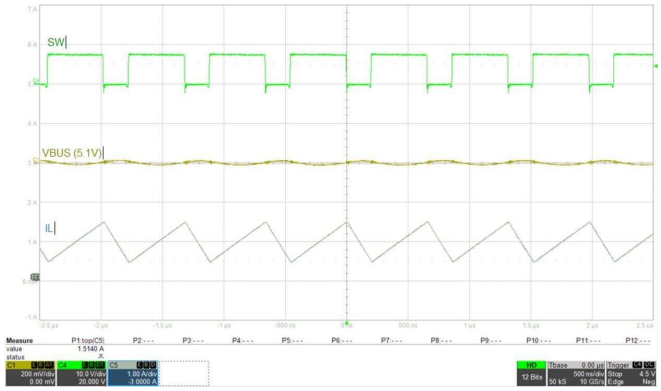
Figure 25. Buck Mode (OTG) Startup



VBAT = 7.6 V Adapter removed with OTG = HIGH R_{BUS} = 25 Ω

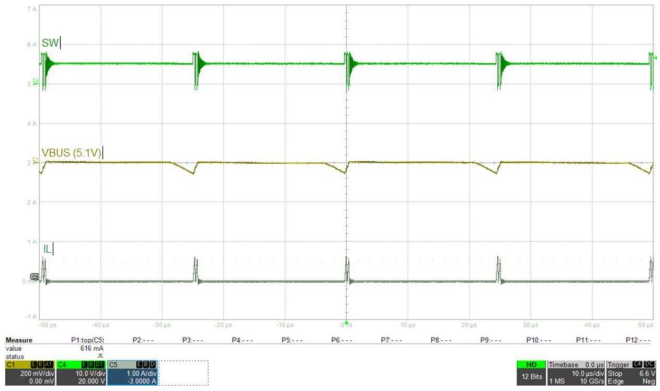
Figure 26. Buck Mode Startup After Adapter Removal

C_{VBUS} = 1 µF, C_{PMID}= 10 µF, C_{BAT} = 10 µF, C_{SYS} = 44 µF, L = DFE252012F-1R0 (1 µH) (unless otherwise specified)



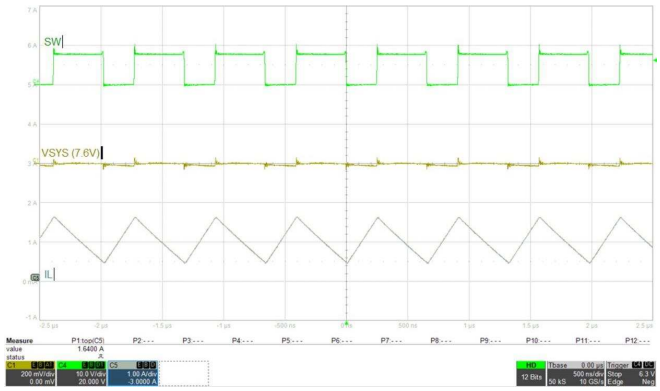
VBAT = 7.6 V VBUS = 5.1 V IBUS = 1 A

Figure 27. Buck Mode (OTG) PWM Switching



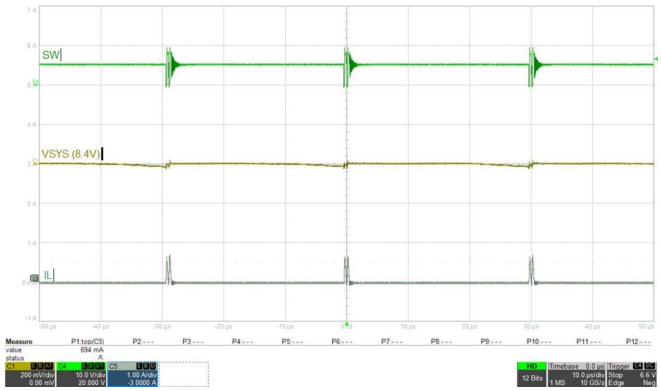
VBAT = 7.6 V VBUS = 5.1 V IBUS = 0 mA

Figure 28. Buck Mode (OTG) PFM Switching



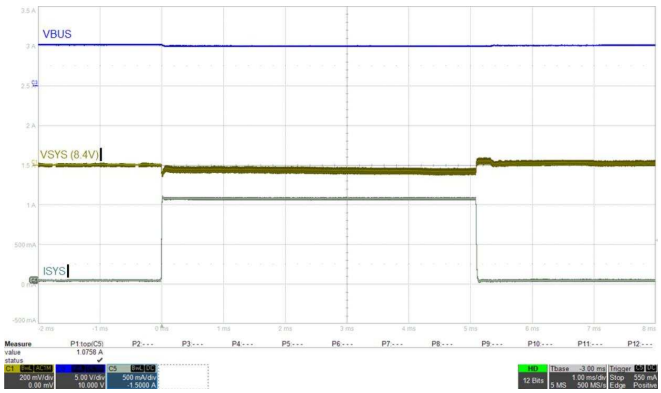
VBUS = 5 V VBAT = 7.6 V ICHG = 1 A

Figure 29. Boost Mode PWM Switching



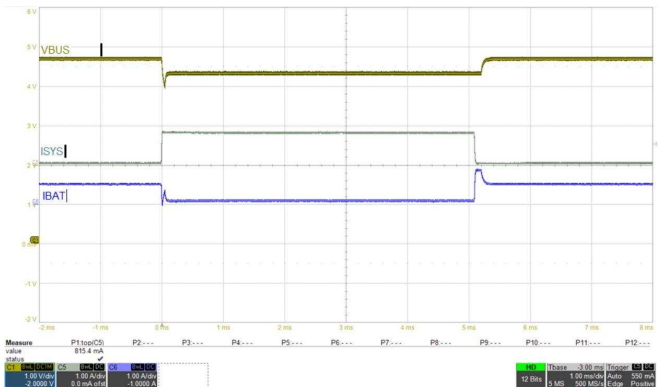
VBUS = 5 V VBAT = 8.4 V Charge disabled

Figure 30. Boost Mode PFM Switching



VBUS = 5 V VBAT = 8.4 V Charge disabled

Figure 31. System Load Transient Response



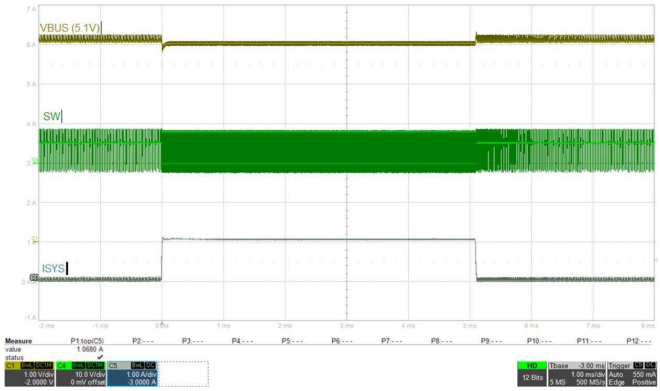
DCP Adapter VBAT = 8.0 V Charge enabled

Figure 32. VINDPM Transient Response

C_{VBUS} = 1 µF, C_{PMID}= 10 µF, C_{BAT} = 10 µF, C_{SYS} = 44 µF, L = DFE252012F-1R0 (1 µH) (unless otherwise specified)

DCP Adapter VBAT = 8.0 V Charge enabled

Figure 33. IINDPM Transient Response



VBAT = 7.6 V VBUS = 5.1 V

Figure 34. Buck Mode (OTG) Load Transient Response

10 Power Supply Recommendations

In order to provide an output voltage on SYS, the device requires a power supply between 3.9-V and 6.2-V input with at least 500-mA current rating connected to VBUS or a 2-cell Li-Ion battery with voltage > VBAT_UVLO connected to BAT. The source current rating needs to be at least 3-A in order for the boost converter of the charger to provide maximum output power to SYS.

11 Layout

11.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loops is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Here is a PCB layout priority list for proper layout. Layout PCB according to this specific order is essential.

1. Put SYS output capacitor as close to SYS and GND pins as possible. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
2. Place PMID input capacitor as close as possible to PMID pins and PGND pins and use shortest copper trace connection or GND plane.
3. Place inductor input terminal to SW pins as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the input current. Minimize parasitic capacitance from this area to any other trace or plane.
4. Decoupling capacitors should be placed on the same side of and next to the IC and make trace connection as short as possible.
5. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground.
6. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
7. Via size and number should be enough for a given current path.

Refer to the EVM design and the Layout Example below for the recommended component placement with trace and via locations.

11.2 Layout Example

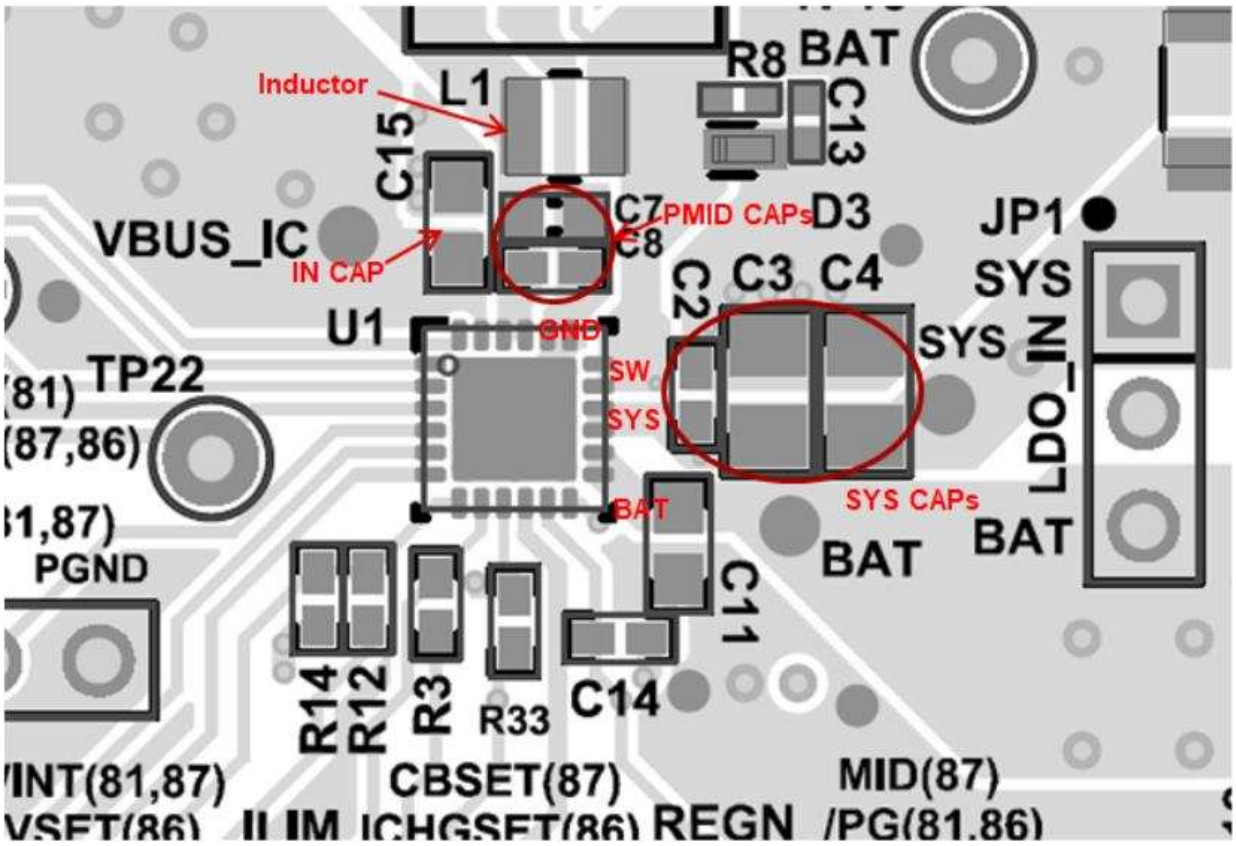


Figure 35. PCB Layout Example

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

12.2 Documentation Support

12.2.1 Related Documentation

For related documentation see the following:

- *BQ2588x Boosting Battery Chargers Evaluation Module User's Guide*

12.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
BQ25886RGER	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25886
BQ25886RGER.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25886
BQ25886RGERG4	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25886
BQ25886RGERG4.A	Active	Production	VQFN (RGE) | 24	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25886
BQ25886RGET	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25886
BQ25886RGET.A	Active	Production	VQFN (RGE) | 24	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ25886

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

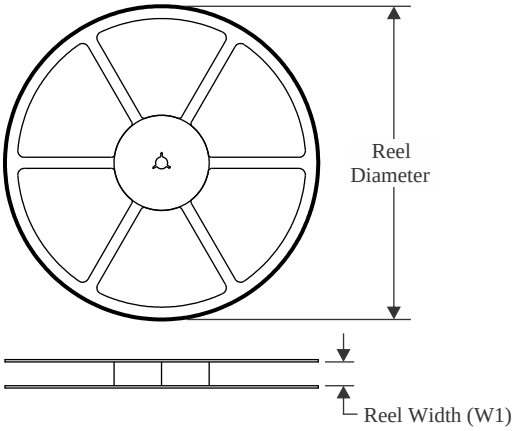
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

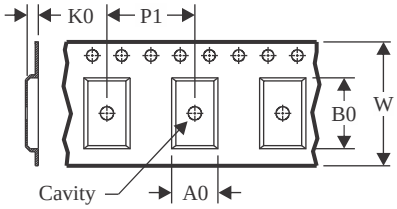
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

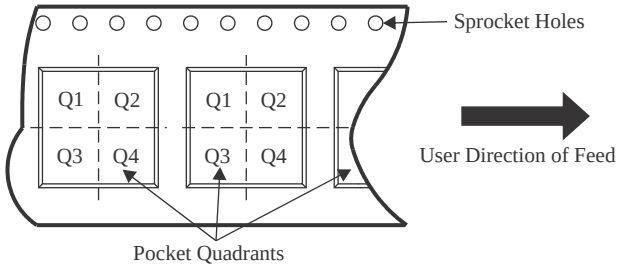


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

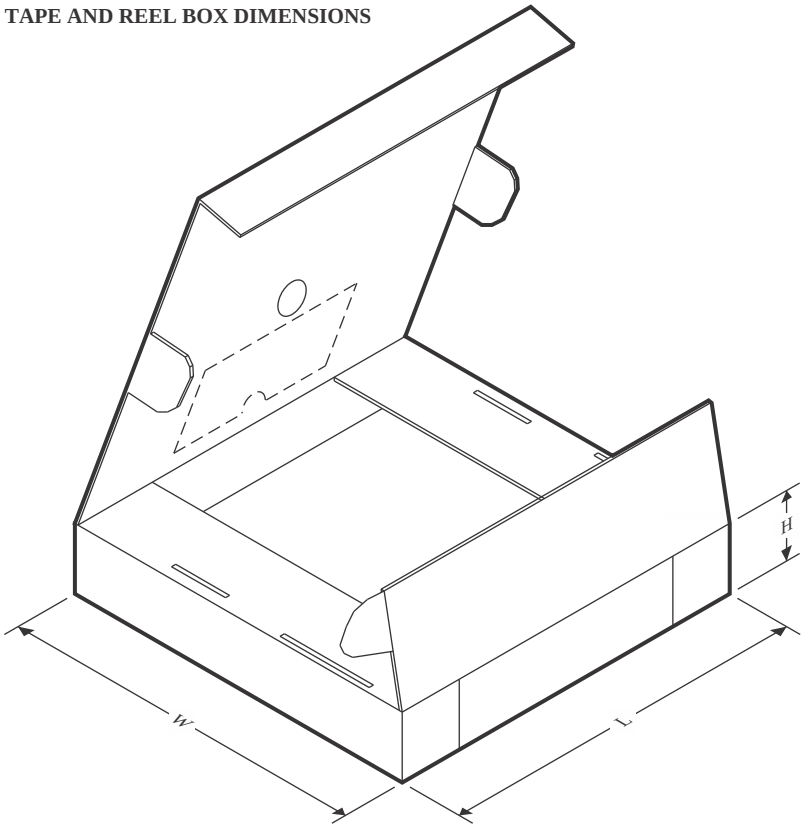
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25886RGER	VQFN	RGE	24	3000	330.0	12.4	4.3	4.3	1.3	8.0	12.0	Q2
BQ25886RGER	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25886RGERG4	VQFN	RGE	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25886RGET	VQFN	RGE	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



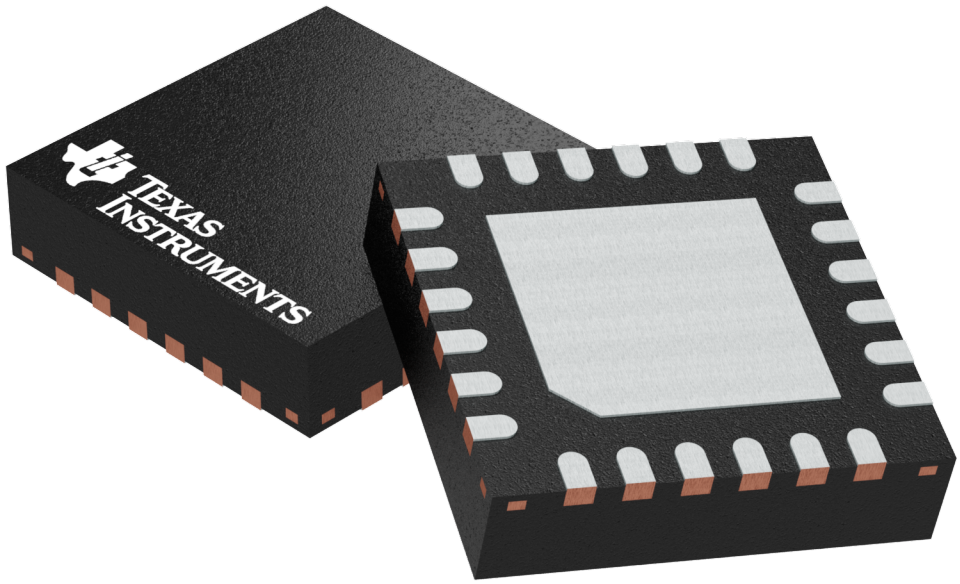
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25886RGER	VQFN	RGE	24	3000	356.0	356.0	36.0
BQ25886RGER	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ25886RGERG4	VQFN	RGE	24	3000	367.0	367.0	35.0
BQ25886RGET	VQFN	RGE	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

RGE 24 VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

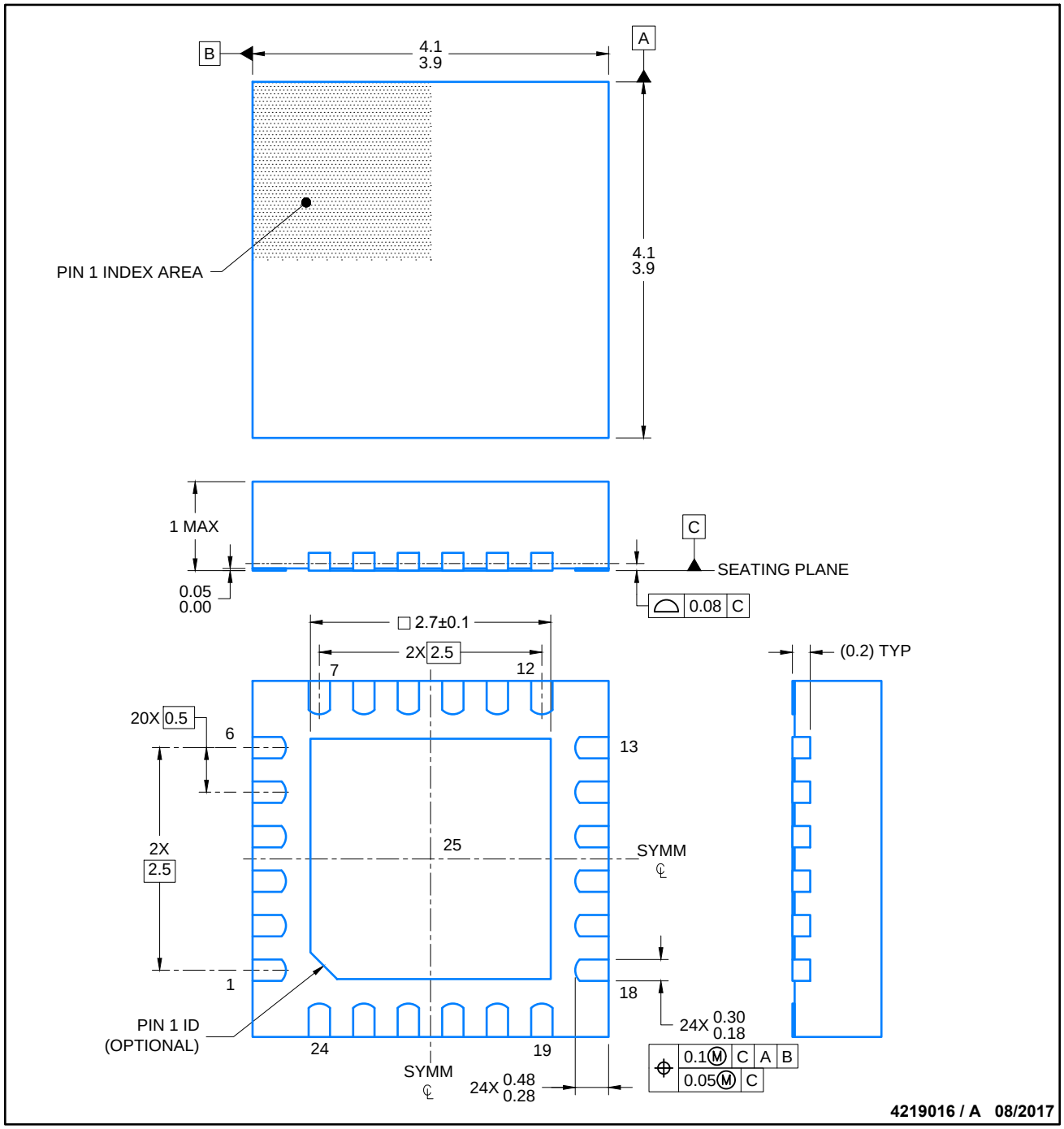
4204104/H

PACKAGE OUTLINE

RGE0024H

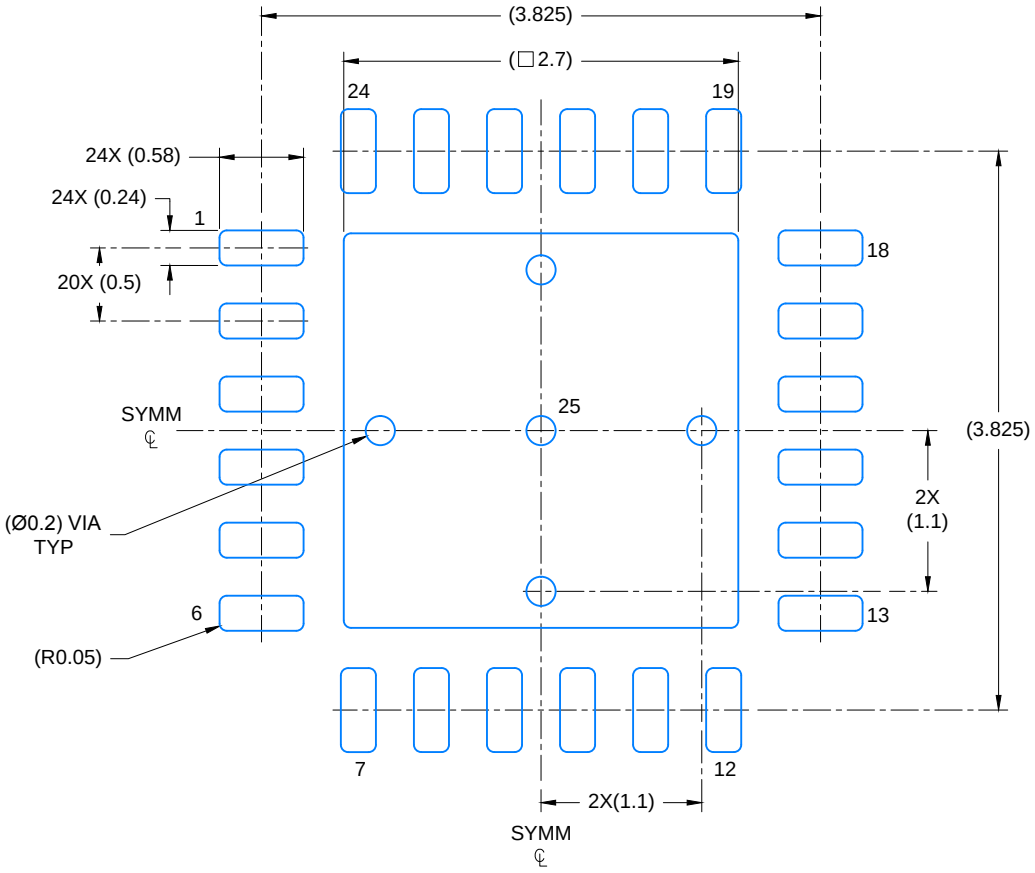
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



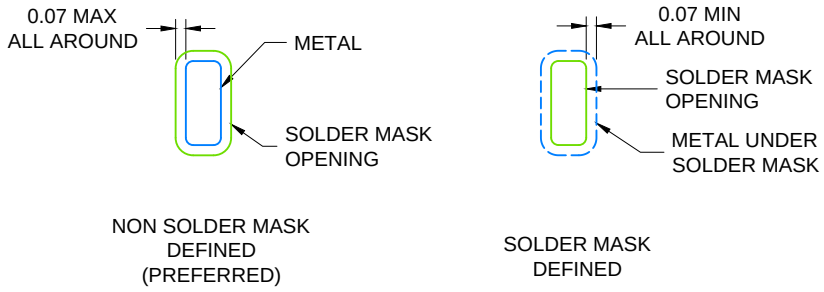
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X



SOLDER MASK DETAILS

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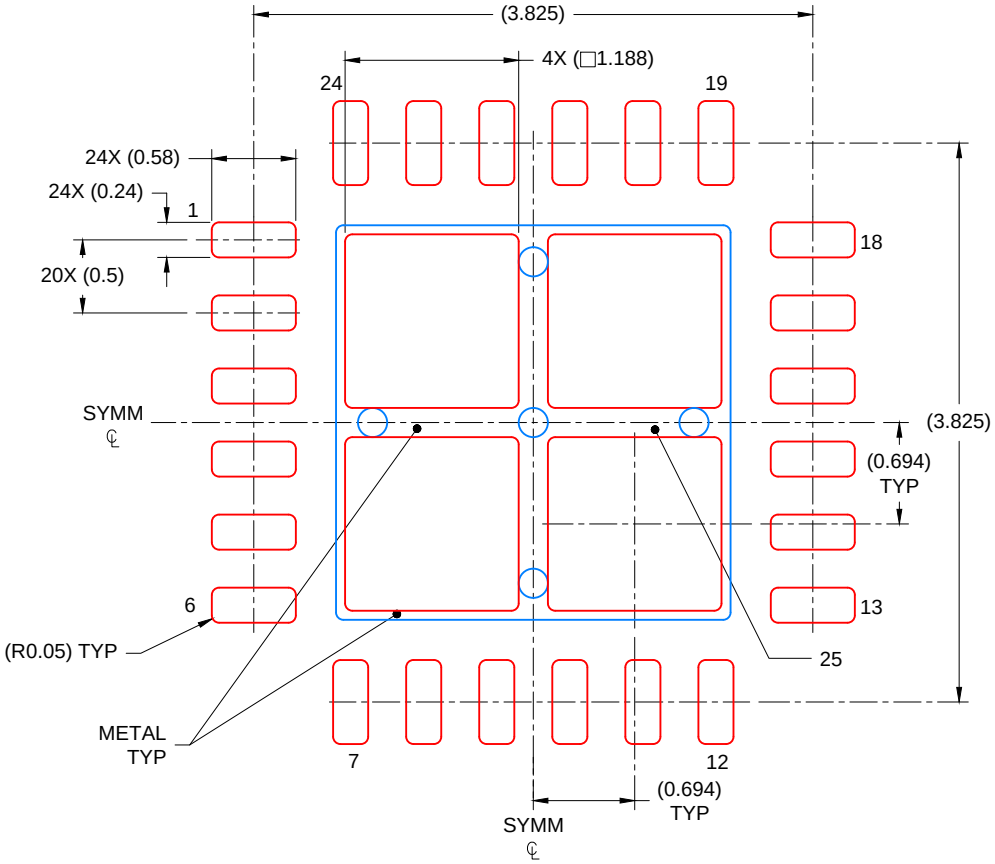
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
78% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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