

# BQ7716xy Overvoltage Protection for 2-Series to 4-Series Cell Li-Ion Batteries with External Delay Capacitor

## 1 Features

- 2-, 3-, and 4-series cell overvoltage protection
- External capacitor-programmed delay timer
- Fixed OVP threshold
- High-accuracy overvoltage protection:  $\pm 10$  mV
- Low power consumption  $I_{CC} \approx 1$   $\mu$ A ( $V_{CELL(ALL)} < V_{PROTECT}$ )
- Low leakage current per cell input  $< 100$  nA
- Small package footprint
  - 8-pin WSON (3.00 mm  $\times$  4.00 mm)

## 2 Applications

- [Power tools](#)
- [UPS battery backup](#)
- [Light electric vehicles](#)
  - eBike
  - eScooter
  - Pedal assist bicycles

## 3 Description

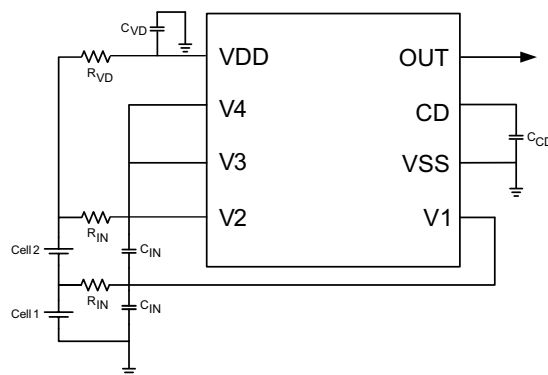
The BQ7716xy device family provides an overvoltage monitor and protector for Li-Ion battery pack systems. Each cell is monitored independently for an overvoltage condition. For quicker production-line testing, the BQ7716xy device provides a Customer Test Mode with greatly reduced delay time.

In the BQ7716xy device, an external delay timer is initiated upon detection of an overvoltage condition on any cell. Upon expiration of the delay timer, the output is triggered into its active state (either high or low, depending on the configuration). The external delay timer feature also includes the ability to detect an open or shorted delay capacitor on the CD pin, which will similarly trigger the output driver in an overvoltage condition.

**Table 3-1. Device Information Table<sup>(1)</sup>**

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ771600	WSON (8)	3.00 mm $\times$ 4.00 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet and the [Device Comparison Table](#).



**Simplified Schematic**



## Table of Contents

<b>1 Features</b> .....	1	8.4 Device Functional Modes.....	11
<b>2 Applications</b> .....	1	<b>9 Application and Implementation</b> .....	13
<b>3 Description</b> .....	1	9.1 Application Information.....	13
<b>4 Revision History</b> .....	2	9.2 Typical Application.....	14
<b>5 Device Comparison Table</b> .....	3	<b>10 Power Supply Recommendations</b> .....	15
<b>6 Pin Configuration and Functions</b> .....	3	<b>11 Layout</b> .....	15
<b>7 Specifications</b> .....	4	11.1 Layout Guidelines.....	15
7.1 Absolute Maximum Ratings.....	4	11.2 Layout Example.....	15
7.2 ESD Ratings.....	4	<b>12 Device and Documentation Support</b> .....	16
7.3 Recommended Operating Conditions.....	4	12.1 Receiving Notification of Documentation Updates..	16
7.4 Thermal Information.....	4	12.2 Support Resources.....	16
7.5 Electrical Characteristics.....	6	12.3 Trademarks.....	16
7.6 Typical Characteristics.....	8	12.4 Electrostatic Discharge Caution.....	16
<b>8 Detailed Description</b> .....	9	12.5 Export Control Notice.....	16
8.1 Overview.....	9	12.6 Glossary.....	16
8.2 Functional Block Diagram.....	9	<b>13 Mechanical, Packaging, and Orderable Information</b> .....	17
8.3 Feature Description.....	9		

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision D (July 2015) to Revision E (April 2021)</b>	<b>Page</b>
• Removed Product Preview devices.....	3
• Removed Product Preview devices.....	6
<b>Changes from Revision C (August 2014) to Revision D (July 2015)</b>	<b>Page</b>
• Changed QFN to WSON .....	1
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Changed the BQ771605 to Production Data.....	3
• Added table note 2, which was hidden inadvertently.....	4
• Moved <i>Pin Details</i> to <i>Feature Description</i> section .....	9
• Moved from <i>Application Information</i> section to <i>Design Requirements</i> section .....	14

## 5 Device Comparison Table

PART NUMBER	OVP (V)	OV HYSTERESIS (V)	OUTPUT DRIVE	TAPE AND REEL (LARGE)	TAPE AND REEL (SMALL)
BQ771600	4.3	0.3	CMOS Active High	BQ771600DPJR	BQ771600DPJT
BQ771601	4.225	0.05	CMOS Active High	BQ771601DPJR	BQ771601DPJT
BQ771602	4.225	0.05	NCH Active Low, Open Drain	BQ771602DPJR	BQ771602DPJT
BQ771604	4.2	0.05	CMOS Active High	BQ771604DPJR	BQ771604DPJT
BQ771605	3.85	0.25	NCH Active Low	BQ771605DPJR	BQ771605DPJT
BQ771611	4.35	0.3	CMOS Active High	BQ771611DPJR	BQ771611DPJT
BQ771612	3.9	0.3	CMOS Active High	BQ771612DPJR	BQ771612DPJT
BQ7716xy future options <sup>(1)</sup>	3.85–4.65	0–0.3	CMOS Active High or NCH Active Low, Open Drain	BQ7716xyTBD	BQ7716xyTBD

(1) Contact TI.

## 6 Pin Configuration and Functions

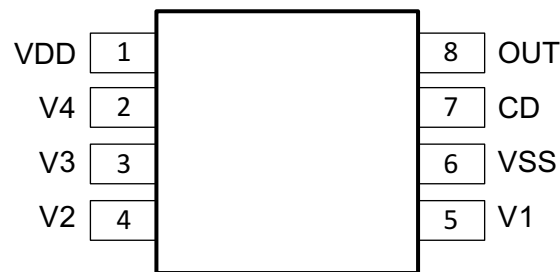


Figure 6-1. DPJ Package 8-Pin WSON Top View

Table 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.	I/O <sup>(1)</sup>	
CD	7	I/O	External capacitor connection for delay timer
OUT	8	OA	Output drive for overvoltage fault signal
VDD	1	P	Power supply
VSS	6	P	Electrically connected to IC ground and negative terminal of the lowest cell in the stack
V1	5	I	Sense input for positive voltage of the lowest cell in the stack
V2	4	I	Sense input for positive voltage of the second cell from the bottom of the stack
V3	3	I	Sense input for positive voltage of the third cell from the bottom of the stack
V4	2	I	Sense input for positive voltage of the fourth cell from the bottom of the stack

(1) IA = Input Analog, OA = Output Analog, P = Power Connection

## 7 Specifications

### 7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
Supply voltage range <sup>(2)</sup>	VDD–VSS	–0.3	30	V
Input voltage range <sup>(2)</sup>	V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	–0.3	30	V
Output voltage range <sup>(2)</sup>	OUT–VSS	–0.3	30	V
Continuous total power dissipation, P <sub>TOT</sub>		See package dissipation rating.		
Functional temperature		–40	110	°C
Lead temperature (soldering, 10 s), T <sub>SOLDER</sub>		300		°C
Storage temperature, T <sub>stg</sub>		–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Absolute maximum ratings for input voltage range, output voltage range, and supply voltage are assured by design and not tested in production.

### 7.2 ESD Ratings

		VALUE	UNIT
V <sub>ESD</sub> Rating	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±500	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V <sub>DD</sub> <sup>(1)</sup>	Supply voltage	3		20	V
V4–V3, V3–V2, V2–V1, V1–VSS, or CD–VSS	Input voltage range	0		5	V
T <sub>A</sub>	Operating ambient temperature range	–40		110	°C

- (1) See [Section 9.2](#).

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		BQ7716xy		UNIT
		DPJ (WSON)		
		8 PINS		
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	56.6		°C/W
R <sub>θJC(top)</sub>	Junction-to-case(top) thermal resistance	56.4		°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	30.6		°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	1.0		°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	37.8		°C/W

THERMAL METRIC <sup>(1)</sup>	BQ7716xy	UNIT
	DPJ (WSON)	
	8 PINS	
R <sub>θJC(bot)</sub> Junction-to-case(bottom) thermal resistance	11.3	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

## 7.5 Electrical Characteristics

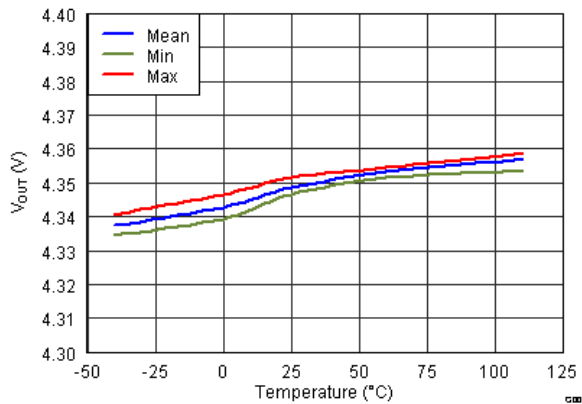
Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 14.4\text{V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $+110^\circ\text{C}$  and  $V_{DD} = 3\text{V}$  to  $20\text{V}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>VOLTAGE PROTECTION THRESHOLD VCx</b>						
$V_{OV}$	$V_{(PROTECT)}$ Overvoltage Detection	BQ771600		4.300		V
		BQ771601		4.225		V
		BQ771602		4.225		V
		BQ771604		4.200		V
		BQ771605		3.850		V
		BQ771611		4.350		V
		BQ771612		3.900		V
$V_{HYS}$	OV Detection Hysteresis	BQ771600	250	300	400	mV
		BQ771601	25	50	75	mV
		BQ771602	25	50	75	mV
		BQ771604	25	50	75	mV
		BQ771605	200	250	300	mV
		BQ771611	250	300	400	mV
		BQ771612	250	300	400	mV
$V_{OA}$	OV Detection Accuracy	$T_A = 25^\circ\text{C}$	-10		10	mV
$V_{OADRIFT}$	OV Detection Accuracy Across Temperature	$T_A = -40^\circ\text{C}$	-40		44	mV
		$T_A = 0^\circ\text{C}$	-20		20	mV
		$T_A = 60^\circ\text{C}$	-24		24	mV
		$T_A = 110^\circ\text{C}$	-54		54	mV
<b>SUPPLY AND LEAKAGE CURRENT</b>						
$I_{CC}$	Supply Current	$(V_4-V_3) = (V_3-V_2) = (V_2-V_1) = (V_1-V_{SS}) = 4.0\text{V}$ (See <a href="#">Figure 8-3.</a> )		1	2	$\mu\text{A}$
$I_{IN}$	Input Current at Vx Pins	$(V_4-V_3) = (V_3-V_2) = (V_2-V_1) = (V_1-V_{SS}) = 4.0\text{V}$ (See <a href="#">Figure 8-3.</a> )	-0.1		0.1	$\mu\text{A}$

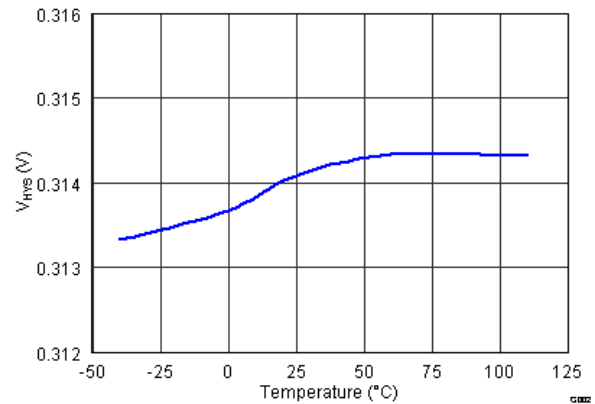
Typical values stated where  $T_A = 25^\circ\text{C}$  and  $V_{DD} = 14.4\text{V}$ , MIN/MAX values stated where  $T_A = -40^\circ\text{C}$  to  $+110^\circ\text{C}$  and  $V_{DD} = 3\text{V}$  to  $20\text{V}$  (unless otherwise noted).

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>OUTPUT DRIVE OUT, CMOS ACTIVE HIGH VERSIONS ONLY</b>						
$V_{OUT1}$	Output Drive Voltage, Active High	$(V4-V3), (V3-V2), (V2-V1),$ or $(V1-VSS) > V_{OV}, V_{DD} = 14.4\text{V}, I_{OH} = 100\ \mu\text{A}$	6		V	
		If three of four cells are short circuited, only one cell remains powered and $> V_{OV}, V_{DD} = V_x$ (cell voltage), $I_{OH} = 100\ \mu\text{A}$	$V_{DD} - 0.3$		V	
		$(V4-V3), (V3-V2), (V2-V1),$ and $(V1-VSS) < V_{OV}, V_{DD} = 14.4\text{V}, I_{OL} = 100\ \mu\text{A}$ measured into OUT pin	250	400	mV	
$I_{OUTH1}$	OUT Source Current (During OV)	$(V4-V3), (V3-V2), (V2-V1),$ or $(V1-VSS) > V_{OV}, V_{DD} = 14.4\text{V}, \text{OUT} = 0\text{V}.$ Measured out of OUT pin		4.5	mA	
$I_{OUTL1}$	OUT Sink Current (No OV)	$(V4-V3), (V3-V2), (V2-V1),$ and $(V1-VSS) < V_{OV}, V_{DD} = 14.4\text{V}, \text{OUT} = V_{DD}.$ Measured into OUT pin	0.5	14	mA	
<b>OUTPUT DRIVE OUT, NCH OPEN DRAIN ACTIVE LOW VERSIONS ONLY</b>						
$V_{OUT2}$	Output Drive Voltage, Active Low	$(V4-V3), (V3-V2), (V2-V1),$ or $(V1-VSS) > V_{OV}, V_{DD} = 14.4\text{V}, I_{OL} = 100\ \mu\text{A}$ measured into OUT pin		250	400	mV
$I_{OUTH2}$	OUT Sink Current (During OV)	$(V4-V3), (V3-V2), (V2-V1),$ or $(V1-VSS) > V_{OV}, V_{DD} = 14.4\text{V}.$ $\text{OUT} = V_{DD}.$ Measured into OUT pin	0.5	14	mA	
$I_{OUTLK}$	OUT Pin Leakage	$(V4-V3), (V3-V2), (V2-V1),$ and $(V1-VSS) < V_{OV}, V_{DD} = 14.4\text{V}, \text{OUT} = V_{DD}.$ Measured out of OUT pin		100	nA	
<b>DELAY TIMER</b>						
$t_{CD}$	OV Delay Time	$C_{CD} = 0.1\ \mu\text{F}$	1	1.5	2	s
$V_{CD}$	CD Fault Detection External Comparator Threshold, Initial Charge Value	The CD pin will first be quickly charged to this value before being discharged back to VSS.		1.5		V
$t_{CHGDELAY}$	CD Charging Delay	OVP to OUT delay with CD shorted to ground	20		170	ms
$I_{CHG}$	OV Detection Charging Current	CD pin fast charging current from VSS to $V_{CD}$ to begin delay countdown		300		$\mu\text{A}$
$I_{DSG}$	OV Detection Discharging Current	CD pin discharging current from $V_{DELAY}$ to VSS		100		nA

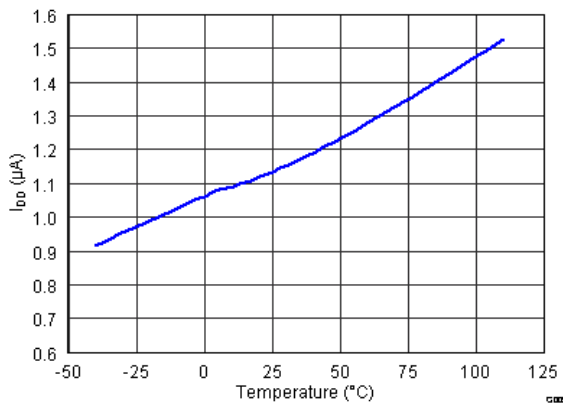
## 7.6 Typical Characteristics



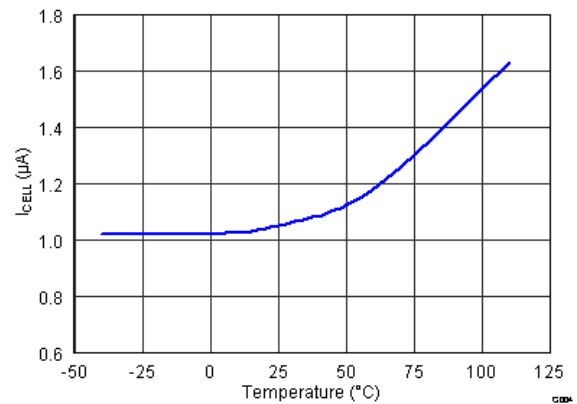
**Figure 7-1. Overvoltage Threshold (OVT) vs. Temperature**



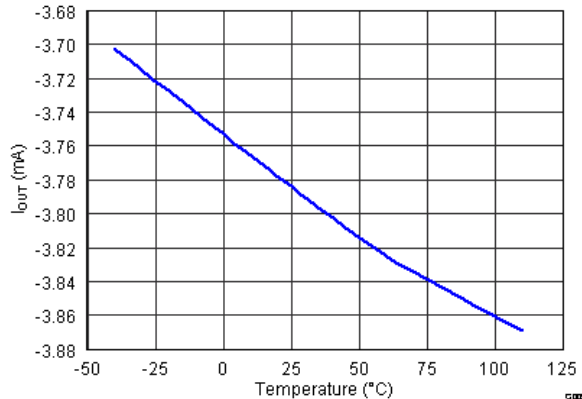
**Figure 7-2. Hysteresis  $V_{HYS}$  vs. Temperature**



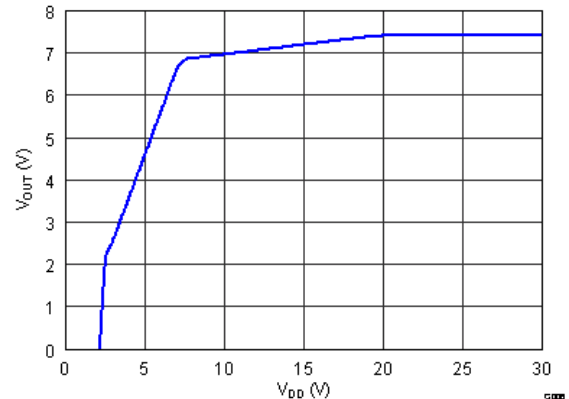
**Figure 7-3.  $I_{DD}$  Current Consumption vs. Temperature at  $V_{DD} = 16\text{ V}$**



**Figure 7-4.  $I_{CELL}$  vs. Temperature at  $V_{CELL} = 9.2\text{ V}$**



**Figure 7-5. Output Current  $I_{OUT}$  vs. Temperature**



**Figure 7-6.  $V_{OUT}$  vs.  $V_{DD}$**



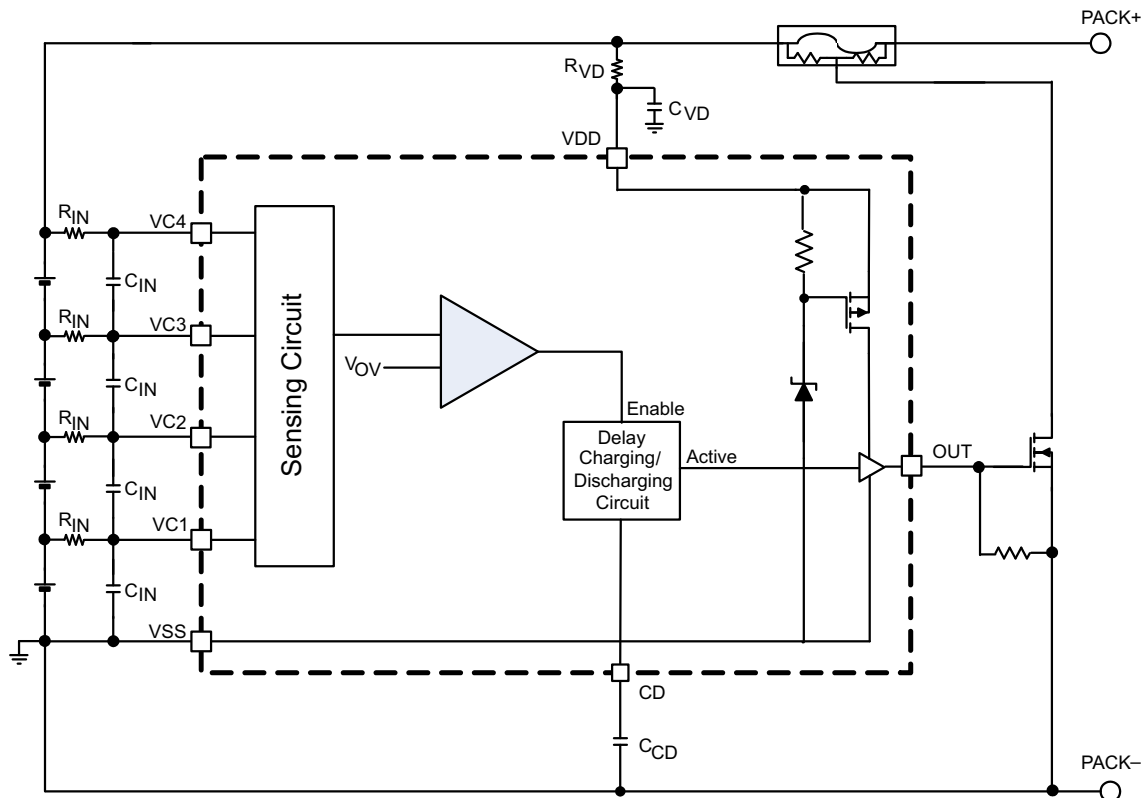
## 8 Detailed Description

### 8.1 Overview

In the BQ7716xy family of devices for overvoltage protection, each cell is monitored independently and an external delay timer is initiated if an overvoltage condition is detected when any cell voltage is higher than the protection voltage threshold,  $V_{OV}$ . After the delay time expires, the OUT pin is inserted.

For quicker production-line testing, the device provides a Customer Test Mode with greatly reduced delay time.

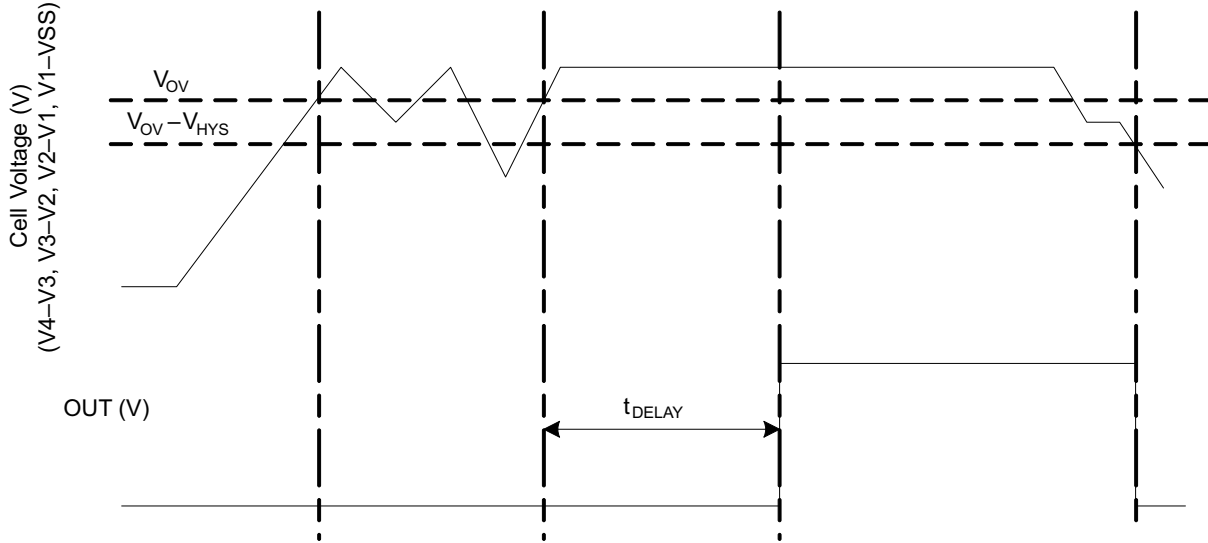
### 8.2 Functional Block Diagram



### 8.3 Feature Description

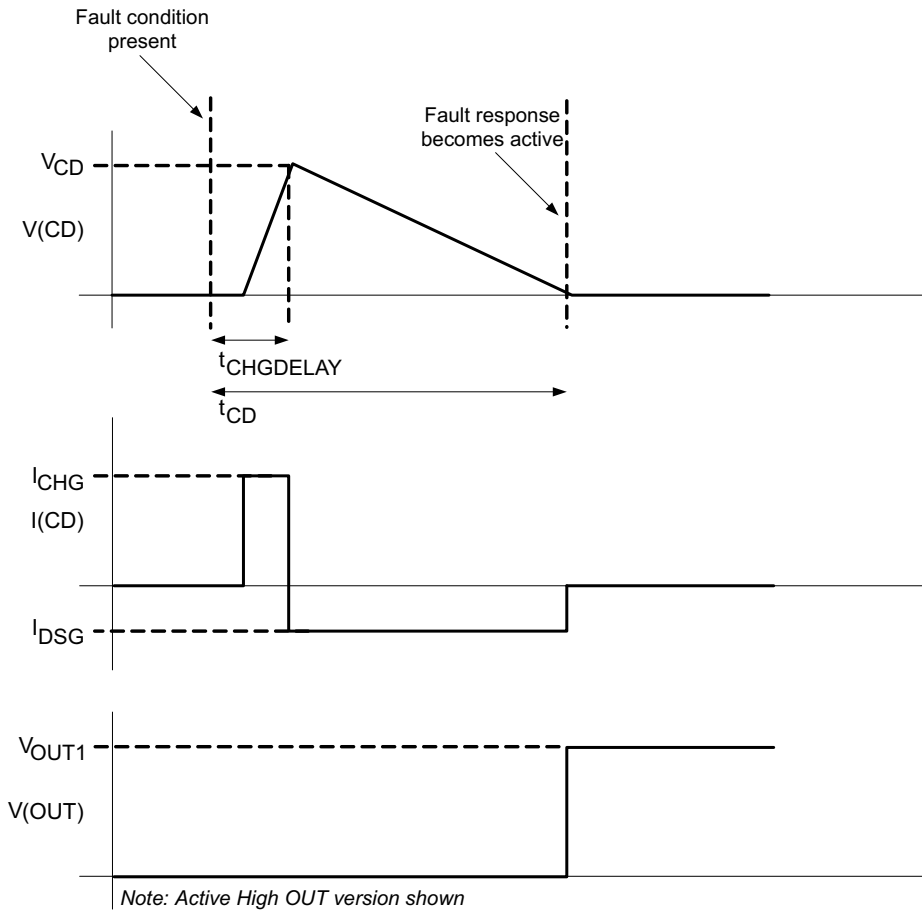
In the BQ7716xy device, each cell is monitored independently. Overvoltage is detected by comparing the actual cell voltage to a protection voltage reference,  $V_{OV}$ . If any cell voltage exceeds the programmed OV value, a timer circuit is activated. This timer circuit charges the CD pin to a nominal value, then slowly discharges it with a fixed current back down to VSS. When the CD pin falls below a nominal threshold near VSS, the OUT terminal goes from inactive to active state. Additionally, a timeout detection circuit checks to ensure that the CD pin successfully begins charging to above VSS and subsequently drops back down to VSS, and if a timeout error is detected in either direction, it will similarly trigger the OUT pin to become active. See [Figure 8-1](#) for reference.

For an NCH Open Drain Active Low configuration, the OUT pin pulls down to VSS when active (OV present), and is high impedance when inactive (no OV).



**Figure 8-1. Timing for Overvoltage Sensing**

Figure 8-2 shows an overview of the behavior of the CD pin during an OV sequence.



**Figure 8-2. CD Pin Mechanism**

**8.3.1 Sense Positive Input for V<sub>x</sub>**

This is an input to sense each single battery cell voltage. A series resistor and a capacitor across the cell for each input is required for noise filtering and stable voltage monitoring.

### 8.3.2 Output Drive, OUT

This terminal serves as the fault signal output, and may be ordered in either active HIGH or LOW options.

### 8.3.3 Supply Input, VDD

This terminal is the unregulated input power source for the IC. A series resistor is connected to limit the current, and a capacitor is connected to ground for noise filtering.

### 8.3.4 External Delay Capacitor, CD

This terminal is connected to an external capacitor that is used for setting the delay timer during an overvoltage fault event.

The CD pin includes a timeout detection circuit to ensure that the output drives active even with a shorted or open capacitor during an overvoltage event.

The capacitor connected on the CD pin rapidly charges to a voltage if any one of the cell inputs exceeds the OV threshold. Then the delay circuit gradually discharges the capacitor on the CD pin. Once this capacitor discharges below a set voltage, the OUT transitions from an inactive to active state.

To calculate the delay, use the following equation:

$$t_{CD} \text{ (s)} = K \times C_{CD} \text{ (}\mu\text{F)}, \text{ where } K = 10 \text{ to } 20 \text{ range.} \quad (1)$$

Example: If  $C_{CD} = 0.1 \mu\text{F}$  (typical), then the delay timer range is

$$t_{CD} \text{ (s)} = 10 \times 0.1 = 1 \text{ s (Minimum)}$$

$$t_{CD} \text{ (s)} = 20 \times 0.1 = 2 \text{ s (Maximum)}$$

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#### Note

The tolerance on the capacitor used for  $C_{CD}$  increases the range of the  $t_{CD}$  timer.

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## 8.4 Device Functional Modes

### 8.4.1 NORMAL Mode

When all of the cell voltages are below the overvoltage threshold, VOV, the device operates in NORMAL mode. The device monitors the differential cell voltages connected across (V1–VSS), (V2–V1), (V3–V2), and (V4–V3). The OUT pin is inactive and if configured:

- Active high is low
- Active low is being externally pulled up and is an open drain

### 8.4.2 OVERVOLTAGE Mode

OVERVOLTAGE mode is detected if any of the cell voltages exceeds the overvoltage threshold, VOV for configured OV delay time. The OUT pin is activated after a delay time set by the capacitance in the CD pin. The OUT pin will either pull high internally, if configured as active high, or will be pulled low internally, if configured as active low. When all of the cell voltages fall below the (VOV–VHYS), the device returns to NORMAL mode

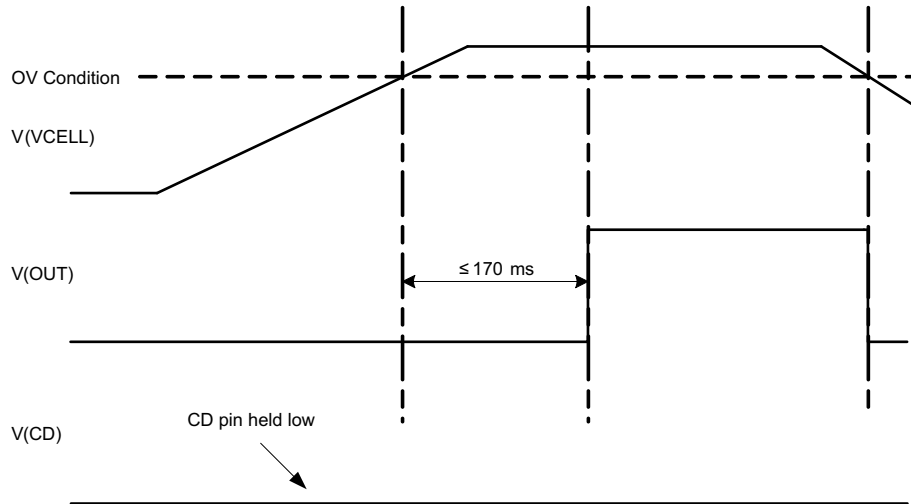
### 8.4.3 Customer Test Mode

It is possible to reduce test time for checking the overvoltage function by simply shorting the external CD capacitor to VSS. In this case, the OV delay would be reduced to the  $t_{(CHGDELAY)}$  value, which has a maximum of 170 ms.

**CAUTION**

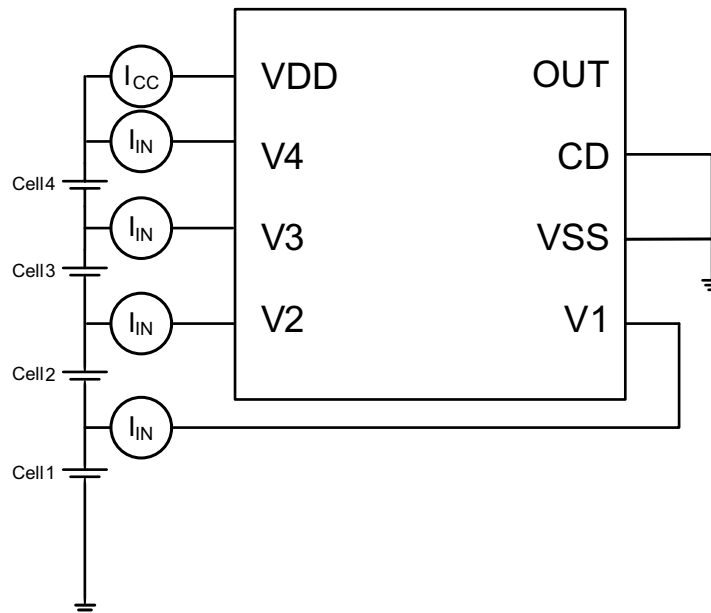
Avoid exceeding any Absolute Maximum Voltages on any pins when placing the part into Customer Test Mode. Also avoid exceeding Absolute Maximum Voltages for the individual cell voltages (V4–V3), (V3–V2), (V2–V1), and (V1–VSS). Stressing the pins beyond the rated limits may cause permanent damage to the device.

Figure 8-3 shows the timing for the Customer Test Mode.



**Figure 8-3. Timing for Customer Test Mode**

Figure 8-4 shows the measurement for current consumption for the product for both VDD and Vx.



**Figure 8-4. Configuration for IC Current Consumption Test**

## 9 Application and Implementation

### Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

### 9.1 Application Information

Figure 9-1 shows each external component.

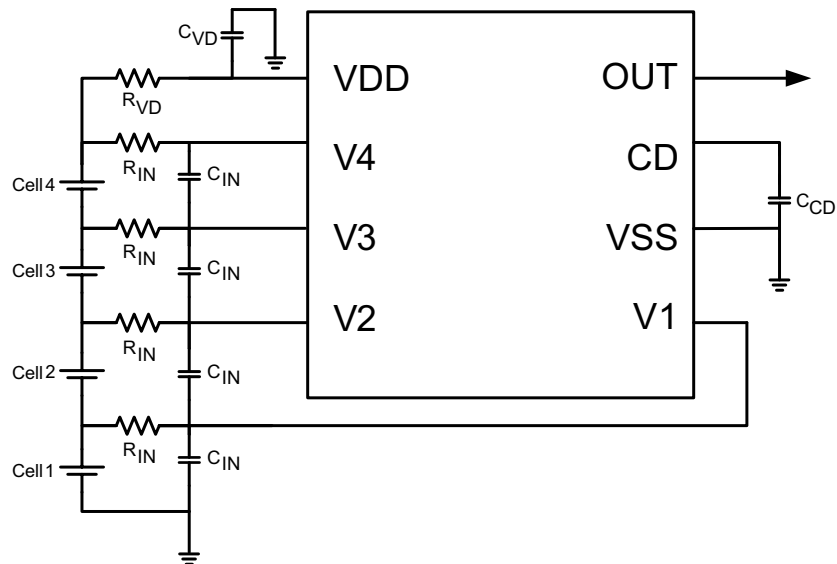


Figure 9-1. Application Configuration

### Note

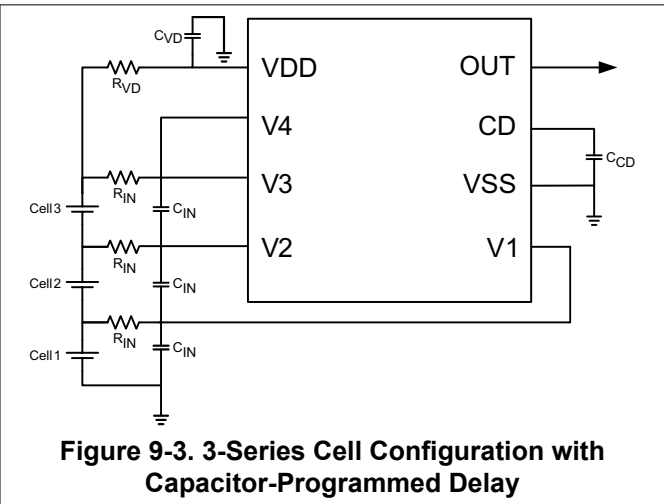
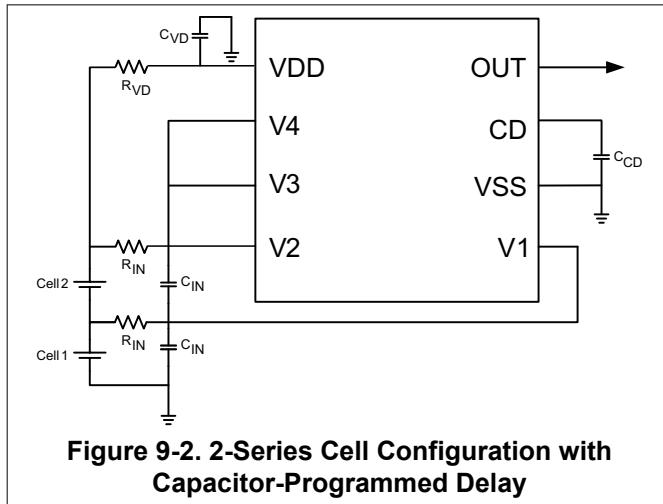
In the case of an Open Drain Active Low configuration, an external pull-up resistor is required on the OUT terminal.

Changes to the ranges stated in Table 9-1 will impact the accuracy of the cell measurements.

### Note

The device is calibrated using an  $R_{IN}$  value = 1 k $\Omega$ . Using a value other than this recommended value changes the accuracy of the cell voltage measurements and  $V_{OV}$  trigger level.

## 9.2 Typical Application



### Note

In these application examples of 2 s and 3 s, an external pull-up resistor is required on the OUT terminal to configure for an Open Drain Active Low operation.

### 9.2.1 Design Requirements

Changes to the ranges stated in [Table 9-1](#) will impact the accuracy of the cell measurements.

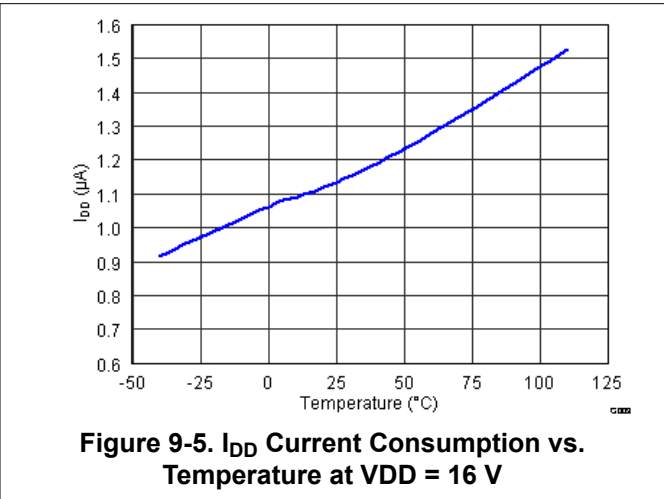
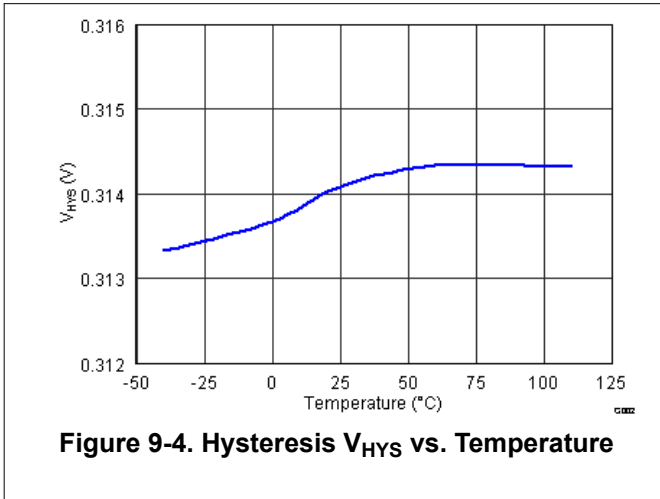
**Table 9-1. Design Parameters**

PARAMETER	EXTERNAL COMPONENT	MIN	NOM	MAX	UNIT
Voltage monitor filter resistance	$R_{IN}$	900	1000	1100	$\Omega$
Voltage monitor filter capacitance	$C_{IN}$	0.01		0.1	$\mu\text{F}$
Supply voltage filter resistance	$R_{VD}$	100		1K	$\Omega$
Supply voltage filter capacitance	$C_{VD}$		0.1		$\mu\text{F}$
CD external delay capacitance	$C_{CD}$		0.1	1	$\mu\text{F}$
OUT Open drain version pull-up resistance to PACK+	$R_{OUT}$		100k		$\Omega$

### 9.2.2 Detailed Design Procedure

- Determine the number of cells in series. The device supports a 2-S to 4-S cell configuration. For 2S and 3S, the top unused pin(s) should be shorted as shown in [Figure 9-2](#) and [Figure 9-3](#).
- Determine the overvoltage protection delay. Follow the calculation example described in [Section 8.3.4](#). Select the correct capacitor to connect to the CD pin.
- Follow the application schematic to connect the device. If the OUT pin is configured to open drain, an external pull-up resistor should be used. Refer to the Out Sink Current specification,  $I_{OUTH2}$  to ensure a proper pull-up resistor value is used, so that the OUT pin sink current is able to pull down the pin during OV condition.

### 9.2.3 Application Curves



## 10 Power Supply Recommendations

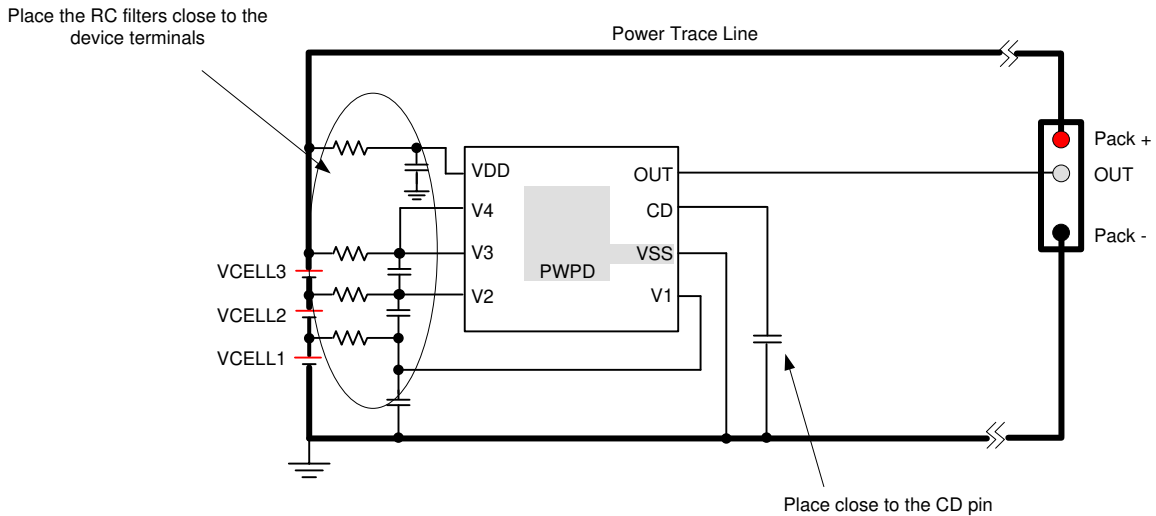
The maximum power of this device is 20 W on VDD.

## 11 Layout

### 11.1 Layout Guidelines

1. Ensure the RC filters for the Vx pins and VDD pin are placed as close as possible to the target terminal, reducing the tracing loop area.
2. The capacitor for CD pin should be placed close to the IC terminals.

### 11.2 Layout Example



**Figure 11-1. Layout**

## 12 Device and Documentation Support

### 12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.5 Export Control Notice

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### 12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.



## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ771600DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		771600	<a href="#">Samples</a>
BQ771600DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		771600	<a href="#">Samples</a>
BQ771601DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		771601	<a href="#">Samples</a>
BQ771601DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		771601	<a href="#">Samples</a>
BQ771602DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		771602	<a href="#">Samples</a>
BQ771602DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		771602	<a href="#">Samples</a>
BQ771604DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771604	<a href="#">Samples</a>
BQ771604DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	771604	<a href="#">Samples</a>
BQ771605DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771605	<a href="#">Samples</a>
BQ771605DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771605	<a href="#">Samples</a>
BQ771611DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771611	<a href="#">Samples</a>
BQ771611DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771611	<a href="#">Samples</a>
BQ771612DPJR	ACTIVE	WSON	DPJ	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771612	<a href="#">Samples</a>
BQ771612DPJT	ACTIVE	WSON	DPJ	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	771612	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

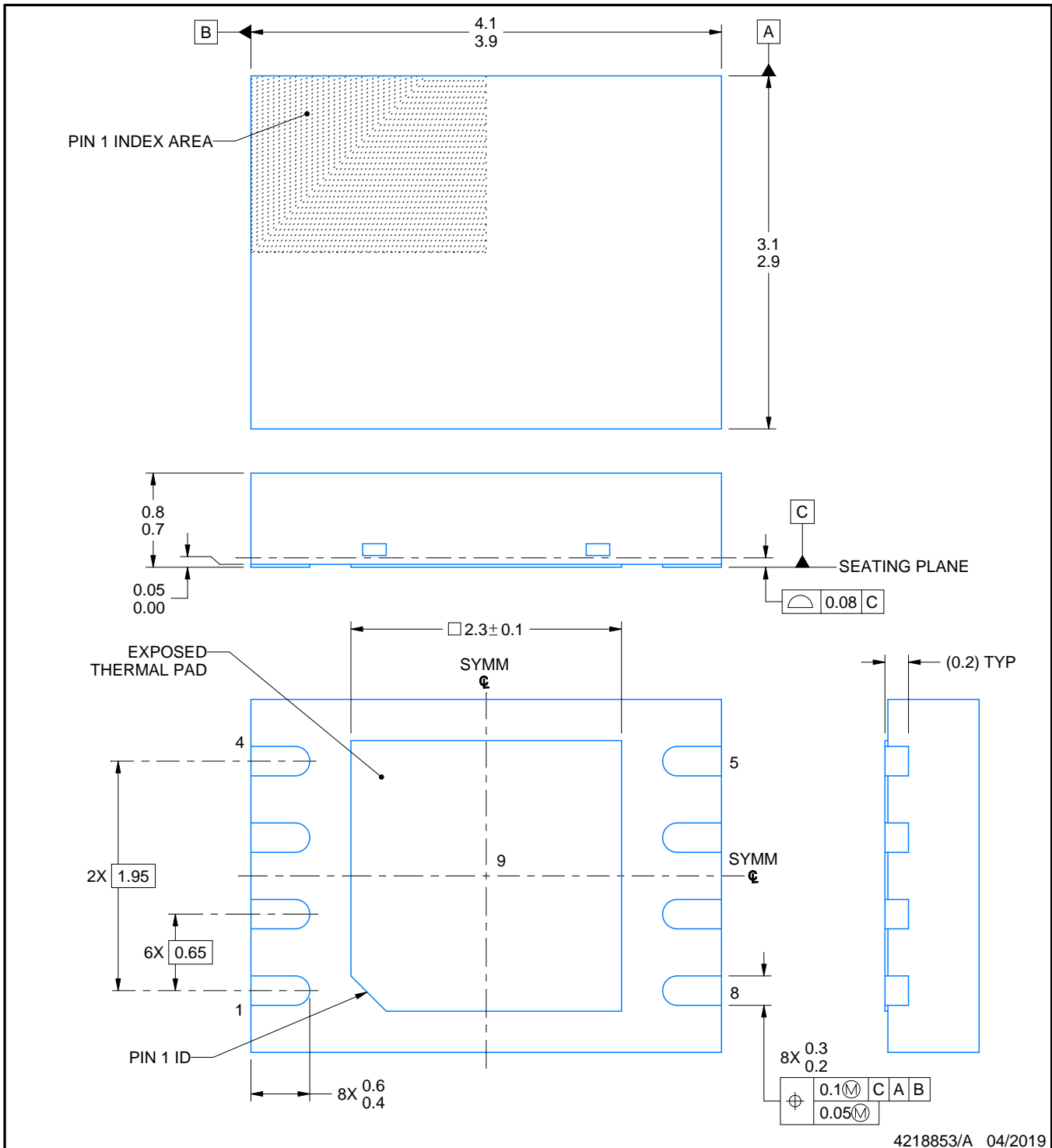
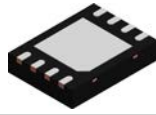
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771600DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771600DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771600DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771600DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771601DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771602DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771602DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771604DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771604DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771605DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771605DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771611DPJR	WSO	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771611DPJT	WSO	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ771612DPJR	WSON	DPJ	8	3000	330.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2
BQ771612DPJT	WSON	DPJ	8	250	180.0	12.4	3.3	4.3	1.1	8.0	12.0	Q2

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ771600DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771600DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771600DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771600DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771601DPJR	WSON	DPJ	8	3000	367.0	367.0	35.0
BQ771601DPJR	WSON	DPJ	8	3000	346.0	346.0	33.0
BQ771601DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771601DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771602DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771602DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771604DPJR	WSON	DPJ	8	3000	346.0	346.0	33.0
BQ771604DPJT	WSON	DPJ	8	250	210.0	185.0	35.0
BQ771605DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771605DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771611DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771611DPJT	WSON	DPJ	8	250	182.0	182.0	20.0
BQ771612DPJR	WSON	DPJ	8	3000	335.0	335.0	25.0
BQ771612DPJT	WSON	DPJ	8	250	182.0	182.0	20.0



NOTES:

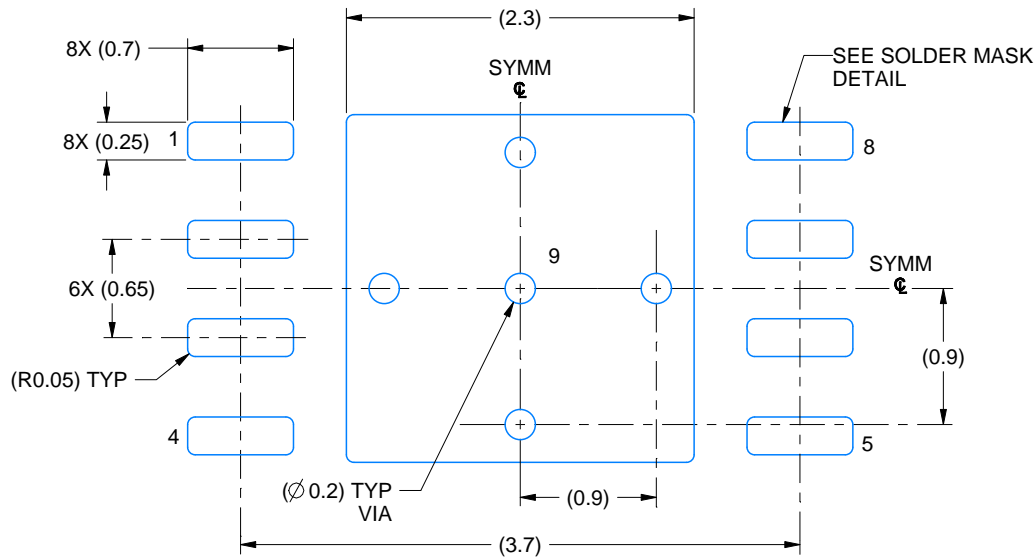
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

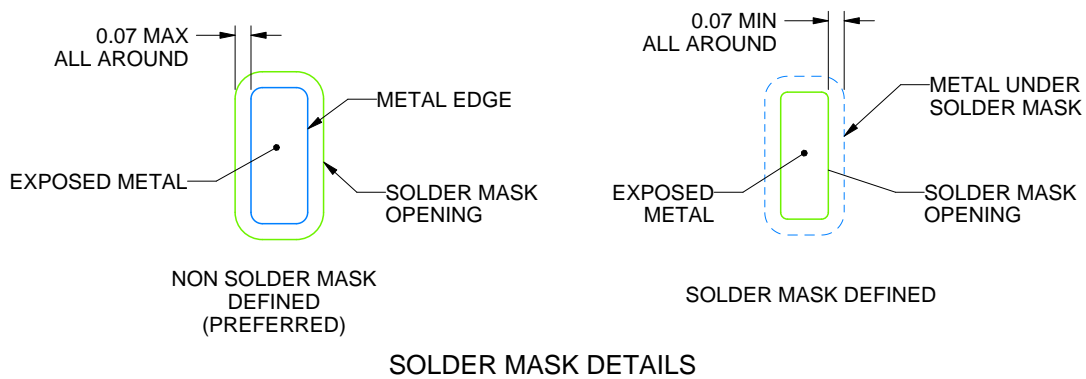
DPJ0008A

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 20X



4218853/A 04/2019

NOTES: (continued)

- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
- Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

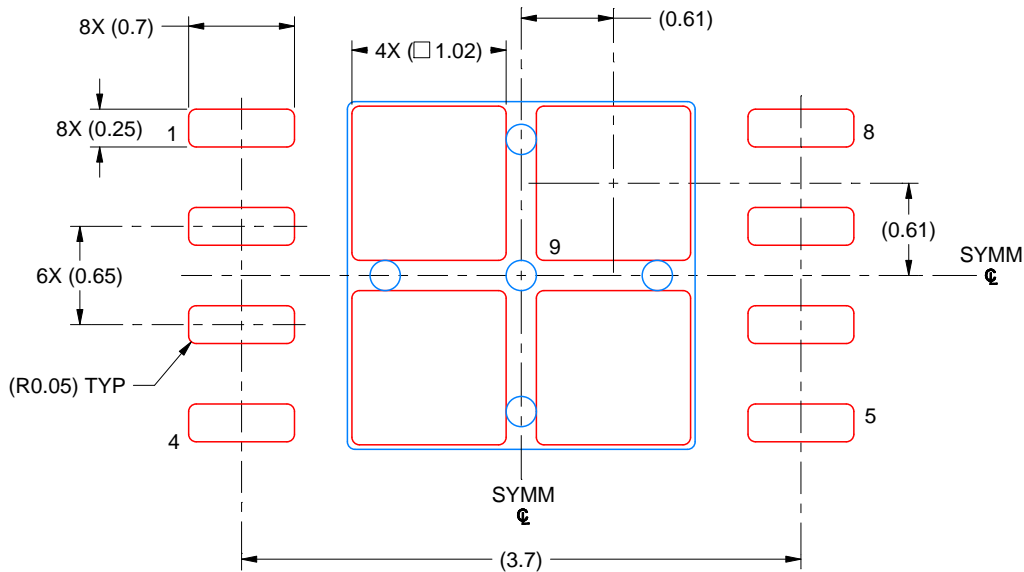


# EXAMPLE STENCIL DESIGN

DPJ0008A

WSO - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE  
BASED ON 0.125 MM THICK STENCIL  
SCALE: 20X

EXPOSED PAD 9  
79% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4218853/A 04/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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