CC330x SimpleLink™ Wi-Fi 6 and Bluetooth® Low Energy companion IC

1 Features

Key Features

- Wi-Fi 6 (802.11ax)
- Bluetooth low energy 5.3 in CC33x1 devices
- Companion IC to any processor or MCU host capable of running a TCP/IP stack
- Integrated 2.4-GHz PA for complete wireless solution with up to +20-dBm output power.
- Operating temperature: -40°C to +105°C
- Application throughput up to 50 Mbps

Extended Features

- Wi-Fi 6
  - 2.4 GHz, 20 MHz, single spatial stream
  - MAC, baseband, and RF transceiver with support for IEEE 802.11 b/g/n/ax
  - Target wake time (TWT), OFDMA, MU-MIMO (Downlink), Basic Service Set Coloring, and trigger frame for improved efficiency
  - Hardware-based encryption and decryption supporting WPA2 and WPA3
  - Excellent interoperability
  - Support for 4 bit SDIO or SPI host interfaces
- Bluetooth Low Energy 5.3
  - LE Coded PHYs (Long Range), LE 2M PHY (High Speed) and Advertising Extension
  - Host controller interface (HCI) transport with option for UART or shared SDIO
- Enhanced Security
  - Secured host interface
  - Firmware authentication
  - Anti-rollback protection
- Multirole support (for example, concurrent STA and AP) to connect with Wi-Fi devices on different RF channels (Wi-Fi networks)
- Optional antenna diversity or selection
- 3-wire or 1-wire PTA for external coexistence with additional 2.4-GHz radios (for example, Thread or Zigbee)
- Power Management
  - V_{MAIN}, V_{IO}, V_{pp}: 1.8 V
  - V_{PA}: 3.0 V to 3.6V
- Clock Sources
  - 40-MHz XTAL fast clock
  - Internal LFOSC or external 32.768-kHz slow clock
- Small Package Size
  - Easy to design with 40-pin, 5-mm x 5-mm quad flat noleaded (QFN) package, 0.4-mm pitch

2 Applications

- Grid Infrastructure
  - Electricity Meter
  - String Inverter
  - Micro Inverter
  - Energy Storage Power Conversion System (PCS)
  - EV Charging Infrastructure
- Building and Home Automation
  - HVAC Controller
  - HVAC Gateway
  - Thermostat
  - Building Security Gateway
  - Garage door system
  - IP network camera/ Video doorbell
  - Wireless security camera
- Appliances
  - Refrigerator & freezer
  - Oven
  - Washer & dryer
  - Residential water heater & heating system
  - Air purifier & humidifier
  - Coffee machine
  - Air conditioner indoor unit
  - Vacuum robot
  - Robotic lawn mower
- Medical
  - Infusion pump
  - Electronic hospital bed & bed control
  - Multiparameter patient monitor
  - Blood pressure monitor
  - CPAP machine
  - Telehealth systems
  - Ultrasound scanner
  - Ultrasound smart probe
  - Electric toothbrush
- Retail Automation and Payment
- Printers

ADVANCE INFORMATION

3 Description

The SimpleLink™ Wi-Fi CC33xx family of devices is where affordability meets reliability, enabling engineers to connect more applications with confidence. CC33xx are single-chip Wi-Fi 6 and Bluetooth Low Energy 5.3 devices. The CC3300 and CC3301 are the first devices in this pin to pin compatible family.

- CC3300: A 2.4GHz Wi-Fi 6 companion IC.
- CC3301: A 2.4GHz Wi-Fi 6 and Bluetooth low energy 5.3 companion IC.

The CC330x offers the latest standards from Wi-Fi and BLE while maintaining compatibility with Wi-Fi 4 (802.11 b/g/n) and Wi-Fi 5 (802.11ac). These CC330x are the 10th-generation connectivity combo chip from Texas Instruments. As such, the CC330x is based upon proven technology. These devices are ideal for use in cost-sensitive embedded applications with a Linux or RTOS host running TCP/IP, CC330x brings the efficiency of Wi-Fi 6 to embedded device applications for the internet of things (IoT), with a small PCB footprint and highly optimized bill of materials.

Device Information

PART NUMBER	Wi-Fi 2.4-GHz SISO	Bluetooth Low Energy
CC3300ENJARSBR	✓	
CC3301ENJARSBR	✓	✓

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4 System Diagram

Figure 4-1 shows a basic system diagram for the CC3301.

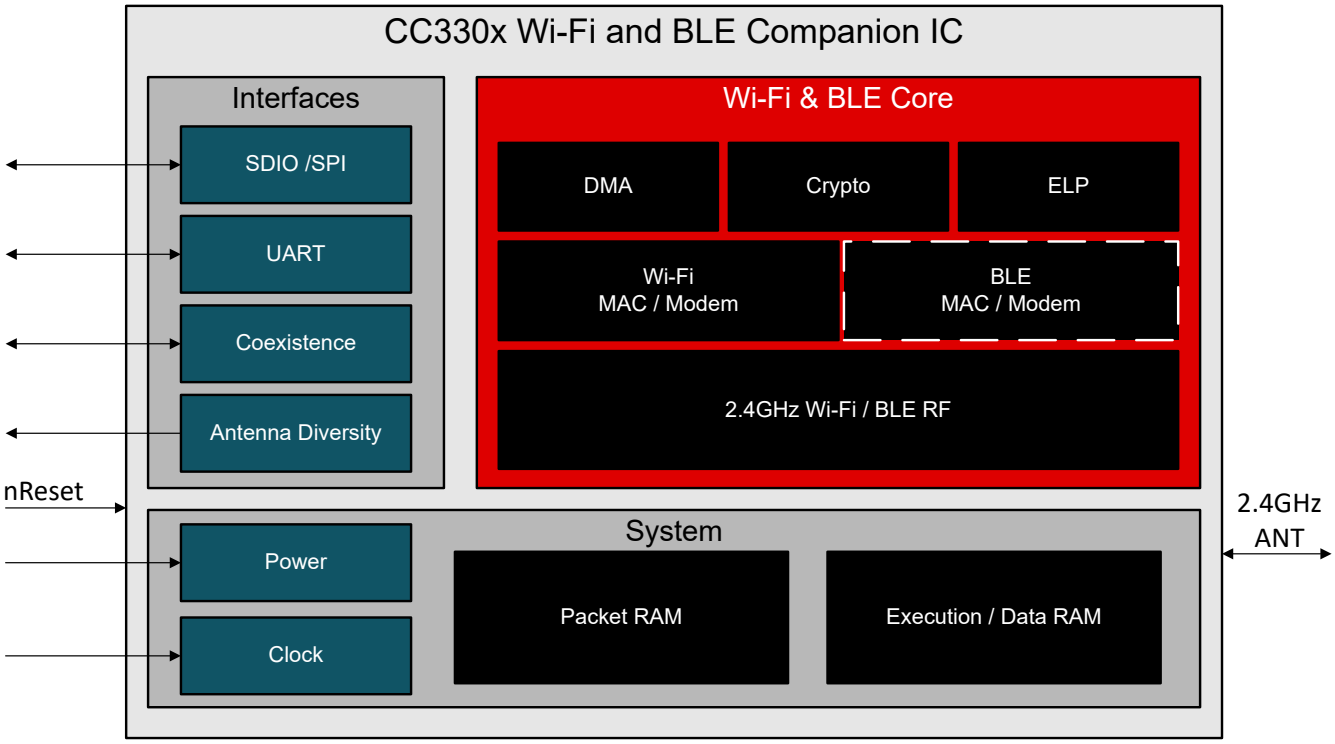

Figure 4-1. CC3301 high-Level System Diagram

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from April 24, 2023 to September 14, 2023 (from Revision A (April 2023) to Revision B (September 2023))	Page
• Updated specifications and descriptions	1

6 Terminal Configuration and Functions

6.1 Pin Diagram

Figure 6-1 shows pin assignments for the 40-pin WQFN package.

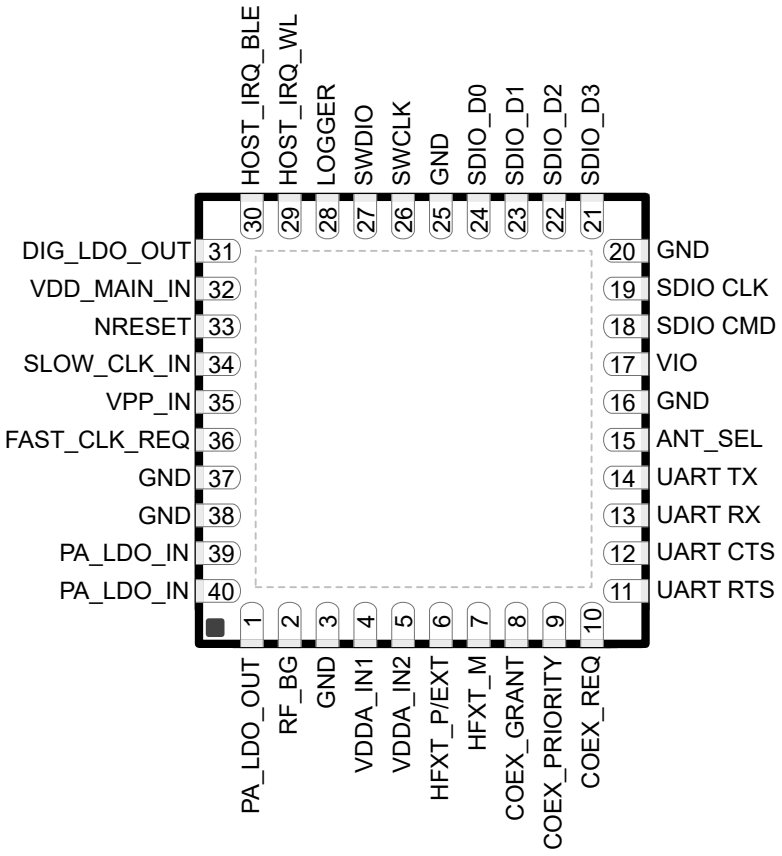

Figure 6-1. CC3301 Pin Diagram

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6.2 Pin Attributes

Table 6-1. Pin Attributes

PIN	SIGNAL NAME	TYPE	DIR (I/O)	VOLTAGE LEVEL	SHUTDOWN STATE	STATE AFTER POWER-UP	DESCRIPTION
1	PA_LDO_OUT	Analog					RF power amplifier LDO output
2	RF_BG	RF	I/O				Bluetooth Low Energy and WLAN 2.4-GHz RF port
3	VSS	GND					VSS
4	VDDA_IN1	POW					1.8 V supply for analog domain
5	VDDA_IN2	POW					1.8 V supply for analog domain
6	HFXT_P/EXT	Analog		Sine/square			XTAL_P fast clock input
7	HFXT_M	Analog					XTAL_N
8	COEX_GRANT[2]	Digital	O	V_{IO}	PD	PD	External coexistence interface - grant
9	COEX_PRIORITY[2]	Digital	I	V_{IO}	PU	PU	External coexistence interface - priority
10	COEX_REQ[2]	Digital	I	V_{IO}	PU	PU	External coexistence interface - request
11	UART RTS	Digital	O	V_{IO}	PU	PU	Device RTS signal - flow control for BLE HCI
12	UART CTS	Digital	I	V_{IO}	PU	PU	Device CTS signal - flow control for BLE HCI
13	UART RX	Digital	I	V_{IO}	PU	PU	UART RX for BLE HCI
14	UART TX	Digital	O	V_{IO}	PU	PU	UART TX for BLE HCI
15	ANT_SEL[2]	Digital	O	V_{IO}	PD	PD	Antenna select control line
16	VSS	GND					VSS
17	VIO	POW					1.8 V IO supply
18	SDIO CMD	Digital	I/O	V_{IO}	HiZ	HiZ	SDIO command or SPI PICO
19	SDIO CLK	Digital	I	V_{IO}	HiZ	HiZ	SDIO clock or SPI clock
20	VSS	GND					VSS
21	SDIO D3	Digital	I/O	V_{IO}	HiZ	PU	SDIO data D3 or SPI CS
22	SDIO D2	Digital	I/O	V_{IO}	HiZ	HiZ	SDIO data D2
23	SDIO D1	Digital	I/O	V_{IO}	HiZ	HiZ	SDIO data D1
24	SDIO D0	Digital	I/O	V_{IO}	HiZ	HiZ	SDIO data D0 or SPI POCI
25	VSS	GND					VSS
26	SWCLK	Digital	I	V_{IO}	PD	PD	Serial wire debug clock
27	SWDIO	Digital	I/O	V_{IO}	PU	PU	Serial wire debug I/O
28	LOGGER[3]	Digital	O	V_{IO}	PU	PU	Tracer (UART TX debug logger)
29	HOST_IRQ_WL[3]	Digital	O	V_{IO}	PD	0	Interrupt request to host for WLAN
30	HOST_IRQ_BLE[3]	Output	O	V_{IO}	PD	PD	Interrupt request to host for BLE (in shared SDIO mode)

Table 6-1. Pin Attributes (continued)

PIN	SIGNAL NAME	TYPE	DIR (I/O)	VOLTAGE LEVEL	SHUTDOWN STATE	STATE AFTER POWER-UP	DESCRIPTION
31	DIG_LDO_OUT	Analog	O				Digital LDO output to decoupling capacitor
32	VDD_MAIN_IN	POW					1.8 V supply input for SRAM and digital
33	nRESET	Digital	I	V_{IO}	PD	PD	Reset line for enabling or disabling device (active low)
34	SLOW_CLK_IN	Digital	I	V_{IO}	PD	PD	32.768-kHz RTC clock input
35	VPP_IN	POW					1.8 V OTP programming input supply
36	FAST_CLK_REQ	Digital	O	V_{IO}	PD	PD	Fast clock request from the device
37	VSS	GND					VSS
38	VSS	GND					VSS
39	PA_LDO_IN	POW					3.3 V supply for PA
40	PA_LDO_IN	POW					3.3 V supply for PA

1. All digital I/O's (with the exception of SDIO signals) are Hi-Z when the device is in shutdown mode with internal PU/PD according to the "shutdown state" column.
2. See software release notes for support level.
3. LOGGER, HOST_IRQ_WL, and HOST_IRQ_BLE pins are sensed by the device during boot, see hardware integration guide.

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7 Specifications

All specifications are given at the CC3301 pins. Typical values are measured with nominal device at 25°C.

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

PARAMETER		PINS	MIN	MAX	UNIT
V_{PA}	V_{DD} PA Voltage	39,40	–0.5	4.2	V
V_{MAIN}	Main supply voltage for analog and digital - VDD_MAIN_IN, VDDA_IN1, VDDA_IN2	32, 4, 5	–0.5	1.98	V
V_{IO}	VDD IO Voltage	17	–0.5	1.98	V
	Input Voltage to all digital pins		–0.5	V_{IO} + 0.5	V
	HFXT_P Input Voltage	6	–0.5	2.1	V
T_A	Operating Ambient Temperature		–40	105	°C
T_J	Operating Junction Temperature		–40	130	°C
T_{stg}	Storage temperature		–55	155	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

Over operating free-air temperature range (unless otherwise noted)

PARAMETER		PINS	MIN	TYP	MAX	UNIT
V_{MAIN}	Main supply voltage digital and analog - VDD_MAIN_IN, VDDA_IN1, VDDA_IN2	32,4,5	1.62	1.8	1.98	V
V_{PA}	DC supply rail for PA	39,40	3	3.3	3.6	
V_{IO}	DC supply rail for input/output	17	1.62	1.8	1.98	
V_{PP}	DC supply rail for OTP memory	35		1.8		
T_A	Operating ambient temperature		–40		85/105(1)	°C
	Maximum power dissipation				2	W

(1) The CC3300 and CC3301 devices may operate at temperatures of up to 105°C. This allows the device to be used reliably in applications that may be exposed to higher ambient temperature over certain periods of the product's life. At temperatures higher than 85°C, the WLAN/BLE performance may degrade.

7.4 Electrical Characteristics

PARAMETER	DESCRIPTION	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IH}	High Level Input Voltage		0.65 x V_{IO}		V_{IO}	V
V_{IL}	Low Level Input Voltage		0		0.35 x V_{IO}	
V_{OH}	High Level Output Voltage	at 4mA	V_{IO} – 0.45		V_{IO}	
V_{OL}	Low Level Output Voltage	at 4mA	0		0.45	

7.5 Thermal Resistance Characteristics

THERMAL METRIC(1)	DESCRIPTION		UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (According to JEDEC EIA/JESD 51 document)	30.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	16.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	10	
Ψ_{JT}	Junction-to-top characterization parameter	0.1	
Ψ_{JB}	Junction-to-board characterization parameter	10	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	1.7	

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.6 WLAN Performance: 2.4-GHz Receiver Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		2412		2472	MHZ
Sensitivity: 8% PER for 11b rates, 10% PER for 11g/n/ax rates	1 Mbps DSSS		-98		dBm
	2 Mbps DSSS		-95		
	11 Mbps CCK		-90		
	6 Mbps OFDM		-93.5		
	54 Mbps OFDM		-75.8		
	HT MCS0 MM 4K		-93		
	HT MCS7 MM 4K		-73.6		
	HE MCS0 4K		-91.3		
	HE MCS0 4K ER upper 106		-93.3		
	HE MCS7 4K		-72.4		
Maximum input level (10% PER)	1 Mbps DSSS	-4			dBm
	OFDM	-20			
Adjacent Channel Rejection	1 Mbps DSSS	45			dB
	11 Mbps CCK	40			
	6 Mbps OFDM	20			
	54 Mbps OFDM	3			
	HT MCS0	20			
	HT MCS7	3			
	HE MCS0	16			
	HE MCS7	0			
RSSI Accuracy	-90 dBm to -30dBm	-3		3	dB

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7.7 WLAN Performance: 2.4-GHz Transmitter Power

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Operational Frequency Range		2412		2472	MHz
Maximum output power at V_{PA} > 3.0 V	1 Mbps DSSS		20.5		dBm
	6 Mbps OFDM		20.5		
	54 Mbps OFDM		17		
	HT MCS0 MM		20		
	HT MCS7 MM		16.5		
	HE MCS0		20		
	HE MCS7		16		

7.8 BLE Performance: Receiver Characteristics

Packet length = 255 bytes, f_{RF}=2440 MHz, PER = 30.2%, unless otherwise noted.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
BLE 125Kbps (LE Coded) Receiver Characteristics					
Receiver sensitivity			TBD		dBm
Receiver saturation			TBD		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency.	TBD		TBD	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate.	TBD		TBD	ppm
Co-channel rejection(1)	Wanted signal at -79 dBm, modulated interferer in channel		TBD		dB
Selectivity, ±1 MHz(1)	Wanted signal at -79 dBm, modulated interferer at ±1 MHz.		TBD		dB
Selectivity, ±2 MHz(1)	Wanted signal at -79 dBm, modulated interferer at ±2 MHz.		TBD		dB
Selectivity, ±3 MHz(1)	Wanted signal at -79 dBm, modulated interferer at ±3 MHz.		TBD		dB
Selectivity, ±4 MHz(1)	Wanted signal at -79 dBm, modulated interferer at ±4 MHz.		TBD		dB
RSSI Dynamic Range			TBD		dB
RSSI Accuracy	Starting from the sensitivity limit across the given dynamic range.		TBD		dB
BLE 500Kbps (LE Coded) Receiver Characteristics					
Receiver sensitivity			TBD		dBm
Receiver saturation			TBD		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency.	TBD		TBD	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate.	TBD		TBD	ppm
Co-channel rejection(1)	Wanted signal at -72 dBm, modulated interferer in channel.		TBD		dB
Selectivity, ±1 MHz(1)	Wanted signal at -72 dBm, modulated interferer at ±1 MHz.		TBD		dB
Selectivity, ±2 MHz(1)	Wanted signal at -72 dBm, modulated interferer at ±2 MHz.		TBD		dB
Selectivity, ±3 MHz(1)	Wanted signal at -72 dBm, modulated interferer at ±3 MHz.		TBD		dB

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Packet length = 255 bytes, f_{RF}=2440 MHz, PER = 30.2%, unless otherwise noted.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Selectivity, ±4 MHz(1)	Wanted signal at -72 dBm, modulated interferer at ±4 MHz.		TBD		dB
RSSI Range			TBD		dB
RSSI Accuracy			TBD		dB
BLE 1Mbps (LE 1M) Receiver Characteristics					
Receiver sensitivity	37-byte packets		–98.35		dBm
Receiver sensitivity	255 byte-packets		–97.3		dBm
Receiver saturation			0		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency.	TBD		TBD	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate	TBD		TBD	ppm
Co-channel rejection(1)	Wanted signal at -67 dBm, modulated interferer in channel		17		dB
Selectivity, ±1 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±1 MHz		6 / 4(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±2 MHz.		-35 / -30(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±3 MHz		-36 / -32(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±4 MHz		-32		dB
Out-of-band blocking	30 MHz to 2000 MHz, Wanted signal at -67 dBm		–23		dBm
Out-of-band blocking	2003 MHz to 2399 MHz, Wanted signal at -67 dBm		–30		dBm
Out-of-band blocking	2484 MHz to 2997 MHz, Wanted signal at -67 dBm		–30		dBm
Out-of-band blocking	3000 MHz to 6 GHz, Wanted signal at -67 dBm		–21		dBm
Intermodulation	Wanted signal at 2402 MHz, -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–40		dBm
Spurious emissions, 30 to 1000 MHz	Measurement in a 50-Ω single-ended load			–65	dBm
Spurious emissions, 1 to 12.75 GHz	Measurement in a 50 Ω single-ended load			–60	dBm
RSSI dynamic range			70		dB
RSSI accuracy			±4		dB
BLE 2Mbps (LE 2M) Receiver Characteristics					
Receiver sensitivity			–94.9		dBm
Receiver saturation			0		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency.	TBD		TBD	ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate	TBD		TBD	ppm
Co-channel rejection(1)	Wanted signal at -67 dBm, modulated interferer in channel		17		dB
Selectivity, ±2 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±2 MHz.		10 / 12(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±4 MHz		-32 / -30(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±6 MHz		-33 / -32(2)		dB

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Packet length = 255 bytes, f_{RF}=2440 MHz, PER = 30.2%, unless otherwise noted.

PARAMETER	TEST CONDITION	MIN	TYP	MAX	UNIT
Alternate channel rejection, ±8 MHz(1)	Wanted signal at -67 dBm, modulated interferer at ±8 MHz		-33 / -32(2)		dB
Out-of-band blocking	30 MHz to 2000 MHz, Wanted signal at -67 dBm		–23		dBm
Out-of-band blocking	2003 MHz to 2399 MHz, Wanted signal at -67 dBm		–32		dBm
Out-of-band blocking	2484 MHz to 2997 MHz, Wanted signal at -67 dBm		–32		dBm
Out-of-band blocking	3000 MHz to 6 GHz, Wanted signal at -67 dBm		–21		dBm
Intermodulation	Wanted signal at 2402 MHz, -64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–44		dBm
RSSI dynamic range			64		dB
RSSI Accuracy			±4		dB

(1) Numbers given as C/I dB
(2) X / Y, where X is +N MHz and Y is –N MHz

7.9 BLE Performance - Transmitter Characteristics

The CC330X devices support BLE TX setting 0,5,10, or 20 dBm

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Output Power, highest setting			20		dBm

7.10 Current Consumption - WLAN Static Modes

PARAMETER	TEST CONDITION		SUPPLY	TYP	MAX	UNIT
Continuous TX	1 DSSS	TX power = 20.5 dBm	V_{Main}	95	TBD	mA
			V_{PA}	250	TBD	
	6 OFDM	TX power = 20.5 dBm	V_{Main}	100	TBD	
			V_{PA}	250	TBD	
	54 OFDM	TX power = 17 dBm	V_{Main}	130	TBD	
			V_{PA}	160	TBD	
	HT MCS0	TX power = 20 dBm	V_{Main}	130	TBD	
			V_{PA}	235	TBD	
	HT MCS7	TX power = 16.5 dBm	V_{Main}	130	TBD	
			V_{PA}	152	TBD	
	HE MCS0	TX power = 20 dBm	V_{Main}	100	TBD	
			V_{PA}	205	TBD	
	HE MCS7	TX power = 16 dBm	V_{Main}	130	TBD	
			V_{PA}	140	TBD	
Continuous RX			V_{Main}	60.5	TBD	
			V_{PA}	0		
Continuous Listen (for beacon)			V_{Main}	55.5	TBD	
			V_{PA}	0		

7.11 Current Consumption - WLAN Use Cases

MODE	DESCRIPTION	MIN	TYP	MAX	UNIT
DTIM=1	WLAN beacon reception every DTIM=1 (~102ms)		TBD		µA
DTIM=3	WLAN beacon reception every DTIM=3 (~306ms)		TBD		
DTIM=5	WLAN beacon reception every DTIM=5 (~510ms)		TBD		

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7.12 Current Consumption - BLE Static Modes

PARAMETER	TEST CONDITION	SUPPLY	TYP	MAX	UNIT
TX, Max Duty Cycle	TX power = 0 dBm	V_{Main}	90	TBD	mA
		V_{PA}	30	TBD	
	TX power = 10 dBm	V_{Main}	TBD	TBD	
		V_{PA}	TBD	TBD	
	TX power = 20 dBm	V_{Main}	90	TBD	
		V_{PA}	260	TBD	
RX		V_{Main}	TBD	TBD	
		V_{PA}	TBD		

7.13 Current Consumption - Device States

Nominal device at room temp

MODE	DESCRIPTION	SUPPLY	TYP	UNIT
Shutdown	External supplies are available, device held in reset (nReset is low)	V_{Main}	5	uA
		V_{PA}	6	
Sleep	Low power mode - RAM in retention	V_{Main}	175	
		V_{PA}	6	

7.14 Timing and Switching Characteristics

7.14.1 Power Supply Sequencing

For proper operation of the CC330x device, perform the recommended power-up sequencing as follows:

1. All supplies (VDD_MAIN, VDDA, VIO, VPA) must be available before Reset is released.
2. For an external slow clock, ensure that the clock is stable before Reset is deasserted (high).
3. The Reset pin should be held low for 10 us after stabilization of the external power supplies.

7.14.2 Clocking Specifications

The CC330x device uses two clocks for operation:

- A fast clock running at 40 MHz for WLAN/BLE functions
- A slow clock running at 32.768 kHz for low power modes

The slow clock can be generated internally or externally. The fast clock must be generated externally.

7.14.2.1 Slow Clock Generated Internally

In order to minimize external components, the slow clock can be generated by an internal oscillator. However, this clock is less acurrate and consumes more power than sourcing the slow clock externally. For this scenario the Slow_CLK_IN pin should be left not connected.

7.14.2.2 Slow Clock Using an External Oscillator

For optimal power consumption, the slow clock can be generated externally by an oscillator or sourced from elsewhere in the system. The external source must meet the requirements listed below. This clock should be fed into the CC330x pin Slow_CLK_IN and should be stable before nReset is deasserted and device is enabled.

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7.14.2.2.1 External Slow Clock Requirements

PARAMETER		Description	MIN	TYP	MAX	UNIT
	Input slow clock frequency	Square wave		32768		Hz
	Frequency accuracy	Inital + temperature + aging			±250	ppm
	Input Duty cycle		30	50	70	%
T_r/T_f	Rise and fall time	10% to 90% (rise) and 90% to 10% (fall) of digital signal level			100	ns
V_{IL}	Input low level		0		0.35 x V_{IO}	V
V_{IH}	Input high level		0.65 x V_{IO}		1.95	V
	Input impedence		1			MΩ
	Input capacitance				5	pF

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7.14.2.3 Fast Clock Using an External Crystal (XTAL)

The CC330x device incorporates an internal crystal oscillator to support a crystal-based fast clock (XTAL). The crystal is fed directly between HFXT_P and HFXT_M pins with suitable loading capacitors, and must meet the requirements below.

7.14.2.3.1 External Fast Clock XTAL Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supported frequencies			40		MHz
Frequency accuracy	Initial + temperature + aging			+/- 25	ppm
Load Capacitance, C_L (1)		5		13	pF
Equivalent series resistance, ESR				30	Ω
Drive level			100		uW

(1) Load capacitance, C_L= [C1*C2] / [C1 + C2] + C_P, where C1, C2 are the capacitors connected on HFXT_P and HFXT_M, respectively, and C_P is the parasitic capacitance (typically 1 to 2 pF). For example, for C1 = C2 = 6.2pF and C_P = 2pF, then C_L = 5pF.

7.15 Interface Timing Characteristics

7.15.1 SDIO Timing Specifications

SDIO is the main host interface for WLAN, and it supports a maximum clock rate of 52 MHz. The CC330x device also supports shared SDIO interface for both BLE and WLAN.

7.15.1.1 SDIO Timing Diagram - Default Speed

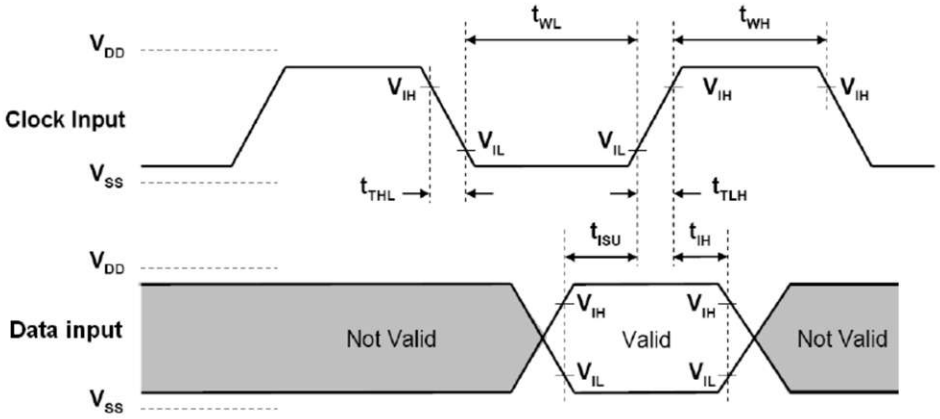


Figure 7-1. SDIO Default Input Timing

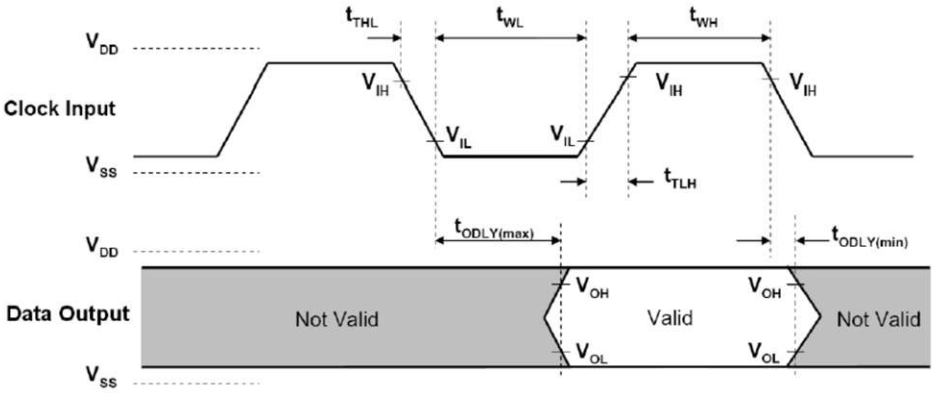


Figure 7-2. SDIO Default Output Timing

7.15.1.2 SDIO Timing Parameters - Default Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		26	MHz
t_{High}	High Period	10		ns
t_{Low}	Low Period	10		
t_{TLH}	Rise time, CLK		10	
t_{THL}	Fall time, CLK		10	
t_{ISU}	Setup time, input valid before CLK ↑	5		
t_{IH}	Hold time, input valid after CLK ↑	5		
t_{ODLY}	Delay time, CLK ↓ to output valid	2.5	14	
C_L	Capacitive load on outputs		40	pF

ADVANCE INFORMATION

7.15.1.3 SDIO Timing Diagram - High Speed

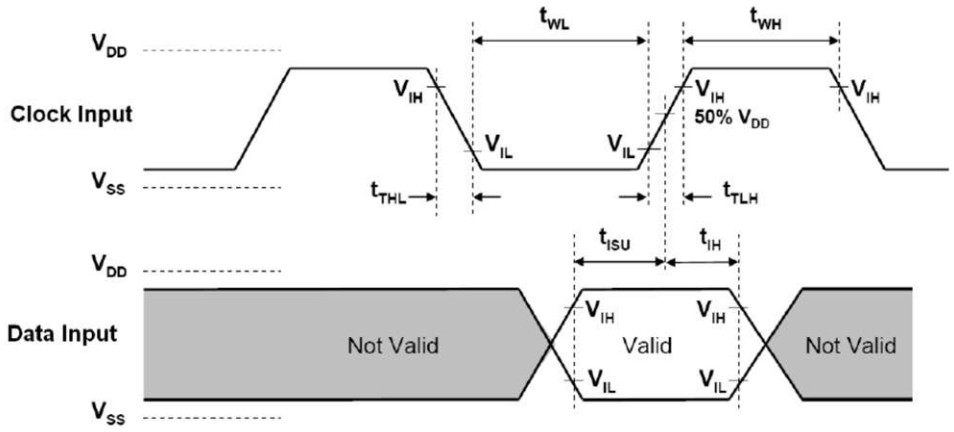


Figure 7-3. SDIO HS Input Timing

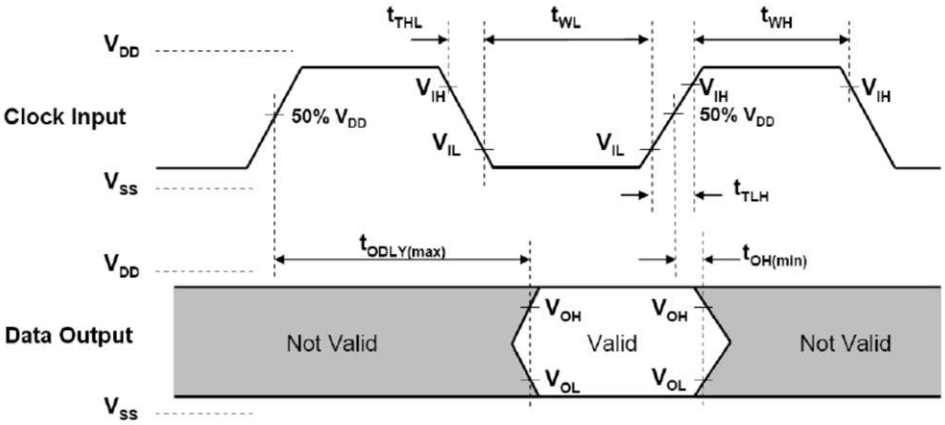


Figure 7-4. SDIO HS Output Timing

7.15.1.4 SDIO Timing Parameters - High Speed

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		52	MHz
t_{High}	High Period	7		ns
t_{Low}	Low Period	7		
t_{TLH}	Rise time, CLK		3	
t_{THL}	Fall time, CLK		3	
t_{ISU}	Setup time, input valid before CLK ↑	6		
t_{IH}	Hold time, input valid after CLK ↑	2		
t_{ODLY}	Delay time, CLK ↓ to output valid	2.5	14	
C_L	Capacitive load on outputs		40	pF

7.15.2 SPI Timing Specifications

SPI is another host interface for WLAN. The CC330x device also supports shared SPI interface for both BLE and WLAN.

7.15.2.1 SPI Timing Diagram

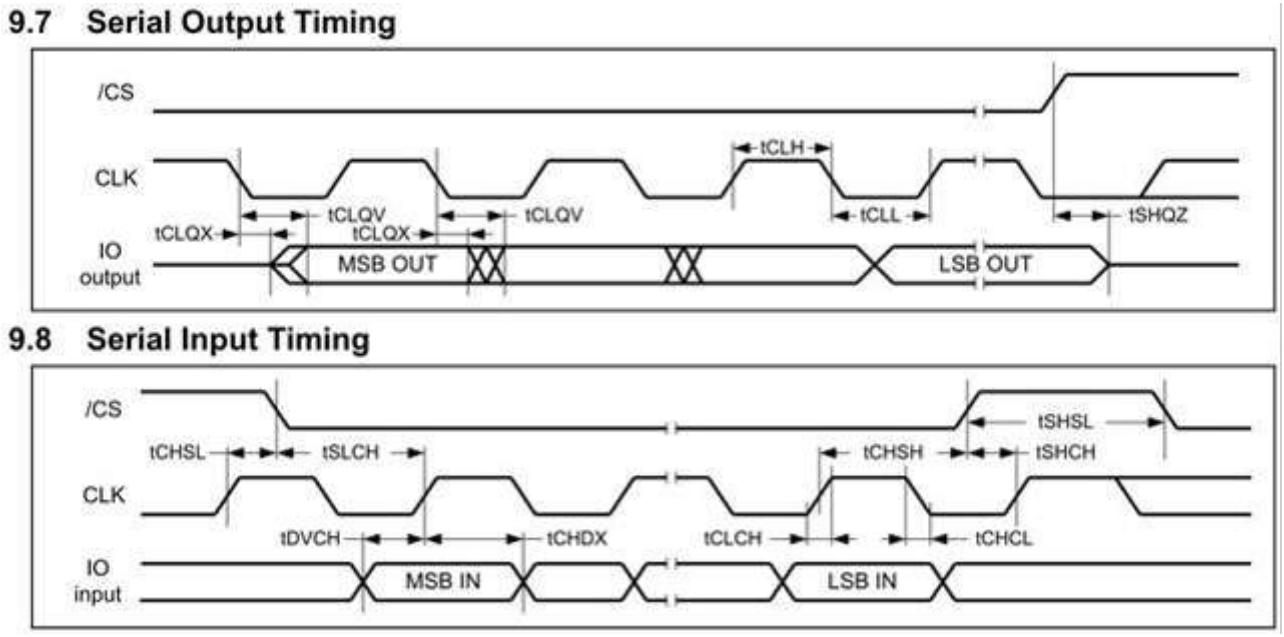


Figure 7-5. SPI Timing

7.15.2.2 SPI Timing Parameters

PARAMETER	DESCRIPTION	MIN	MAX	UNIT
f_{clock}	Clock frequency, CLK		26	MHz
t_{High}	High Period	10		ns
t_{Low}	Low Period	10		
t_{TLH}	Rise time, CLK		3	
t_{THL}	Fall time, CLK		3	
t_{CSsu}	CS Setup time, CS valid before CLK ↑	3		
t_{ISU}	PICO, input valid before CLK ↑	3		
t_{IH}	PICO Hold time, input valid after CLK ↑	3		
t_{Dr}, t_{Df} - Active	Delay time, CLK ↑/↓ to output valid	2.5	10	
t_{Dr}, t_{Df} - Sleep	Delay time, CLK ↑/↓ to output valid		12	
C_L	Capacitive load on outputs		40	pF

ADVANCE INFORMATION

7.15.3 UART 4-Wire Interface

UART is the main host interface for BLE, which supports host controller interface (HCI) transport layer.

7.15.3.1 UART Timing Parameters

PARAMETER	CONDITION	MIN	TYP	MAX	UNIT
Baud rate		37.5		4364	kbps
Baud rate accuracy per byte	Receive/Transmit	-2.5		+1.5	%
Baud rate accuracy per bit	Receive/Transmit	-12.5		+12.5	%
CTS low to TX_DATA on		0	2		ms
CTS high to TX_DATA off	Hardware flow control			1	Byte
CTS high pulse width		1			bit
RTS low to RX_DATA on		0	2		ms
RTS high to RX_DATA off	Interupt set to 1/4 FIFO			16	Byte

8 Applications, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

Figure 8-1 shows the reference schematic for the CC3301 using an optimized bill of materials, listed in Table 8-1.

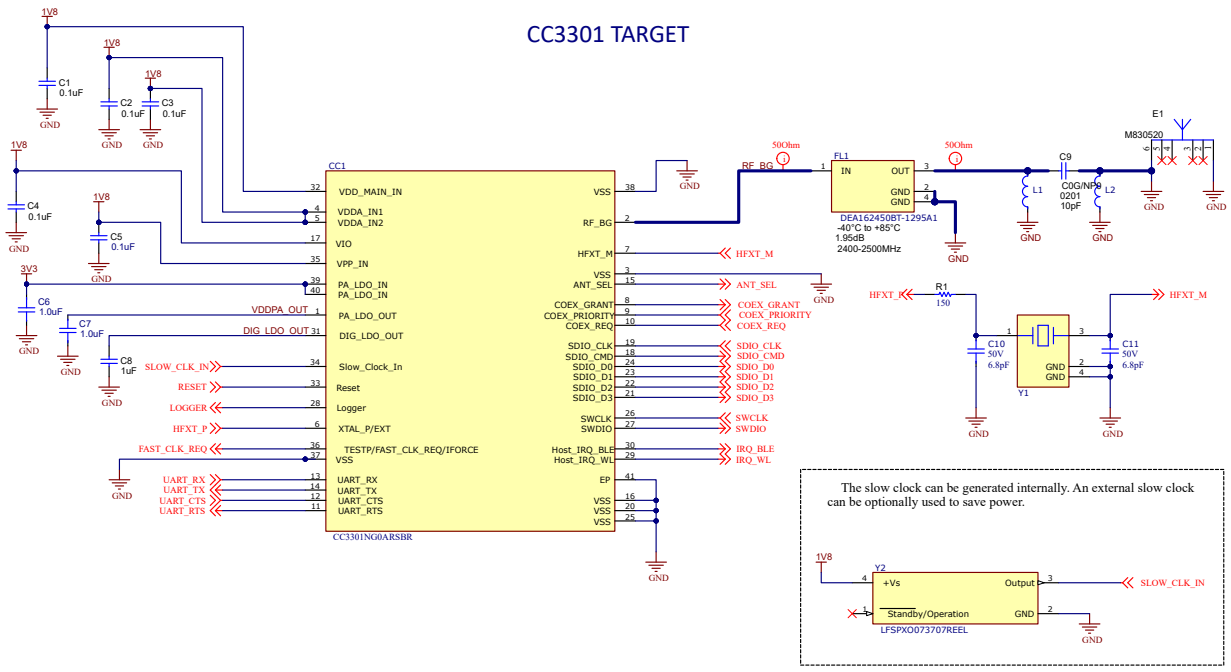


Figure 8-1. CC3301 Reference Schematic

Table 8-1. Bill of Materials

ITEM	DESIGNATOR OR REFERENCE	QUANTITY	VALUE	PART NUMBER	MANUFACTURER	DESCRIPTION	PACKAGE REFERENCE
1	C_1, C_2, C_3, C_4, C_5	5	0.1 µF	GRM033C71A104KE14D	Murata	CAP, CERM, 0.1 uF, 10 V,+/- 10%, X7S, 0201 Matching component: CAP, CERM, 10 pF, 50 V, +/- 5%, C0G/NP0, 0201	0201
2	C_6, C_7	2	1 µF	GRM033D70J105ME01D	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 1.0uF, X7T, +22%/-33%, 20%, 6.3V	0201
3	C_8	1	1 µF	GRM155R70J105MA12D	Murata	CAP, CERM, 1 uF, 6.3 V, +/- 20%, X7R, 0402	0402
4	C_9	1	10 pF	GJM0335C1E100JB01D	Murata	CAP, CERM, 10 pF, 25 V, +/- 5%, C0G/NP0, 0201	0201
5	C_{10}, C_{11}	2	6.8 pF	GJM0335C1H6R8BB01	Murata	Chip Multilayer Ceramic Capacitors for General Purpose, 0201, 6.8pF, C0G, 30ppm/°C, 0.25pF, 50V	0201
6	R1	1	150 Ω	RC0201FR-7D150RL	YAGEO	RES, 150, 1%, 0.05 W, 0201	0201
6	L_1, L_2	2	3.9 nH	LQP03HQ3N9B02D	Murata	Matching component: 3.9 nH Unshielded Thick Film Inductor 500mA 170mOhm Max 0201	0201
7	CC1	1		CC3301NG0ARSBR	Texas Instruments	CC3301NG0ARSBR-2.4GHz Wi-Fi 6 and Bluetooth Low Energy 5.2 Combo Transceiver	WQFN40
7	Y1	1		LFSPXO073707REEL	IQD Frequency Products	Optional: 32.768 kHz XO (Standard) CMOS Oscillator 1.8V Enable/ Disable 4-SMD, No Lead	SMT4_2MM0_1MM6
8	Y2	1		TZ3877AAAO44	Tai-Saw Technology	Crystal Unit SMD 2.0x1.6 40.0MHz	SMT4_2MM05_1MM65
9	FL1	1		DEA162450BT-1295A1	TDK	2.45GHz Center Frequency Band Pass RF Filter, 100MHz Bandwidth, 1.8dB 0603, 3 PC Pad	SMT_FILTER_1MM60_0MM80
10	E1	1		M830520	Ethertronics	WLAN ANTENNA 802.11, SMD	

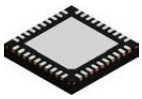
ADVANCE INFORMATION

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

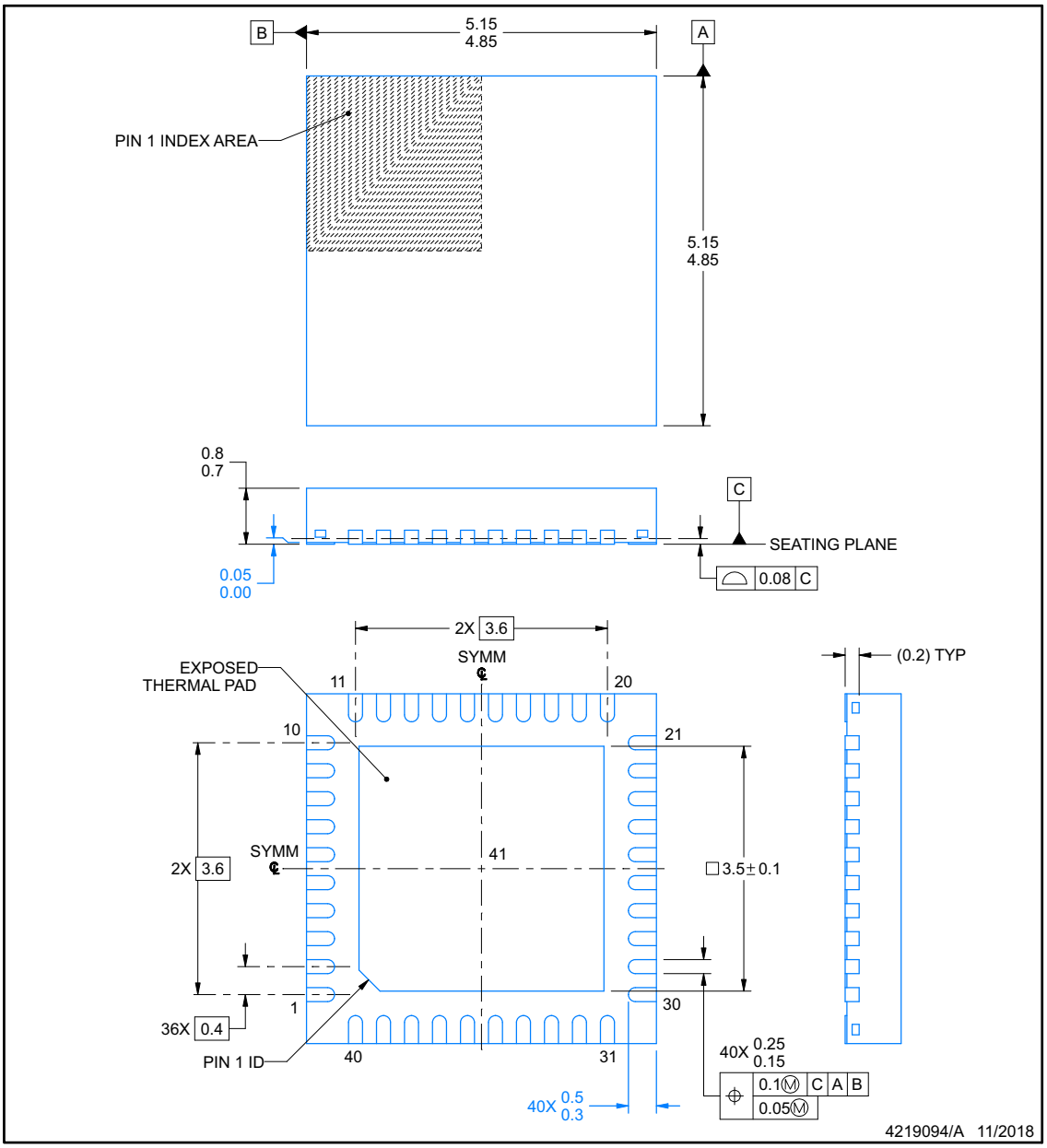
PACKAGE OUTLINE

RSB0040B



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XCC3300ENJARSBR	ACTIVE	WQFN	RSB	40	3000	TBD	Call TI	Call TI	-40 to 105		Samples
XCC3301ENJARSBR	ACTIVE	WQFN	RSB	40	3000	TBD	Call TI	Call TI	-40 to 105		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

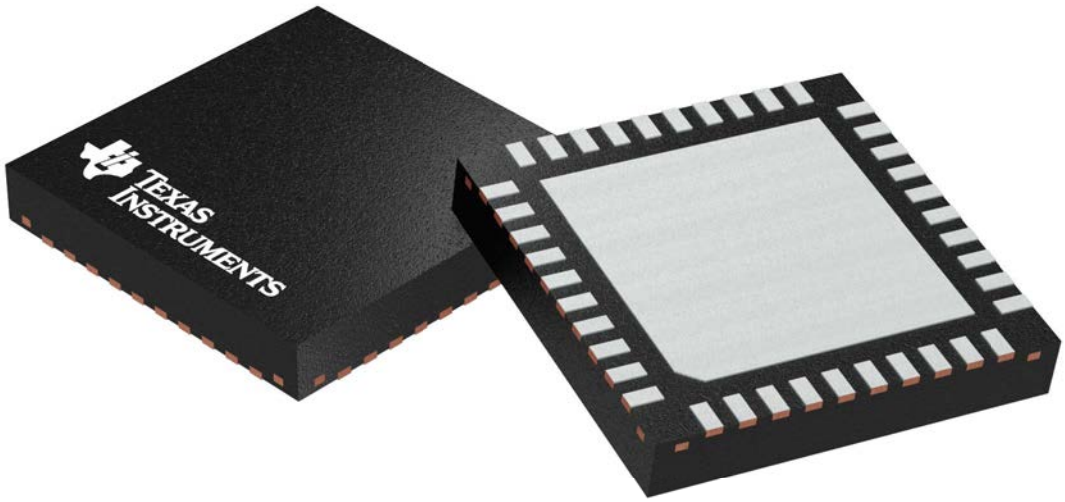
GENERIC PACKAGE VIEW

RSB 40

WQFN - 0.8 mm max height

5 x 5 mm, 0.4 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

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