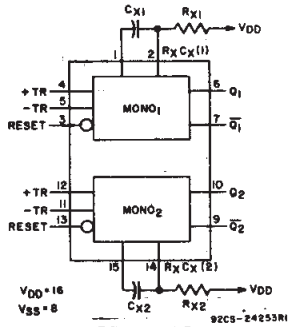
TEXAS INSTRUMENTS
Data sheet acquired from Harris Semiconductor
SCHS093C − Revised October 2003

CD14538B Types

CMOS Dual Precision Monostable Multivibrator

High-Voltage Types (20-Volt Rating)

Features:
- *Retriggerable/resettable capability*
- *Trigger and reset propagation delays independent of R_x, C_x*
- *Triggering from leading or trailing edge*
- *Q and $\overline{Q}$ buffered outputs available*
- *Separate resets*
- *Replaces CD4538B Type*



CD14538B
FUNCTIONAL DIAGRAM

■ CD14538B dual precision monostable multivibrator provides stable retriggerable/resettable one-shot operation for any fixed-voltage timing application.

An external resistor (R_X) and an external capacitor (C_X) control the timing and accuracy for the circuit. Adjustment of R_X and C_X provides a wide range of output pulse widths from the Q and $\overline{Q}$ terminals. The time delay from trigger input to output transition (trigger propagation delay) and the time delay from reset input to output transition (reset propagation delay) are independent of R_X and C_X. Precision control of output pulse widths is achieved through linear CMOS techniques.

Leading-edge-triggering (+TR) and trailing-edge-triggering (−TR) inputs are provided for triggering from either edge of an input pulse. An unused +TR input should be tied to V_{SS}. An unused −TR input should be tied to V_{DD}. A RESET (on low level) is provided for immediate termination of the output pulse or to prevent output pulses when power is turned on. An unused RESET input should be tied to V_{DD}. However, if an entire section of the CD14538B is not used, its inputs must be tied to either V_{DD} or V_{SS}. See Table I.

In normal operation the circuit retriggers (extends the output pulse one period) on the application of each new trigger pulse. For operation in the non-retriggerable mode, $\overline{Q}$ is connected to −TR when leading-edge triggering (+TR) is used or Q is connected to +TR when trailing-edge triggering (−TR) is used. The time period (T) for this multivibrator can be calculated by: $T = R_XC_X$.

The minimum value of external resistance, R_X, is 4 KΩ. The minimum and maximum values of external capacitance, C_X, are 0 pF and 100 μF, respectively.

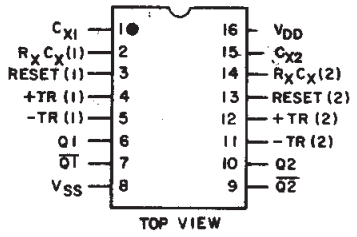
The CD14538B is interchangeable with type MC14538 and is similar to and pin-compatible with the CD4098B* and CD4538B. It can replace the CD4538B which type is not recommended for new designs.

The CD14538B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

*T = 0.5 R_XC_X for $C_X \geq 1000$ pF #T = R_XC_X; $C_X$min = 5000 pF

- *Wide range of output-pulse widths*
- *Schmitt-trigger input allows unlimited rise and fall times on +TR and −TR inputs*
- *100% tested for maximum quiescent current at 20 V*
- *Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25° C*
- *Noise margin (full package-temperature range):*
  - *1 V at $V_{DD} = 5$ V*
  - *2 V at $V_{DD} = 10$ V*
  - *2.5 V at $V_{DD} = 15$ V*
- *5-V, 10-V, and 15-V parametric ratings*
- *Standardized, symmetrical output characteristics*
- *Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices."*

Applications:
- *Pulse delay and timing*
- *Pulse shaping*



TERMINALS 1, 8, 15 ARE ELECTRICALLY CONNECTED INTERNALLY

92CS-24848RI

Terminal Assignment

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MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE RANGE, (V_{DD})
Voltages referenced to V_{SS} Terminal) ..... -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to V_{DD} +0.5V
DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
POWER DISSIPATION PER PACKAGE (P_D):
For T_A = -55°C to +100°C 500mW
For T_A = +100°C to +125°C ..... Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) 100mW
OPERATING-TEMPERATURE RANGE (T_A) ..... -55°C to +125°C
STORAGE TEMPERATURE RANGE (T_{stg}) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

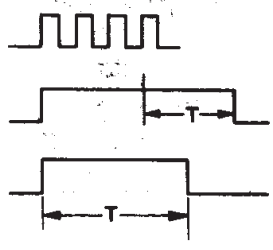
RECOMMENDED OPERATING CONDITIONS
For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC		V_{DD} (V)	LIMITS		UNITS
			Min.	Max.	
Supply-Voltage Range (For T_A=Full Package-Temperature Range)		—	3	18	V
Input Pulse Width +TR, -TR, or RESET	t_{WH}, t_{WL}	5 10 15	140 80 60	— — —	ns

TABLE I
CD4538B FUNCTIONAL TERMINAL CONNECTIONS

FUNCTIION	V_{DD} TO TERM. NO.		V_{SS} TO TERM. NO.		INPUT PULSE TO TERM. NO.		OTHER CONNECTIONS	
	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$	$MONO_1$	$MONO_2$
Leading-Edge Trigger/ Retriggerable	3, 5	11, 13			4	12		
Leading-Edge Trigger/ Non-Retriggerable	3	13			4	12	5-7	11-9
Trailing-Edge Trigger/ Retriggerable	3	13	4	12	5	11		
Trailing-Edge Trigger/ Non-Retriggerable	3	13			5	11	4-6	12-10

NOTES:
1. A RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS AN OUTPUT PULSE WIDTH WHICH IS EXTENDED ONE FULL TIME PERIOD (T) AFTER APPLICATION OF THE LAST TRIGGER PULSE.
2. A NON—RETRIGGERABLE ONE-SHOT MULTIVIBRATOR HAS A TIME PERIOD (T) REFERENCED FROM THE APPLICATION OF THE FIRST TRIGGER PULSE.



STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V_O (V)	V_{IN} (V)	V_{DD} (V)	-55	-40	+85	+125	Min.	+25 Typ.	Max.	
Quiescent Device Current, I_{DD} Max.	—	0,5	5	5	5	150	150	—	0.04	5	μA
	—	0,10	10	10	10	300	300	—	0.04	10	
	—	0,15	15	20	20	600	600	—	0.04	20	
	—	0,20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I_{OL} Min.	0.4	0,5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0,10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0,15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I_{OH} Min.	4.6	0,5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	
	2.5	0,5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0,10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0,15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V_{OL} Max.	—	0,5	5	0.05				—	0	0.05	V
	—	0,10	10	0.05				—	0	0.05	
	—	0,15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V_{OH} Min.	—	0,5	5	4.95				4.95	5	—	
	—	0,10	10	9.95				9.95	10	—	
	—	0,15	15	14.95				14.95	15	—	
Input Low Voltage, V_{IL} Max.	0.5,4.5	—	5	1.5				—	—	1.5	V
	1,9	—	10	3				—	—	3	
	1.5,13.5	—	15	4				—	—	4	
Input High Voltage, V_{IH} Min.	0.5,4.5	—	5	3.5				3.5	—	—	
	1,9	—	10	7				7	—	—	
	1.5,13.5	—	15	11				11	—	—	
Input Current, I_{IN} Max.	—	0,18	18	±0.1	±0.1	±1	±1	—	$±10^{-5}$	±0.1	μA

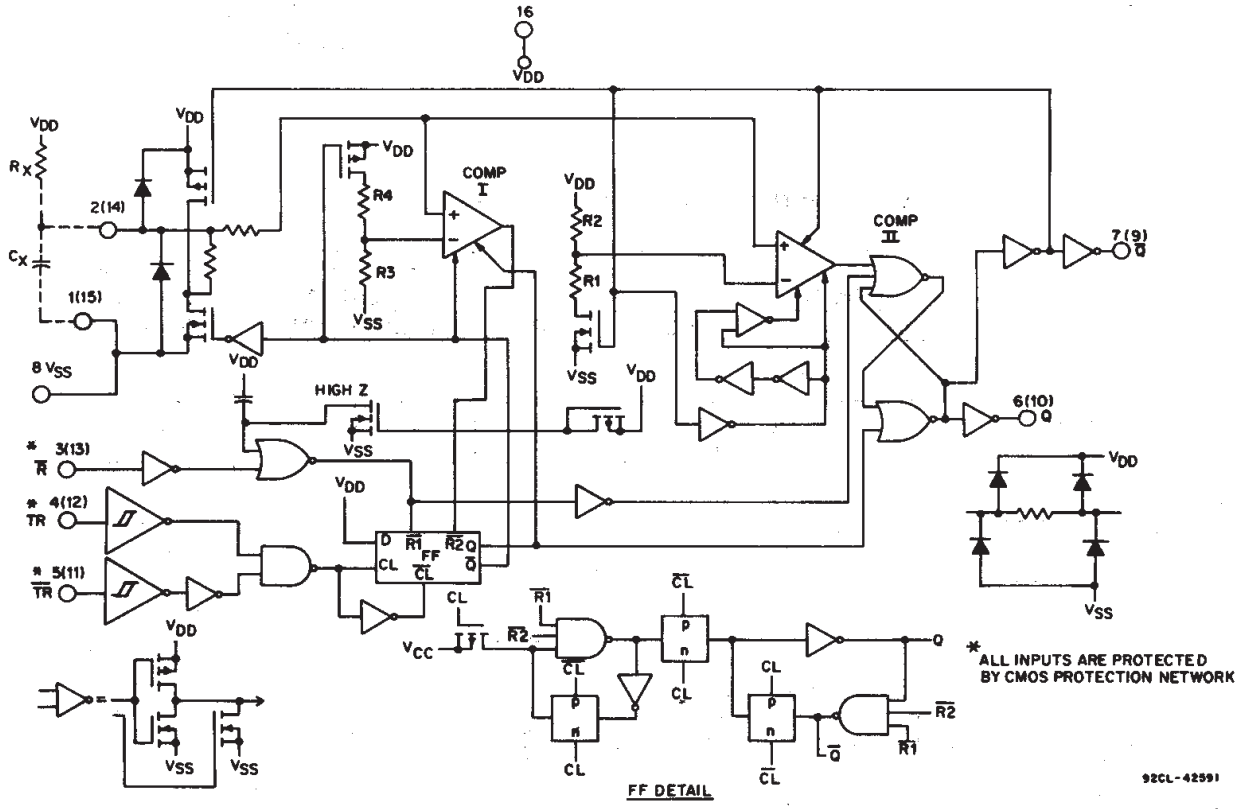


Fig. 1 - Logic diagram (½ of device shown).

DYNAMIC ELECTRICAL CHARACTERISTICS, At T_A=25° C; Input t_r,t_f=20 ns, C_L=50 pF

CHARACTERISTIC		TEST CONDITIONS V_{DD} (V)	LIMITS Min.	LIMITS Typ.	LIMITS Max.	UNITS
Transition Time	t_{TLH}, t_{THL}	5	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time: +TR or -TR to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	5	—	300	600	
		10	—	150	300	
		15	—	100	220	
Reset to Q or $\overline{Q}$		5	—	250	500	
		10	—	125	250	
		15	—	95	190	
Minimum Input Pulse Width: +TR, -TR or Reset	t_{WH}, t_{WL}	5	—	80	140	
		10	—	40	80	
		15	—	30	60	
Output Pulse Width - Q or $\overline{Q}$: C_X = 0.002 μF, R_X = 100 KΩ	T	5	198	210	230	μs
		10	200	212	232	
		15	202	214	234	
C_X=0.1 μF, R_X=100 KΩ		5	9.4	9.97	10.5	ms
		10	9.4	9.95	10.6	
		15	9.5	10	10.6	
C_X=10 μF, R_X=100 KΩ		5	0.95	1	1.06	s
		10	0.95	1	1.06	
		15	0.96	1.01	1.07	
Pulse Width Match between circuits in same package: C_X=0.1 μF, R_X=100 KΩ	$\frac{100\,(T_1-T_2)}{T_1}$	5	—	±1	—	%
		10	—	±1	—	
		15	—	±1	—	
Minimum Retrigger Time	t_{rr}	5	0	—	—	ns
		10	0	—	—	
		15	0	—	—	
Input Capacitance	C_{IN}	Any Input	—	5	7.5	pF

*Note: Minimum R_X value=4 KΩ, minimum C_X value=5000 pF.

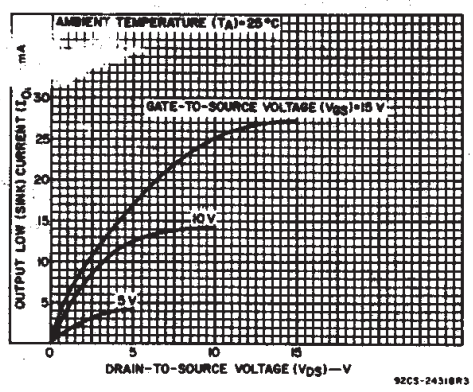


Fig. 2 - Typical output low (sink) current characteristics.

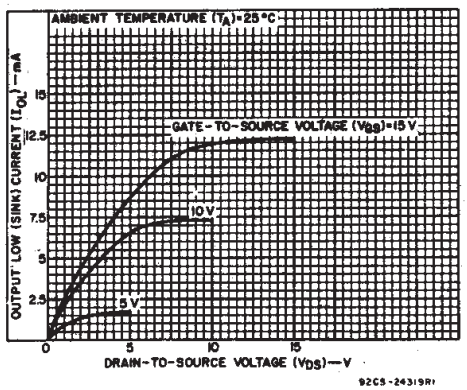


Fig. 3 - Minimum output low (sink) current characteristics.

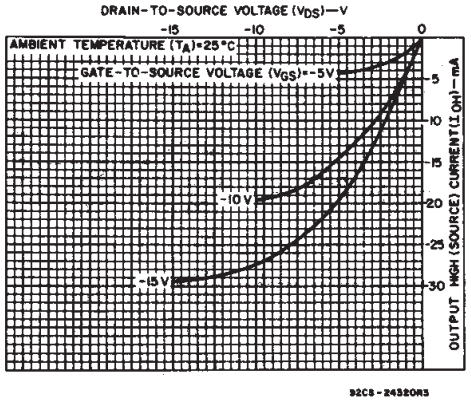


Fig. 4 - Typical output high (source) current characteristics.

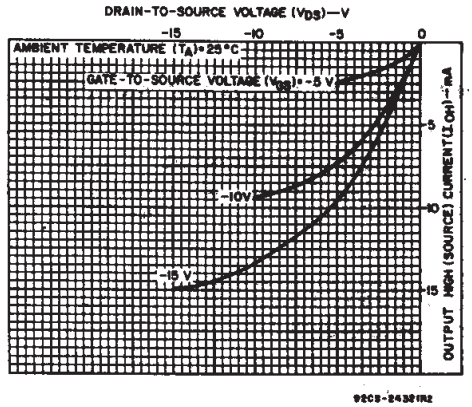


Fig. 5 - Minimum output high (source) current characteristics.

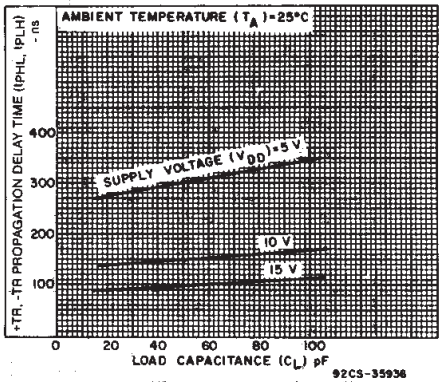


Fig. 6 - Typical propagation delay time as a function of load capacitance (+TR or −TR to Q or $\overline{Q}$).

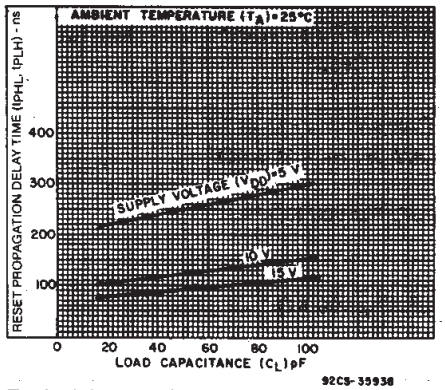


Fig. 7 - Typical propagation delay time as a function of load capacitance (RESET to Q or $\overline{Q}$).

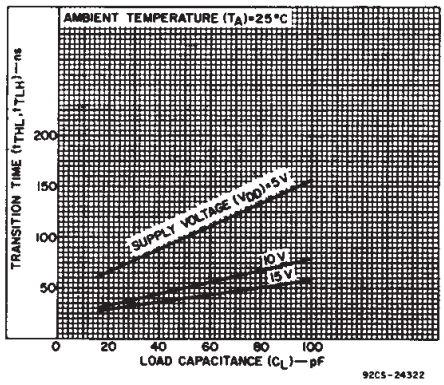


Fig. 8 - Typical transition time as a function of load capacitance.

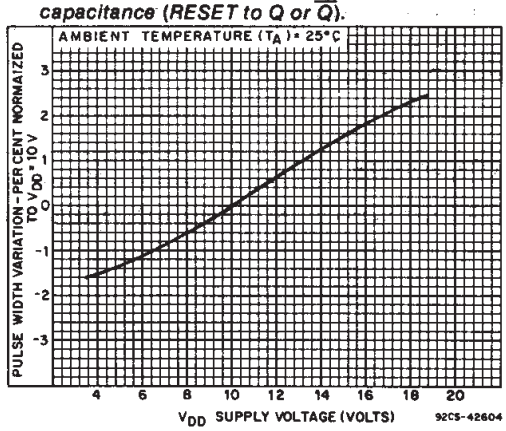


Fig. 9 - Typical pulse-width variation as a function of supply voltage.

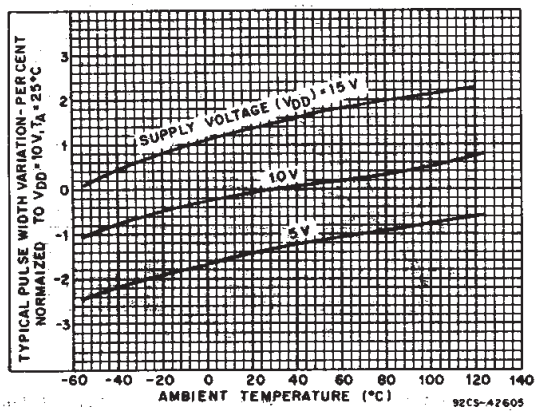


Fig. 10 - Typical pulse-width variation as a function of temperature (R_X=100 KΩ, C_X=0.1 μF).

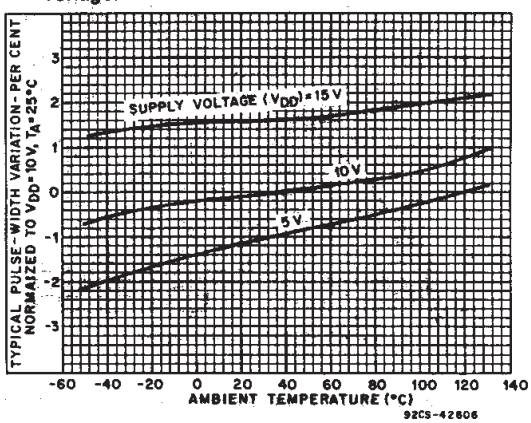


Fig. 11 - Typical pulse-width variation as a function of temperature (R_X=100 KΩ, C_X=2000 pF).

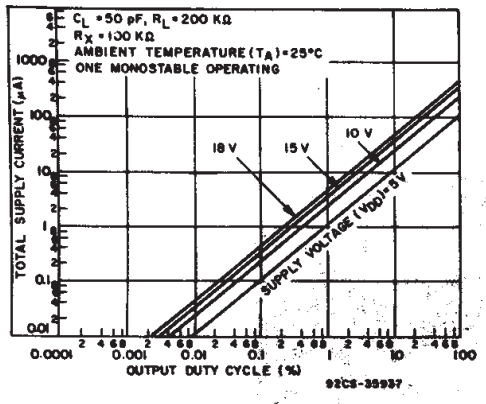


Fig. 12 - Typical total supply current as a function of output duty cycle.

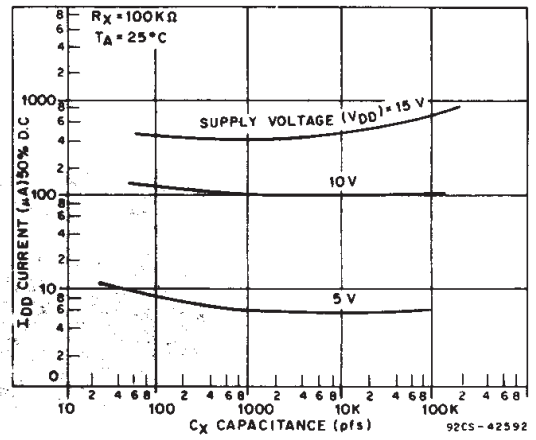
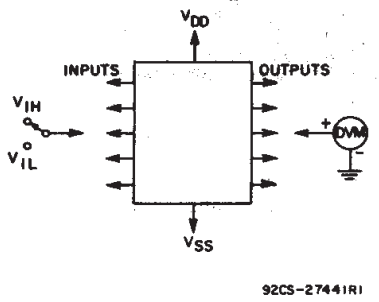


Fig. 13 - Typical total supply current as a function of load capacitance.



NOTE:
1. Test any combination of inputs.
2. When measuring V_{IH} or V_{IL} for Schmitt trigger inputs (+TR, -TR), the input must first be brought to V_{DD} or V_{SS}, respectively, then reduced to the specified limit.

Fig. 14 - Input voltage test circuit.

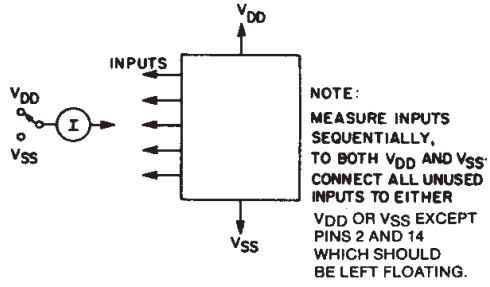


Fig. 15 - Input leakage-current test circuit.

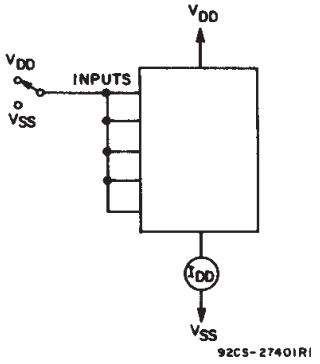


Fig. 16 - Quiescent device current test circuit.

Power-Down Mode

During a rapid power-down condition, as would occur with a power-supply short circuit or with a poorly filtered power supply, the energy stored in C_X could discharge into Pin 2 or 14. To avoid possible device damage in this mode, when C_X is ≥ 0.5 microfarad, a protection diode with a 1-ampere or higher rating (1N5395 or equivalent) and a separate ground return for C_X should be provided as shown in Fig. 17.

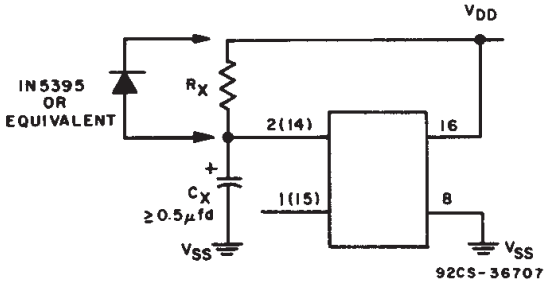


Fig. 17 - Rapid power-down protection circuit.

An alternate protection method is shown in Fig. 18, where a 51-ohm current-limiting resistor is inserted in series with C_X. Note that a small pulse width decrease will occur however, and R_X must be appropriately increased to obtain the originally desired pulse width.

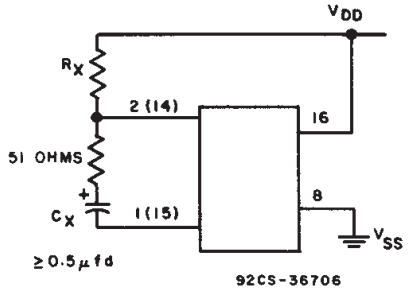
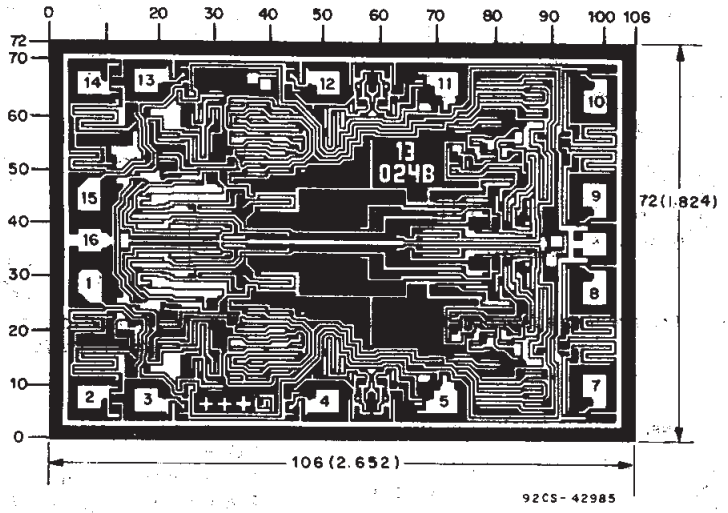


Fig. 18 - Alternate rapid power-down protection circuit.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^{-3} inch).

Dimensions and pad layout for CD14538BH.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-9055701EA	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9055701EA CD14538BF3A
CD14538BE	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD14538BE
CD14538BE.A	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD14538BE
CD14538BF	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD14538BF
CD14538BF.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD14538BF
CD14538BF3A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9055701EA CD14538BF3A
CD14538BF3A.A	NRND	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-9055701EA CD14538BF3A
CD14538BM	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD14538BM
CD14538BM96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD14538BM
CD14538BM96.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD14538BM
CD14538BMT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	CD14538BM
CD14538BNSR	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD14538B
CD14538BNSR.A	Active	Production	SOP (NS) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CD14538B
CD14538BPW	Obsolete	Production	TSSOP (PW) | 16	-	-	Call TI	Call TI	-55 to 125	CM538B
CD14538BPWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM538B
CD14538BPWR.A	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM538B
CD14538BPWRG4	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	CM538B

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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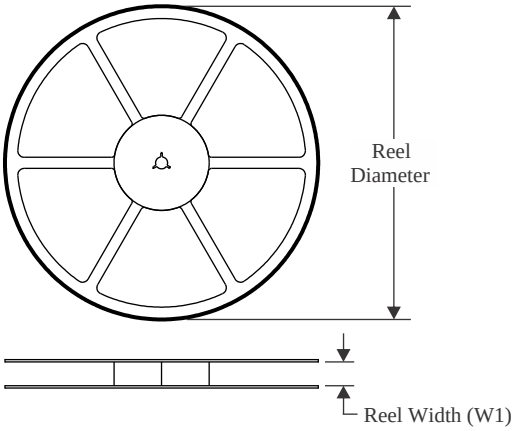
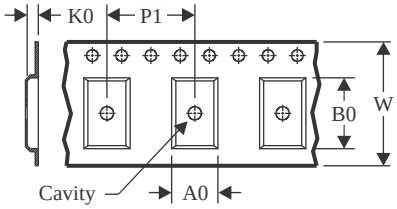
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

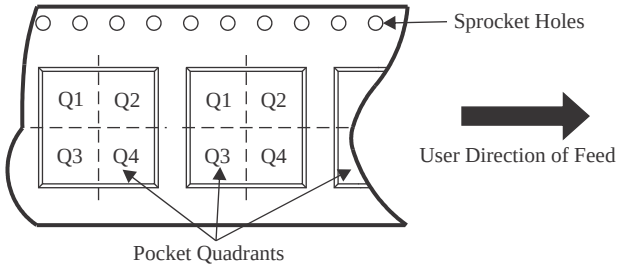


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

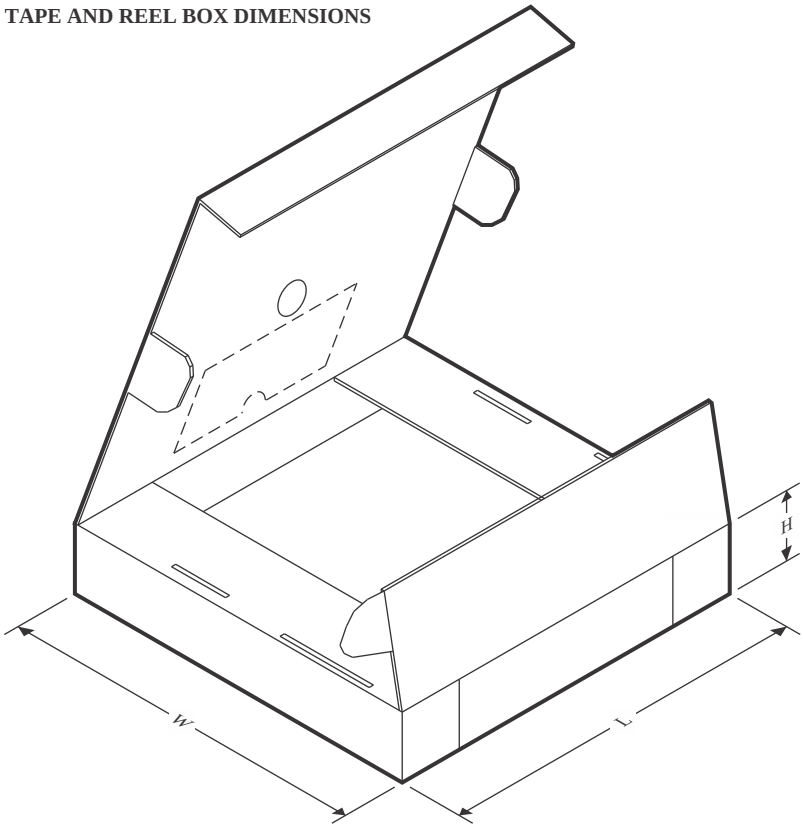
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD14538BM96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD14538BNSR	SOP	NS	16	2000	330.0	16.4	8.45	10.55	2.5	12.0	16.2	Q1
CD14538BPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

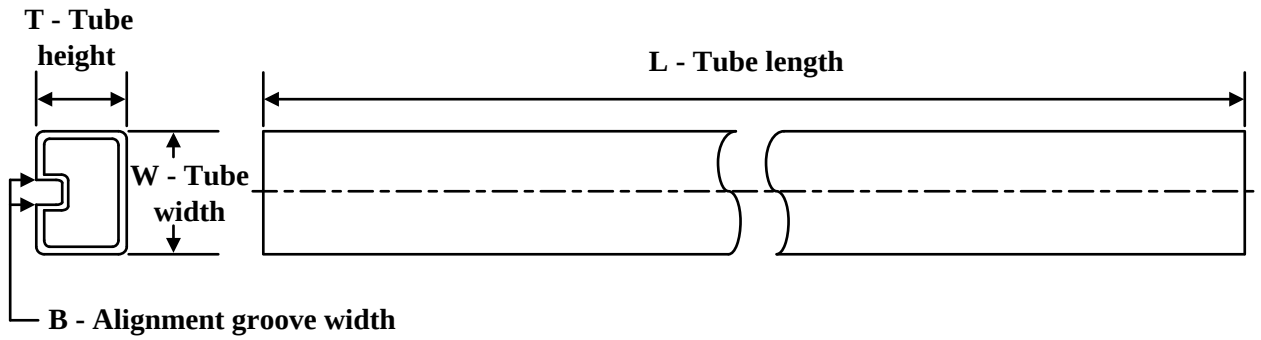
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

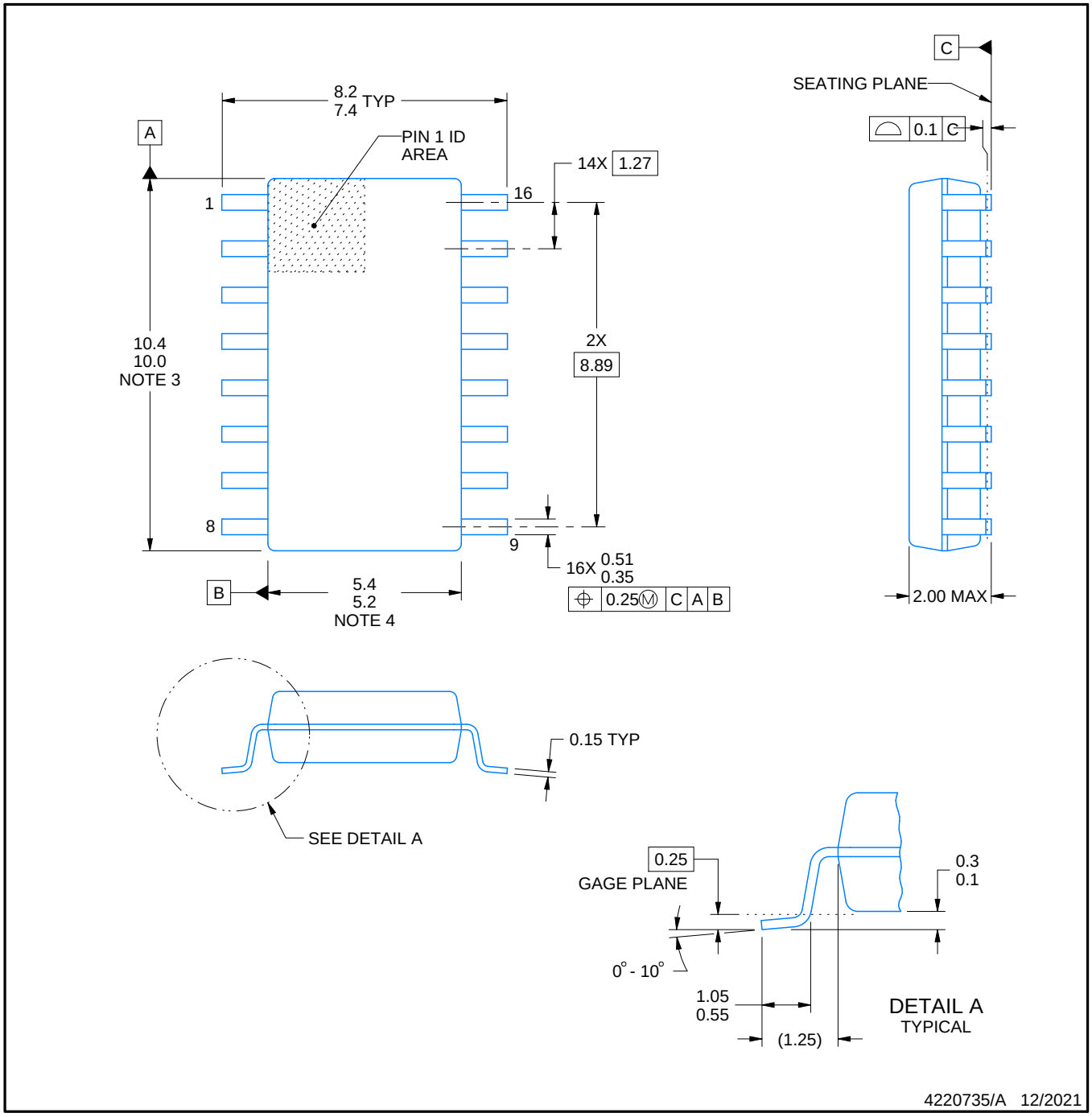
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD14538BM96	SOIC	D	16	2500	353.0	353.0	32.0
CD14538BNSR	SOP	NS	16	2000	353.0	353.0	32.0
CD14538BPWR	TSSOP	PW	16	2000	353.0	353.0	32.0

TUBE



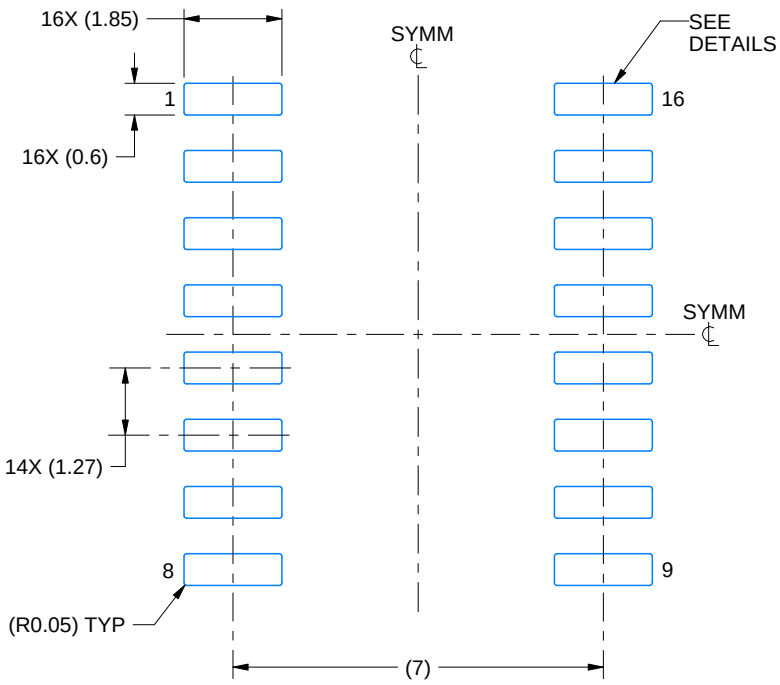
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD14538BE	N	PDIP	16	25	506	13.97	11230	4.32
CD14538BE.A	N	PDIP	16	25	506	13.97	11230	4.32

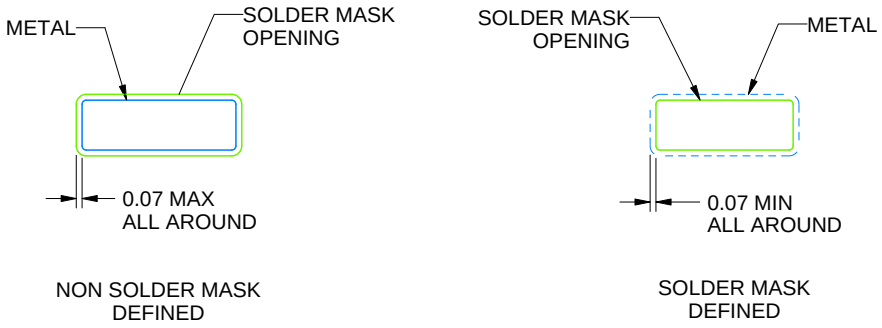


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.



LAND PATTERN EXAMPLE
SCALE:7X

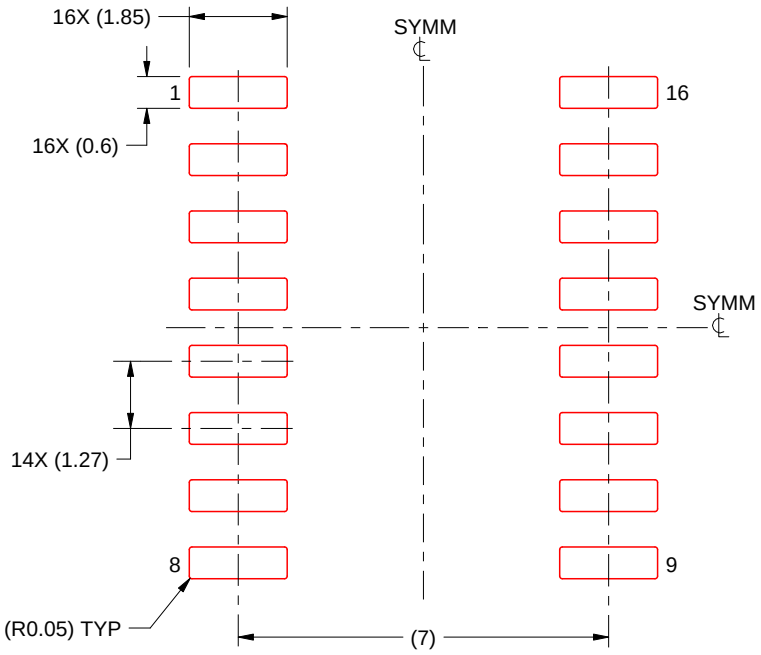


SOLDER MASK DETAILS

4220735/A 12/2021

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



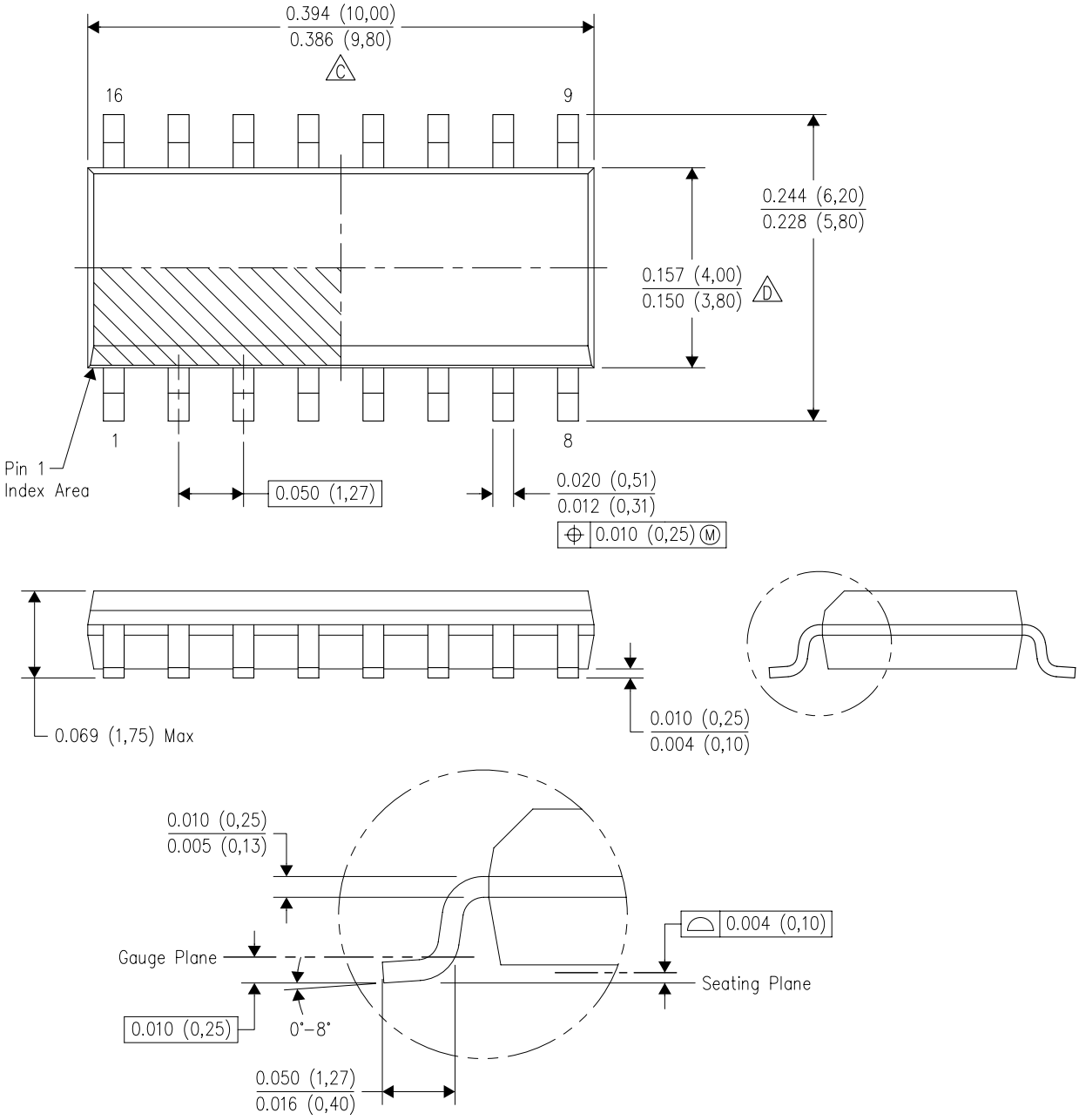
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220735/A 12/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE

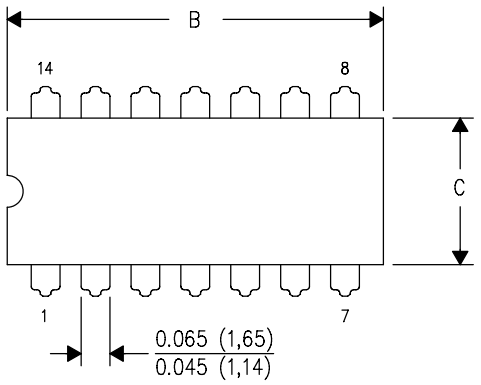


NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

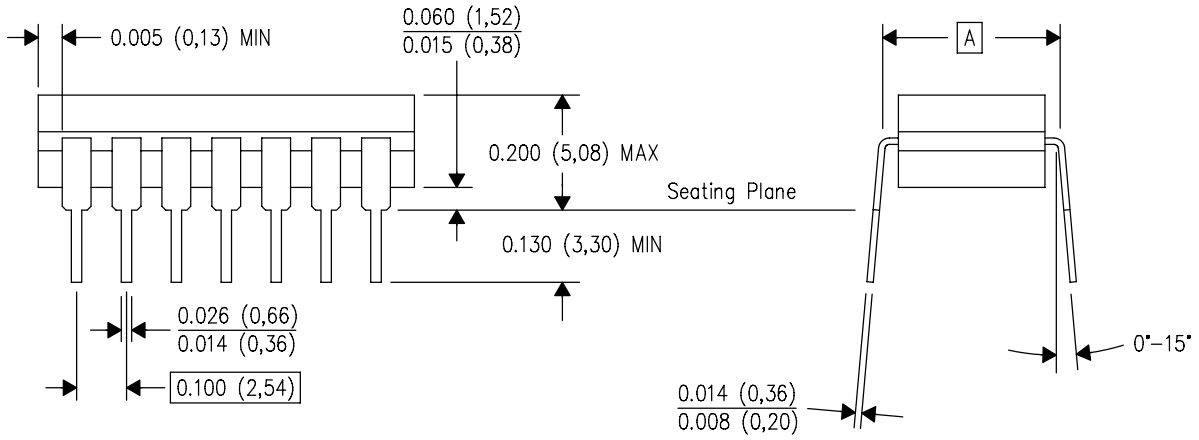
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

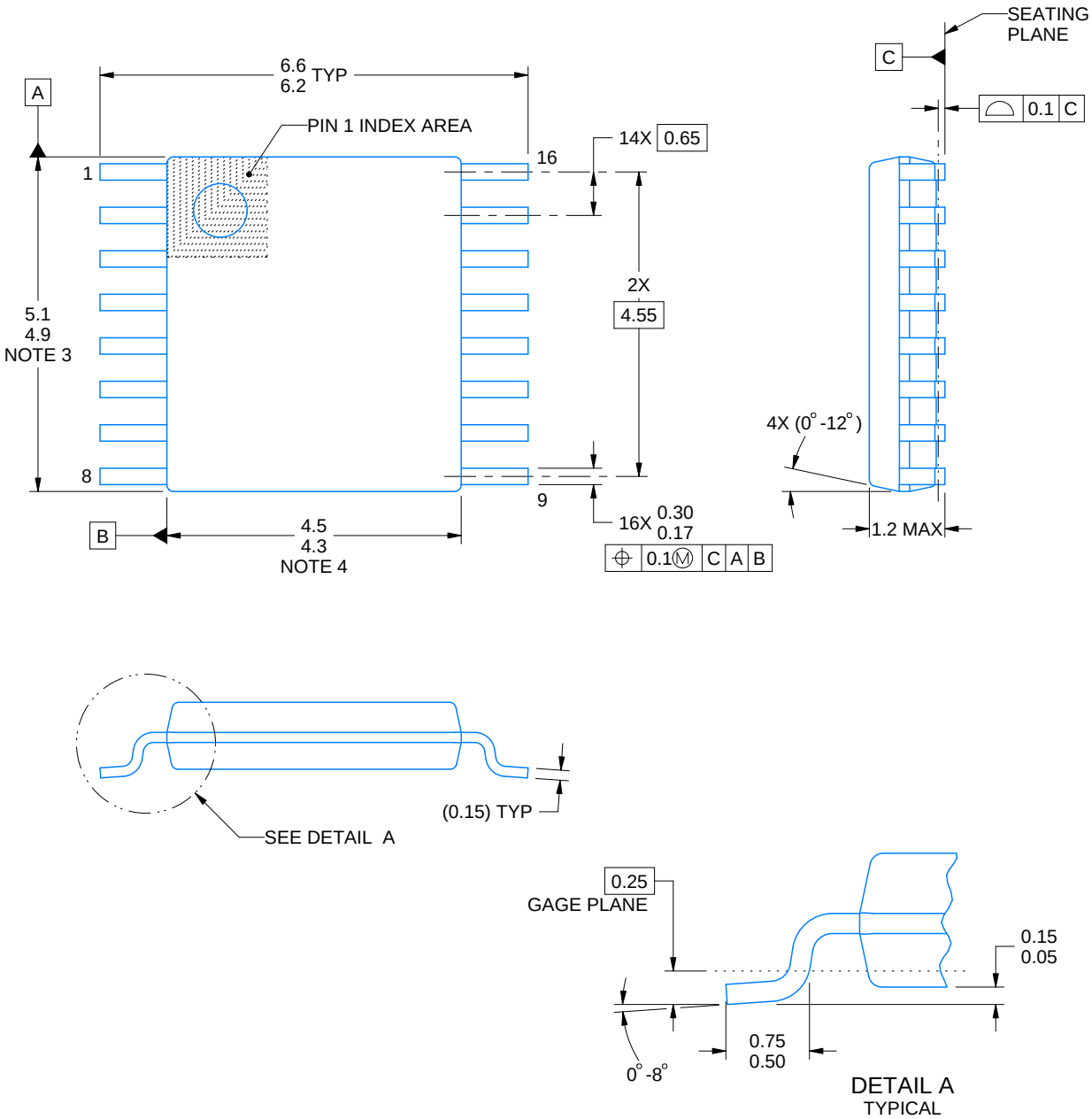
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

PACKAGE OUTLINE

PW0016A

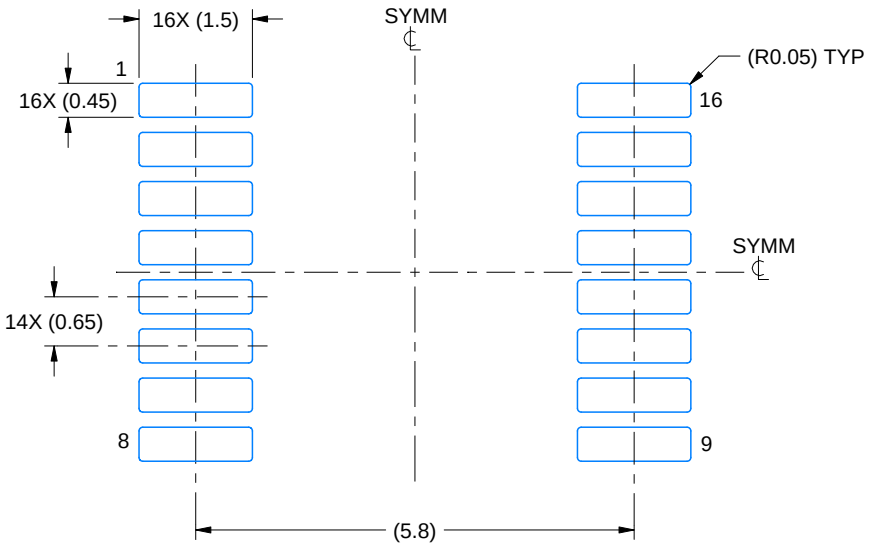
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

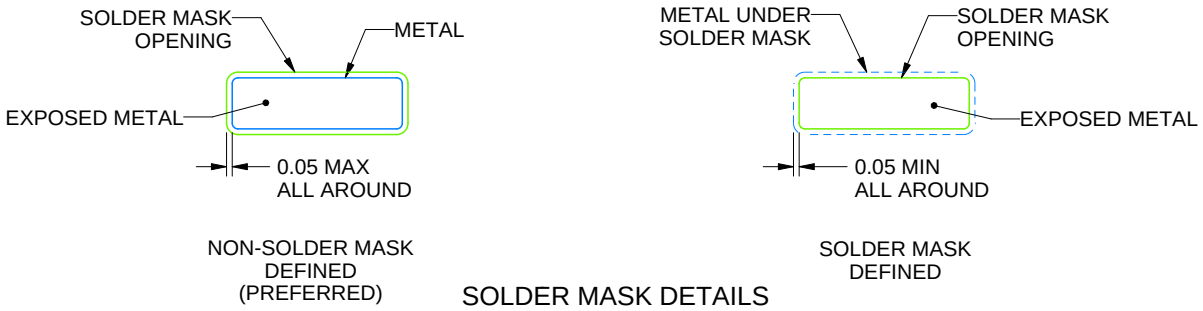


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

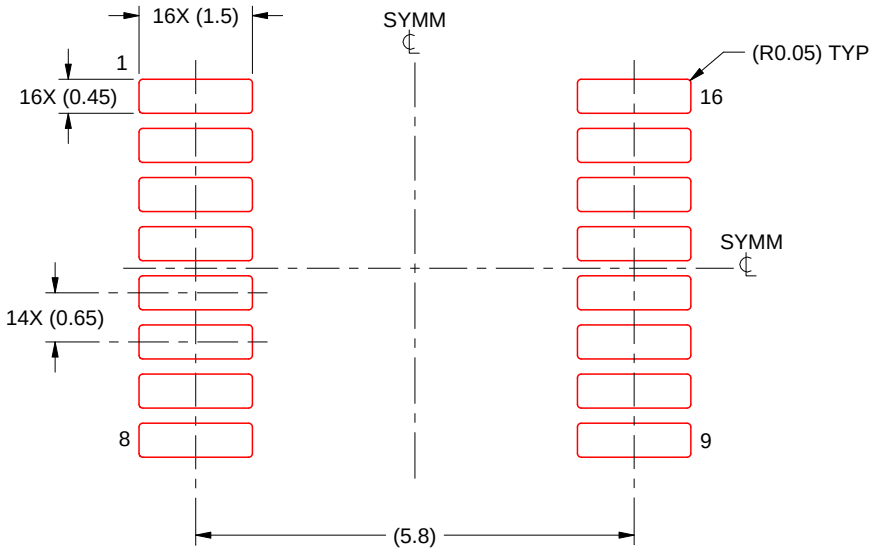


SOLDER MASK DETAILS

4220204/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/B 12/2023

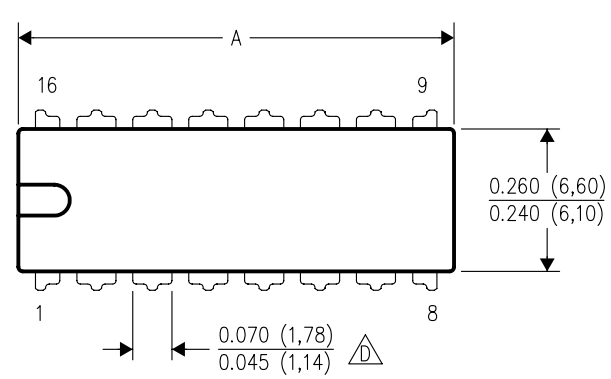
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

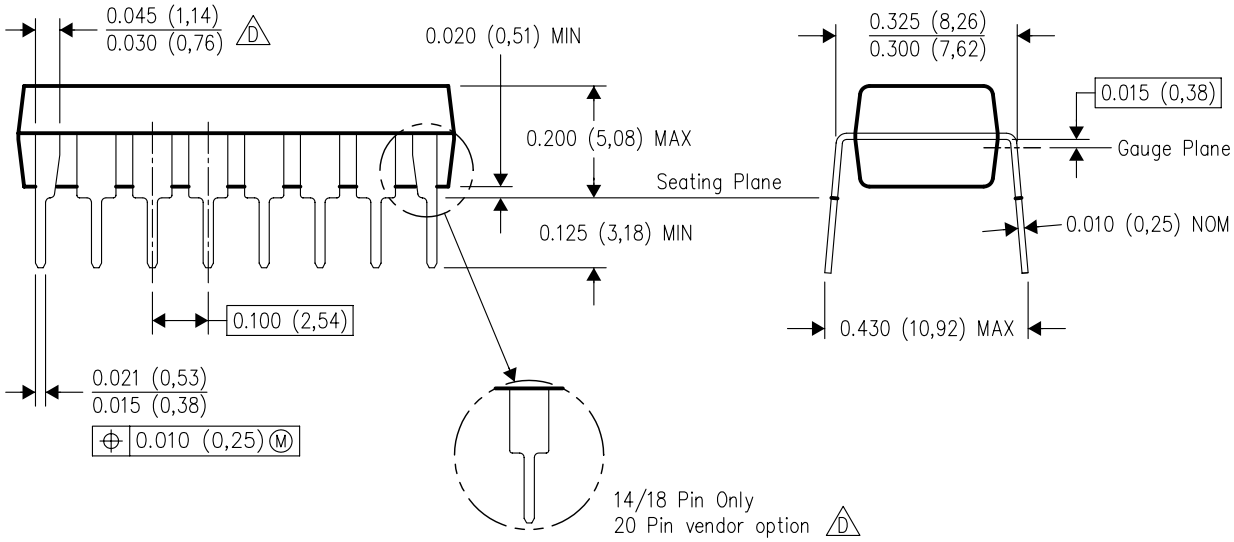
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

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