The CD40107B is a dual 2-input NAND buffer/driver containing two independent 2-input NAND buffers with open-drain single n-channel transistor outputs. This device features a wired-OR capability and high output sink current capability (136 mA typ. at VDD = 10 V, VGS = 1 V). The CD40107B is supplied in 8-lead hermetic dual-in-line ceramic packages (F3A suffix), 8-lead dual-in-line plastic packages (E suffix), 8-lead small-outline packages (M, M96, MT, and PSR suffixes), and 8-lead thin shrink small-outline packages (PW and PWR suffixes).

**Features:**
- 32 times standard B-Series output current drive sinking capability — 136 mA typ. @ VDD = 10 V, VGS = 1 V
- 100% tested for quiescent current at 20 V
- Maximum input current of 1 μA at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- 5-V, 10-V, and 15-V parametric ratings
- Noise margin, full package temperature range, RL to VDD = 10 kΩ:
  - 1 V at VDD = 5 V
  - 2 V at VDD = 10 V
  - 2.5 V at VDD = 15 V

**Applications**
- Driving relays, lamps, LEDs
- Line driver
- Level shifter (up or down)

**MAXIMUM RATINGS, Absolute-Maximum Values:**
- DC SUPPLY-VOLTAGE RANGE, (VDD)
  - Voltages referenced to VSS Terminal: -0.5V to +20V
- INPUT VOLTAGE RANGE, ALL INPUTS: -0.5V to VDD +0.5V
- DC INPUT CURRENT, ANY ONE INPUT: ±10mA
- POWER DISSIPATION PER PACKAGE (PD):
  - For TA = +25°C: 500mW
  - Derate Linearity at 12mW/°C to 200mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types): 100mW
- OPERATING-TEMPERATURE RANGE (TA):
  - -55°C to +125°C
- STORAGE TEMPERATURE RANGE (Tstg):
  - -65°C to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):
  - At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max: +265°C

**RECOMMENDED OPERATING CONDITIONS**
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply-Voltage Range (For TA&lt;0°C)</td>
<td>3</td>
<td>18</td>
</tr>
<tr>
<td>Full Package-Temperature Range</td>
<td></td>
<td></td>
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</table>
CD40107B Types

**Dynamic Electrical Characteristics**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Propagation Delay:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-to-Low, t_PHL</td>
<td>R_L = 120 Ω</td>
<td>5</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>45</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>30</td>
</tr>
<tr>
<td>Low-to-High, t_PHL</td>
<td>R_L = 120 Ω</td>
<td>5</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>50</td>
</tr>
<tr>
<td>Transition Time:</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>High-to-Low, t_TPHL</td>
<td>R_L = 120 Ω</td>
<td>5</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>10</td>
</tr>
<tr>
<td>Low-to-High, t_TPLH</td>
<td>R_L = 120 Ω</td>
<td>5</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>35</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>25</td>
</tr>
<tr>
<td>Average Input Capacitance, C_{IN}</td>
<td>Any Input</td>
<td>5</td>
<td>7.5</td>
</tr>
<tr>
<td>Average Output Capacitance, C_{OUT}</td>
<td>Any Output</td>
<td>30</td>
<td></td>
</tr>
</tbody>
</table>

* R_L is external pull-up resistor to V_{DD}.

**Static Electrical Characteristics**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Conditions</th>
<th>Limits at Indicated Temperatures (°C)</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>V_{O} (V)</td>
<td>V_{IN} (V)</td>
</tr>
<tr>
<td>Quiescent Device</td>
<td></td>
<td>-</td>
<td>0.5</td>
</tr>
<tr>
<td>Current IDD Max.</td>
<td></td>
<td>-</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>0.15</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-</td>
<td>0.20</td>
</tr>
<tr>
<td>Output Low (Sink) Current I_{OL} Min.</td>
<td>0.4</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>0.5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.5</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>1</td>
<td>0.1</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.5</td>
<td>0.15</td>
</tr>
<tr>
<td>Output High (Source) Current I_{OH} Min.</td>
<td>No Internal Pull-Up Device</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Input Low Voltage V_{IL} Max.*</td>
<td>4.5</td>
<td>-</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>9</td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>13.5</td>
<td>-</td>
<td>15</td>
</tr>
<tr>
<td>Input High Voltage V_{IH} Min.*</td>
<td>0.5,4.5</td>
<td>-</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>1.9</td>
<td>-</td>
<td>10</td>
</tr>
<tr>
<td></td>
<td>1.5,13.5</td>
<td>-</td>
<td>15</td>
</tr>
<tr>
<td>Input Current I_{IN} Max.</td>
<td>-</td>
<td>0.18</td>
<td>18</td>
</tr>
<tr>
<td>Output Leakage Current I_{OZ} Max.</td>
<td>18</td>
<td>0.18</td>
<td>18</td>
</tr>
</tbody>
</table>

* Measured with external pull-up resistor, R_L = 10 kΩ to V_{DD}.

**Figures:**
- Fig. 4: Typical transition time as a function of load capacitance.
- Fig. 5: Typical propagation delay time as a function of load capacitance.
- Fig. 6: Typical power dissipation as a function of input frequency.
- Fig. 7: Power-dissipation test circuit for CD40107BE.
**CD40107B Types**

Dimensions and Pad Layout for CD40107B.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10⁻³ inch).

---

**Terminal Assignments**

**CD40107B**

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Special Considerations for CD40107B

1. Limiting Capacitive Currents for CL > 500 pF, VDD > 15 V.
   For VDD > 15 V, and load capacitance (CL) from output to ground > 500 pF, an external 25 Ω series limiting resistor should be inserted between the output terminal and CL. No external resistor is necessary if CL < 500 pF or VDD < 15 V.

2. Driving Inductive Loads
   When using the CD40107B to drive inductive loads, the load should be shunted with a diode to prevent high voltages from developing across the CD40107B output.
# Packaging Information

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (5)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD40107BE</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>CD40107BE</td>
<td></td>
</tr>
<tr>
<td>CD40107BEE4</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>P</td>
<td>8</td>
<td>50</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>CD40107BE</td>
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<tr>
<td>CD40107BF</td>
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<td>CDIP</td>
<td>J</td>
<td>14</td>
<td>1</td>
<td>TBD</td>
<td>SNPB</td>
<td>N / A for Pkg Type</td>
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</tr>
<tr>
<td>CD40107BF3A</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>14</td>
<td>1</td>
<td>TBD</td>
<td>SNPB</td>
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<td>-55 to 125</td>
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<tr>
<td>CD40107BM</td>
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<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>75</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CM0107</td>
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<tr>
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<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CM0107</td>
<td></td>
</tr>
<tr>
<td>CD40107BPSR</td>
<td>ACTIVE</td>
<td>SO</td>
<td>PS</td>
<td>8</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CM0107B</td>
<td></td>
</tr>
<tr>
<td>CD40107BPW</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>8</td>
<td>150</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CM0107B</td>
<td></td>
</tr>
<tr>
<td>CD40107BPWR</td>
<td>ACTIVE</td>
<td>TSSOP</td>
<td>PW</td>
<td>8</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CM0107B</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD40107B, CD40107B-MIL:**

- Catalog: CD40107B
- Military: CD40107B-MIL

**NOTE:** Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD40107BM96</td>
<td>SOIC</td>
<td>D</td>
<td>8</td>
<td>2500</td>
<td>330.0</td>
<td>12.4</td>
<td>6.4</td>
<td>5.2</td>
<td>2.1</td>
<td>8.0</td>
<td>12.0</td>
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<td>D</td>
<td>8</td>
<td>2500</td>
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<td>5.2</td>
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<td>Q1</td>
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<td>TSSOP</td>
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*All dimensions are nominal.*
**TAPE AND REEL BOX DIMENSIONS**

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<th>Height (mm)</th>
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<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
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</tbody>
</table>

*All dimensions are nominal*
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
design recommendations.

9. Board assembly site may have different recommendations for stencil design.
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.

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EXAMPLE BOARD LAYOUT

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

SEE DETAIL A
1
12X (.100 )
[2.54]
SYMM
7
14X (.039)
[1]
SYMM
8

SEE DETAIL B
14

DETIAL A
SCALE: 15X

.R02 MAX
[0.05]
ALL AROUND

.SOLDER MASK OPENING

METAL

_DETIAL A
SCALE: 15X

.R02 MAX
[0.05]
ALL AROUND

.SOLDER MASK OPENING

METAL

4214771/A 05/2017
NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
MECHANICAL DATA

PS (R-PDSO-G8)  PLASTIC SMALL-OUTLINE PACKAGE

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
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