CMOS Quad
AND/OR Select Gate

High-Voltage Types (20-Volt Rating)

- CD4019B types consist of four AND/OR select gate configurations, each consisting of two 2-input AND gates driving a single 2-input OR gate. Selection is accomplished by bits K0 and K1. In addition to selection of either channel A or channel B information, the control bits can be applied simultaneously to accomplish the logical A + B function.

The CD4019B types are supplied in 16-lead hermetic dual-in-line ceramic packages (F3A suffix), 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).

FEATURES:
- Medium-speed operation
- t\(_{PHL} = t_{PLH} = 60\) ns (typ.) at \(C_L = 50\) pF, \(V_{DD} = 10\) V
- Standardized, symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- 5-V, 10-V, and 15-V parametric ratings
- Maximum input current of 1 \(\mu\)A at 18 V over full package-temperature range; 100 nA at 18 V and 25°C
- Noise margin (full package-temperature range) = 1 V at \(V_{DD} = 5\) V
  2 V at \(V_{DD} = 10\) V
  2.5 V at \(V_{DD} = 15\) V

MAXIMUM RATINGS, Absolute-Maximum Values:
- DC SUPPLY-VOLTAGE RANGE (\(V_{DD}\))
  - Voltages referenced to \(V_{SS}\) Terminal
  - -0.5 V to +20 V
- INPUT VOLTAGE RANGE, ALL INPUTS
  - -0.5 V to \(V_{DD} + 0.5\) V
- DC INPUT CURRENT, ANY ONE INPUT
  - \(\pm 10\) mA

POWER DISSIPATION PER PACKAGE (\(P_D\)):
- For \(T_A = -55^\circ\)C to +100°C: 500 mW
- For \(T_A = +100^\circ\)C to +125°C: Derate Linearity at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR
- For \(T_A = FULL PACKAGE-TEMPERATURE RANGE (All Package Types)\): 100 mW
- OPERATING-TEMPERATURE RANGE (\(T_A\))
  - -55°C to +125°C
- STORAGE TEMPERATURE RANGE (\(T_{STG}\))
  - -65°C to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):
  - At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max

RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>(V_{DD}) (V)</th>
<th>Min.</th>
<th>Max.</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply Voltage Range (For (T_A = FULL PACKAGE TEMPERATURE RANGE))</td>
<td>–</td>
<td>3</td>
<td>18</td>
<td>V</td>
</tr>
</tbody>
</table>

Fig. 1—Logic diagram.
# CD4019B Types

## STATIC ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>CONDITIONS</th>
<th>LIMITS AT INDICATED TEMPERATURES (°C)</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>$V_O$ (V)</td>
<td>$V_{IN}$ (V)</td>
<td>$V_{DD}$ (V)</td>
</tr>
<tr>
<td>Quescent Device Current, $I_{DD}$ Max.</td>
<td>-</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td>Output Low (Sink) Current, $I_{OL}$ Min.</td>
<td>0.4</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td>Output High (Source) Current, $I_{OH}$ Min.</td>
<td>4.6</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td>Output Voltage: Low-Level, $V_{OL}$ Max.</td>
<td>-</td>
<td>0.5</td>
<td>5</td>
</tr>
<tr>
<td>Input Low Voltage, $V_{IL}$ Max.</td>
<td>0.5</td>
<td>4.5</td>
<td>-</td>
</tr>
<tr>
<td>Input High Voltage, $V_{IH}$ Min.</td>
<td>0.5</td>
<td>4.5</td>
<td>-</td>
</tr>
<tr>
<td>Input Current $I_{IN}$ Max.</td>
<td>-</td>
<td>0.18</td>
<td>18</td>
</tr>
</tbody>
</table>

---

**Fig. 2** - Typical output low (sink) current characteristics.

**Fig. 3** - Minimum output low (sink) current characteristics.

**Fig. 4** - Typical output high (source) current characteristics.

**Fig. 5** - Minimum output high (source) current characteristics.

**Fig. 6** - Typical transition time as a function of load capacitance.

**Fig. 7** - Propagation delay time as a function of load capacitance.

3-63
## CD4019B Types

**Dynamic Electrical Characteristics**

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>Propagation Delay Time: t_{PLH} - t_{PHL}</td>
<td>V_{DD} (V)</td>
<td>Min.</td>
<td>Typ.</td>
</tr>
<tr>
<td></td>
<td>5</td>
<td>15</td>
<td>300</td>
</tr>
<tr>
<td></td>
<td>10</td>
<td>60</td>
<td>120</td>
</tr>
<tr>
<td></td>
<td>15</td>
<td>50</td>
<td>100</td>
</tr>
<tr>
<td>Transition Time: t_{THL} - t_{TLH}</td>
<td></td>
<td>5</td>
<td>100</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td></td>
<td>15</td>
<td>40</td>
</tr>
<tr>
<td>Input Capacitance, C_{IN}</td>
<td></td>
<td>All A and B Inputs</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td></td>
<td>K_{B} and K_{D} Inputs</td>
<td>10</td>
</tr>
</tbody>
</table>

![Fig. 8 — Typical dynamic power dissipation as a function of input frequency.](image)

![Fig. 9 — Dynamic power dissipation test circuit.](image)

![Fig. 10 — Quiescent device current test circuit.](image)

![Fig. 11 — Input voltage test circuit.](image)

![Fig. 12 — Input current test circuit.](image)

## Typical Applications

**Fig. 13 — AND/OR select gating.**

**Fig. 14 — "Shift left:shift right" register.**
CD4019B Types

TYPICAL APPLICATIONS (CONT'D)

Fig. 15 — AND/OR Exclusive-OR selector.

Fig. 16 — "True complement" selector.

Dimensions and pad layout for CD4019BH

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10^-3 inch).
## PACKAGE OPTION ADDENDUM

### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD4019BE</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>CD4019BE</td>
<td>Samples</td>
</tr>
<tr>
<td>CD4019BEE4</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>CD4019BE</td>
<td>Samples</td>
</tr>
<tr>
<td>CD4019BF</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>CD4019BF</td>
<td>Samples</td>
</tr>
<tr>
<td>CD4019BF3A</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>CD4019BF3A</td>
<td>Samples</td>
</tr>
<tr>
<td>CD4019BM</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>40</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CD4019BM</td>
<td>Samples</td>
</tr>
<tr>
<td>CD4019BM96</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CD4019BM</td>
<td>Samples</td>
</tr>
<tr>
<td>CD4019BMT</td>
<td>ACTIVE</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CD4019BMT</td>
<td>Samples</td>
</tr>
<tr>
<td>CD4019BNSR</td>
<td>ACTIVE</td>
<td>SO</td>
<td>NS</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CD4019BNSR</td>
<td>Samples</td>
</tr>
<tr>
<td>CD4019BPWR</td>
<td>ACTIVE</td>
<td>TSSOP PW</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>CU NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 125</td>
<td>CM019B</td>
<td>Samples</td>
</tr>
<tr>
<td>JM38510/05352BEA</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>JM38510/05352BEA</td>
<td>Samples</td>
</tr>
<tr>
<td>M38510/05352BEA</td>
<td>ACTIVE</td>
<td>CDIP</td>
<td>J</td>
<td>16</td>
<td>1</td>
<td>TBD</td>
<td>A42</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>M38510/05352BEA</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- ** OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4019B, CD4019B-MIL:

- Catalog: CD4019B
- Military: CD4019B-MIL

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications
### TAPE AND REEL INFORMATION

#### REEL DIMENSIONS

![Reel Diagram]

#### TAPE DIMENSIONS

<table>
<thead>
<tr>
<th>A0</th>
<th>Dimension designed to accommodate the component width</th>
</tr>
</thead>
<tbody>
<tr>
<td>B0</td>
<td>Dimension designed to accommodate the component length</td>
</tr>
<tr>
<td>K0</td>
<td>Dimension designed to accommodate the component thickness</td>
</tr>
<tr>
<td>W</td>
<td>Overall width of the carrier tape</td>
</tr>
<tr>
<td>P1</td>
<td>Pitch between successive cavity centers</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD4019BM96</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>330.0</td>
<td>16.4</td>
<td>6.5</td>
<td>10.3</td>
<td>2.1</td>
<td>8.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>CD4019BNSR</td>
<td>SO</td>
<td>NS</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>16.4</td>
<td>8.2</td>
<td>10.5</td>
<td>2.5</td>
<td>12.0</td>
<td>16.0</td>
<td>Q1</td>
</tr>
<tr>
<td>CD4019BPWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>330.0</td>
<td>12.4</td>
<td>6.9</td>
<td>5.6</td>
<td>1.6</td>
<td>8.0</td>
<td>12.0</td>
<td>Q1</td>
</tr>
</tbody>
</table>
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal*

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD4019BM96</td>
<td>SOIC</td>
<td>D</td>
<td>16</td>
<td>2500</td>
<td>333.2</td>
<td>345.9</td>
<td>28.6</td>
</tr>
<tr>
<td>CD4019BNSR</td>
<td>SO</td>
<td>NS</td>
<td>16</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>38.0</td>
</tr>
<tr>
<td>CD4019BPWR</td>
<td>TSSOP</td>
<td>PW</td>
<td>16</td>
<td>2000</td>
<td>367.0</td>
<td>367.0</td>
<td>35.0</td>
</tr>
</tbody>
</table>
J (R-GDIP-T**)

CERAMIC DUAL IN-LINE PACKAGE

14 LEADS SHOWN

<table>
<thead>
<tr>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>0.300 (7.62) BSC</td>
<td>0.300 (7.62) BSC</td>
<td>0.300 (7.62) BSC</td>
<td>0.300 (7.62) BSC</td>
</tr>
<tr>
<td>B MAX</td>
<td>0.785 (19.94)</td>
<td>0.840 (21.34)</td>
<td>0.960 (24.38)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>B MIN</td>
<td>—</td>
<td>—</td>
<td>—</td>
<td>—</td>
</tr>
<tr>
<td>C MAX</td>
<td>0.300 (7.62)</td>
<td>0.300 (7.62)</td>
<td>0.310 (7.87)</td>
<td>0.300 (7.62)</td>
</tr>
<tr>
<td>C MIN</td>
<td>0.245 (6.22)</td>
<td>0.245 (6.22)</td>
<td>0.220 (5.59)</td>
<td>0.245 (6.22)</td>
</tr>
</tbody>
</table>

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.
**NOTES:**

A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
⚠ The 20 pin end lead shoulder width is a vendor option, either half or full width.
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
\[\text{Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.}\]
\[\text{Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.}\]
E. Reference JEDEC MS-012 variation AC.
NOTES:  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Publication IPC-7351 is recommended for alternate designs.  
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.  
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.
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