CD4026B, CD4033B Types

CMOS
Decade Counters/Dividers

High-Voltage Types (20-Volt Rating)
With Decoded 7-Segment Display Outputs and:
  Display Enable — CD4026B
  Ripple Blanking — CD4033B

- CD4026B and CD4033B each consist of a 5-stage Johnson decade counter and an output decoder which converts the Johnson code to 7-segment decoded output for driving one stage in a numerical display.
These devices are particularly advantageous in display applications where low power dissipation and/or low package count are important.
Inputs common to both types are CLOCK, RESET, & CLOCK INHIBIT; common outputs are CARRY OUT and the seven decoded outputs (a, b, c, d, e, f, g). Additional inputs and outputs for the CD4026B include DISPLAY ENABLE input and DISPLAY ENABLE and UNGATED "C-SEGMENT" outputs. Signals peculiar to the CD4033B are RIPPLE-BLANKING INPUT and LAMP TEST INPUT and a RIPPLE-BLANKING OUTPUT.
A high RESET signal clears the decade counter to its zero count. The counter is advanced one count at the positive clock signal transition if the CLOCK INHIBIT signal is low. Counter advancement via the clock line is inhibited when the CLOCK INHIBIT signal is high. The CLOCK INHIBIT signal can be used as a negative-edge clock if the clock line is held high. Antiregating is provided on the JOHNSON counter, thus assuring proper counting sequence. The CARRY-OUT (COUT) signal completes one cycle every ten CLOCK INPUT cycles and is used to clock the succeeding decade directly in a multi-decade counting chain. The seven decoded outputs (a, b, c, d, e, f, g) illuminate the proper segments in a seven-segment display device used for representing the decimal numbers 0 to 9. The 7-segment outputs go high on selection in the CD4033B; in the CD4026B these outputs go high only when the DISPLAY ENABLE IN is high.

TERMINAL DIAGRAMS

CD4026B
CD4033B

MAXIMUM RATINGS, Absolute-Maximum Values:
DC SUPPLY-VOLTAGE RANGE, (VDD) .................................................. -0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS ........................................... -0.5V to VDD +0.5V
DC INPUT CURRENT, ANY ONE INPUT ........................................... ±10mA
POWER DISSIPATION PER PACKAGE (Pd) :
For TA = -55°C to +100°C .................................................. 500mW
For TA = +100°C to +125°C .................................................. Derate Linearity at 12mW/°C to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR
FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) .................................................. 100mW
OPERATING-TEMPERATURE RANGE (TA) ........................................... -55°C to +125°C
STORAGE TEMPERATURE RANGE (Tstg) ........................................... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max .................................................. +265°C

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The CD4026B- and CD4033B-series types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (NSR suffix), and 16-lead thin shrink small-outline packages (PWR and PW suffixes).

### RECOMMENDED OPERATING CONDITIONS

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>VDD (V) LIMITS</th>
<th>UNITS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply-Voltage Range (For $T_A = $ Full Package Temperature Range)</td>
<td>3 18</td>
<td>V</td>
</tr>
<tr>
<td>Clock Input Frequency, $f_{CL}$</td>
<td>5 – 2.5 MHz</td>
<td></td>
</tr>
<tr>
<td>10 – 5.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15 – 8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock Pulse Width, $t_{WCL}$</td>
<td>5 220 ns</td>
<td></td>
</tr>
<tr>
<td>10 100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15 80</td>
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<tr>
<td>Clock Rise and Fall Time, $t_{RCL}$</td>
<td>5 – Unlimited ns</td>
<td></td>
</tr>
<tr>
<td>10 200</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15 30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Clock Inhibit Set Up Time, $t_{SU}$</td>
<td>5 200 ns</td>
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<tr>
<td>10 50</td>
<td></td>
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<tr>
<td>15 30</td>
<td></td>
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</tr>
<tr>
<td>Reset Pulse Width, $t_{W}$</td>
<td>5 200 ns</td>
<td></td>
</tr>
<tr>
<td>10 100</td>
<td></td>
<td></td>
</tr>
<tr>
<td>15 50</td>
<td></td>
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</tr>
<tr>
<td>Reset Removal Time</td>
<td>5 30 ns</td>
<td></td>
</tr>
<tr>
<td>10 15</td>
<td></td>
<td></td>
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<tr>
<td>15 10</td>
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</table>

### STATISTICAL ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>CHARACTERISTIC</th>
<th>VDD (V) LIMITS AT INDICATED TEMPERATURES (°C)</th>
<th>UNITS</th>
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<tr>
<td>Quiescent Device Current, $I_{DD}$ Max.</td>
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<tr>
<td>$V_{OL}$</td>
<td>$-0.5$</td>
<td></td>
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<tr>
<td>$V_{OH}$</td>
<td>$-0.5$</td>
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<tr>
<td>Output Low (Sink) Current, $I_{OL}$ Min.</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>Output High (Source) Current, $I_{OH}$ Min.</td>
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<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>14</td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td>14</td>
<td></td>
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<tr>
<td>Output Voltage: Low-Level, $V_{OL}$ Max.</td>
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<tr>
<td>$V_{OL}$</td>
<td>14</td>
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<tr>
<td>$V_{OH}$</td>
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<tr>
<td>Output Voltage: High-Level, $V_{OH}$ Min.</td>
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<tr>
<td>$V_{OL}$</td>
<td>14</td>
<td></td>
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<tr>
<td>$V_{OH}$</td>
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<tr>
<td>$V_{OH}$</td>
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<tr>
<td>Input High Voltage, $V_{IH}$ Min.</td>
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<tr>
<td>$V_{OL}$</td>
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<tr>
<td>$V_{OH}$</td>
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<tr>
<td>Input Current $I_{IN}$ Max.</td>
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<tr>
<td>$V_{OH}$</td>
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### CD4026B

When the DISPLAY ENABLE IN is low the seven decoded outputs are forced low regardless of the state of the counter. Activation of the display only when required results in significant power savings. This system also facilitates implementation of display-character multiplexing.

The CARRY OUT and UNGATED “C-SEGMENT” signals are not gated by the DISPLAY ENABLE and therefore are available continuously. This feature is a requirement in implementation of certain divider functions such as divide-by-60 and divide-by-12.

### CD4033B

The CD4033B has provisions for automatic blanking of the non-significant zeros in a multi-digit decimal number which results in an easily readable display consistent with normal writing practice. For example, the number 0050.0700 in an eight digit display would be displayed as 50.07. Zero suppression on the integer side is obtained by connecting the RBI terminal of the CD4033B associated with the most significant digit in the display to a low-level voltage and connecting the RBO terminal of that stage to the RBI terminal of the CD4033B in the next lower-significant position in the display. This procedure is continued for each succeeding CD4033B on the integer side of the display.

On the fraction side of the display the RBI of the CD4033B associated with the least significant bit is connected to a low-level voltage and the RBO of that CD4033B is connected to the RBI terminal of the CD4033B in the next more-significant-bit position. Again, this procedure is continued for all CD4033B's on the fraction side of the display.

In a purely fractional number the zero immediately preceding the decimal point can be displayed by connecting the RBI of that stage to a high-level voltage (instead of to the RBO of the next more-significant-stage). For example: 0.0964; Likewise, the zero in a number such as 763.0 can be displayed by connecting the RBI of the CD4033B associated with it to a high-level voltage.

Ripple blanking of non-significant zeros provides an appreciable savings in display power.

The CD4033B has a LAMP TEST input which, when connected to a high-level voltage, overrides normal decoder operation and enables a check to be made on possible display malfunctions by putting the seven outputs in the high state.
CD4026B, CD4033B Types

Fig. 1 – CD4026B logic diagram.

Fig. 2 – CD4033B logic diagram.

Fig. 3 – CD4026B timing diagram.

Fig. 4 – CD4033B timing diagram.

Fig. 5 – Detail of typical flip-flop stage for both types.

Fig. 6 – Typical n-channel output low (sink) current characteristics.

Fig. 7 – Minimum n-channel output low (sink) current characteristics.

Fig. 8 – Typical p-channel output high (source) current characteristics.
## CD4026B, CD4033B Types

### Dynamic Electrical Characteristics

At $T_A = 25^\circ C$, input $t_{rr}, t_f = 20\,\text{ns}$, $C_L = 60\,\text{pF}, R_L = 200\,\text{k}\Omega$

<table>
<thead>
<tr>
<th>Characteristic</th>
<th>Test Conditions</th>
<th>Limits</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>VDD (V)</td>
<td>Min.</td>
<td>Typ.</td>
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</tbody>
</table>

#### Clocked Operation

- **Propagation Delay Time:**
  - Carry-Out Line: $t_{PHL}, t_{PDL}$
    - 5 – 250 500
    - 10 – 100 200
    - 15 – 75 150
  
  - Decode Outlines
    - 5 – 350 700
  
- **Transition Time:**
  - Carry-Out Line: $t_{THL}, t_{TLH}$
    - 5 – 100 200
    - 10 – 50 100
    - 15 – 25 50

- **Maximum Clock Input Frequency, $f_{CL}$**
  - 5 – 2.5 5 – MHz
  - 10 – 5.5 11 – MHz
  - 15 – 8 16 – MHz

- **Min. Clock Pulse Width, $t_W$**
  - 5 – 110 220
  - 10 – 50 100
  - 15 – 40 80

- **Clock and Clock Inhibit Rise or Fall Time:**
  - $t_{RCL}, t_{ICL}$
    - 5 – Unlimited
    - 10
    - 15

- **Average Input Capacitance, $C_{IN}$**
  - Any Input
    - 5
    - 7
    - pF

#### Reset Operation

- **Propagation Delay Time:**
  - To Carry-Out Line: $t_{PHL}$
    - 5 – 275 550
    - 10 – 120 240
    - 15 – 80 160
  
  - To Decode Outlines: $t_{PHL}, t_{PDL}$
    - 5 – 300 600
    - 10 – 125 250
    - 15 – 90 180

- **Min. Reset Pulse Width, $t_W$**
  - 5 – 100 120
  - 10 – 50 100
  - 15 – 25 50

- **Min. Reset Removal Time**
  - 5 – 0 30
  - 10 – 0 15
  - 15 – 0 10

---

*Measured with respect to carry-out line.*

---

**Fig. 9** – Minimum p-channel output high (source) current characteristics.

**Fig. 10** – Typical propagation delay time as a function of load capacitance for decoded outputs.

**Fig. 11** – Typical propagation delay time as a function of load capacitance for carry-out outputs.

**Fig. 12** – Typical maximum clock input-frequency as a function of supply voltage.
CD4026B, CD4033B Types

Fig. 13 — Typical power dissipation as a function of clock input frequency.

Fig. 14 — Dynamic power dissipation test circuit for CD4033B.

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIALLY AVAILABLE LIGHT EMITTING DIODE DISPLAYS

Fig. 15 — Quiescent device current.

Fig. 16 — Input voltage.

Fig. 17 — Input current.

Chip dimensions and pad layout for CD4026B
Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (1 mil = 0.001 inch).

Chip dimensions and pad layout for CD4033B
CD4026B, CD4033B Types

INTERFACING THE CD4026B AND CD4033B WITH COMMERCIAL AVAILABLE 7-SEGMENT DISPLAY DEVICES*

LOW-Power INCANDESCENT READOUTS
P/NLITE SERIES Q and R
TUBE REQUIREMENTS $V_{CC}(V) \text{ mA/Segment}$
0-02-15 1.5 8
0-04-30 3 8
0-08-30 3 8
R-R5-20 2 4.3
R-R4-30 3 4.3

ASSUMED TRANSISTOR CHARACTERISTICS $V_{BE} = 0.7 V$ $V_{CC} = 15 V$
$V_{CE} = 5 V$
$V_{CC} = 5 V$
$V_{CE} = 5 V$
$V_{CE} = 5 V$

92CM-3170

* The interfacing buffers shown, while a necessity with the CD4026A and CD4033A, are not required when using the "B" devices; the "B" outputs (10 times the "A" outputs) can drive most display devices directly at voltages above 10 V.

NEON READOUT (NIXIE TUBE)
1. Alco Electronics – MG19
2. Burrage – 8971, 8971, 8971

TUBE REQUIREMENTS $V_{CC}(V) \text{ mA/Segment}$
Alco MG19 180 0.5
Burrage 8971, 170 3
Burrage 8971, 8971, 170 6

TRANSISTOR CHARACTERISTICS
Leakage with transistor cutoff = 0.05 mA
$V_{CE} > V_{T}$

92CM-3170

LOW VOLTAGE VACUUM FLUORESCENT READOUTS
1. Tung Sol DIGIVAC 8/1 Type DT1704A or DT1705C
2. Nippon Electric (NEC) Type DG12E or DG015

TUBE REQUIREMENTS: 100 to 300 μA/segment at tube voltages of 12 V to 26 V depending on required brightness; Filament requirement 45 mA at 16 V, ac or dc.

92CM-3170
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD4026BE</td>
<td>ACTIVE</td>
<td>PDIP</td>
<td>N</td>
<td>16</td>
<td>25</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
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<tr>
<td>CD4026BEE4</td>
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<td>NIPDAU</td>
<td>N / A for Pkg Type</td>
<td>-55 to 125</td>
<td>CD4026BE</td>
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<tr>
<td>CD4026BNSR</td>
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<td>SO</td>
<td>NS</td>
<td>16</td>
<td>2000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
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<td>-55 to 125</td>
<td>CD4026B</td>
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<td>TSSOP</td>
<td>PW</td>
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<td>Call TI</td>
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<td>-55 to 125</td>
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<td>N</td>
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<td>-55 to 125</td>
<td>CM033B</td>
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</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a “~” will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

- Reel Diameter
- Reel Width (W1)

TAPE DIMENSIONS

- K0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component thickness
- A0: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
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TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

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**TUBE**

- **T** - Tube height
- **L** - Tube length
- **W** - Tube width
- **B** - Alignment groove width

*All dimensions are nominal*

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<tr>
<th>Device</th>
<th>Package Name</th>
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</tbody>
</table>
NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

8. Board assembly site may have different recommendations for stencil design.
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

9. Board assembly site may have different recommendations for stencil design.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15.
N (R—PDIP—T**)  PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

<table>
<thead>
<tr>
<th>DIM</th>
<th>14</th>
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<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
</tr>
</tbody>
</table>

| MS—001 VARIATION | AA | BB | AC | AD |

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Falls within JEDEC MS—001, except 18 and 20 pin minimum body length (Dim A).
⚠️ The 20 pin end lead shoulder width is a vendor option, either half or full width.

14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002
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