1 Features
• Standardized symmetrical output characteristics
• Medium speed operation: \( t_{PHL}, t_{PLH} = 30 \text{ ns at } 10 \text{ V (Typical)} \)
• 100% Tested for quiescent current at 20 V
• Maximum input current of 1 µA at 18 V over full package-temperature range, 100 nA at 18 V and 25°C
• Meets all requirements of JEDEC tentative standard No. 13B, Standard Specifications for Description of B Series CMOS Devices

2 Applications
• Logic inversion
• Pulse shaping
• Oscillators
• High-input-impedance amplifiers

3 Description
The CD4069UB device consist of six CMOS inverter circuits. These devices are intended for all general-purpose inverter applications where the medium-power TTL-drive and logic-level-conversion capabilities of circuits such as the CD4009 and CD4049 hex inverter and buffers are not required.

Device Information\(^{(1)}\)

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE (PINS)</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CD4069UBE</td>
<td>PDIP (14)</td>
<td>19.30 mm × 6.35 mm</td>
</tr>
<tr>
<td>CD4069UBF</td>
<td>CDIP (14)</td>
<td>19.56 mm × 6.67 mm</td>
</tr>
<tr>
<td>CD4069UBM</td>
<td>SOIC (14)</td>
<td>8.65 mm × 3.91 mm</td>
</tr>
<tr>
<td>CD4069UBNSR</td>
<td>SO (14)</td>
<td>10.30 mm × 5.30 mm</td>
</tr>
<tr>
<td>CD4069UBPW</td>
<td>TSSOP (14)</td>
<td>5.00 mm × 4.40 mm</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For all available packages, see the orderable addendum at the end of the data sheet.

CD4069UB Functional Diagram

\[ V_{DD} = \text{Pin 14} \]
\[ V_{SS} = \text{Pin 7} \]
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (February 2016) to Revision E  Page

- Removed artifact “–” at tPHE term on the second Features bullet ............................................... 1
- Corrected Vt spec MIN/MAX values in the Abs Max Ratings table .................................................. 4
- Corrected parameter I0B max term to I0D in the Elec Characteristics table .................................... 5
- Corrected parameter IOL min term to IOL in the Elec Characteristics table ............................... 5
- Corrected parameter VCL max term to VCL in the Elec Characteristics table ............................. 6
- Corrected parameter VIL max term to VIL in the Elec Characteristics table .............................. 6
- Corrected parameter VIN min term to VIN in the Elec Characteristics table ............................ 6
- Added Y-axis label to Figure 1 image object ................................................................................. 8
- Changed text string from "–tPHE" to "of tPHE" in the Feature Description paragraph ...................... 13

Changes from Revision C (August 2003) to Revision D  Page

- Added ESD Ratings table, Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section .................................................. 1
5 Pin Configuration and Functions

D, J, N, NS, and PW Packages
14-Pin PDIP, CDIP, SOIC, SO, and TSSOP
Top View

<table>
<thead>
<tr>
<th>PIN</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>1</td>
<td>A input</td>
</tr>
<tr>
<td>B</td>
<td>3</td>
<td>B input</td>
</tr>
<tr>
<td>C</td>
<td>5</td>
<td>C input</td>
</tr>
<tr>
<td>D</td>
<td>9</td>
<td>D input</td>
</tr>
<tr>
<td>E</td>
<td>11</td>
<td>E input</td>
</tr>
<tr>
<td>F</td>
<td>13</td>
<td>F input</td>
</tr>
<tr>
<td>G = A</td>
<td>2</td>
<td>G output</td>
</tr>
<tr>
<td>H = B</td>
<td>4</td>
<td>H output</td>
</tr>
<tr>
<td>I = C</td>
<td>6</td>
<td>I output</td>
</tr>
<tr>
<td>J = D</td>
<td>8</td>
<td>J output</td>
</tr>
<tr>
<td>K = E</td>
<td>10</td>
<td>K output</td>
</tr>
<tr>
<td>L = F</td>
<td>12</td>
<td>L output</td>
</tr>
<tr>
<td>VDD</td>
<td>14</td>
<td>Positive supply</td>
</tr>
<tr>
<td>VSS</td>
<td>7</td>
<td>Negative supply</td>
</tr>
</tbody>
</table>

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Product Folder Links: CD4069UB
6 Specifications

6.1 Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{\text{DD}})</td>
<td>DC supply-voltage (voltages referenced to V(_{\text{SS}}) terminal)</td>
<td>−0.5</td>
<td>20</td>
</tr>
<tr>
<td>V(_{\text{I}})</td>
<td>Input voltage, all inputs</td>
<td>−0.5</td>
<td>V(_{\text{DD}}) + 0.5</td>
</tr>
<tr>
<td>I(_{\text{IK}})</td>
<td>DC input current, any one input</td>
<td>−10</td>
<td>10</td>
</tr>
<tr>
<td>P(_{\text{D}})</td>
<td>Power dissipation per package</td>
<td>−55°C to 100°C</td>
<td>500</td>
</tr>
<tr>
<td></td>
<td></td>
<td>100°C to 125°C</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>Device dissipation per output transistor</td>
<td>Full range (all package types)</td>
<td>100</td>
</tr>
<tr>
<td>T(_{\text{J}})</td>
<td>Junction temperature</td>
<td>265</td>
<td>°C</td>
</tr>
<tr>
<td>T(_{\text{stg}})</td>
<td>Storage temperature</td>
<td>−65</td>
<td>150</td>
</tr>
</tbody>
</table>

\(^{(1)}\) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

\(^{(2)}\) During soldering at distance 1/16 inch ± 1/32 inch (1.59 mm ± 0.79 mm) from case for 10 s maximum

6.2 ESD Ratings

<table>
<thead>
<tr>
<th>ESD MODEL</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{\text{ESD}})</td>
<td>Electrostatic discharge</td>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
</tr>
</tbody>
</table>

\(^{(1)}\) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

\(^{(2)}\) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V(_{\text{DD}})</td>
<td>Supply voltage</td>
<td>3</td>
<td>18</td>
</tr>
<tr>
<td>T(_{\text{A}})</td>
<td>Operating temperature</td>
<td>−55</td>
<td>125</td>
</tr>
</tbody>
</table>

6.4 Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>CD4069UB</th>
<th>D (SOIC)</th>
<th>J (CDIP)</th>
<th>N (PDIP)</th>
<th>NS (SO)</th>
<th>PW (TSSOP)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\text{JUA}})</td>
<td>Junction-to-ambient thermal resistance</td>
<td>94.9</td>
<td>—</td>
<td>57.9</td>
<td>91.2</td>
<td>122.1</td>
</tr>
<tr>
<td>(R_{\text{JUC(top)}})</td>
<td>Junction-to-case (top) thermal resistance</td>
<td>56.4</td>
<td>28.5</td>
<td>45.5</td>
<td>48.8</td>
<td>50.8</td>
</tr>
<tr>
<td>(R_{\text{JUB}})</td>
<td>Junction-to-board thermal resistance</td>
<td>49.2</td>
<td>—</td>
<td>37.7</td>
<td>50</td>
<td>63.8</td>
</tr>
<tr>
<td>(\psi_{\text{JT}})</td>
<td>Junction-to-top characterization parameter</td>
<td>21.1</td>
<td>—</td>
<td>30.6</td>
<td>15</td>
<td>6.3</td>
</tr>
<tr>
<td>(\psi_{\text{JB}})</td>
<td>Junction-to-board characterization parameter</td>
<td>48.9</td>
<td>—</td>
<td>37.6</td>
<td>49.6</td>
<td>63.3</td>
</tr>
<tr>
<td>(R_{\text{JUC(bot)}})</td>
<td>Junction-to-case (bottom) thermal resistance</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
<td>N/A</td>
</tr>
</tbody>
</table>

\(^{(1)}\) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPR4953.
### 6.5 Electrical Characteristics – Dynamic

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>t\textsubscript{PLH}, t\textsubscript{PHL}</td>
<td>V\textsubscript{DD} (V) = 5</td>
<td>55</td>
<td>110</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>V\textsubscript{DD} (V) = 10</td>
<td>30</td>
<td>60</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V\textsubscript{DD} (V) = 15</td>
<td>25</td>
<td>50</td>
<td></td>
<td></td>
</tr>
<tr>
<td>t\textsubscript{THL}, t\textsubscript{TLH}</td>
<td>V\textsubscript{DD} (V) = 5</td>
<td>100</td>
<td>200</td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td></td>
<td>V\textsubscript{DD} (V) = 10</td>
<td>50</td>
<td>100</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>V\textsubscript{DD} (V) = 15</td>
<td>40</td>
<td>80</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C\textsubscript{IN}</td>
<td>Any input</td>
<td>10</td>
<td>15</td>
<td></td>
<td>pF</td>
</tr>
</tbody>
</table>

### 6.6 Electrical Characteristics – Static

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>I\textsubscript{DD}</td>
<td>V\textsubscript{IN} = 0V or 5 V, V\textsubscript{DD} = 5 V</td>
<td>T\textsubscript{A} = –55°C</td>
<td>0.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = –40°C</td>
<td>0.25</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 25°C</td>
<td>0.01</td>
<td>0.25</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 85°C</td>
<td>7.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 125°C</td>
<td>7.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{OL}</td>
<td>V\textsubscript{O} = 0.4 V, V\textsubscript{IN} = 5 V, V\textsubscript{DD} = 5 V</td>
<td>T\textsubscript{A} = –55°C</td>
<td>0.64</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = –40°C</td>
<td>0.61</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 25°C</td>
<td>0.51</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 85°C</td>
<td>0.42</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 125°C</td>
<td>0.36</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{OL}</td>
<td>V\textsubscript{O} = 0.5 V, V\textsubscript{IN} = 10 V, V\textsubscript{DD} = 10 V</td>
<td>T\textsubscript{A} = –55°C</td>
<td>1.6</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = –40°C</td>
<td>1.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 25°C</td>
<td>1.3</td>
<td>2.6</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 85°C</td>
<td>1.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 125°C</td>
<td>0.9</td>
<td></td>
<td></td>
</tr>
<tr>
<td>I\textsubscript{OL}</td>
<td>V\textsubscript{O} = 1.5 V, V\textsubscript{IN} = 15 V, V\textsubscript{DD} = 15 V</td>
<td>T\textsubscript{A} = –55°C</td>
<td>4.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = –40°C</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 25°C</td>
<td>3.4</td>
<td>6.8</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 85°C</td>
<td>2.8</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>T\textsubscript{A} = 125°C</td>
<td>2.4</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
## Electrical Characteristics – Static (continued)

$T_A = 25^\circ C$; input $t_r$, $t_f = 20$ ns; $C_L = 50$ pF; $R_L = 200$ kΩ (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{OH}$</td>
<td>Output high (source) current</td>
<td>$V_O = 4.6$ V, $V_{IN} = 0$ V, $V_{DD} = 5$ V</td>
<td>$T_A = -55^\circ C$</td>
<td>$-0.64$</td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = -40^\circ C$</td>
<td>$-0.61$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 25^\circ C$</td>
<td>$-0.51$</td>
<td>$-1$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 85^\circ C$</td>
<td>$-0.42$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 125^\circ C$</td>
<td>$-0.36$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{OH}$</td>
<td></td>
<td>$V_O = 2.5$ V, $V_{IN} = 0$ V, $V_{DD} = 5$ V</td>
<td>$T_A = -55^\circ C$</td>
<td>$-2$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = -40^\circ C$</td>
<td>$-1.8$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 25^\circ C$</td>
<td>$-1.6$</td>
<td>$-3.2$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 85^\circ C$</td>
<td>$-1.3$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 125^\circ C$</td>
<td>$-1.15$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OL}$</td>
<td>Low-level output voltage</td>
<td>$V_O = 9.5$ V, $V_{IN} = 0$ V, $V_{DD} = 10$ V</td>
<td>$T_A = -55^\circ C$</td>
<td>$-1.6$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = -40^\circ C$</td>
<td>$-1.5$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 25^\circ C$</td>
<td>$-1.3$</td>
<td>$-2.6$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 85^\circ C$</td>
<td>$-1.1$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 125^\circ C$</td>
<td>$-0.9$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{OH}$</td>
<td></td>
<td>$V_O = 13.5$ V, $V_{IN} = 0$ V, $V_{DD} = 15$ V</td>
<td>$T_A = -55^\circ C$</td>
<td>$-4.2$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = -40^\circ C$</td>
<td>$-4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 25^\circ C$</td>
<td>$-3.4$</td>
<td>$-6.8$</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 85^\circ C$</td>
<td>$-2.8$</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>$T_A = 125^\circ C$</td>
<td>$-2.4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IL}$</td>
<td>Input low voltage</td>
<td>$V_O = 5$ V, $V_{DD} = 5$ V</td>
<td>$T_A = 25^\circ C$</td>
<td>0</td>
<td>0.05</td>
</tr>
<tr>
<td></td>
<td></td>
<td>All other temperatures</td>
<td>0.05</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{IH}$</td>
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<td>$V_{IL}$</td>
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<td>$V_O = 0$ V, $V_{DD} = 5$ V</td>
<td>$T_A = 25^\circ C$</td>
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<td>$V_{IL}$</td>
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### Electrical Characteristics – Static (continued)

\( T_A = 25°C; \) input \( t_r, t_f = 20 \text{ ns}; C_L = 50 \text{ pF}; R_L = 200 \text{ kΩ} \) (unless otherwise noted)

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<th>PARAMETER</th>
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<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<td>( I_{IN} )</td>
<td>( V_{IN} = 0 \text{ V to} 18 \text{ V}, V_{DD} = 18 \text{ V} )</td>
<td>( T_A = –55°C )</td>
<td>±01</td>
<td></td>
<td>µA</td>
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<tr>
<td></td>
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<td>( T_A = –40°C )</td>
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<td>( T_A = 25°C )</td>
<td>±10^-5</td>
<td>±1</td>
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<td></td>
<td>( T_A = 85°C )</td>
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<td>( T_A = 125°C )</td>
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### 6.7 Typical Characteristics

#### Figure 1. Minimum and Maximum Voltage Transfer Characteristics

- **Input Voltage (V)**
  - 0
  - 2.5
  - 5
  - 7.5
  - 10
  - 12.5
  - 15
  - 17.5

- **Output Voltage (V)**
  - 0
  - 2.5
  - 5
  - 7.5
  - 10
  - 12.5
  - 15
  - 17.5

**Legend:**
- $V_{DD} = 5$ V
- $V_{DD} = 10$ V
- $V_{DD} = 15$ V
- $V_{DD}$ at 5 V
- $V_{DD}$ at 10 V
- $V_{DD}$ at 15 V

#### Figure 2. Typical Voltage Transfer Characteristics as a Function of Temperature

- **Input Voltage (V)**
  - 0
  - 2.5
  - 5
  - 7.5
  - 10
  - 12.5
  - 15
  - 17.5

- **Output Voltage (V)**
  - 0
  - 2.5
  - 5
  - 7.5
  - 10
  - 12.5
  - 15
  - 17.5

**Legend:**
- 5 V at -55°C
- 5 V at 125°C
- 10 V at -55°C
- 10 V at 125°C
- 15 V at -55°C
- 15 V at 125°C

#### Figure 3. Typical Current and Voltage Transfer Characteristics

- **Input Voltage (V)**
  - 0
  - 2.5
  - 5
  - 7.5
  - 10
  - 12.5
  - 15
  - 17.5

- **Output Voltage (V)**
  - 0
  - 2.5
  - 5
  - 7.5
  - 10
  - 12.5
  - 15
  - 17.5

**Legend:**
- $I_O$ at 5 V
- $I_O$ at 10 V
- $I_O$ at 15 V

#### Figure 4. Typical Output Low (Sink) Current Characteristics

- **Drain-to-Source Voltage (V)**
  - 0
  - 5
  - 10
  - 15
  - 20
  - 25

- **Output Low (Sink) Current (mA)**
  - 0
  - 2.5
  - 5
  - 7.5
  - 10
  - 12.5
  - 15
  - 17.5

**Legend:**
- Gate-to-Source Voltage = 5 V
- Gate-to-Source Voltage = 10 V
- Gate-to-Source Voltage = 15 V

#### Figure 5. Minimum Output Low (Sink) Current Characteristics

- **Drain-to-Source Voltage (V)**
  - 0
  - 5
  - 10
  - 15
  - 20
  - 25

- **Output Low (Sink) Current (mA)**
  - 0
  - 2.5
  - 5
  - 7.5
  - 10
  - 12.5
  - 15
  - 17.5

**Legend:**
- Gate-to-Source Voltage = 5 V
- Gate-to-Source Voltage = 10 V
- Gate-to-Source Voltage = 15 V

#### Figure 6. Typical Output High (Source) Current Characteristics

- **Drain-to-Source Voltage (V)**
  - 0
  - 5
  - 10
  - 15
  - 20
  - 25

- **Output High (Source) Current (mA)**
  - 0
  - 2.5
  - 5
  - 7.5
  - 10
  - 12.5
  - 15
  - 17.5

**Legend:**
- Gate-to-Source Voltage = -5 V
- Gate-to-Source Voltage = -10 V
- Gate-to-Source Voltage = -15 V
7 Parameter Measurement Information

Figure 7. Minimum Output High (Source) Current Characteristics

Figure 8. Typical Propagation Delay Time vs Load Capacitance

Figure 9. Typical Propagation Delay Time vs Supply Voltage

Figure 10. Schematic Diagram of One of Six Identical Inverters
Figure 11. Quiescent Device Current Test Circuit

Figure 12. Noise Immunity Test Circuit

Figure 13. Input Leakage Current Test Circuit
Figure 14. Dynamic Electrical Characteristics Test Circuit and Waveform

Figure 15. Typical Crystal Oscillator Circuit

Figure 16. High-Input Impedance Amplifier

Figure 17. Typical RC Oscillator Circuit
Upper Switching Point:
\[ V_p = \frac{R_R + R_I}{R_I} \cdot \frac{V_{DD}}{2} \]

Lower Switching Point:
\[ V_n = \frac{R_I - R_R}{R_I} \cdot \frac{V_{DD}}{2} \]

\[ R_I > R_R \]

**Figure 18. Input Pulse Shaping Circuit**

**Figure 19. Dynamic Power Dissipation Test Circuit**
8 Detailed Description

8.1 Overview
The CD4069UB device has six inverter circuits. The recommended operating range is from 3 V to 18 V. The CD4069UB-series types are supplied in 14-pin hermetic dual-in-line ceramic packages (F3A suffix), 14-pin dual-in-line plastic packages (E suffix), 14-pin small-outline packages (M, MT, M96, and NSR suffixes), and 14-pin thin shrink small-outline packages (PW and PWR suffixes).

8.2 Functional Block Diagram

8.3 Feature Description
CD4069UB has standardized symmetrical output characteristics and a wide operating voltage range from 3 V to 18 V with quiescent current tested at 20 V. This has a medium operation speed of $t_{\text{PHL}}, t_{\text{PLH}} = 30$ ns (typical) at 10 V. The operating temperature is from –55°C to 125°C. CB4069B meets all requirements of JEDEC tentative standard No. 13B, *Standard Specifications for Description of B Series CMOS Devices*.

8.4 Device Functional Modes
Table 1 shows the functional modes for CD4069UB.

Table 1. Function Table

<table>
<thead>
<tr>
<th>INPUT A, B, C, D, E, F</th>
<th>OUTPUT G, H, I, J, K, L</th>
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</thead>
<tbody>
<tr>
<td>H</td>
<td>L</td>
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<tr>
<td>L</td>
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9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information
The CD4069UB device has a low input current of 1 µA at 18 V over full package-temperature range and 100 nA at 18 V, 25°C. This device has a wide operating voltage range from 3 V to 18 V and used in high voltage applications.

9.2 Typical Application

![Diagram of CD4069UB Application](https://www.ti.com/lit/an/sch054e/sch054e.pdf)

Figure 20. CD4069UB Application

9.2.1 Design Requirements
The CD4069UB device is the industry's highest logic inverter operating at 18 V under recommended conditions. The lower drive capabilities makes it suitable for driving light loads like LED and greatly reduces chances of overshoots and undershoots.

9.2.2 Detailed Design Procedure
The recommended input conditions for Figure 20 includes rise time and fall time specifications (see Δt/ΔV in Recommended Operating Conditions) and specified high and low levels (see $V_{IH}$ and $V_{IL}$ in Recommended Operating Conditions). Inputs are not overvoltage tolerant and must be below $V_{CC}$ level because of the presence of input clamp diodes to $V_{CC}$.

The recommended output condition for the CD4069UB application includes specific load currents. Load currents must be limited so as to not exceed the total power (continuous current through $V_{CC}$ or GND) for the device. These limits are located in the Absolute Maximum Ratings. Outputs must not be pulled above $V_{CC}$. 

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Typical Application (continued)

9.2.3 Application Curves

Figure 21. Typical Transition Time vs Load Capacitance

Figure 22. Typical Dynamic Power Dissipation vs Frequency

Figure 23. Variation of Normalized Propagation Delay Time ($t_{PHL}$ and $t_{PLH}$) With Supply Voltage
10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in Recommended Operating Conditions.

Each $V_{CC}$ pin must have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1-$\mu$F capacitor. If there are multiple $V_{CC}$ pins, then TI recommends a 0.01-$\mu$F or 0.022-$\mu$F capacitor for each power pin. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. 0.1-$\mu$F and 1-$\mu$F capacitors are commonly used in parallel. The bypass capacitor must be installed as close to the power pin as possible for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices, inputs must never float.

In many cases, digital logic device functions or parts of these functions are unused (for example, when only two inputs of a triple-input and gate are used, or only 3 of the 4 buffer gates are used). Such input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. This rule must be observed under all circumstances specified in the next paragraph.

All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. See the application note, Implications of Slow or Floating CMOS Inputs (SCBA004), for more information on the effects of floating inputs. The logic level must apply to any particular unused input depending on the function of the device. Generally, they are tied to GND or $V_{CC}$ (whichever is convenient).

11.2 Layout Example
12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer
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12.2 Documentation Support

12.2.1 Related Documentation
For related documentation see the following:
• Implications of Slow or Floating CMOS Inputs, SCBA004

12.3 Community Resource
The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community Ti’s Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support Ti’s Design Support Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.4 Trademarks
E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.5 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary
SLYZ022 — Ti Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
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</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD4069UB, CD4069UB-MIL:

- **Catalog**: CD4069UB
- **Military**: CD4069UB-MIL

NOTE: Qualified Version Definitions:

- **Catalog**: TI's standard catalog product
- **Military**: QML certified for Military and Defense Applications
### TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**

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</table>

*All dimensions are nominal.*

- **A0** Dimension designed to accommodate the component width
- **B0** Dimension designed to accommodate the component length
- **K0** Dimension designed to accommodate the component thickness
- **W** Overall width of the carrier tape
- **P1** Pitch between successive cavity centers

---

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- **Q1**
- **Q2**
- **Q3**
- **Q4**
### TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
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</thead>
<tbody>
<tr>
<td>CD4069UBM96</td>
<td>SOIC</td>
<td>D</td>
<td>14</td>
<td>2500</td>
<td>853.0</td>
<td>449.0</td>
<td>35.0</td>
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<td>364.0</td>
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<td>2000</td>
<td>364.0</td>
<td>364.0</td>
<td>27.0</td>
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</table>
TUBE

---

**device**

<table>
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<tr>
<th>Device</th>
<th>Package Name</th>
<th>Package Type</th>
<th>Pins</th>
<th>SPQ</th>
<th>L (mm)</th>
<th>W (mm)</th>
<th>T (µm)</th>
<th>B (mm)</th>
</tr>
</thead>
<tbody>
<tr>
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<td>506</td>
<td>13.97</td>
<td>11230</td>
<td>4.32</td>
</tr>
<tr>
<td>CD4069UBE</td>
<td>N</td>
<td>PDIP</td>
<td>14</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
<td>4.32</td>
</tr>
<tr>
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<td>PDIP</td>
<td>14</td>
<td>25</td>
<td>506</td>
<td>13.97</td>
<td>11230</td>
<td>4.32</td>
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<tr>
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<td>N</td>
<td>PDIP</td>
<td>14</td>
<td>25</td>
<td>506</td>
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<td>TSSOP</td>
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<td>90</td>
<td>530</td>
<td>10.2</td>
<td>3600</td>
<td>3.5</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
EXAMPLE BOARD LAYOUT

SOLDER MASK OPENING

METAL

14X (.039) [1]

SEE DETAIL A

12X (.100) [2.54]

14X (.063) [1.6]

SYMM

LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

SEE DETAIL B

METAL

SOLDER MASK OPENING

.002 MAX [0.05] ALL AROUND

.002 MAX [0.05] ALL AROUND

SOLDER MASK OPENING

METAL

DETAIL A
SCALE: 15X

DETIAL B
13X, SCALE: 15X

4214771/A  05/2017
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.

⚠️ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0.15) each side.

⚠️ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0.43) each side.

E. Reference JEDEC MS-012 variation AB.
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
NOTES:  
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.  
B. This drawing is subject to change without notice.  
\[\text{Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 each side.}\]  
\[\text{Body width does not include interlead flash. Interlead flash shall not exceed 0.25 each side.}\]  
E. Falls within JEDEC MO–153
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
N (R-PDIP-T**)  PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

<table>
<thead>
<tr>
<th>PINS **</th>
<th>14</th>
<th>16</th>
<th>18</th>
<th>20</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>0.775 (19.69)</td>
<td>0.775 (19.69)</td>
<td>0.920 (23.37)</td>
<td>1.060 (26.92)</td>
</tr>
<tr>
<td>A MIN</td>
<td>0.745 (18.92)</td>
<td>0.745 (18.92)</td>
<td>0.850 (21.59)</td>
<td>0.940 (23.88)</td>
</tr>
</tbody>
</table>

ometrics: All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.
**MECHANICAL DATA**

**NS (R-PDSO-G**)  
14-PINS SHOWN  

**PLASTIC SMALL-OUTLINE PACKAGE**

<table>
<thead>
<tr>
<th>DIM</th>
<th>14</th>
<th>16</th>
<th>20</th>
<th>24</th>
</tr>
</thead>
<tbody>
<tr>
<td>A MAX</td>
<td>10,50</td>
<td>10,50</td>
<td>12,90</td>
<td>15,30</td>
</tr>
<tr>
<td>A MIN</td>
<td>9,90</td>
<td>9,90</td>
<td>12,30</td>
<td>14,70</td>
</tr>
</tbody>
</table>

**NOTES:**  
A. All linear dimensions are in millimeters.  
B. This drawing is subject to change without notice.  
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.
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