

# CDx4HC374 High-Speed CMOS Logic Octal D-Type Flip-Flop, 3-State Positive-Edge Triggered

## 1 Features

- Buffered inputs
- Common three-state output enable control
- Three-state outputs
- Bus line driving capability
- Typical propagation delay (clock to Q) = 15 ns at  $V_{CC} = 5\text{ V}$ ,  $C_L = 15\text{ pF}$ ,  $T_A = 25^\circ\text{C}$
- Fanout (over temperature range)
  - Standard outputs: 10 LSTTL loads
  - Bus driver outputs: 15 LSTTL loads
- Wide operating temperature range:  $-55^\circ\text{C}$  to  $125^\circ\text{C}$
- Balanced propagation delay and transition times
- Significant power reduction compared to LSTTL Logic ICs
- HC types
  - 2-V to 6-V operation
  - High noise immunity:  $N_{IL} = 30\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5\text{ V}$
- HCT types
  - 4.5-V to 5.5-V Operation
  - Direct LSTTL input logic compatibility,  $V_{IL} = 0.8\text{ V}$  (max),  $V_{IH} = 2\text{ V}$  (min)
  - CMOS input compatibility,  $I_I \leq 1\mu\text{A}$  at  $V_{OL}$ ,  $V_{OH}$

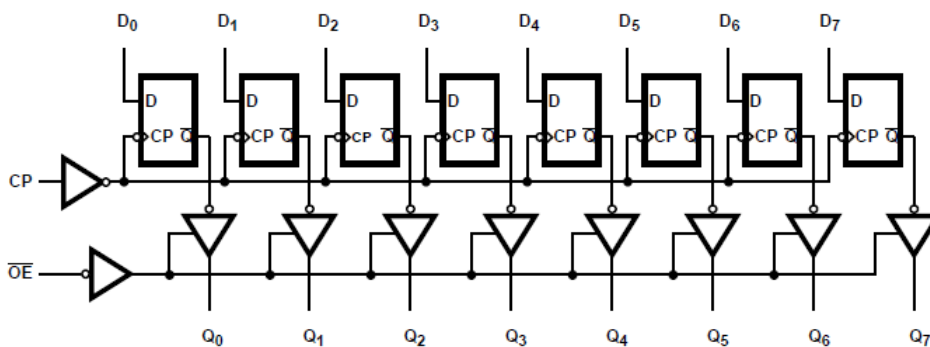
## 2 Description

The 'HC374, 'HCT374, 'HC574, and 'HCT574 are octal D-type flip-flops with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The output enable ( $\overline{OE}$ ) controls the 3-state outputs and is independent of the register operation. When  $\overline{OE}$  is HIGH, the outputs are in the high-impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

### Device Information

PART NUMBER	PACKAGE <sup>(1)</sup>	BODY SIZE (NOM)
CD54HC374F3A	CDIP (20)	26.92 mm × 6.92 mm
CD54HC574F	CDIP (20)	26.92 mm × 6.92 mm
CD54HCT374F3A	CDIP (20)	26.92 mm × 6.92 mm
CD54HCT574F	CDIP (20)	26.92 mm × 6.92 mm
CD74HC374M	SOIC (20)	12.80 mm × 7.50 mm
CD74HC574M	SOIC (20)	12.80 mm × 7.50 mm
CD74HCT374M	SOIC (20)	12.80 mm × 7.50 mm
CD74HCT574M	SOIC (20)	12.80 mm × 7.50 mm
CD74HC374E	PDIP (20)	25.40 mm × 6.35 mm
CD74HC574E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT374E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT574E	PDIP (20)	25.40 mm × 6.35 mm
CD74HCT574PWR	TSSOP (20)	6.50 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Functional Diagram



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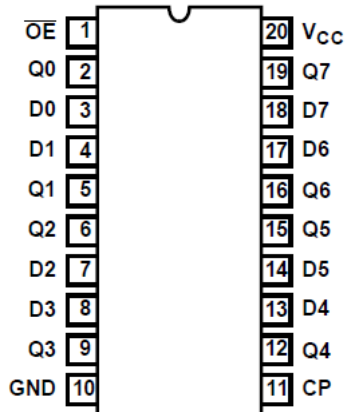
### 3 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

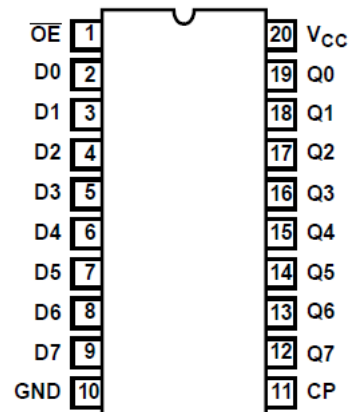
<b>Changes from Revision D (January 2022) to Revision E (October 2022)</b>	<b>Page</b>
• Increased R $\theta$ JA for packages: DW (58 to 109.1); N ( 69 to 84.6); PW (83 to 131.8).....	4

<b>Changes from Revision C (May 2004) to Revision D (January 2022)</b>	<b>Page</b>
• Updated the numbering, formatting, tables, figures, and cross-references throughout the document to reflect modern data sheet standards.....	1

## 4 Pin Configuration and Functions



**HC(T) 374**  
J, DW, or N package  
20-Pin CDIP, SOIC, or PDIP  
Top View



**HC(T) 574**  
J, DW, N, or PW package  
20-Pin CDIP, SOIC, PDIP, or TSSOP  
Top View

## 5 Specifications

### 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	-0.5	7	V
I <sub>IK</sub>	Input diode current	For V <sub>I</sub> < -0.5 V or V <sub>I</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>OK</sub>	Output diode current	For V <sub>O</sub> < -0.5 V or V <sub>O</sub> > V <sub>CC</sub> + 0.5 V		±20 mA
I <sub>O</sub>	Drain current, per output	For -0.5 V < V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±35 mA
I <sub>O</sub>	Output source or sink current per output pin	For V <sub>O</sub> > -0.5 V or V <sub>O</sub> < V <sub>CC</sub> + 0.5 V		±25 mA
	Continuous current through V <sub>CC</sub> or ground current		±50	mA
T <sub>J</sub>	Junction temperature		150	°C
T <sub>stg</sub>	Storage temperature range	-65	150	°C
	Lead temperature (Soldering 10s) (SOIC - Lead Tips Only)		300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 5.2 Recommended Operating Conditions

		MIN	MAX	UNIT	
V <sub>CC</sub>	Supply voltage range	HC types	2	6	V
		HCT types	4.5	5.5	
V <sub>I</sub> , V <sub>O</sub>	DC input or output voltage	0	V <sub>CC</sub>	V	
	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T <sub>A</sub>	Temperature range	-55	125	°C	

### 5.3 Thermal Information

THERMAL METRIC		DW (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		20 PINS	20 PINS	20 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)</sup>	109.1	84.6	131.8	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	76	72.5	72.2	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	77.6	65.3	82.8	°C/W
ψ <sub>JT</sub>	Junction-to-top characterization parameter	51.5	55.3	21.5	°C/W
ψ <sub>JB</sub>	Junction-to-board characterization parameter	77.1	65.2	82.4	°C/W
R <sub>θJC(bot)</sub>	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

## 5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
V <sub>IH</sub>	High level input voltage		2	1.5		1.5		1.5		V	
			4.5	3.15		3.15		3.15			
			6	4.2		4.2		4.2			
V <sub>IL</sub>	Low level input voltage		2		0.5		0.5		0.5	V	
			4.5		1.35		1.35		1.35		
			6		1.8		1.8		1.8		
V <sub>OH</sub>	High level output voltage CMOS loads	I <sub>OH</sub> = – 20 μA	2	1.9		1.9		1.9		V	
		I <sub>OH</sub> = – 20 μA	4.5	4.4		4.4		4.4			
	High level output voltage TTL loads	I <sub>OH</sub> = – 20 μA	6	5.9		5.9		5.9		V	
		I <sub>OH</sub> = – 6 mA	4.5	3.98		3.84		3.7			
V <sub>OL</sub>	Low level output voltage CMOS loads	I <sub>OL</sub> = 20 μA	2		0.1		0.1		0.1	V	
		I <sub>OL</sub> = 20 μA	4.5		0.1		0.1		0.1		
		I <sub>OL</sub> = 20 μA	6		0.1		0.1		0.1		
	Low level output voltage TTL loads	I <sub>OL</sub> = 6 mA	4.5		0.26		0.33		0.4	V	
		I <sub>OL</sub> = 7.8 mA	6		0.26		0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	6		±0.1		±1		±1	μA	
I <sub>CC</sub>	Quiescent device current	V <sub>I</sub> = V <sub>CC</sub> or GND	6		8		80		160	μA	
V <sub>IL</sub> or V <sub>IH</sub>	Three-state leakage current	V <sub>O</sub> = V <sub>CC</sub> or GND	6		±0.5		±5.0		±10	μA	
<b>HCT TYPES</b>											
V <sub>IH</sub>	High level input voltage		4.5 to 5.5	2		2		2		V	
V <sub>IL</sub>	Low level input voltage		4.5 to 5.5		0.8		0.8		0.8	V	
V <sub>OH</sub>	High level output voltage CMOS loads	I <sub>OH</sub> = – 20 μA	4.5	4.4		4.4		4.4		V	
	High level output voltage TTL loads	I <sub>OH</sub> = – 6 mA	4.5	3.98		3.84		3.7			
V <sub>OL</sub>	Low level output voltage CMOS loads	I <sub>OL</sub> = 20 μA	4.5		0.1		0.1		0.1	V	
	Low level output voltage TTL loads	I <sub>OL</sub> = 6 mA	4.5		0.26		0.33		0.4		
I <sub>I</sub>	Input leakage current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		±0.1		±1		±1	μA	
I <sub>CC</sub>	Quiescent device current	V <sub>I</sub> = V <sub>CC</sub> or GND	5.5		8		80		160	μA	
V <sub>IL</sub> or V <sub>IH</sub>	Three-state leakage current	V <sub>O</sub> = V <sub>CC</sub> or GND	6		±0.5		±5.0		±10	μA	

### 5.4 Electrical Characteristics (continued)

PARAMETER		TEST CONDITIONS <sup>(2)</sup>	V <sub>CC</sub> (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$\Delta I_{CC}$ <sup>(1)</sup>	HCT374 Additional quiescent device current per input pin	D0 - D7 inputs held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	108		135		147	μA
		CP input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	324		405		441	μA
		OE input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	468		585		637	μA
	HCT574 Additional quiescent device current per input pin	D0 - D7 inputs held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	144		180		196	μA
		CP input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	270		337.5		367.5	μA
		OE input held at V <sub>CC</sub> – 2.1	4.5 to 5.5		100	216		270		294	μA

(1) For dual-supply systems, theoretical worst case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8mA.

(2) V<sub>I</sub> = V<sub>IH</sub> or V<sub>IL</sub>, unless otherwise noted.

### 5.5 Prerequisite for Switching Characteristics

PARAMETER		V <sub>CC</sub> (V)	25°C			–40°C to 85°C			–55°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>HC TYPES</b>												
f <sub>MAX</sub>	Maximum clock frequency	2	6		5		4				MHz	
		4.5	30		25		20					
		6	35		29		23					
t <sub>W</sub>	Clock pulse width	2	80		100		120				ns	
		4.5	16		20		24					
		6	14		17		20					
t <sub>SU</sub>	Setup time data to clock	2	60		75		90				ns	
		4.5	12		15		18					
		6	10		13		15					
t <sub>H</sub>	Hold time data to clock	2	5		5		5				ns	
		4.5	5		5		5					
		6	5		5		5					
<b>HCT TYPES</b>												
f <sub>MAX</sub>	Maximum clock frequency	4.5	30		25		20				MHz	
t <sub>W</sub>	Clock pulse width	4.5	16		20		24				ns	
t <sub>SU</sub>	Setup time data to clock	4.5	12		15		18				ns	
t <sub>H</sub>	Hold time data to clock	4.5	5		5		5				ns	

## 5.6 Switching Characteristics

 $C_L = 50 \text{ pF}$ , Input  $t_r$ ,  $t_f = 6 \text{ ns}$ 

PARAMETER		TEST CONDITIONS	$V_{CC}$ (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
$t_{PLH}$ , $t_{PHL}$	Propagation delay Clock to output	$C_L = 50 \text{ pF}$	2		165		205		250	ns	
			4.5		33		41		50		
		$C_L = 15 \text{ pF}$	5		15					ns	
			6		28		35		43		
$t_{PLZ}$ , $t_{PHZ}$	Output disable to Q	$C_L = 50 \text{ pF}$	2		135		170		205	ns	
			4.5		27		34		41		
		$C_L = 15 \text{ pF}$	5		11					ns	
			6		23		29		35		
$t_{PZL}$ , $t_{PZH}$	Output enable to Q	$C_L = 50 \text{ pF}$	2		150		190		225	ns	
			4.5		30		38		45		
		$C_L = 15 \text{ pF}$	5		12					ns	
			6		26		33		38		
$f_{MAX}$	Maximum clock frequency	$C_L = 15 \text{ pF}$	5		60					MHz	
$t_{THL}$ , $t_{TLH}$	Output transition time	$C_L = 50 \text{ pF}$	2		60		75		90	ns	
			4.5		12		15		18		
			6		10		13		15		
$C_I$	Input capacitance	$C_L = 50 \text{ pF}$			10		10		10	pF	
$C_O$	Three-state output capacitance				20		20		20	pF	
$C_{PD}$	Power dissipation capacitance <sup>(1) (2)</sup>	$C_L = 15 \text{ pF}$	5		39					pF	
<b>HCT TYPES</b>											
$t_{PHL}$ , $t_{PLH}$	Propagation delay Clock to output	$C_L = 50 \text{ pF}$	4.5		33		41		50	ns	
		$C_L = 15 \text{ pF}$	5		15						
$t_{PLZ}$ , $t_{PHZ}$	Output disable to Q	$C_L = 50 \text{ pF}$	4.5		28		35		42	ns	
		$C_L = 15 \text{ pF}$	5		11						
$t_{PZL}$ , $t_{PZH}$	Output enable to Q	$C_L = 50 \text{ pF}$	4.5		30		38		45	ns	
		$C_L = 15 \text{ pF}$	5		12						
$f_{MAX}$	Maximum clock frequency	$C_L = 15 \text{ pF}$	5		60					MHz	
$t_{TLH}$ , $t_{THL}$	Output transition time	$C_L = 50 \text{ pF}$	4.5		12		15		18	ns	
$C_I$	Input capacitance	$C_L = 50 \text{ pF}$			10		10		10	pF	
$C_O$	Three-state output capacitance				20		20		20	pF	
$C_{PD}$	Power dissipation capacitance <sup>(1) (2)</sup>	$C_L = 15 \text{ pF}$	5		47					pF	

(1)  $C_{PD}$  is used to determine the dynamic power consumption, per package.

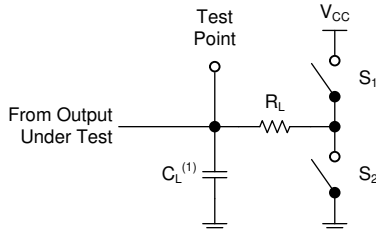
(2)  $P_D = C_{PD} V_{CC}^2 f_i + \sum V_{CC}^2 f_o C_L$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## 6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_t < 6 \text{ ns}$ .

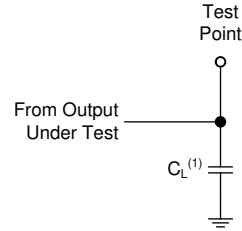
For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



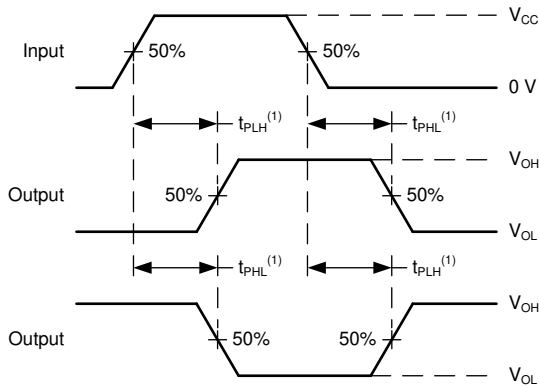
(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-1. Load Circuit for 3-State Outputs**



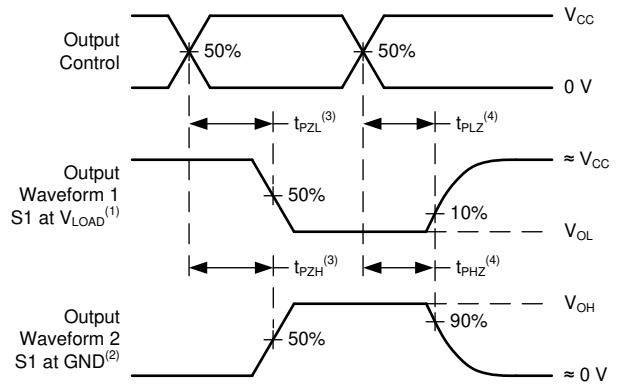
(1)  $C_L$  includes probe and test-fixture capacitance.

**Figure 6-2. Load Circuit for Push-Pull Outputs**



(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 6-3. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs**



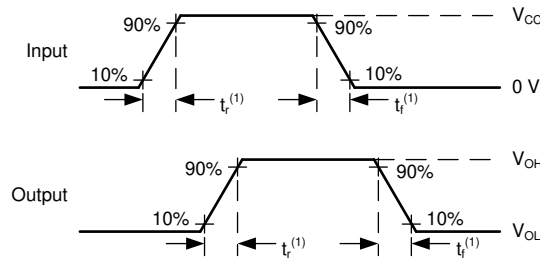
(1) S1 = CLOSED; S2 = OPEN.

(2) S1 = OPEN; S2 = CLOSED.

(3)  $t_{PZL}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

(4)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

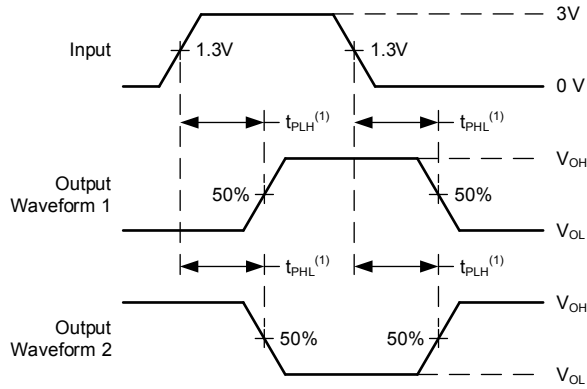
**Figure 6-4. Voltage Waveforms, Standard CMOS Inputs Propagation Delays**



(1) The greater between  $t_r$  and  $t_f$  is the same as  $t_t$ .

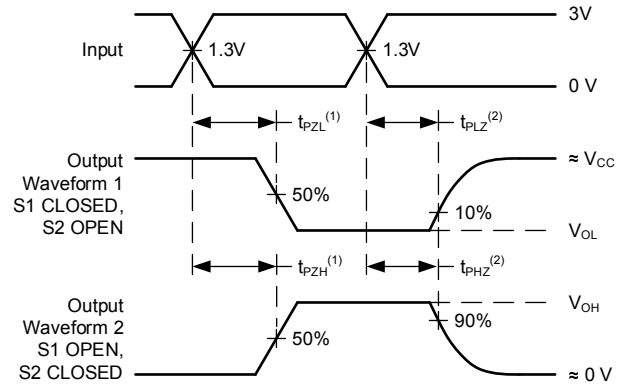
**Figure 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs**





(1) The greater between  $t_{PLH}$  and  $t_{PHL}$  is the same as  $t_{pd}$ .

**Figure 6-6. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs**



(1)  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .

(2)  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .

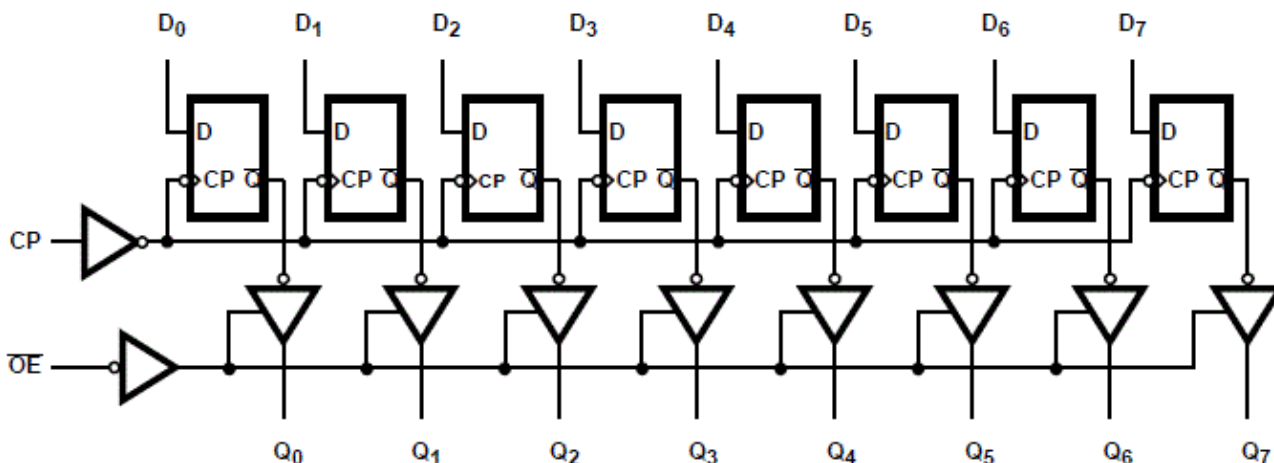
**Figure 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays**

## 7 Detailed Description

### 7.1 Overview

The 'HC374, 'HCT374, 'HC574, and 'HCT574 are octal D-type flip-flops with 3-state outputs and the capability to drive 15 LSTTL loads. The eight edge-triggered flip-flops enter data into their registers on the LOW to HIGH transition of clock (CP). The output enable ( $\overline{OE}$ ) controls the 3-state outputs and is independent of the register operation. When  $\overline{OE}$  is HIGH, the outputs are in the high-impedance state. The 374 and 574 are identical in function and differ only in their pinout arrangements.

### 7.2 Functional Block Diagram



### 7.3 Device Functional Modes

Table 7-1. Truth Table<sup>(1)</sup>

INPUTS			OUTPUT
$\overline{OE}$	CP	Dn	Qn
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

- (1) H = high level (steady state), L = low level (steady state), X = don't care, ↑ = transition from low to high level, Q0 = the level of Q before the indicated steady-state input conditions were established, Z = high impedance state

## 8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- $\mu$ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1- $\mu$ F and 1- $\mu$ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 9 Layout

### 9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices, inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or  $V_{CC}$ , whichever makes more sense for the logic function or is more convenient.

## 10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

### 10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](http://ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 10.2 Support Resources

TI E2E™ [support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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### 10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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### 10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 10.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">5962-8974201RA</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974201RA CD54HCT574F3A
<a href="#">CD54HC374F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8407101RA CD54HC374F3A
<a href="#">CD54HC574F</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC574F
<a href="#">CD54HC574F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC574F3A
<a href="#">CD54HCT374F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8550701RA CD54HCT374F3A
<a href="#">CD54HCT574F</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT574F
<a href="#">CD54HCT574F3A</a>	Active	Production	CDIP (J)   20	20   TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8974201RA CD54HCT574F3A
<a href="#">CD74HC374E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU   NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC374E
<a href="#">CD74HC374M</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-55 to 125	HC374M
<a href="#">CD74HC374M96</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC374M
<a href="#">CD74HC574E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC574E
<a href="#">CD74HC574M</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-55 to 125	HC574M
<a href="#">CD74HC574M96</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC574M
<a href="#">CD74HCT374E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU   NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT374E
<a href="#">CD74HCT374M</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-55 to 125	HCT374M
<a href="#">CD74HCT374M96</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT374M
<a href="#">CD74HCT574E</a>	Active	Production	PDIP (N)   20	20   TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT574E
<a href="#">CD74HCT574M</a>	Obsolete	Production	SOIC (DW)   20	-	-	Call TI	Call TI	-55 to 125	HCT574M
<a href="#">CD74HCT574M96</a>	Active	Production	SOIC (DW)   20	2000   LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT574M
<a href="#">CD74HCT574PWR</a>	Active	Production	TSSOP (PW)   20	2000   LARGE T&R	Yes	NIPDAU   NIPDAU	Level-1-260C-UNLIM	-55 to 125	HK574

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

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**OTHER QUALIFIED VERSIONS OF CD54HC374, CD54HC574, CD54HCT374, CD54HCT574, CD74HC374, CD74HC574, CD74HCT374, CD74HCT574 :**

- Catalog : [CD74HC374](#), [CD74HC574](#), [CD74HCT374](#), [CD74HCT574](#)
- Automotive : [CD74HCT574-Q1](#), [CD74HCT574-Q1](#)
- Enhanced Product : [CD74HCT574-EP](#), [CD74HCT574-EP](#)
- Military : [CD54HC374](#), [CD54HC574](#), [CD54HCT374](#), [CD54HCT574](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC374M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HC574M96	SOIC	DW	20	2000	330.0	24.4	10.9	13.3	2.7	12.0	24.0	Q1
CD74HC574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT374M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574M96	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
CD74HCT574PWR	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC374M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC574M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HC574M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT374M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT574M96	SOIC	DW	20	2000	367.0	367.0	45.0
CD74HCT574PWR	TSSOP	PW	20	2000	356.0	356.0	35.0

**TUBE**


\*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC374E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HC574E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT374E	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT374EE4	N	PDIP	20	20	506	13.97	11230	4.32
CD74HCT574E	N	PDIP	20	20	506	13.97	11230	4.32

# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

# EXAMPLE BOARD LAYOUT

DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# PW0020A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220206/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



# EXAMPLE BOARD LAYOUT

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220206/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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