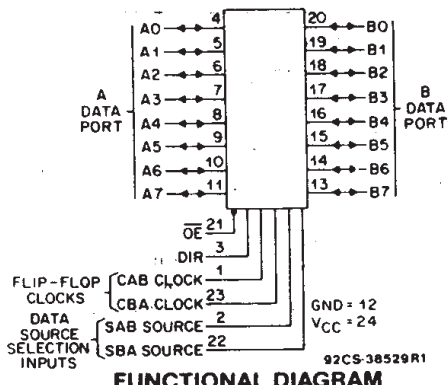


# CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648



Data sheet acquired from Harris Semiconductor  
SCHS293



## Octal-Bus Transceiver/Registers, 3-State

CD54/74AC/ACT646 - Non-Inverting  
CD54/74AC/ACT648 - Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
5.3 ns @  $V_{CC} = 5V, T_A = 25^\circ C, C_L = 50 pF$

### Family Features:

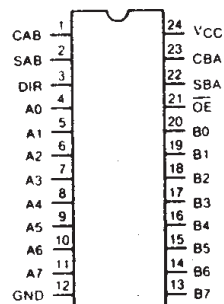
- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Registered Trademark of Fairchild Semiconductor Corp.

The RCA CD54/74AC646 and CD54/74AC648 and the CD54/74ACT646 and CD54/74ACT648 3-state, octal-bus transceiver/registers use the RCA ADVANCED CMOS technology. The CD54/74AC648 and CD54/74ACT648 have inverting outputs. The CD54/74AC646 and CD54/74ACT646 have non-inverting outputs. These devices are bus transceivers with D-type flip-flops which act as internal storage registers on the LOW-to-HIGH transition of either CAB or CBA clock inputs. Output Enable (OE) and Direction (DIR) inputs control the transceiver functions. Data present at the high-impedance output can be stored in either register or both but only one of the two buses can be enabled as outputs at any one time. The Select controls (SAB and SBA) can multiplex stored and transparent (real time) data. The Direction control determines which data bus will receive data when the Output Enable (OE) is LOW. In the high-impedance mode (Output Enable HIGH), A data can be stored in one register and B data can be stored in the other register. The clocks are not gated with the Direction (DIR) and Output Enable (OE) terminals; data at the A or B terminals can be clocked into the storage flip-flops at any time.

The CD74AC/ACT646 and CD74AC/ACT648 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to 70°C); Industrial (-40 to +85°C); and Extended Industrial/Military (-55 to +125°C).

The CD54AC/ACT646 and CD54AC/ACT648, available in chip form (H suffix), are operable over the -55 to +125°C temperature range.



TERMINAL ASSIGNMENT

This data sheet is applicable to the CD74AC646 and CD74ACT646. The CD54AC646, CD54/74AC648, CD54ACT646, and CD54/74ACT648 were not acquired from Harris Semiconductor.

# CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648

FUNCTION TABLE

INPUTS						DATA I/O#		OPERATION OR FUNCTION	
OE	DIR	CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	646	648
X	X		X	X	X	Input	Not specified	Store A, B unspecified	Store A, B unspecified
X	X	X		X	X	Not specified	Input	Store B, A unspecified	Store B, A unspecified
H	X			X	X	Input	Input	Store A and B Data Isolation, hold storage	Store A and B Data Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-Time B Data to A Bus Stored B Data to A Bus	Real-Time $\bar{B}$ Data to A Bus Stored $\bar{B}$ Data to A Bus
L	L	X	H or L	X	H				
L	H	X	X	L	X	Input	Output	Real-Time A Data to B Bus Stored A Data to B Bus	Real-Time $\bar{A}$ Data to B Bus Stored $\bar{A}$ Data to B Bus
L	H	H or L	X	H	X				

#The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs. To prevent excess currents in the High-Z modes, all I/O terminals should be terminated with 10 kΩ resistors.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

- DC SUPPLY-VOLTAGE ( $V_{CC}$ ) ..... -0.5 to 6 V
- DC INPUT DIODE CURRENT,  $I_{IK}$  (for  $V_I < -0.5$  V or  $V_I > V_{CC} + 0.5$  V) .....  $\pm 20$  mA
- DC OUTPUT DIODE CURRENT,  $I_{OK}$  (for  $V_O < -0.5$  V or  $V_O > V_{CC} + 0.5$  V) .....  $\pm 50$  mA
- DC OUTPUT SOURCE OR SINK CURRENT per Output Pin,  $I_O$  (for  $V_O > -0.5$  V or  $V_O < V_{CC} + 0.5$  V) .....  $\pm 50$  mA
- DC  $V_{CC}$  OR GROUND CURRENT ( $I_{CC}$  OR  $I_{GND}$ ) .....  $\pm 100$  mA\*
- POWER DISSIPATION PER PACKAGE ( $P_D$ ):
  - For  $T_A = -55$  to  $+100^\circ\text{C}$  (PACKAGE TYPE E) ..... 500 mW
  - For  $T_A = +100$  to  $+125^\circ\text{C}$  (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/ $^\circ\text{C}$  to 300 mW
  - For  $T_A = -55$  to  $+70^\circ\text{C}$  (PACKAGE TYPE M) ..... 400 mW
  - For  $T_A = +70$  to  $+125^\circ\text{C}$  (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/ $^\circ\text{C}$  to 70 mW
- OPERATING-TEMPERATURE RANGE ( $T_A$ ) .....  $-55$  to  $+125^\circ\text{C}$
- STORAGE TEMPERATURE ( $T_{STG}$ ) .....  $-65$  to  $+150^\circ\text{C}$
- LEAD TEMPERATURE (DURING SOLDERING):
  - At distance  $1/16 \pm 1/32$  in. ( $1.59 \pm 0.79$  mm) from case for 10 s maximum .....  $+265^\circ\text{C}$
  - Unit inserted into PC board min. thickness  $1/16$  in. ( $1.59$  mm) with solder contacting lead tips only .....  $+300^\circ\text{C}$

\*For up to 4 outputs per device; add  $\pm 25$  mA for each additional output.

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, $V_{CC}$ *: (For $T_A =$ Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, $V_I, V_O$	0	$V_{CC}$	V
Operating Temperature, $T_A$	-55	+125	$^\circ\text{C}$
Input Rise and Fall Slew Rate, $dt/dv$			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.

# CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, * {	-0.05	1.5	1.4	—	1.4	—	1.4	—	V
			-0.05	3	2.9	—	2.9	—	2.9	—	
			-0.05	4.5	4.4	—	4.4	—	4.4	—	
			-4	3	2.58	—	2.48	—	2.4	—	
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, * {	0.05	1.5	—	0.1	—	0.1	—	0.1	V
			0.05	3	—	0.1	—	0.1	—	0.1	
			0.05	4.5	—	0.1	—	0.1	—	0.1	
			12	3	—	0.36	—	0.44	—	0.5	
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

Technical Data

# CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> #,*	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> #,*	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>i</sub>	V <sub>CC</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>oz</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>CC</sub>	V <sub>CC</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

9

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.  
\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C. 75 ohms at +125°C.

**ACT INPUT LOADING TABLE**

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
DIR	0.67
OE	1.17
An, Bn	0.4

\*Unit load is ΔI<sub>CC</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

Technical Data

**CD54/74AC646, CD54/74AC648**  
**CD54/74ACT646, CD54/74ACT648**

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f <sub>max</sub>	1.5	11	—	10	—	MHz
		3.3*	101	—	89	—	
		5†	143	—	125	—	
Setup Time Data to Clock	t <sub>SU</sub>	1.5	27	—	31	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
Hold Time Data to Clock	t <sub>H</sub>	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Clock Pulse Width	t <sub>w</sub>	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	

\*3.3 V: min. is @ 3 V

†5 V: min is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus 646	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	154	—	169	ns
		3.3*	4.8	17.1	4.7	18.9	
		5†	3.5	12.3	3.4	13.5	
Store A Data to B Bus Store B Data to A Bus 648	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	154	—	169	ns
		3.3	4.8	17.1	4.7	18.9	
		5	3.5	12.3	3.4	13.5	
A Data to B Bus B Data to A Bus 646	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	125	—	138	ns
		3.3	4	14	3.9	15.4	
		5	2.8	10	2.8	11	
A Data to B Bus B Data to A Bus 648	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	125	—	138	ns
		3.3	4	14	3.9	15.4	
		5	2.8	10	2.8	11	
Select to Data 646	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
Select to Data 648	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	1.5	—	154	—	169	ns
		3.3	5.2	18.4	5.1	20.2	
		5	3.5	12.3	3.4	13.5	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	150 Typ.		150 Typ.		pF
Min. (Valley) During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OH</sub> V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OL</sub> V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

$$P_D = V_{CC}^2 C_{PD} f_i + \sum (V_{CC}^2 C_L f_o)$$

where f<sub>i</sub> = input frequency  
 f<sub>o</sub> = output frequency  
 C<sub>L</sub> = output load capacitance  
 V<sub>CC</sub> = supply voltage.

# CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648

**PREREQUISITE FOR SWITCHING: ACT Series**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f <sub>max</sub>	5*	125	—	110	—	MHz
Setup Time Data to Clock	t <sub>SU</sub>	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t <sub>H</sub>	5	2	—	2	—	ns
Clock Pulse Width	t <sub>w</sub>	5	3.9	—	4.5	—	ns

\*5 V: min. is @ 4.5 V

**SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus 646	t <sub>PLH</sub> t <sub>PHL</sub>	5*	4	14.1	3.9	15.5	ns
Store $\bar{A}$ Data to B Bus Store $\bar{B}$ Data to A Bus 648	t <sub>PLH</sub> t <sub>PHL</sub>	5	4	14.1	3.9	15.5	ns
A Data to B Bus B Data to A Bus 646	t <sub>PLH</sub> t <sub>PHL</sub>	5	3.2	11.4	3.1	12.5	ns
$\bar{A}$ Data to B Bus $\bar{B}$ Data to A Bus 648	t <sub>PLH</sub> t <sub>PHL</sub>	5	3.2	11.4	3.1	12.5	ns
Select to Data 646	t <sub>PLH</sub> t <sub>PHL</sub>	5	3.7	13.2	3.6	14.5	ns
Select to Data 648	t <sub>PLH</sub> t <sub>PHL</sub>	5	4	14.1	3.9	15.5	ns
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	150 Typ.		150 Typ.		pF
Min. (Valley) During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OH</sub>  V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OL</sub>  V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

9

\*5 V: min. is @ 5.5 V  
max. is @ 4.5 V

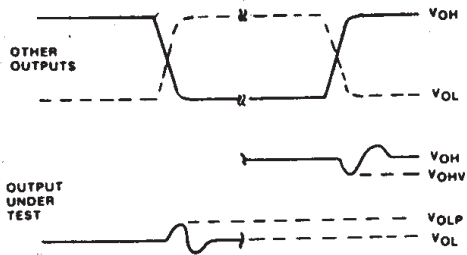
§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

$$P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_o) + V_{CC} \Delta I_{CC}$$

f<sub>i</sub> = input frequency  
 f<sub>o</sub> = output frequency  
 C<sub>L</sub> = output load capacitance  
 V<sub>CC</sub> = supply voltage.

# CD54/74AC646, CD54/74AC648 CD54/74ACT646, CD54/74ACT648

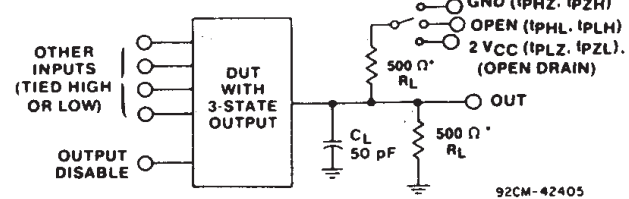
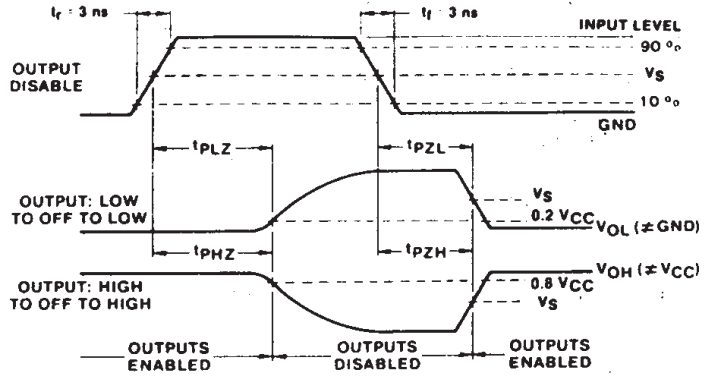
## PARAMETER MEASUREMENT INFORMATION



- NOTES:
1.  $V_{OHV}$  AND  $V_{OLP}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
  2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
 $PRR \leq 1 \text{ MHz}$ ,  $t_r = 3 \text{ ns}$ ,  $t_f = 3 \text{ ns}$ , SKEW 1 ns.
  3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH  $0.1 \mu\text{F}$  CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

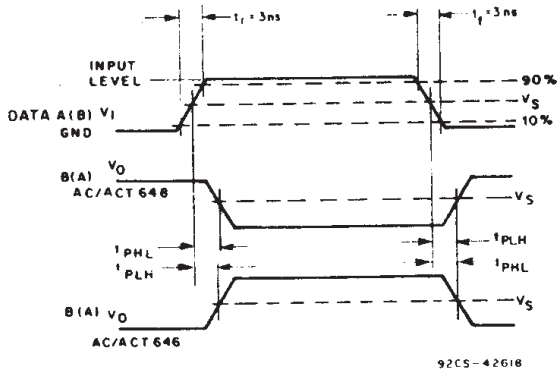
92CS-42406

Fig. 1 - Simultaneous switching transient waveforms.



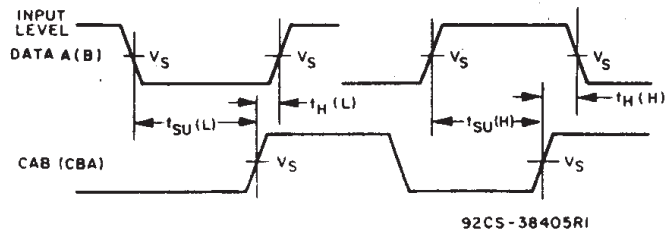
\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

Fig. 2 - Three-state propagation delay waveforms and test circuit.



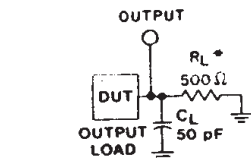
92CS-42618

Fig. 3 - Propagation delay times.



92CS-38405RI

Fig. 4 - Data setup and hold times.



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5 \text{ V}$ ,  $R_L = 1 \text{ k}\Omega$

92CS-42389

Fig. 5 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	0.5 $V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	0.5 $V_{CC}$	0.5 $V_{CC}$

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74AC646M	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC646M	<a href="#">Samples</a>
CD74AC646M96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC646M	<a href="#">Samples</a>
CD74AC646MG4	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC646M	<a href="#">Samples</a>
CD74ACT646M	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT646M	<a href="#">Samples</a>
CD74ACT646M96	ACTIVE	SOIC	DW	24	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT646M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

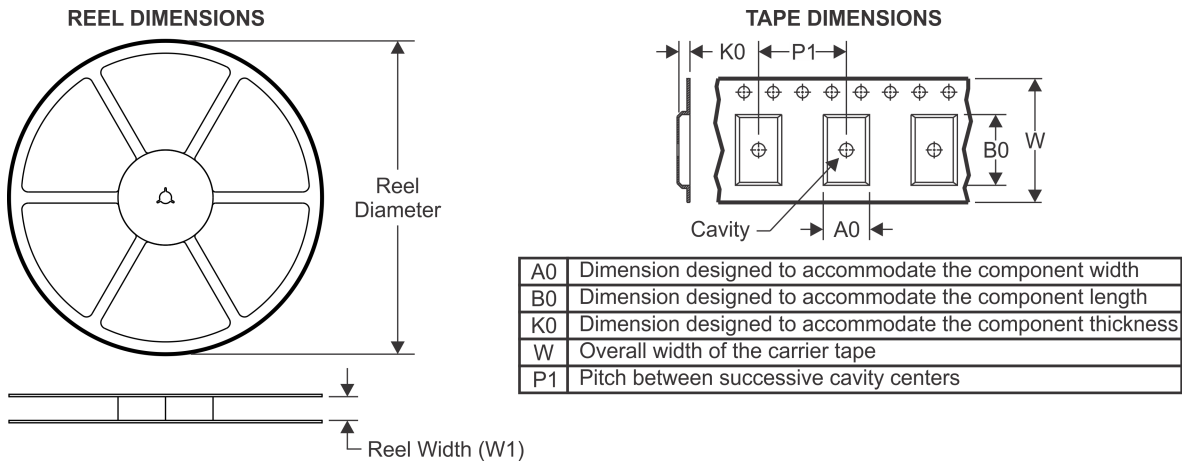
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC646M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74ACT646M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC646M96	SOIC	DW	24	2000	350.0	350.0	43.0
CD74ACT646M96	SOIC	DW	24	2000	350.0	350.0	43.0

DW (R-PDSO-G24)

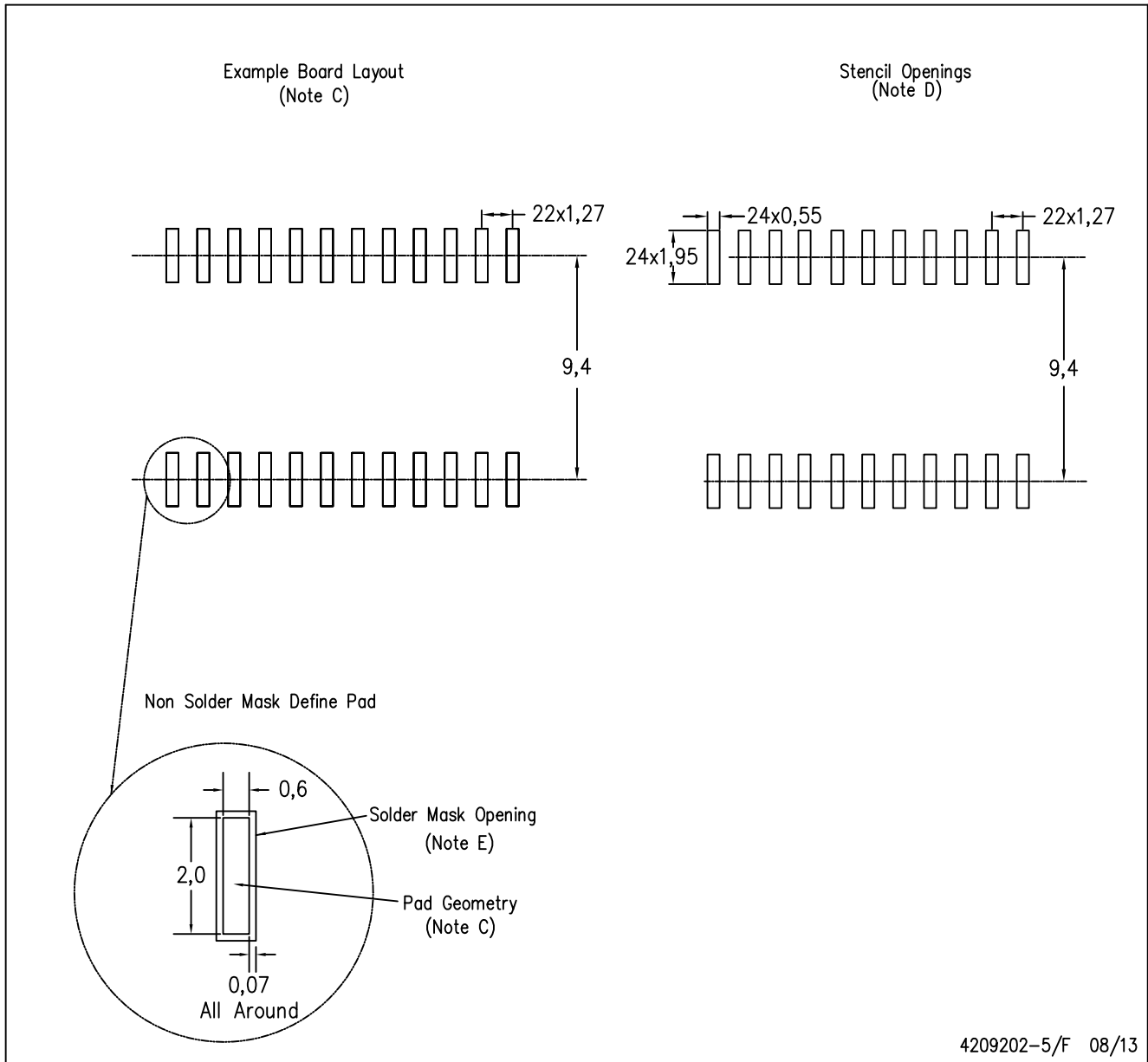
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated