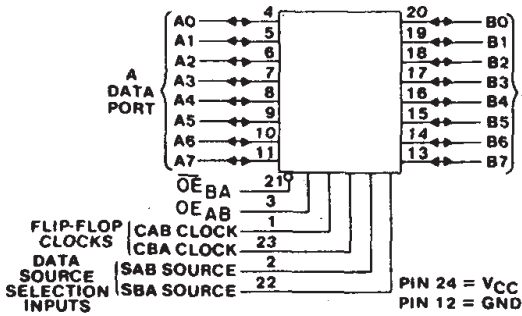


# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652



Data sheet acquired from Harris Semiconductor  
SCHS294



## Octal-Bus Transceiver/Registers, 3-State

CD54/74AC/ACT651 - Inverting  
CD54/74AC/ACT652 - Non-Inverting

### Type Features:

- Buffered inputs
- Typical propagation delay:  
5.3 ns @  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{ C}$ ,  $C_L = 50\text{ pF}$

FUNCTIONAL DIAGRAM

92CS-42677

The RCA CD54/74AC651 and CD54/74AC652 and the CD54/74ACT651 and CD54/74ACT652 3-state, octal-bus transceiver/registers use the RCA ADVANCED CMOS technology. The CD54/74AC651 and CD54/74ACT651 have inverting outputs. The CD54/74AC652 and CD54/74ACT652 have non-inverting outputs. These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Output Enables  $OE_{AB}$  and  $\overline{OE}_{BA}$  are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. A LOW input level selects real-time data, and a HIGH selects stored data. The following examples demonstrate the four fundamental bus-management functions that can be performed with the octal-bus transceivers and registers.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling  $OE_{AB}$  and  $\overline{OE}_{BA}$ . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

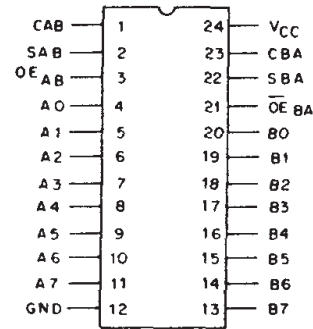
The CD74AC/ACT651 and CD74AC/ACT652 are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over the following temperature ranges: Commercial (0 to  $70^\circ\text{ C}$ ); Industrial ( $-40$  to  $+85^\circ\text{ C}$ ); and Extended Industrial/Military ( $-55$  to  $+125^\circ\text{ C}$ ).

The CD54AC/ACT651 and CD54AC/ACT652, available in chip form (H suffix), are operable over the  $-55$  to  $+125^\circ\text{ C}$  temperature range.

### Family Features:

- Exceeds 2-kV ESD Protection - MIL-STD-883, Method 3015
- SCR-Latchup-resistant CMOS process and circuit design
- Speed of bipolar FAST\*/AS/S with significantly reduced power consumption
- Balanced propagation delays
- AC types feature 1.5-V to 5.5-V operation and balanced noise immunity at 30% of the supply
- $\pm 24\text{-mA}$  output drive current
  - Fanout to 15 FAST\* ICs
  - Drives 50-ohm transmission lines

\*FAST is a Registered Trademark of Fairchild Semiconductor Corp.



92CS-42678

TERMINAL ASSIGNMENT

This data sheet is applicable to the CD74AC652, CD74ACT651, and CD74ACT652. The CD54/74AC651, CD54AC652, CD54ACT651, and CD54ACT652 were not acquired from Harris Semiconductor.

# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

FUNCTION TABLE

OE <sub>AB</sub> OE <sub>BA</sub>		INPUTS				DATA I/O		OPERATION OR FUNCTION	
		CAB	CBA	SAB	SBA	A0 THRU A7	B0 THRU B7	651	652
L	H	H or L	H or L	X	X	Input	Input	Isolation*	Isolation*
L	H			X	X	Input	Input	Store A and B Data	Store A and B Data
X	H		H or L	X	X	Input	Unspecified†	Store A, Hold B	Store A, Hold B
H	H			X‡	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L		X	X	Unspecified†	Input	Hold A, Store B	Hold, A Store B
L	L			X	X‡	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B̄ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B̄ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time Ā Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored Ā Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored Ā Data to B Bus and Stored B̄ Data to A bus	Stored A Data to B Bus Stored B Data to A Bus

\* To prevent excess currents in the High-Z (isolation) modes, all I/O terminals should be terminated with 10kΩ to 1MΩ resistors.

† The data output functions may be enabled or disabled by various signals at the OE<sub>AB</sub> or OE<sub>BA</sub> inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.  
Select control = H: clocks must be staggered in order to load both registers.

**MAXIMUM RATINGS, Absolute-Maximum Values:**

- DC SUPPLY-VOLTAGE (V<sub>CC</sub>) ..... -0.5 to 6 V
- DC INPUT DIODE CURRENT, I<sub>IK</sub> (for V<sub>I</sub> < -0.5 V or V<sub>I</sub> > V<sub>CC</sub> + 0.5 V) ..... ±20 mA
- DC OUTPUT DIODE CURRENT, I<sub>OK</sub> (for V<sub>O</sub> < -0.5 V or V<sub>O</sub> > V<sub>CC</sub> + 0.5 V) ..... ±50 mA
- DC OUTPUT SOURCE OR SINK CURRENT per Output Pin, I<sub>O</sub> (for V<sub>O</sub> > -0.5 V or V<sub>O</sub> < V<sub>CC</sub> + 0.5 V) ..... ±50 mA
- DC V<sub>CC</sub> or GROUND CURRENT (I<sub>CC</sub> or I<sub>GND</sub>) ..... ±100 mA\*
- POWER DISSIPATION PER PACKAGE (P<sub>D</sub>):
  - For T<sub>A</sub> = -55 to +100°C (PACKAGE TYPE E) ..... 500 mW
  - For T<sub>A</sub> = +100 to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8 mW/°C to 300 mW
  - For T<sub>A</sub> = -55 to +70°C (PACKAGE TYPE M) ..... 400 mW
  - For T<sub>A</sub> = +70 to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6 mW/°C to 70 mW
- OPERATING-TEMPERATURE RANGE (T<sub>A</sub>) ..... -55 to +125°C
- STORAGE TEMPERATURE (T<sub>stg</sub>) ..... -65 to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):
  - At distance 1/16 ± 1/32 in. (1.59 ± 0.79 mm) from case for 10 s maximum ..... +265°C
  - Unit inserted into PC board min. thickness 1/16 in. (1.59 mm) with solder contacting lead tips only ..... +300°C

\*For up to 4 outputs per device; add ± 25 mA for each additional output.

**RECOMMENDED OPERATING CONDITIONS:**

For maximum reliability, normal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTICS	LIMITS		UNITS
	MIN.	MAX.	
Supply-Voltage Range, V <sub>CC</sub> *: (For T <sub>A</sub> = Full Package-Temperature Range)			
AC Types	1.5	5.5	V
ACT Types	4.5	5.5	V
DC Input or Output Voltage, V <sub>I</sub> , V <sub>O</sub>	0	V <sub>CC</sub>	V
Operating Temperature, T <sub>A</sub>	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv			
at 1.5 V to 3 V (AC Types)	0	50	ns/V
at 3.6 V to 5.5 V (AC Types)	0	20	ns/V
at 4.5 V to 5.5 V (ACT Types)	0	10	ns/V

\*Unless otherwise specified, all voltages are referenced to ground.



# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

STATIC ELECTRICAL CHARACTERISTICS: AC Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage V <sub>IH</sub>			1.5	1.2	—	1.2	—	1.2	—	V	
			3	2.1	—	2.1	—	2.1	—		
			5.5	3.85	—	3.85	—	3.85	—		
Low-Level Input Voltage V <sub>IL</sub>			1.5	—	0.3	—	0.3	—	0.3	V	
			3	—	0.9	—	0.9	—	0.9		
			5.5	—	1.65	—	1.65	—	1.65		
High-Level Output Voltage V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, * }	-0.05	1.5	1.4	—	1.4	—	1.4	V	
			-0.05	3	2.9	—	2.9	—	2.9		
			-0.05	4.5	4.4	—	4.4	—	4.4		
			-4	3	2.58	—	2.48	—	2.4		
			-24	4.5	3.94	—	3.8	—	3.7		
			-75	5.5	—	—	3.85	—	—		
Low-Level Output Voltage V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub>	#, * }	0.05	1.5	—	0.1	—	0.1	—	V	
			0.05	3	—	0.1	—	0.1	—		
			0.05	4.5	—	0.1	—	0.1	—		
			12	3	—	0.36	—	0.44	—		0.5
			24	4.5	—	0.36	—	0.44	—		0.5
			75	5.5	—	—	—	1.65	—		—
Input Leakage Current I <sub>I</sub>	V <sub>CC</sub> or GND		5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current I <sub>OZ</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>CC</sub> or GND		5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI I <sub>CC</sub>	V <sub>CC</sub> or GND	0	5.5	—	8	—	80	—	160	μA	

#Test one output at a time for a 1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\* Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

STATIC ELECTRICAL CHARACTERISTICS: ACT Series

CHARACTERISTICS	TEST CONDITIONS		V <sub>cc</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C						UNITS	
				+25		-40 to +85		-55 to +125			
	V <sub>i</sub> (V)	I <sub>o</sub> (mA)		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
High-Level Input Voltage	V <sub>IH</sub>		4.5 to 5.5	2	—	2	—	2	—	V	
Low-Level Input Voltage	V <sub>IL</sub>		4.5 to 5.5	—	0.8	—	0.8	—	0.8	V	
High-Level Output Voltage	V <sub>OH</sub>	V <sub>IH</sub> or V <sub>IL</sub> #,*	-0.05	4.5	4.4	—	4.4	—	4.4	—	V
			-24	4.5	3.94	—	3.8	—	3.7	—	
			-75	5.5	—	—	3.85	—	—	—	
			-50	5.5	—	—	—	—	3.85	—	
Low-Level Output Voltage	V <sub>OL</sub>	V <sub>IH</sub> or V <sub>IL</sub> #,*	0.05	4.5	—	0.1	—	0.1	—	0.1	V
			24	4.5	—	0.36	—	0.44	—	0.5	
			75	5.5	—	—	—	1.65	—	—	
			50	5.5	—	—	—	—	—	1.65	
Input Leakage Current	I <sub>i</sub>	V <sub>cc</sub> or GND	5.5	—	±0.1	—	±1	—	±1	μA	
3-State Leakage Current	I <sub>oz</sub>	V <sub>IH</sub> or V <sub>IL</sub> V <sub>O</sub> = V <sub>cc</sub> or GND	5.5	—	±0.5	—	±5	—	±10	μA	
Quiescent Supply Current, MSI	I <sub>cc</sub>	V <sub>cc</sub> or GND	0	5.5	—	8	—	80	—	160	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High 1 Unit Load	ΔI <sub>cc</sub>	V <sub>cc</sub> -2.1	4.5 to 5.5	—	2.4	—	2.8	—	3	mA	

9

#Test one output at a time for a .1-second maximum duration. Measurement is made by forcing current and measuring voltage to minimize power dissipation.

\*Test verifies a minimum 50-ohm transmission-line-drive capability at +85°C, 75 ohms at +125°C.

**ACT INPUT LOADING TABLE**

INPUT	UNIT LOAD*
CAB, CBA	1.25
SAB, SBA	1.2
OE <sub>AB</sub>	0.67
OE <sub>BA</sub>	1.17
An, Bn	0.4

\*Unit load is ΔI<sub>cc</sub> limit specified in Static Characteristics Chart, e.g., 2.4 mA max. @ 25°C.

# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

PREREQUISITE FOR SWITCHING: AC Series

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f <sub>max</sub>	1.5	11	—	10	—	MHz
		3.3*	101	—	89	—	
		5†	143	—	125	—	
Setup Time Data to Clock	t <sub>SU</sub>	1.5	27	—	31	—	ns
		3.3	3.1	—	3.5	—	
		5	2.2	—	2.5	—	
Hold Time Data to Clock	t <sub>H</sub>	1.5	2	—	2	—	ns
		3.3	2	—	2	—	
		5	2	—	2	—	
Clock Pulse Data to Clock	t <sub>w</sub>	1.5	44	—	50	—	ns
		3.3	4.9	—	5.6	—	
		5	3.5	—	4	—	

\*3.3 V: min. is @ 3 V

†5 V: min. is @ 4.5 V

SWITCHING CHARACTERISTICS: AC Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus 652	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	154	—	169	ns
		3.3*	4.8	17.1	4.7	18.9	
		5†	3.5	12.3	3.4	13.5	
Store A Data to B Bus Store B Data to A Bus 651	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	154	—	169	ns
		3.3	4.8	17.1	4.7	18.9	
		5	3.5	12.3	3.4	13.5	
A Data to B Bus B Data to A Bus 652	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	125	—	138	ns
		3.3	4	14	3.9	15.4	
		5	2.8	10	2.8	11	
A Data to B Bus B Data to A Bus 651	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	125	—	138	ns
		3.3	4	14	3.9	15.4	
		5	2.8	10	2.8	11	
Select to Data 652	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
Select to Data 651	t <sub>PLH</sub> t <sub>PHL</sub>	1.5	—	136	—	150	ns
		3.3	4.3	15.3	4.2	16.8	
		5	3.1	10.9	3	12	
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	1.5	—	154	—	169	ns
		3.3	5.2	18.4	5.1	20.2	
		5	3.5	12.3	3.4	13.5	
Power Dissipation Capacitance	C <sub>PD</sub> §	—	150 Typ.		150 Typ.		pF
Min. (Valley) During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OH</sub> V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

\*3.3 V: min. is @ 3.6 V  
max. is @ 3 V

†5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per package.

$$P_D = V_{CC}^2 C_{PD} f_i + \sum (V_{CC}^2 C_{L} f_o) \text{ where } f_i = \text{input frequency}$$

$$f_o = \text{output frequency}$$

$$C_L = \text{output load capacitance}$$

$$V_{CC} = \text{supply voltage}$$

# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652

**PREREQUISITE FOR SWITCHING: ACT Series**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Max. Frequency	f <sub>max</sub>	5*	125	—	110	—	MHz
Setup Time Data to Clock	t <sub>SU</sub>	5	2.2	—	2.5	—	ns
Hold Time Data to Clock	t <sub>H</sub>	5	2	—	2	—	ns
Clock Pulse Width	t <sub>w</sub>	5	3.9	—	4.5	—	ns

\*5 V: min. is @ 4.5 V

**SWITCHING CHARACTERISTICS: ACT Series; t<sub>r</sub>, t<sub>f</sub> = 3 ns, C<sub>L</sub> = 50 pF**

CHARACTERISTICS	SYMBOL	V <sub>CC</sub> (V)	AMBIENT TEMPERATURE (T <sub>A</sub> ) - °C				UNITS
			-40 to +85		-55 to +125		
			MIN.	MAX.	MIN.	MAX.	
Propagation Delays: Store A Data to B Bus Store B Data to A Bus 652	t <sub>PLH</sub> t <sub>PHL</sub>	5*	4	14.1	3.9	15.5	ns
Store $\bar{A}$ Data to B Bus Store B Data to A Bus 651	t <sub>PLH</sub> t <sub>PHL</sub>	5	4	14.1	3.9	15.5	ns
A Data to B Bus B Data to A Bus 652	t <sub>PLH</sub> t <sub>PHL</sub>	5	3.2	11.4	3.1	12.5	ns
$\bar{A}$ Data to B Bus B Data to A Bus 651	t <sub>PLH</sub> t <sub>PHL</sub>	5	3.2	11.4	3.1	12.5	ns
Select to Data 652	t <sub>PLH</sub> t <sub>PHL</sub>	5	3.7	13.2	3.6	14.5	ns
Select to Data 651	t <sub>PLH</sub> t <sub>PHL</sub>	5	4	14.1	3.9	15.5	ns
3-State Enabling/ Disabling Time Bus to Output or Register to Output	t <sub>PZL</sub> t <sub>PZH</sub> t <sub>PLZ</sub> t <sub>PHZ</sub>	5	4	14.1	3.9	15.5	ns
Power Dissipation Capacitance	C <sub>PD</sub> §	—	150 Typ.		150 Typ.		pF
Min. (Valley) During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OH</sub> V <sub>OHV</sub> See Fig. 1	5	4 Typ. @ 25°C				V
Max. (Peak) During Switching of Other Outputs (Output Under Test Not Switching)	V <sub>OL</sub> V <sub>OLP</sub> See Fig. 1	5	1 Typ. @ 25°C				V
Input Capacitance	C <sub>I</sub>	—	—	10	—	10	pF
3-State Output Capacitance	C <sub>O</sub>	—	—	15	—	15	pF

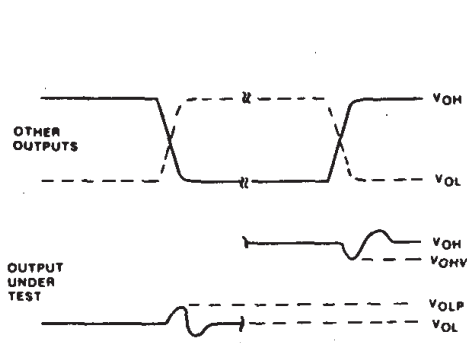
\*5 V: min. is @ 5.5 V  
max. is @ 4.5 V

§C<sub>PD</sub> is used to determine the dynamic power consumption, per package

$$P_D = V_{CC}^2 C_{PD} f_i + \sum V_{CC}^2 C_L f_o + V_{CC} \Delta I_{CC}$$

where f<sub>i</sub> = input frequency  
f<sub>o</sub> = output frequency  
C<sub>L</sub> = output load capacitance  
V<sub>CC</sub> = supply voltage.

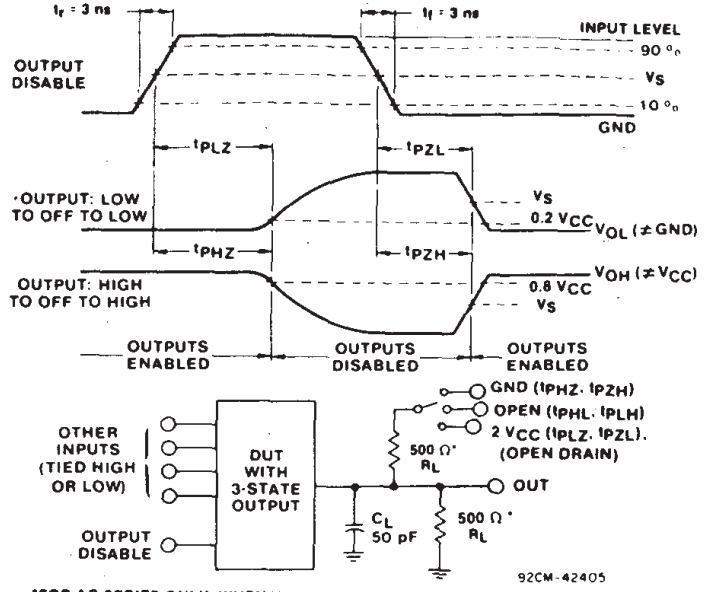
# CD54/74AC651, CD54/74AC652 CD54/74ACT651, CD54/74ACT652



- NOTES:
1.  $V_{OHV}$  AND  $V_{OLP}$  ARE MEASURED WITH RESPECT TO A GROUND REFERENCE NEAR THE OUTPUT UNDER TEST.
  2. INPUT PULSES HAVE THE FOLLOWING CHARACTERISTICS:  
PRR = 1 MHz,  $t_r = 3$  ns,  $t_f = 3$  ns, SKEW 1 ns.
  3. R.F. FIXTURE WITH 700-MHz DESIGN RULES REQUIRED. IC SHOULD BE SOLDERED INTO TEST BOARD AND BYPASSED WITH 0.1  $\mu$ F CAPACITOR. SCOPE AND PROBES REQUIRE 700-MHz BANDWIDTH.

92CS-42405

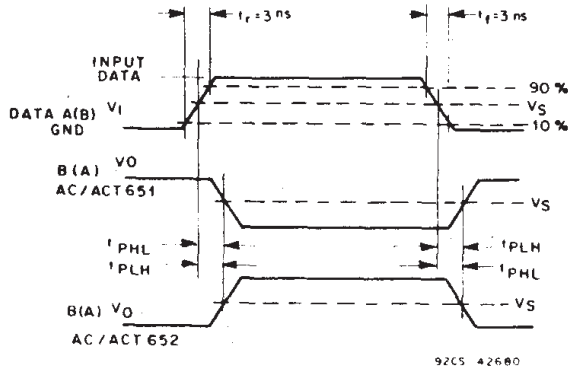
Fig. 1 - Simultaneous switching transient waveforms.



\*FOR AC SERIES ONLY: WHEN  $V_{CC} = 1.5$  V,  $R_L = 1$  k $\Omega$

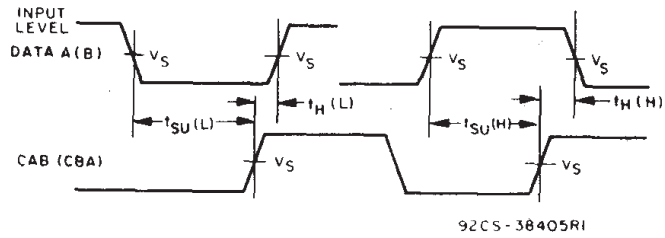
92CM-42405

Fig. 2 - Three-state propagation delay waveforms and test circuit.



92CS 42680

Fig. 3 - Propagation delay times.



92CS-38405R1

Fig. 4 - Data setup and hold times.

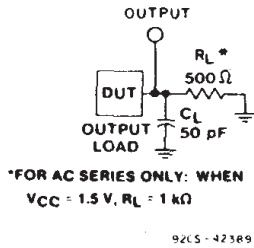


Fig. 5 - Test circuit.

	CD54/74AC	CD54/74ACT
Input Level	$V_{CC}$	3 V
Input Switching Voltage, $V_S$	$0.5 V_{CC}$	1.5 V
Output Switching Voltage, $V_S$	$0.5 V_{CC}$	$0.5 V_{CC}$



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74AC652M	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC652M	<a href="#">Samples</a>
CD74AC652M96	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	AC652M	<a href="#">Samples</a>
CD74ACT652M	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT652M	<a href="#">Samples</a>
CD74ACT652M96	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	ACT652M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74AC652M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74ACT652M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74AC652M96	SOIC	DW	24	2000	350.0	350.0	43.0
CD74ACT652M96	SOIC	DW	24	2000	350.0	350.0	43.0

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