CD74HC4051-EP Analog Multiplexer and Demultiplexer

1 Features

- Controlled Baseline
  - One Assembly and Test Site, One Fabrication Site
- Extended Temperature Performance of –55°C to 125°C
- Enhanced Diminishing Manufacturing Sources (DMS) Support
- Enhanced Product Change Notification
- Qualification Pedigree(1)
- Wide Analog Input Voltage Range of ±5 V Max
- Low ON-Resistance
  - 70 Ω Typical (V_{CC} – V_{EE} = 4.5 V)
  - 40 Ω Typical (V_{CC} – V_{EE} = 9 V)
- Low Crosstalk Between Switches
- Fast Switching and Propagation Speeds
- Break-Before-Make Switching
- Operation Control Voltage = 2 V to 6 V
- Switch Voltage = 0 V to 10 V
- High Noise Immunity N_{IL} = 30%, N_{IH} = 30% of V_{CC}, V_{CC} = 5 V (1)

2 Applications

Supports Defense and Aerospace Applications

(1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

3 Description

The CD74HC4051-EP is a digitally controlled analog switch that uses silicon gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

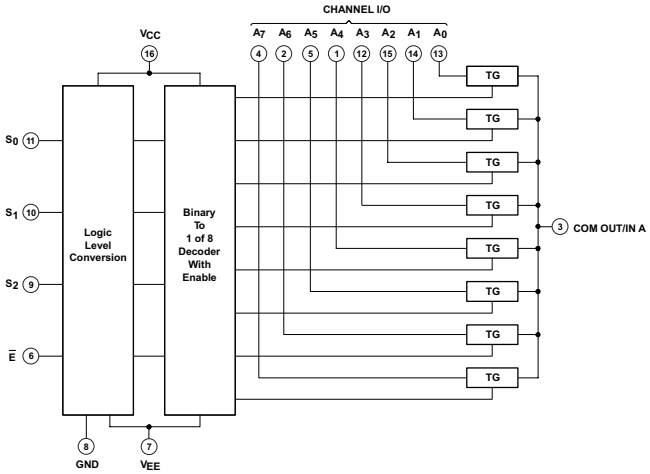
This analog multiplexer and demultiplexer controls analog voltages that may vary across the voltage supply range (that is, V_{CC} to V_{EE}). These bidirectional switches allow the use of any analog input as an output and vice versa. The switches have low ON-resistance and low OFF leakages. In addition, the device has an enable control ($\overline{E}$) that, when high, disables all switches to their OFF state.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
CD74HC4051-EP	SOIC (16)	4.00 mm × 10.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Functional Block Diagram



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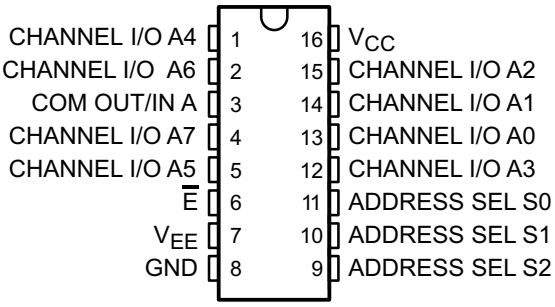
4 Revision History

Changes from Original (September 2002) to Revision A	Page
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging*, and *Orderable Information* section.	1

5 Pin Configuration And Functions

D Package
16-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A4	1	I/O	Channel 4 input / output
A6	2	I/O	Channel 6 Input / output
A	3	I/O	COM OUT/ IN
A7	4	I/O	Channel 7 Input / Output
A5	5	I/O	Channel 5 Input / Output
Ebar	6	I	Enable input
VEE	7	I	Power input level for incoming Channel
GND	8	I	Power GND
VCC	9	I	Power input level for outgoing Channel
A2	10	I/O	Channel 2 Input / Output
A1	11	I/O	Channel 1 Input / Output
A0	12	I/O	Channel 0 Input / Output
A3	13	I/O	Channel 3 Input / Output
S0	14	I	Address Select Input 0
S1	15	I	Address Select Input 1
S2	15	I	Address Select Input 2

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
$V_{CC} - V_{EE}$ (2)	Supply voltage	–0.5	10.5	V
V_{CC}		–0.5	7	
V_{EE}		0.5	–7	
I_{IK}	Input clamp current ($V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V)	–20	20	mA
I_{OK}	Output clamp current ($V_O < V_{EE} – 0.5$ V or $V_O > V_{CC} + 0.5$ V)	–20	20	mA
	Switch current ($V_I > V_{EE} – 0.5$ V or $V_I < V_{CC} + 0.5$ V)	–25	25	mA
	Continuous current through V_{CC} or GND	–50	50	mA
I_{EE}	V_{EE} current	0	20	mA
θ_{JA}	Package thermal impedance (3)		73	°C/W
T_J	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages referenced to GND unless otherwise specified.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions (1)

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (2)		2	6	6	V
	Supply voltage, $V_{CC} – V_{EE}$ (see Figure 4)		2	10	10	V
V_{EE}	Supply voltage, (see (2) and Figure 5)		0	–6	–6	V
V_{IH}	High-level input voltage	VCC = 2 V	1.5			V
		VCC = 4.5 V	3.15			
		VCC = 6 V	4.2			
V_{IL}	Low-level input voltage	VCC = 2 V			0.5	V
		VCC = 4.5 V			1.35	
		VCC = 6 V			1.8	
V_I	Input control voltage		0		V_{CC}	V
V_{IS}	Analog switch I/O voltage		V_{EE}		V_{CC}	V
t_t	Input transition (rise and fall) time	VCC = 2 V	0		1000	ns
		VCC = 4.5 V	0		500	
		VCC = 6 V	0		400	

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.
(2) In certain applications, the external load resistor current may include both V_{CC} and signal-line components. To avoid drawing V_{CC} current when switch current flows into the transmission gate inputs, the voltage drop across the bidirectional switch must not exceed 0.6 V (calculated from r_{on} values shown in Electrical Characteristics table). No V_{CC} current flows through R_L if the switch current flows into the COM OUT/IN A terminal.

Recommended Operating Conditions(1) (continued)

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating free-air temperature	–55		125	°C
C_{pd}	Power dissipation capacitance(3)		50		pF

(3) C_{pd} is used to determine the dynamic power consumption, per package.
$P_D = C_{pd} V_{CC}^2 f_I + \Sigma (C_L + C_S) V_{CC}^2 f_O$
f_O = output frequency
f_I = input frequency
C_L = output load capacitance
C_S = switch capacitance
V_{CC} = supply voltage

6.4 Thermal Information

THERMAL METRIC(1)		CD74HC4051-EP D (SOIC) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	81.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	43.1	
$R_{\theta JB}$	Junction-to-board thermal resistance	39.2	
ψ_{JT}	Junction-to-top characterization parameter	10.7	
ψ_{JB}	Junction-to-board characterization parameter	38.9	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V_{EE}	V_{CC}	T_A = 25°C			T_A = –55°C to 125°C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
r_{on}	I_O = 1 mA, V_I = V_{IH} or V_{IL}, See Figure 1	V_{IS} = V_{CC} or V_{EE}	0 V	4.5 V		70	160			240	Ω
			0 V	6 V		60	140			210	
			–4.5 V	4.5 V		40	120			180	
		V_{IS} = V_{CC} to V_{EE}	0 V	4.5 V		90	180			270	
			0 V	6 V		80	160			240	
			–4.5 V	4.5 V		45	130			195	
Δr_{on}	Between any two channels		0 V	4.5 V		10					Ω
			0 V	6 V		8.5					
			–4.5 V	4.5 V		5					
I_{IZ}	For switch OFF: When V_{IS} = V_{CC}, V_{OS} = V_{EE}; When V_{IS} = V_{EE}, V_{OS} = V_{CC} For switch ON: All applicable combinations of V_{IS} and V_{OS} voltage levels, V_I = V_{IH} or V_{IL}		0 V	6 V			±0.2			±2	µA
			–5 V	5 V			±0.4			±4	
I_{IL}	V_I = V_{CC} or GND		0 V	6 V			±0.1			±1	µA
I_{CC}	I_O = 0, V_I = V_{CC} or GND	When V_{IS} = V_{EE}, V_{OS} = V_{CC}	0 V	6 V			8			160	µA
		When V_{IS} = V_{CC}, V_{OS} = V_{EE}	–5 V	5 V			16			320	

6.6 Analog Channel Characteristics

T_A = 25°C

PARAMETER		TEST CONDITIONS	V_{EE}	V_{CC}	MIN	TYP	MAX	UNIT
C_I	Switch input capacitance					5		pF
C_{COM}	Common output capacitance					25		pF
f_{max}	Minimum switch frequency response at –3 dB	See Figure 6, Figure 2, and (1)(2)	–2.25 V	2.25 V		145		MHz
			–4.5 V	4.5 V		180		
	Sine-wave distortion	See Figure 7	–2.25 V	2.25 V		0.03%		
			–4.5 V	4.5 V		0.018%		
	Switch OFF signal feedthrough	See Figure 8, Figure 3 and (2)(3)	–2.25 V	2.25 V		–73		dB
			–4.5 V	4.5 V		–75		

(1) Adjust input voltage to obtain 0 dBm at V_{OS} for f_{IN} = 1 MHz.
(2) V_{IS} is centered at (V_{CC} – V_{EE})/2.
(3) Adjust input for 0 dBm

6.7 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 9)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{EE}	V_{CC}	T_A = 25°C			T_A = –55°C TO 125°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
t_{pd}	IN	OUT	C_L = 15 pF		5 V			4				ns
			C_L = 50 pF	0 V	2 V			60			90	
					4.5 V			12			18	
					6 V			10			15	
				–4.5 V	4.5 V			8			12	
t_{en}	ADDRESS SEL or $\overline{E}$	OUT	C_L = 15 pF		5 V			19				ns
			C_L = 50 pF	0 V	2 V			225			340	
					4.5 V			45			68	
					6 V			38			57	
				–4.5 V	4.5 V			32			48	
t_{dis}	ADDRESS SEL or $\overline{E}$	OUT	C_L = 15 pF		5 V			19				ns
			C_L = 50 pF	0 V	2 V			225			340	
					4.5 V			45			68	
					6 V			38			57	
				–4.5 V	4.5 V			32			48	
C_I	Control		C_L = 50 pF					10			10	pF

6.8 Typical Characteristics

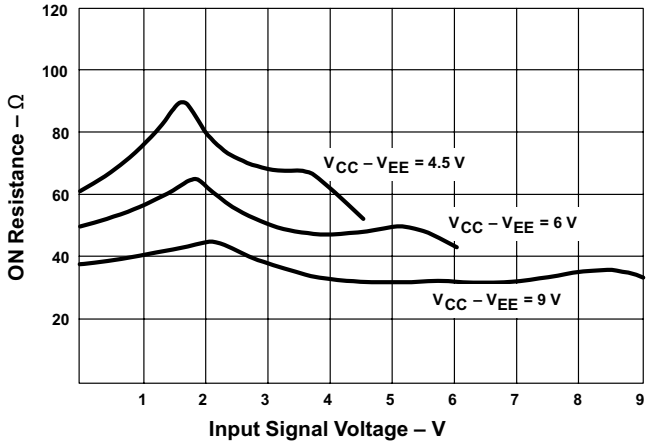


Figure 1. Typical ON-Resistance vs Input Signal Voltage

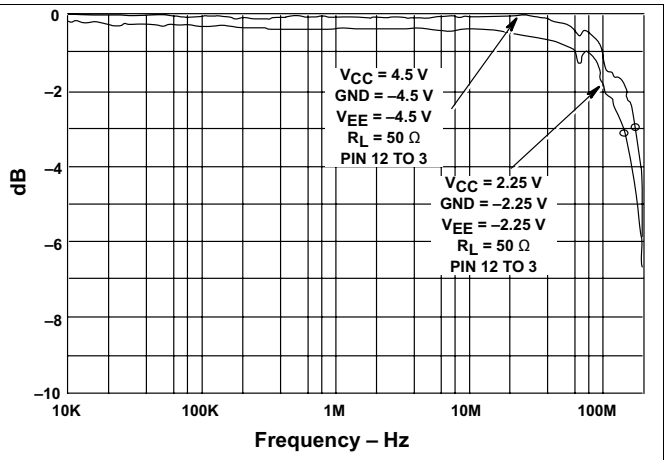


Figure 2. Channel On Bandwidth

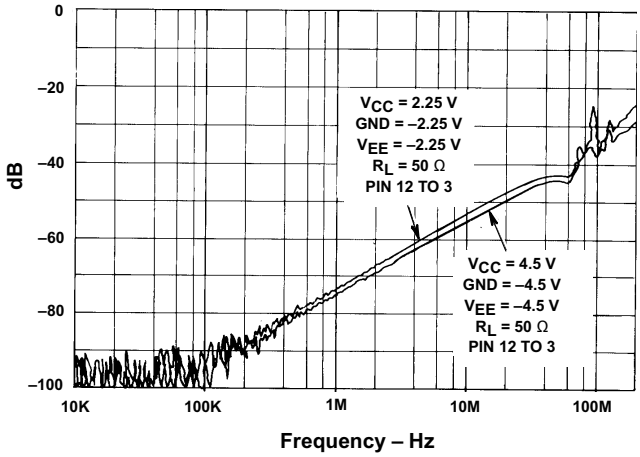


Figure 3. Channel Off Feedthrough

6.8.1 Recommended Operating Area as a Function of Supply Voltages

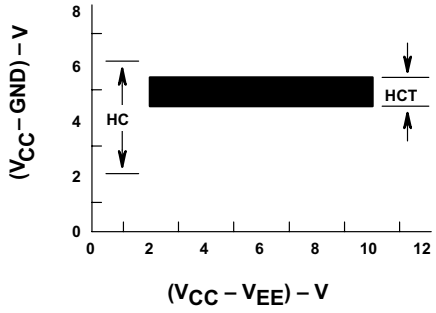


Figure 4. Supply Operating Region

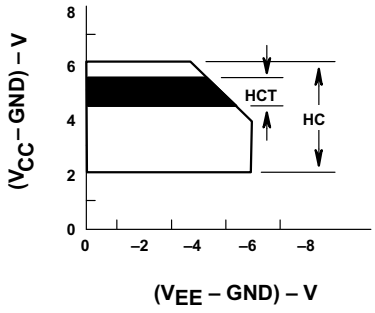


Figure 5. Supply Operating Region

7 Parameter Measurement Information

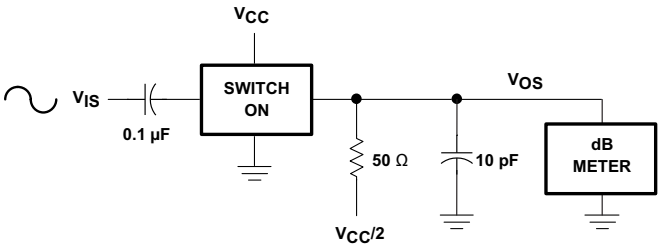


Figure 6. Frequency-Response Test Circuit

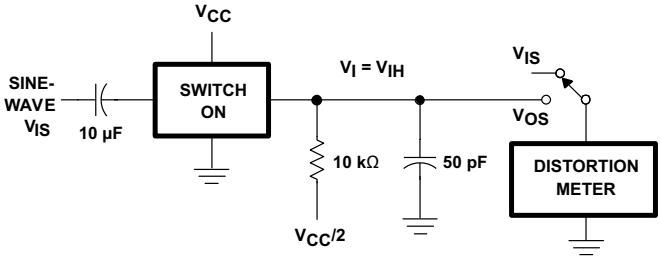


Figure 7. Sine-Wave Distortion Test Circuit

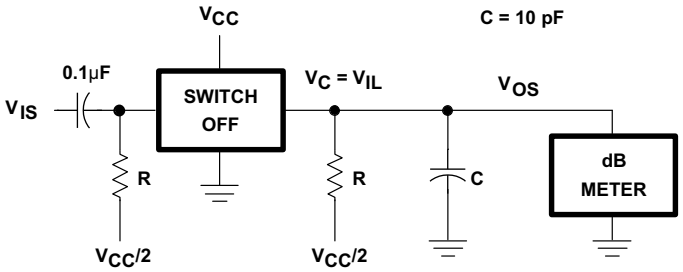
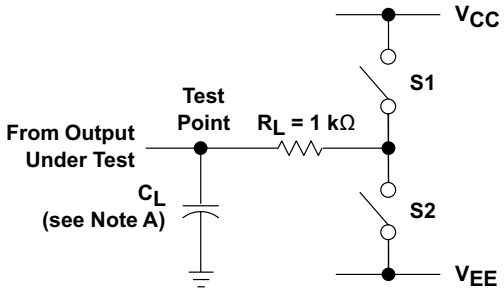


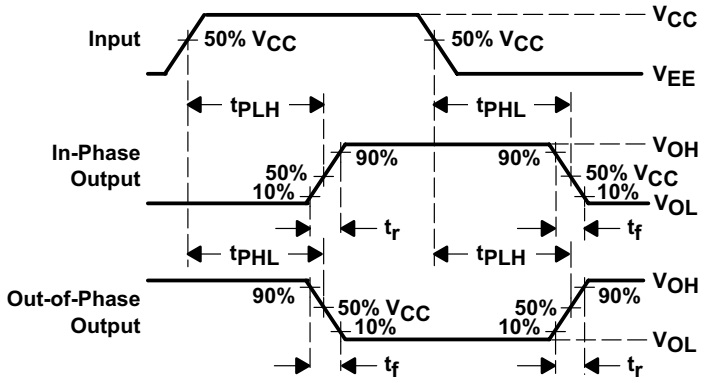
Figure 8. Switch OFF Signal Feedthrough Test Circuit

Parameter Measurement Information (continued)

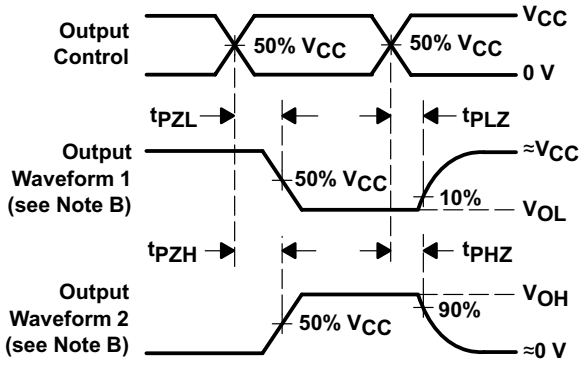


LOAD CIRCUIT

PARAMETER		S1	S2
t_{en}	t_{PZH}	Open	Closed
	t_{PZL}	Closed	Open
t_{dis}	t_{PHZ}	Open	Closed
	t_{PLZ}	Closed	Open
t_{pd}		Open	Open



VOLTAGE WAVEFORMS
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS
OUTPUT ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and test-fixture capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_r = 6 ns, t_f = 6 ns.
D. For clock inputs, f_{max} is measured with the input duty cycle at 50%.
E. The outputs are measured one at a time with one input transition per measurement.
F. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
G. t_{PZL} and t_{PZH} are the same as t_{en}.
H. t_{PLH} and t_{PHL} are the same as t_{pd}.

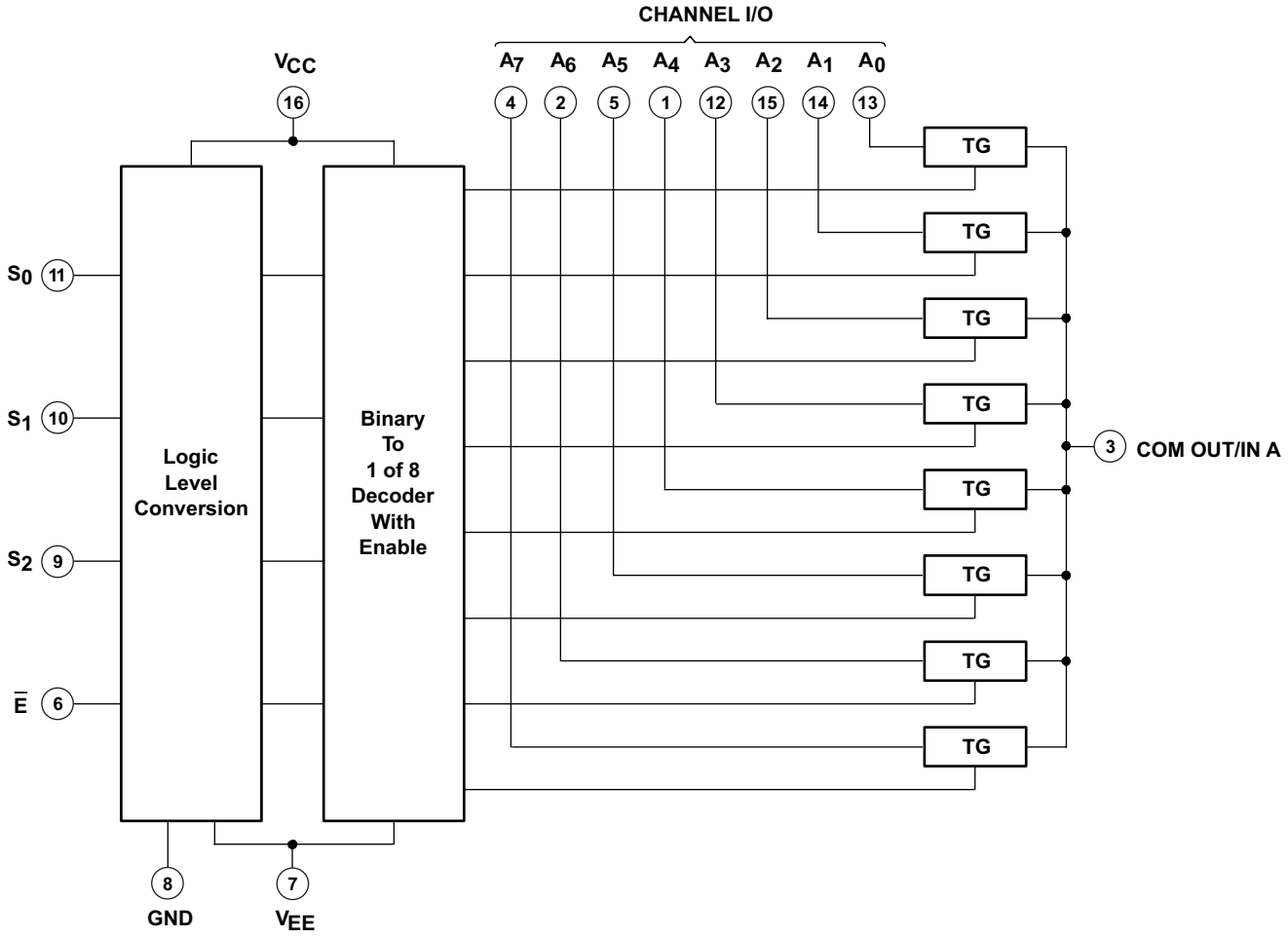
Figure 9. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

The CD74HC4051-EP is a digitally controlled analog switch that uses silicon gate CMOS technology to achieve operating speeds similar to LSTTL, with the low-power consumption of standard CMOS integrated circuits.

8.2 Functional Block Diagram



8.3 Feature Description

This analog multiplexer and demultiplexer controls analog voltages that may vary across the voltage supply range (that is, VCC to VEE). These bidirectional switches allow the use of any analog input as an output and vice versa. The switches have low ON-resistance and low OFF leakages. In addition, the device has an enable control (E) that, when high, disables all switches to their OFF state.

8.4 Device Functional Modes

Table 1. Function Table

INPUTS				ON CHANNEL (S)
E	S2	S1	S0	
L	L	L	L	A0
L	L	L	H	A1
L	L	H	L	A2
L	L	H	H	A3
L	H	L	L	A4
L	H	L	H	A5
L	H	H	L	A6
L	H	H	H	A7
H	X	X	X	None

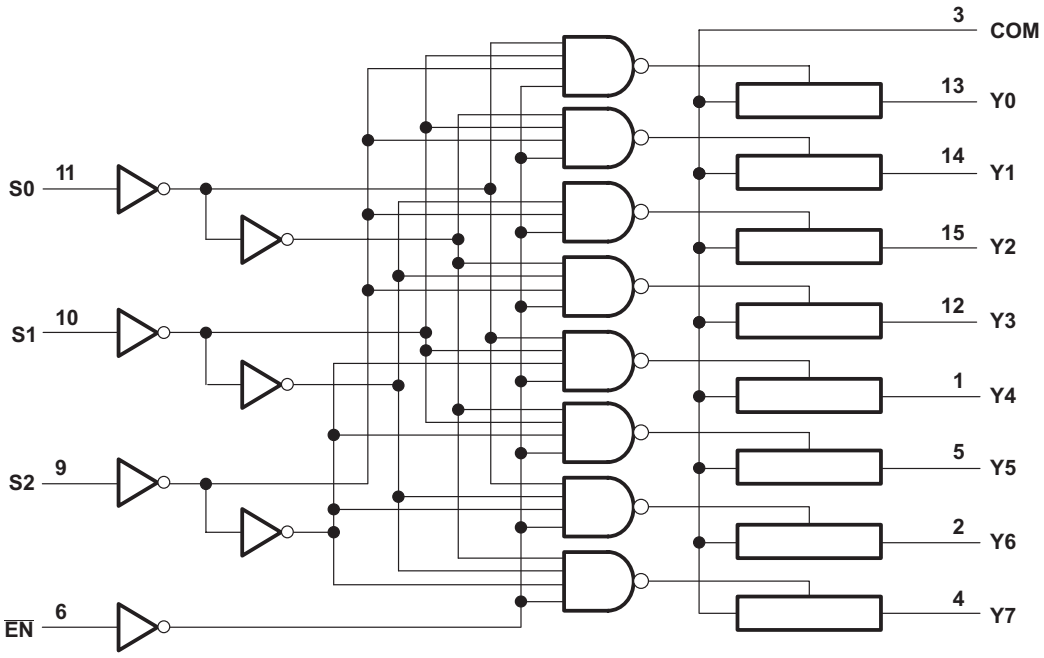


Figure 10. Logic Diagram (Positive Logic)

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 TTL-to-HC Interface

TTL output voltages and HC input voltages are incompatible, especially between the TTL high-level output voltage (V_{OH}) and the HC high-level input voltage (V_{IH}). This problem can be solved in two different ways. The first solution is to provide pullup resistors at the TTL outputs to ensure an adequate high-level TTL output voltage. A alternative method requires the use of level shifters.

9.2 Typical Application

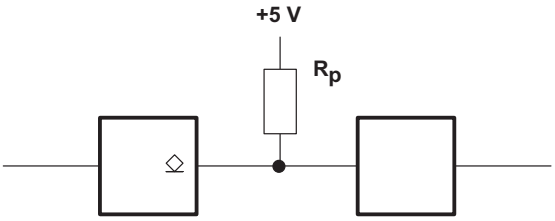


Figure 11. Typical Application Schematic TTL-to-HC Interface Using Open-Collector Output.

9.2.1 Design Requirements

Interfacing TTL open-collector outputs to HC-CMOS inputs requires design of pullup circuit balanced with drive capability to achieve timing and VOL-HC input specifications. Similar technique can be applied when using open-drain outputs.

9.2.2 Detailed Design Procedure

Using pullup resistors to accommodate TTL output signals to interface with HC input circuits (see Figure 11), the design engineer must choose the resistance that is appropriate for the application. The minimum value of the resistor is determined by the maximum current I_{OL} that a TTL circuit can supply at the low-level output (V_{OL}).

$$R_p\,\text{min} = \frac{V_{CC}\,\text{max} - V_{OL}\,\text{min}}{I_{OL} + n \times I_{IL}} \quad (1)$$

where

- n is the number of HC inputs to be driven
- I_{IL} is their input current

I_{IL}, having a value of only a few nanoamperes, is negligible in all calculations.

In the case of a SN74ALS03, Equation 2 defines $R_p$min:

$$R_p\,\text{min} = \frac{5.5\text{V} - 0.4\text{V}}{8\text{mA}} = 640\Omega \quad (2)$$

To calculate the upper limit of this resistor, a sufficient V_{IH} high level must be ensured.

$$R_p\,\text{max} = \frac{V_{CC} - V_{IH}\,\text{min}}{n \times I_{IH}} \quad (3)$$

In this situation, the input current of HC devices is negligible and very high values also are obtained.

Typical Application (continued)

When calculating the maximum allowable resistance, it is important to ensure that the maximum allowable rise time (t_r = 500 ns) at the HC input is not exceeded. Equation 4 then applies:

$$V_{IH} = V_{CC}(1 - e^{\frac{-t}{R_p \times C}})$$

where

- C is the total load capacitance in the circuit (4)

C is composed of the output capacitance of the driving gate (approximately 10 pF), the total input capacitances of gates to be driven (approximately 5 pF each), and the line capacitance (approximately 1 pF/cm). The actual value is calculated by solving the equation for R_p:

$$R_p = \frac{-t}{C \times \ln(1 - \frac{3.5V}{5V})} \quad (5)$$

Assuming the total capacitance, C, is 30 pF, the maximum resistor is:

$$R_p = \frac{-500ns}{30pF \times \ln(1 - \frac{3.5V}{5V})} = 14k\Omega \quad (6)$$

Faster rise times result in lower impedance and more power consumption. The previous calculation is based on the assumption that the driving gate has an open collector. Conditions become more satisfactory, however, when a gate with totem-pole output (that is, SN74ALS00) is used. In that case, the gate output provides the voltage to be brought up to the value V_{OH} = 2.7 V in less than 10 ns (the rise time of the TTL signal). The pullup resistor only has to pull the level to 3.5 V within the desired time. According to the previous formula, and with a required rise time of t_r = 50 ns, the resistor is defined by Equation 7:

$$R_p\,max = \frac{-50ns - 10ns}{30pF \times \ln(1 - \frac{3.5V - 2.7V}{5V - 2.7V})} = 3.12k\Omega \quad (7)$$

The upper limiting value of the resistor is primarily dictated by the rise time required. The larger the resistance, the longer the rise times and propagation delay times. Reducing the resistance increases speed and power dissipation.

The other method of accommodating TTL signals to HC circuits is accomplished with special level shifters. This solution is not recommended because the level shifter itself has no inherent logic functions and increases component and space requirements.

Typical Application (continued)

9.2.3 Application Curves

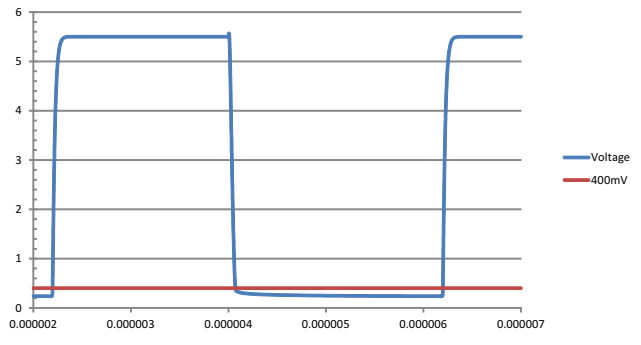


Figure 12. VOH VOL 640-Ω Pullup 8-mA Open Collector

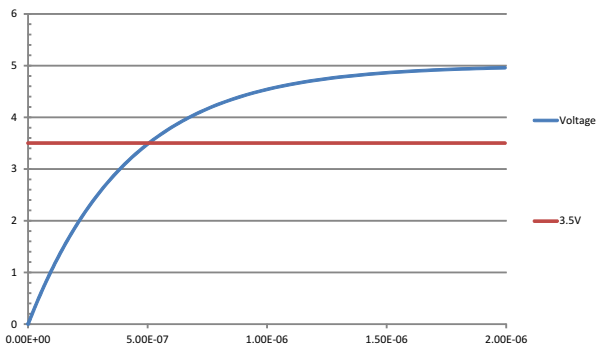


Figure 13. VOH 14-kΩ Pullup 500-ns Max Rise

10 Power Supply Recommendations

The threshold voltage of a CMOS circuit is determined by the geometry of the input transistors. These transistors are designed to sink the same input current at the required threshold voltage. The resulting voltage at the output is equivalent to 50% of the supply voltage V_{CC}. For an HC circuit, the channel width of the P-channel transistor of the input is approximately twice the value of an N-channel transistor. The purpose is to make both transistors have the same current characteristics, thus making the threshold voltage of their input at about 50% of the supply voltage V_{CC}.

11 Layout

11.1 Layout Guidelines

Analog channels inputs and outputs should be routed to optimize system requirements. VCC and VEE should have local decoupling capacitance placed close to device. Typical Cin values are 100 pF and 0.01 uF per supply pin.

11.2 Layout Example

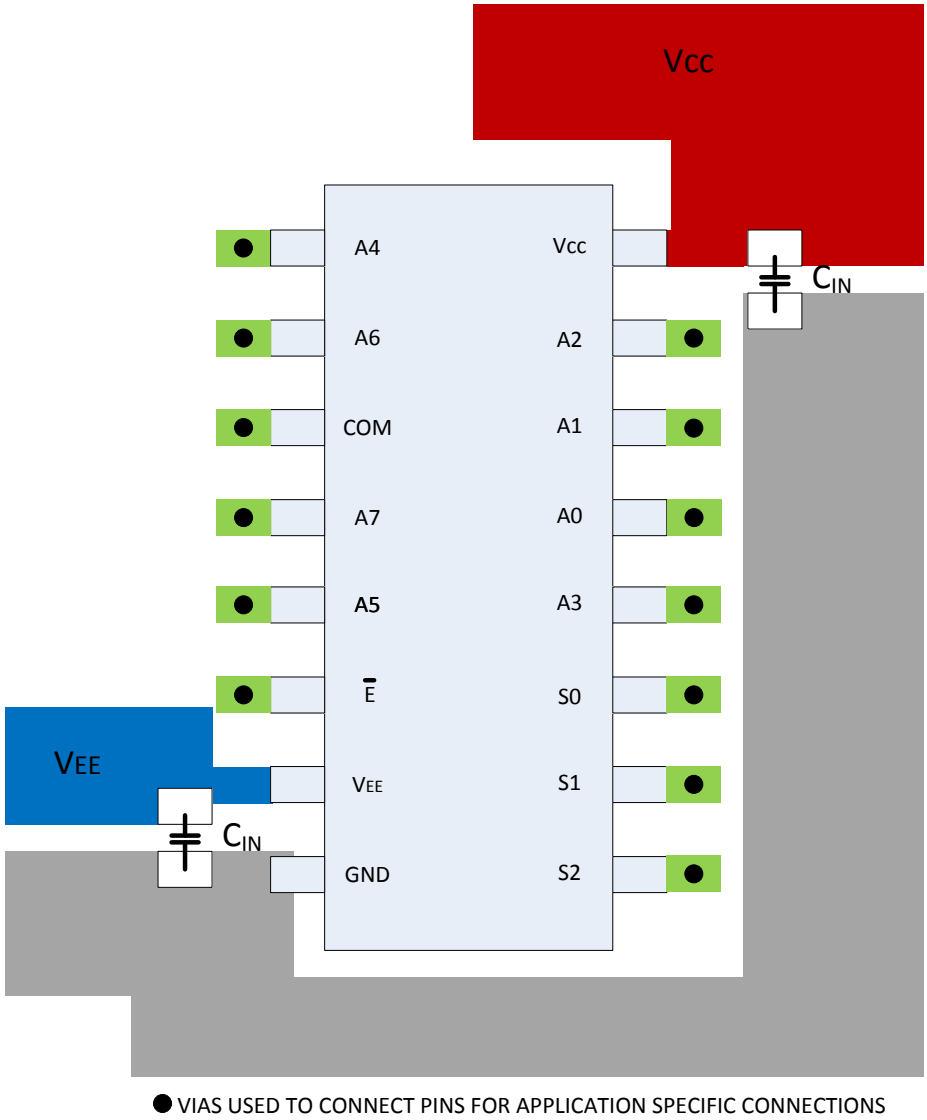


Figure 14. Layout Example

12 Device And Documentation Support

12.1 Trademarks

All trademarks are the property of their respective owners.

12.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.3 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4051MM96EP	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051MEP	Samples
V62/03606-01XE	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4051MEP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF CD74HC4051-EP :

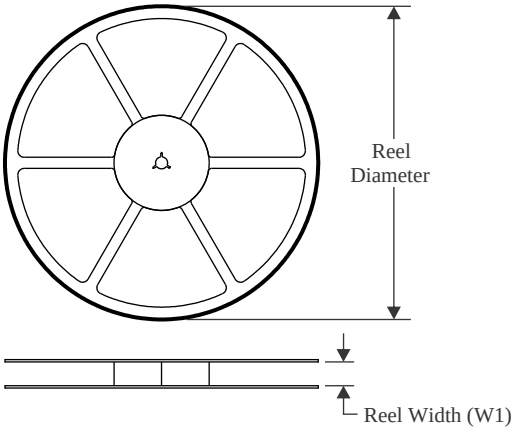
- Catalog: CD74HC4051
- Automotive: CD74HC4051-Q1
- Military: CD54HC4051

NOTE: Qualified Version Definitions:

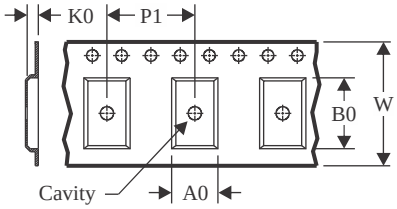
- Catalog - TI's standard catalog product
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

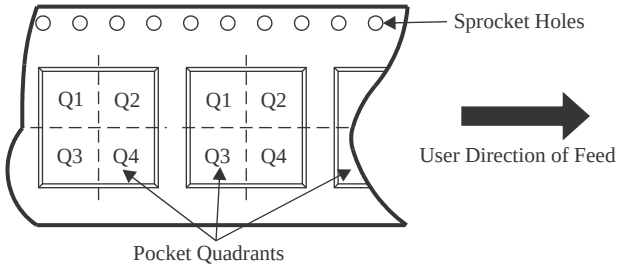


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

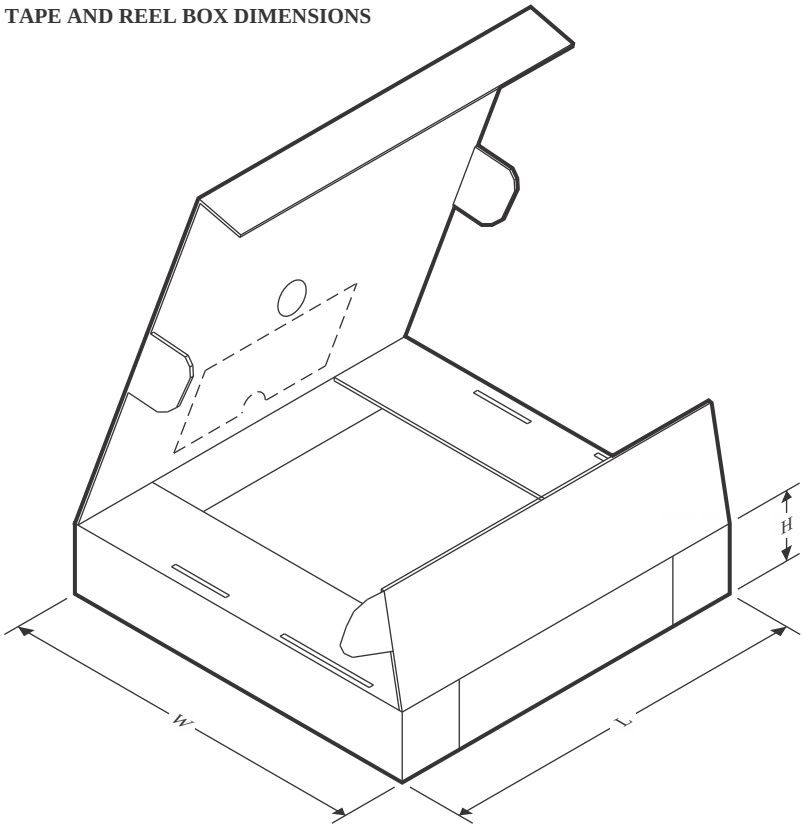
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4051MM96EP	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

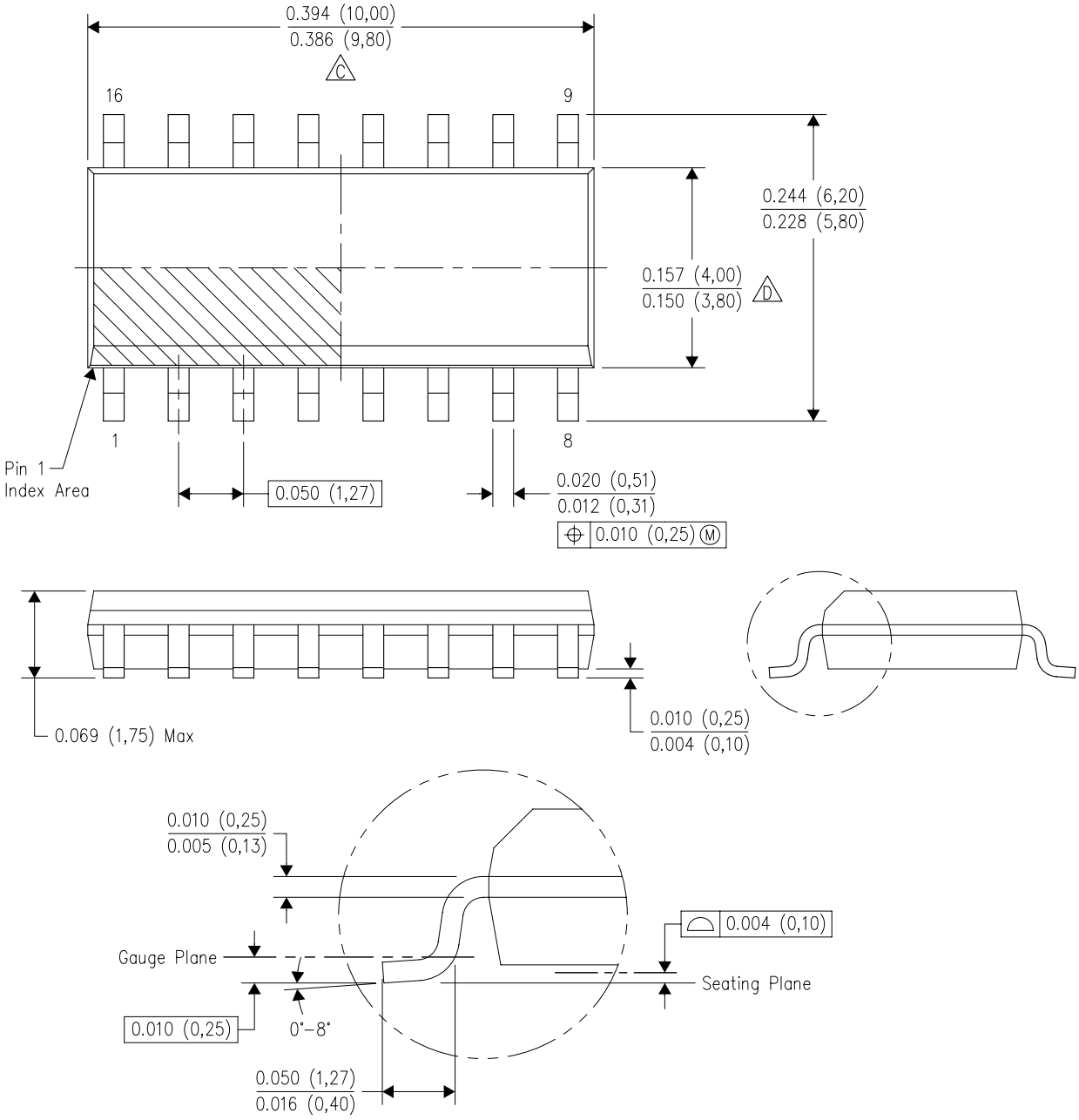
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

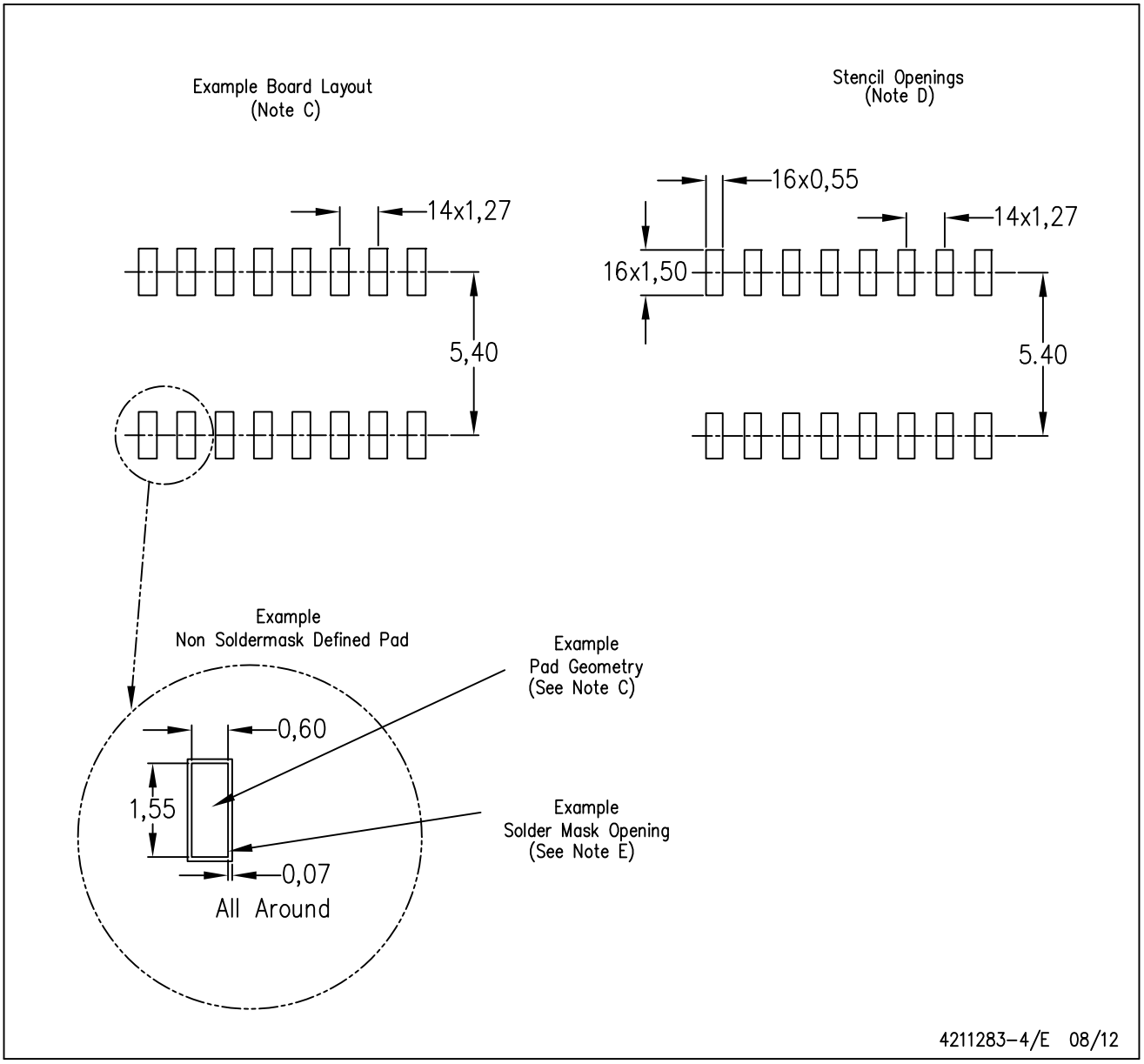
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4051MM96EP	SOIC	D	16	2500	333.2	345.9	28.6

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265