

## High-Speed CMOS Logic 16-Channel Analog Multiplexer/Demultiplexer

### Features

- **Wide Analog Input Voltage Range**
- **Low "ON" Resistance**
  - $V_{CC} = 4.5V$  ..... **70Ω (Typ)**
  - $V_{CC} = 6V$  ..... **60Ω (Typ)**
- **Fast Switching and Propagation Speeds**
- **"Break-Before-Make" Switching. . . . 6ns (Typ) at 4.5V**
- **Available in Both Narrow and Wide-Body Plastic Packages**
- **Fanout (Over Temperature Range)**
  - Standard Outputs . . . . . **10 LSTTL Loads**
  - Bus Driver Outputs . . . . . **15 LSTTL Loads**
- **Wide Operating Temperature Range . . . -55°C to 125°C**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HC Types**
  - **2V to 6V Operation**
  - **High Noise Immunity:  $N_{IL} = 30%$ ,  $N_{IH} = 30%$  of  $V_{CC}$  at  $V_{CC} = 5V$**
- **HCT Types**
  - **4.5V to 5.5V Operation**
  - **Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8V$  (Max),  $V_{IH} = 2V$  (Min)**
  - **CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$**

### Description

The CD74HC4067 and CD74HCT4067 devices are digitally controlled analog switches that utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

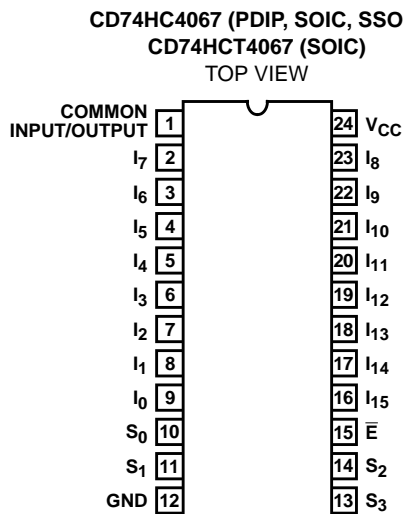
These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range. They are bidirectional switches thus allowing any analog input to be used as an output and vice-versa. The switches have low "on" resistance and low "off" leakages. In addition, these devices have an enable control which when high will disable all switches to their "off" state.

### Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC4067E	-55 to 125	24 Ld PDIP
CD74HC4067M	-55 to 125	24 Ld SOIC
CD74HC4067M96	-55 to 125	24 Ld SOIC
CD74HC4067SM96	-55 to 125	24 Ld SSOP
CD74HCT4067M	-55 to 125	24 Ld SOIC

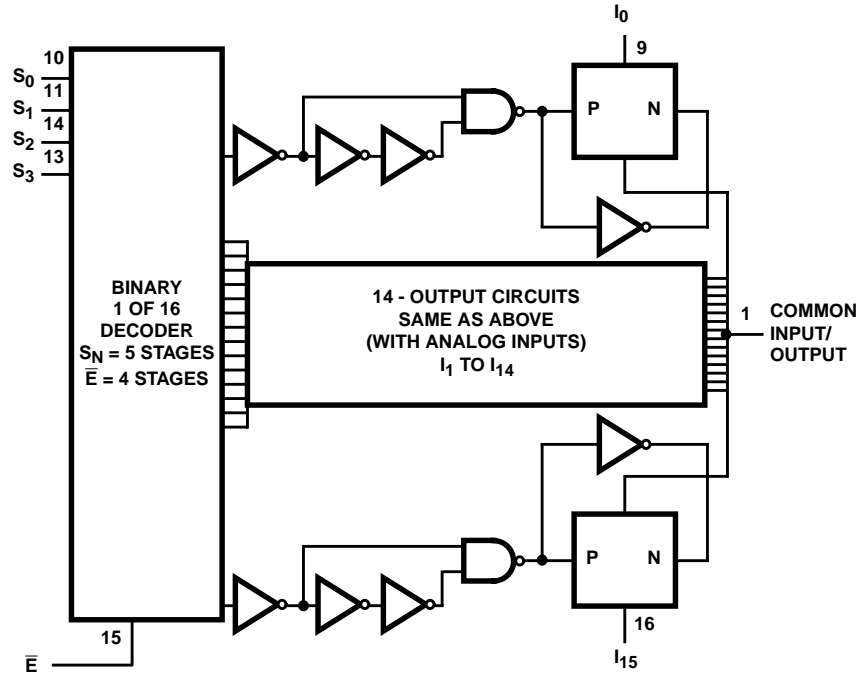
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

### Pinout



CD74HC4067, CD74HCT4067

Functional Diagram



TRUTH TABLE

S <sub>0</sub>	S <sub>1</sub>	S <sub>2</sub>	S <sub>3</sub>	E-bar	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

H= High Level  
 L= Low Level  
 X= Don't Care

# CD74HC4067, CD74HCT4067

## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$ (Voltages Referenced to Ground) .....	-0.5V to 7V
DC Input Diode Current, $I_{IK}$ For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Drain Current, $I_O$ For $-0.5V < V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC Output Diode Current, $I_{OK}$ For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$ .....	$\pm 20mA$
DC Output Source or Sink Current per Output Pin, $I_O$ For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$ .....	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$ .....	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical)	$\theta_{JA}$ ( $^{\circ}C/W$ )
E (PDIP) Package, Note 1 .....	67
M (SOIC) Package, Note 2 .....	46
SM (SSOP) Package, Note 2 .....	63
Maximum Junction Temperature (Plastic Package) .....	150 $^{\circ}C$
Maximum Storage Temperature Range .....	-65 $^{\circ}C$ to 150 $^{\circ}C$

## Operating Conditions

Temperature Range, $T_A$ .....	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	
HC Types .....	.2V to 6V
HCT Types .....	4.5V to 5.5V
DC Input or Output Voltage, $V_I, V_O$ .....	0V to $V_{CC}$
Input Rise and Fall Time	
2V .....	1000ns (Max)
4.5V .....	500ns (Max)
6V .....	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTES:

1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$V_{IS}$ (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>												
High Level Input Voltage	$V_{IH}$	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
Maximum "ON" Resistance $I_O = 1mA$	$R_{ON}$	$V_{CC}$ or GND	$V_{CC}$ or GND	4.5	-	70	160	-	200	-	240	$\Omega$
				6	-	60	140	-	175	-	210	$\Omega$
		$V_{CC}$ to GND	$V_{CC}$ to GND	4.5	-	90	180	-	225	-	270	$\Omega$
				6	-	80	160	-	200	-	240	$\Omega$
Maximum "ON" Resistance Between Any Two Switches	$\Delta R_{ON}$	-	-	4.5	-	10	-	-	-	-	-	$\Omega$
				6	-	8.5	-	-	-	-	-	$\Omega$
Switch "Off" Leakage Current 16 Channels	$I_{IZ}$	$\bar{E} = V_{CC}$	$V_{CC}$ or GND	6	-	-	$\pm 0.8$	-	$\pm 8$	-	$\pm 8$	$\mu A$
Logic Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$

## CD74HC4067, CD74HCT4067

### DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V <sub>I</sub> (V)	V <sub>IS</sub> (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current I <sub>O</sub> = 0mA	I <sub>CC</sub>	V <sub>CC</sub> or GND	-	6	-	-	8	-	80	-	160	μA
<b>HCT TYPES</b>												
High Level Input Voltage	V <sub>IH</sub>	-	-	4.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V <sub>IL</sub>	-	-	4.5	-	-	0.8	-	0.8	-	0.8	V
Maximum "ON" Resistance I <sub>O</sub> = 1mA	R <sub>ON</sub>	V <sub>CC</sub> or GND	V <sub>CC</sub> or GND	4.5	-	70	160	-	200	-	240	Ω
		V <sub>CC</sub> to GND	V <sub>CC</sub> to GND	4.5	-	90	180	-	225	-	270	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR <sub>ON</sub>	-	-	4.5	-	10	-	-	-	-	-	Ω
Switch "Off" Leakage Current 16 Channels	I <sub>Iz</sub>	$\bar{E} = V_{CC}$	V <sub>CC</sub> or GND	6	-	-	±0.8	-	±8	-	±8	μA
Logic Input Leakage Current	I <sub>I</sub>	V <sub>CC</sub> or GND (Note 3)	-	6	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	I <sub>CC</sub>	V <sub>CC</sub> or GND	-	6	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI <sub>CC</sub> (Note 4)	V <sub>CC</sub> -2.1	-	-	-	100	360	-	450	-	490	μA

**NOTES:**

3. Any voltage between V<sub>CC</sub> and GND.
4. For dual-supply systems theoretical worst case (V<sub>I</sub> = 2.4V, V<sub>CC</sub> = 5.5V) specification is 1.8mA.

### HCT Input Loading Table

INPUT	UNIT LOAD
S <sub>0</sub> - S <sub>3</sub>	0.5
$\bar{E}$	0.3

NOTE: Unit Load is ΔI<sub>CC</sub> limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

### Switching Specifications Input t<sub>r</sub>, t<sub>f</sub> = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V <sub>CC</sub> (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
<b>HC TYPES</b>											
Propagation Delay Time Switch In to Out	t <sub>PLH</sub> , t <sub>PHL</sub>	C <sub>L</sub> = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
		C <sub>L</sub> = 15pF	5	-	6	-	-	-	-	-	ns

## CD74HC4067, CD74HCT4067

### Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Switch Turn On $\bar{E}$ to Out	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	69	-	83	ns
			6	-	-	47	-	59	-	71	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
Switch Turn On Sn to Out	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
			6	-	-	51	-	64	-	76	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
Switch Turn Off $\bar{E}$ to Out	$t_{PHZ}, t_{PLZ}$	$C_L = 50\text{pF}$	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	69	-	83	ns
			6	-	-	47	-	59	-	71	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
Switch Turn Off Sn to Out	$t_{PHZ}, t_{PLZ}$	$C_L = 50\text{pF}$	2	-	-	290	-	365	-	435	ns
			4.5	-	-	58	-	73	-	87	ns
			6	-	-	49	-	62	-	74	ns
		$C_L = 50\text{pF}$	5	-	21	-	-	-	-	-	ns
Input (Control) Capacitance	$C_I$	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 5, 6)	$C_{PD}$	-	5	-	93	-	-	-	-	pF	
<b>HCT TYPES</b>											
Propagation Delay Time Switch In to Out	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns
		$C_L = 15\text{pF}$	5	-	6	-	-	-	-	-	ns
Switch Turn On $\bar{E}$ to Out	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
Switch Turn On Sn to Out	$t_{PZH}, t_{PZL}$	$C_L = 50\text{pF}$	4.5	-	-	60	-	75	-	90	ns
		$C_L = 15\text{pF}$	5	-	25	-	-	-	-	-	ns
Switch Turn Off $\bar{E}$ to Out	$t_{PHZ}, t_{PLZ}$	$C_L = 50\text{pF}$	4.5	-	-	55	-	69	-	83	ns
		$C_L = 15\text{pF}$	5	-	23	-	-	-	-	-	ns
Switch Turn Off Sn to Out	$t_{PHZ}, t_{PLZ}$	$C_L = 50\text{pF}$	4.5	-	-	58	-	73	-	87	ns
		$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
Input (Control) Capacitance	$C_I$	-	-	-	10	-	10	-	10	pF	
Power Dissipation Capacitance (Notes 5, 6)	$C_{PD}$	-	5	-	96	-	-	-	-	pF	

**NOTES:**

5.  $C_{PD}$  is used to determine the dynamic power consumption, per package.

6.  $P_D = C_{PD} V_{CC}^2 f_i + \sum (C_L + C_S) V_{CC}^2 f_o$  where  $f_i$  = input frequency,  $f_o$  = output frequency,  $C_L$  = output load capacitance,  $C_S$  = switch capacitance,  $V_{CC}$  = supply voltage.

# CD74HC4067, CD74HCT4067

## Analog Channel Specifications $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$ (V)	HC/HCT	UNITS
Switch Frequency Response Bandwidth at -3dB (Figure 2)	Figure 4, Notes 7, 8	4.5	89	MHz
Sine Wave Distortion	Figure 5	4.5	0.051	%
Feedthrough Noise E to Switch	Figure 6, Notes 8, 9	4.5	TBE	mV
Feedthrough Noise S to Switch			TBE	mV
Switch "OFF" Signal Feedthrough (Figure 3)	Figure 7	4.5	-75	dB
Switch Input Capacitance, $C_S$		-	5	pF
Common Capacitance, $C_{COM}$		-	50	pF

### NOTES:

- Adjust input level for 0dBm at output,  $f = 1\text{MHz}$ .
- $V_{IS}$  is centered at  $V_{CC}/2$ .
- Adjust input for 0dBm at  $V_{IS}$ .

## Typical Performance Curves

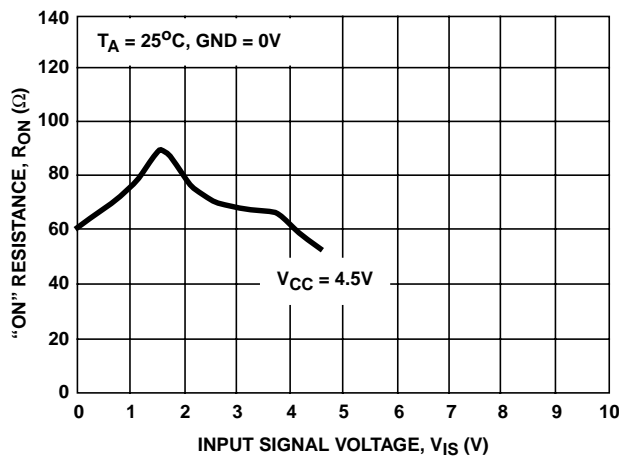


FIGURE 1. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

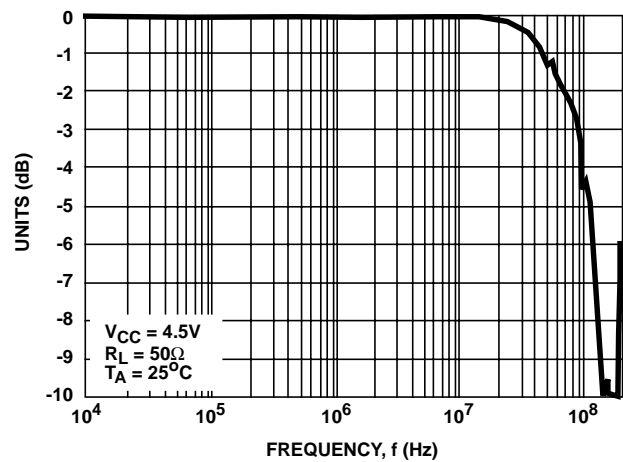


FIGURE 2. TYPICAL SWITCH FREQUENCY RESPONSE

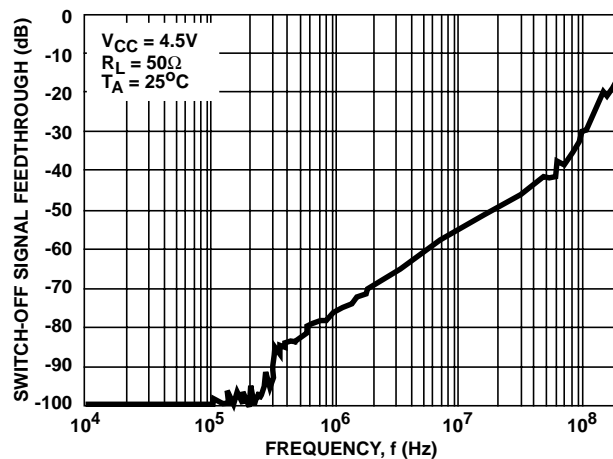


FIGURE 3. TYPICAL SWITCH-OFF SIGNAL FEEDTHROUGH vs FREQUENCY

Analog Test Circuits

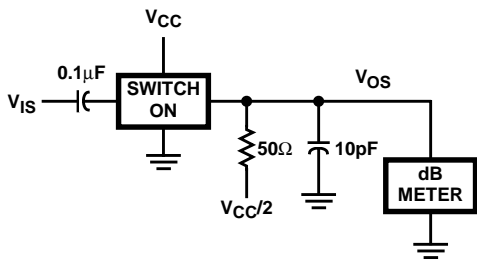
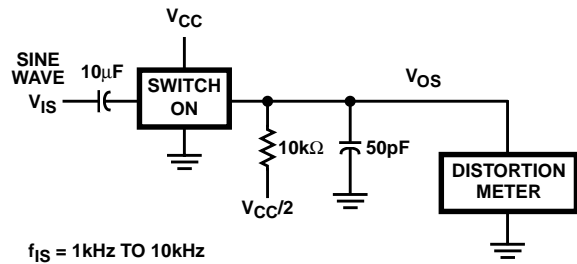


FIGURE 4. FREQUENCY RESPONSE TEST CIRCUIT



$f_{IS} = 1\text{kHz TO } 10\text{kHz}$

FIGURE 5. SINE WAVE DISTORTION TEST CIRCUIT

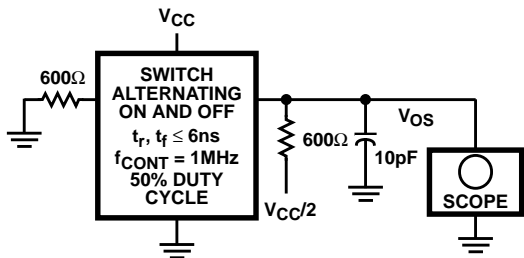


FIGURE 6. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

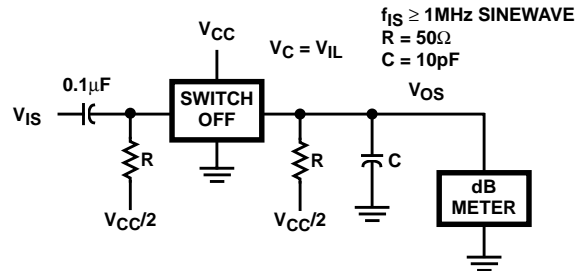


FIGURE 7. SWITCH OFF SIGNAL FEEDTHROUGH TEST CIRCUIT

Test Circuits and Waveforms

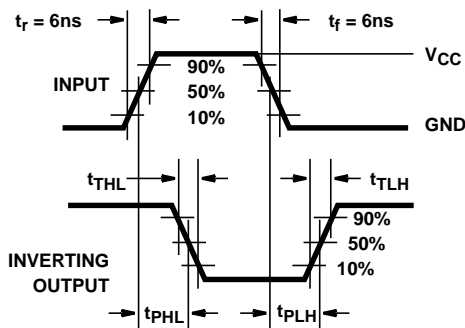


FIGURE 8. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

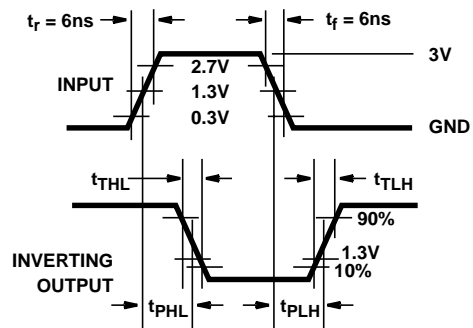


FIGURE 9. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4067M	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067M	<a href="#">Samples</a>
CD74HC4067M96	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 125	HC4067M	<a href="#">Samples</a>
CD74HC4067M96E4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067M	<a href="#">Samples</a>
CD74HC4067M96G4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067M	<a href="#">Samples</a>
CD74HC4067MG4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067M	<a href="#">Samples</a>
CD74HC4067SM96	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4067	<a href="#">Samples</a>
CD74HC4067SM96E4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4067	<a href="#">Samples</a>
CD74HC4067SM96G4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4067	<a href="#">Samples</a>
CD74HCT4067M	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4067M	<a href="#">Samples</a>
CD74HCT4067ME4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4067M	<a href="#">Samples</a>
CD74HCT4067MG4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4067M	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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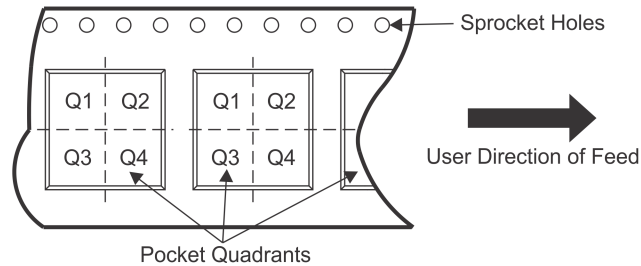
**OTHER QUALIFIED VERSIONS OF CD74HCT4067 :**

- Automotive: [CD74HCT4067-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4067M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74HC4067M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74HC4067M96G4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74HC4067SM96	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4067M96	SOIC	DW	24	2000	364.0	361.0	36.0
CD74HC4067M96	SOIC	DW	24	2000	350.0	350.0	43.0
CD74HC4067M96G4	SOIC	DW	24	2000	350.0	350.0	43.0
CD74HC4067SM96	SSOP	DB	24	2000	853.0	449.0	35.0

DW (R-PDSO-G24)

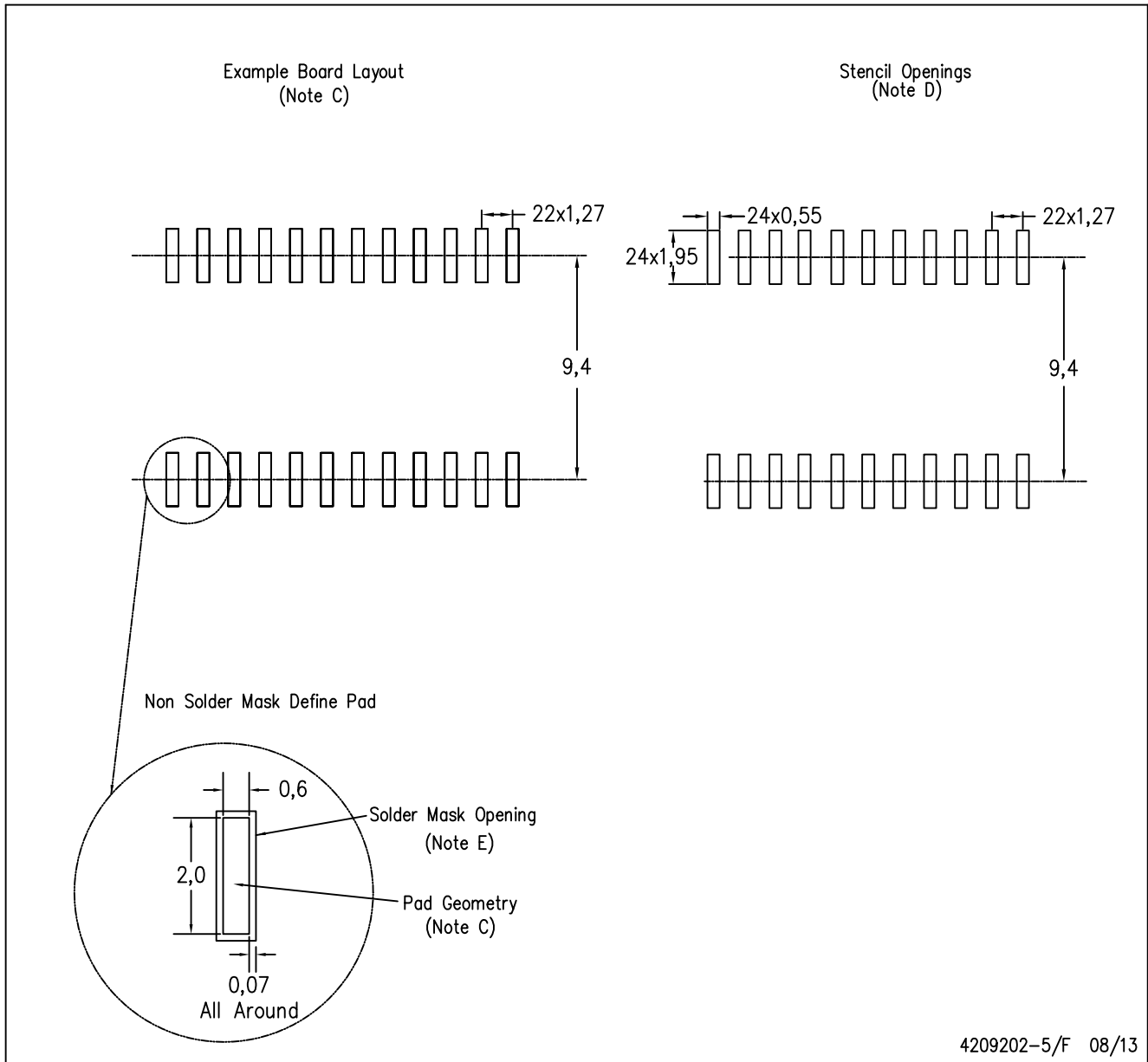
PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Refer to IPC7351 for alternate board design.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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