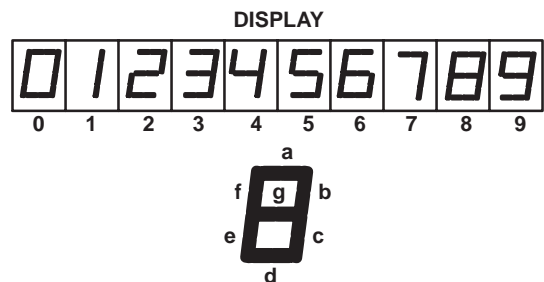
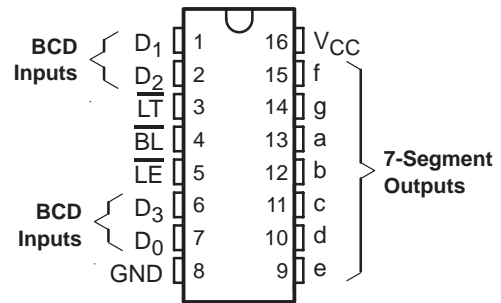


# CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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- 2-V to 6-V  $V_{CC}$  Operation ('HC4511)
- 4.5-V to 5.5-V  $V_{CC}$  Operation (CD74HCT4511)
- High-Output Sourcing Capability
  - 7.5 mA at 4.5 V (CD74HCT4511)
  - 10 mA at 6 V ('HC4511)
- Input Latches for BCD Code Storage
- Lamp Test and Blanking Capability
- Balanced Propagation Delays and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- 'HC4511
  - High Noise Immunity,  $N_{IL}$  or  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5$  V
- CD74HCT4511
  - Direct LSTTL Input Logic Compatibility,  $V_{IL} = 0.8$  V Maximum,  $V_{IH} = 2$  V Minimum
  - CMOS Input Compatibility,  $I_1 \leq 1$   $\mu$ A at  $V_{OL}$ ,  $V_{OH}$

CD54HC4511 ... F PACKAGE  
CD74HC4511 ... E, M, OR PW PACKAGE  
CD74HCT4511 ... E PACKAGE  
(TOP VIEW)



## description/ordering information

The CD54HC4511, CD74HC4511, and CD74HCT4511 are BCD-to-7 segment latch/decoder/drivers with four address inputs ( $D_0$ – $D_3$ ), an active-low blanking ( $\overline{BL}$ ) input, lamp-test ( $\overline{LT}$ ) input, and a latch-enable ( $\overline{LE}$ ) input that, when high, enables the latches to store the BCD inputs. When  $\overline{LE}$  is low, the latches are disabled, making the outputs transparent to the BCD inputs.

These devices have standard-size output transistors, but are capable of sourcing (at standard  $V_{OH}$  levels) up to 7.5 mA at 4.5 V. The HC types can supply up to 10 mA at 6 V.

## ORDERING INFORMATION

$T_A$	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING	
–55°C to 125°C	PDIP – E	Tube of 25	CD74HC4511E	CD74HC4511E	
			CD74HCT4511E	CD74HCT4511E	
	SOIC – M	Tube of 40	CD74HC4511M	HC4511M	
			Reel of 2500		CD74HC4511M96
			Reel of 250		CD74HC4511MT
	TSSOP – PW	Reel of 2000	CD74HC4511PWR	HJ4511	
Reel of 250		CD74HC4511PWT			
CDIP – F	Tube of 25	CD54HC4511F3A	CD54HC4511F3A		

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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# CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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FUNCTION TABLE

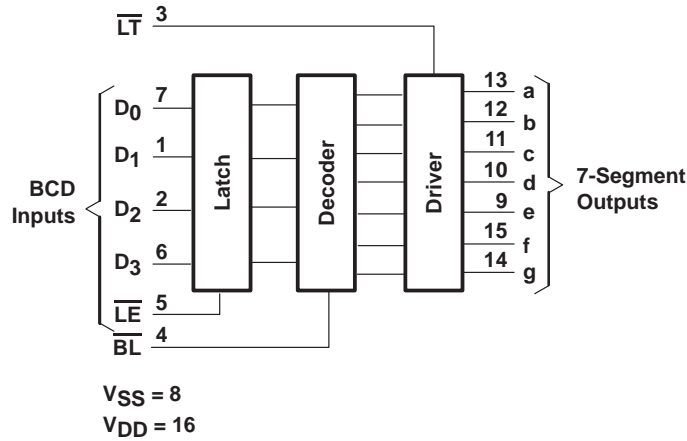
INPUTS								OUTPUTS							
$\overline{LE}$	$\overline{BL}$	$\overline{LT}$	D <sub>3</sub>	D <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>		a	b	c	d	e	f	g	DISPLAY
X	X	L	X	X	X	X		H	H	H	H	H	H	H	8
X	L	H	X	X	X	X		L	L	L	L	L	L	L	Blank
L	H	H	L	L	L	L		H	H	H	H	H	H	L	0
L	H	H	L	L	L	H		L	H	H	L	L	L	L	1
L	H	H	L	L	H	L		H	H	L	H	H	L	H	2
L	H	H	L	L	H	H		H	H	H	H	L	L	H	3
L	H	H	L	H	L	L		L	H	H	L	L	H	H	4
L	H	H	L	H	L	H		H	L	H	H	L	H	H	5
L	H	H	L	H	H	L		L	L	H	H	H	H	H	6
L	H	H	L	H	H	H		H	H	H	L	L	L	L	7
L	H	H	H	L	L	L		H	H	H	H	H	H	H	8
L	H	H	H	L	L	H		H	H	H	L	L	H	H	9
L	H	H	H	L	H	L		L	L	L	L	L	L	L	Blank
L	H	H	H	L	H	H		L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	L		L	L	L	L	L	L	L	Blank
L	H	H	H	H	L	H		L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	L		L	L	L	L	L	L	L	Blank
L	H	H	H	H	H	H		L	L	L	L	L	L	L	Blank
H	H	H	X	X	X	X		†	†	†	†	†	†	†	†

X = Don't care

† Depends on BCD code previously applied when  $\overline{LE} = L$

NOTE: Display is blank for all illegal input codes (BCD > HLLH).

## function diagram





# CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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## absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{CC}$ .....	-0.5 V to 7 V
Input diode current, $I_{IK}$ ( $V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V) (see Note 1) .....	$\pm 20$ mA
Output diode current, $I_{OK}$ ( $V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V) (see Note 1) .....	$\pm 20$ mA
Continuous output source or sink current per output, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 25$ mA
Continuous current through $V_{CC}$ or GND .....	$\pm 50$ mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): E package .....	67°C/W
M package .....	73°C/W
PW package .....	108°C/W
Lead temperature (during soldering):	
At distance $1/16 \pm 1/32$ in ( $1.59 \pm 0.79$ mm) from case for 10 s maximum .....	265°C
Unit inserted into a PC board (minimum thickness $1/16$ in, 1.59 mm), with solder contacting lead tips only .....	300°C
Storage temperature, $T_{stg}$ .....	-65 to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions for 'HC4511 (see Note 3)

		$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$V_{CC}$	Supply voltage	2	6	2	6	2	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V		1.5	1.5	1.5		V
		$V_{CC} = 4.5$ V		3.15	3.15	3.15		
		$V_{CC} = 6$ V		4.2	4.2	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V		0.5	0.5	0.5		V
		$V_{CC} = 4.5$ V		1.35	1.35	1.35		
		$V_{CC} = 6$ V		1.8	1.8	1.8		
$V_I$	Input voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$V_O$	Output voltage	0	$V_{CC}$	0	$V_{CC}$	0	$V_{CC}$	V
$t_t$	Input transition (rise and fall) time	$V_{CC} = 2$ V		1000	1000	1000		ns
		$V_{CC} = 4.5$ V		500	500	500		
		$V_{CC} = 6$ V		400	400	400		

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



# CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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## recommended operating conditions for CD74HCT4511 (see Note 4)

		T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5.5	4.5	5.5	4.5	5.5	V
V <sub>IH</sub>	High-level input voltage	2		2		2		V
V <sub>IL</sub>	Low-level input voltage		0.8		0.8		0.8	V
V <sub>I</sub>	Input voltage		V <sub>CC</sub>		V <sub>CC</sub>		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		V <sub>CC</sub>		V <sub>CC</sub>		V <sub>CC</sub>	V
t <sub>t</sub>	Input transition (rise and fall) time		500		500		500	ns

NOTE 4: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## 'HC4511

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.9	1.9			V	
			4.5 V	4.4	4.4	4.4				
			6 V	5.9	5.9	5.9				
		I <sub>OH</sub> = -7.5 mA	4.5 V	3.98	3.7	3.84				
		I <sub>OH</sub> = -10 mA	6 V	5.48	5.2	5.34				
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.1	0.1	0.1		V		
			4.5 V	0.1	0.1	0.1				
			6 V	0.1	0.1	0.1				
		I <sub>OL</sub> = 4 mA	4.5 V	0.26	0.4	0.33				
		I <sub>OL</sub> = 5.2 mA	6 V	0.26	0.4	0.33				
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0		6 V	±0.1	±1	±1		μA		
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		6 V	8	160	80		μA		
C <sub>i</sub>				10	10	10		pF		

# CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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## CD74HCT4511

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	4.5 V	4.4			4.4		4.4		V
		I <sub>OH</sub> = -4 mA		3.98			3.7		3.84		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	4.5 V	0.1			0.1		0.1		V
		I <sub>OL</sub> = 4 mA		0.26			0.4		0.33		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> to GND		5.5 V	±0.1			±1		±1		μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0		5.5 V	8			160		80		μA
ΔI <sub>CC</sub> †	One input at V <sub>CC</sub> - 2.1 V, Other inputs at 0 or V <sub>CC</sub>		4.5 V to 5.5 V	100 360			490		450		μA
C <sub>i</sub>				10			10		10		pF

† Additional quiescent supply current per input pin, TTL inputs high, 1 unit load. For dual-supply systems, theoretical worst-case (V<sub>I</sub> = 2.4 V, V<sub>CC</sub> = 5.5 V) specification is 1.8 mA.

HCT INPUT LOADING TABLE

INPUT	UNIT LOADS‡
$\overline{LT}$ , $\overline{LE}$	1.5
$\overline{BL}$ , D <sub>n</sub>	0.3

‡ Unit load is ΔI<sub>CC</sub> limit specified in electrical characteristics table, e.g., 360 μA maximum at 25°C.

HC4511 timing requirements over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

	V <sub>CC</sub>	T <sub>A</sub> = 25°C		T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t <sub>w</sub> Pulse duration, $\overline{LE}$ low	2 V	80		120		100		ns
	4.5 V	16		24		20		
	6 V	14		20		17		
t <sub>su</sub> Setup time, BCD inputs before $\overline{LE}$ ↑	2 V	60		90		75		ns
	4.5 V	12		18		15		
	6 V	10		15		13		
t <sub>h</sub> Hold time, BCD inputs before $\overline{LE}$ ↑	2 V	3		3		3		ns
	4.5 V	3		3		3		
	6 V	3		3		3		

# CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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## 'HC4511

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V <sub>CC</sub>	T <sub>A</sub> = 25°C			T <sub>A</sub> = -55°C TO 125°C		T <sub>A</sub> = -40°C TO 85°C		UNIT	
					MIN	TYP	MAX	MIN	MAX	MIN	MAX		
t <sub>pd</sub>	D <sub>n</sub>	Output	C <sub>L</sub> = 50 pF	2 V			300			450		375	ns
				4.5 V			60			90		75	
				6 V			51			77		64	
			C <sub>L</sub> = 15 pF	5 V			25						
	$\overline{\text{LE}}$	Output	C <sub>L</sub> = 50 pF	2 V			270			405		340	
				4.5 V			54			81		68	
				6 V			46			69		58	
	$\overline{\text{BL}}$	Output	C <sub>L</sub> = 50 pF	2 V			220			330		275	
				4.5 V			44			66		55	
				6 V			37			56		47	
	$\overline{\text{LT}}$	Output	C <sub>L</sub> = 50 pF	2 V			160			240		200	
				4.5 V			32			48		40	
6 V						27			41		34		
t <sub>t</sub>	Any	C <sub>L</sub> = 50 pF	2 V			75			110		95	ns	
			4.5 V			15			22		19		
			6 V			13			19		16		

# CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

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## CD74HCT4511

timing requirements over recommended operating free-air temperature range  $V_{CC} = 4.5\text{ V}$  (unless otherwise noted) (see Figure 2)

		$T_A = 25^\circ\text{C}$		$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_w$	Pulse duration, $\overline{LE}$ low	16		24		20		ns
$t_{su}$	Setup time, BCD inputs before $\overline{LE}\uparrow$	16		24		20		ns
$t_h$	Hold time, BCD inputs before $\overline{LE}\uparrow$	5		5		5		ns

## CD74HCT4511

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$V_{CC}$	$T_A = 25^\circ\text{C}$			$T_A = -55^\circ\text{C}$ TO $125^\circ\text{C}$		$T_A = -40^\circ\text{C}$ TO $85^\circ\text{C}$		UNIT	
					MIN	TYP	MAX	MIN	MAX	MIN	MAX		
$t_{pd}$	$D_n$	Output	$C_L = 50\text{ pF}$	4.5 V			60		90		75	ns	
			$C_L = 15\text{ pF}$	5 V			25						
	$\overline{LE}$	Output	$C_L = 50\text{ pF}$	4.5 V					54		81		68
			$C_L = 15\text{ pF}$	5 V			23						
	$\overline{BL}$	Output	$C_L = 50\text{ pF}$	4.5 V							66		55
			$C_L = 15\text{ pF}$	5 V			18						
$\overline{LT}$	Output	$C_L = 50\text{ pF}$	4.5 V							50	41		
		$C_L = 15\text{ pF}$	5 V			13							
$t_t$		Any	$C_L = 50\text{ pF}$	4.5 V					15	22	19	ns	

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TYP	UNIT
$C_{pd}\dagger$	Power dissipation capacitance	'HC4511	114
		CD74HCT4511	110

$\dagger C_{pd}$  is used to determine the dynamic power consumption, per package.

$$P_D = C_{pd} V_{CC}^2 f_i + \sum C_L V_{CC}^2 f_o$$

where:  $f_i$  = input frequency

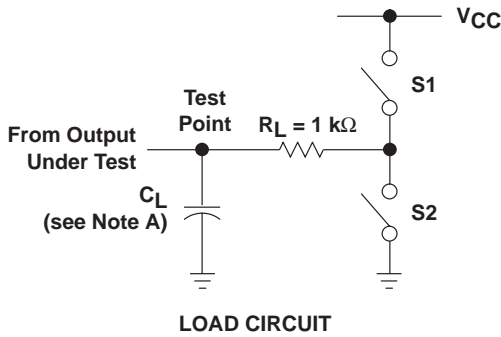
$f_o$  = output frequency

$C_L$  = output load capacitance

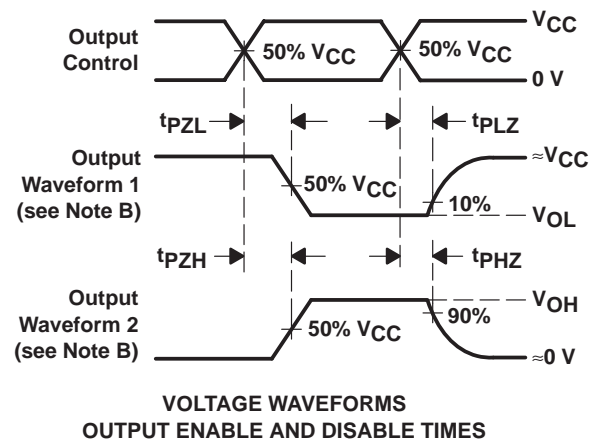
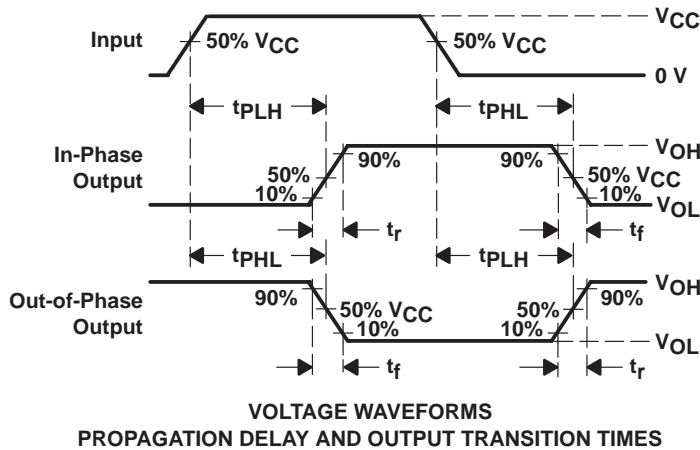
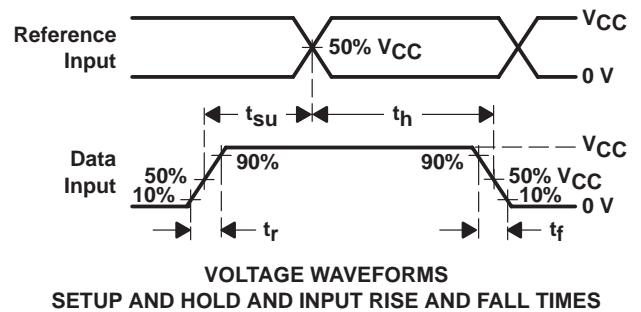
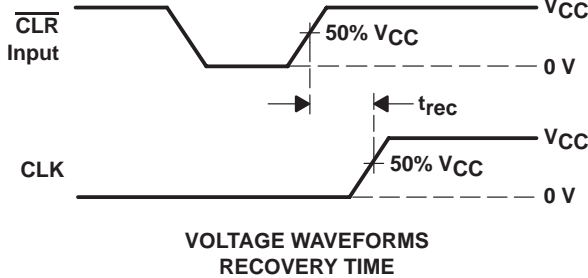
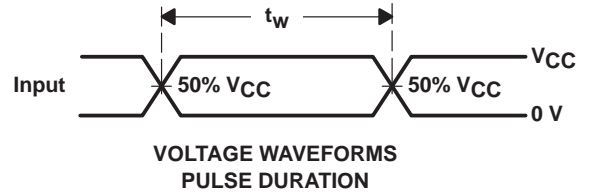
$V_{CC}$  = supply voltage



PARAMETER MEASUREMENT INFORMATION – 'HC4511



PARAMETER		S1	S2
$t_{en}$	$t_{PZH}$	Open	Closed
	$t_{PZL}$	Closed	Open
$t_{dis}$	$t_{PHZ}$	Open	Closed
	$t_{PLZ}$	Closed	Open
$t_{pd}$ or $t_t$		Open	Open



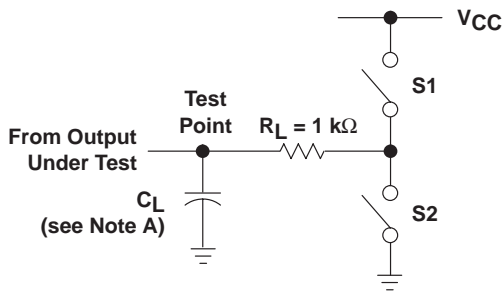
- NOTES: A.  $C_L$  includes probe and test-fixture capacitance.  
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r = 6\text{ ns}$ ,  $t_f = 6\text{ ns}$ .  
D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.  
E. The outputs are measured one at a time with one input transition per measurement.  
F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

# CD54HC4511, CD74HC4511, CD74HCT4511 BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS

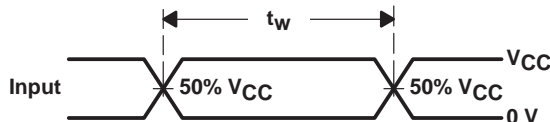
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## PARAMETER MEASUREMENT INFORMATION – CD74HCT4511

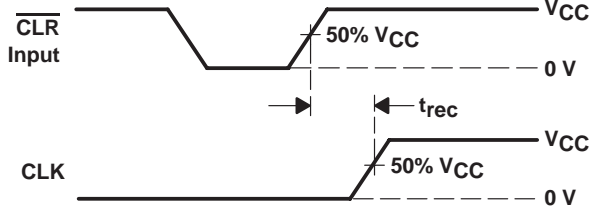


LOAD CIRCUIT

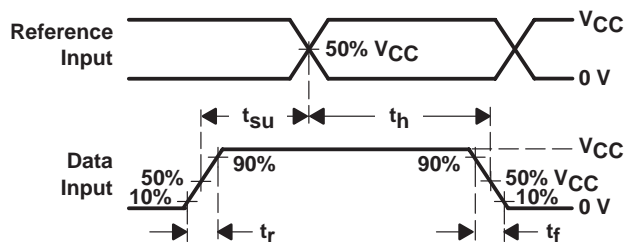
PARAMETER	S1	S2	
$t_{en}$	$t_{PZH}$	Open	Closed
	$t_{PZL}$	Closed	Open
$t_{dis}$	$t_{PHZ}$	Open	Closed
	$t_{PLZ}$	Closed	Open
$t_{pd}$ or $t_t$	Open	Open	



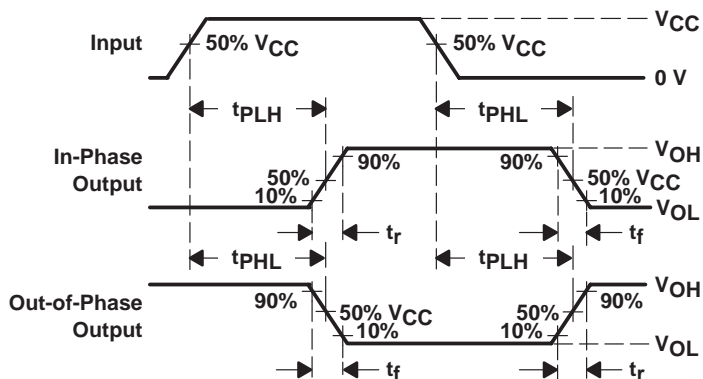
VOLTAGE WAVEFORMS  
PULSE DURATION



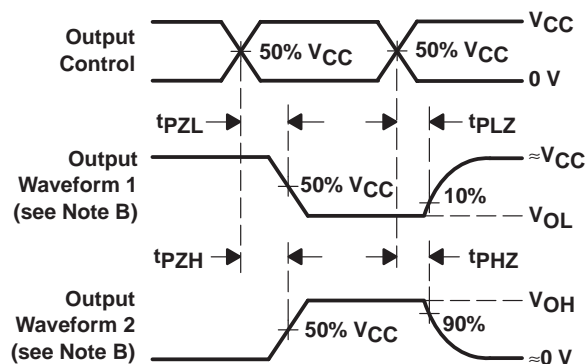
VOLTAGE WAVEFORMS  
RECOVERY TIME



VOLTAGE WAVEFORMS  
SETUP AND HOLD AND INPUT RISE AND FALL TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY AND OUTPUT TRANSITION TIMES



VOLTAGE WAVEFORMS  
OUTPUT ENABLE AND DISABLE TIMES

- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r = 6$  ns,  $t_f = 6$  ns.
  - D. For clock inputs,  $f_{max}$  is measured with the input duty cycle at 50%.
  - E. The outputs are measured one at a time with one input transition per measurement.
  - F.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - G.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - H.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 2. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8773301EA	ACTIVE	CDIP	J	16	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A	<a href="#">Samples</a>
CD54HC4511F3A	ACTIVE	CDIP	J	16	1	TBD	SNPB	N / A for Pkg Type	-55 to 125	5962-8773301EA CD54HC4511F3A	<a href="#">Samples</a>
CD74HC4511E	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4511E	<a href="#">Samples</a>
CD74HC4511EE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC4511E	<a href="#">Samples</a>
CD74HC4511M	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	<a href="#">Samples</a>
CD74HC4511M96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	<a href="#">Samples</a>
CD74HC4511M96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	<a href="#">Samples</a>
CD74HC4511MG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	<a href="#">Samples</a>
CD74HC4511MT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4511M	<a href="#">Samples</a>
CD74HC4511PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	<a href="#">Samples</a>
CD74HC4511PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	<a href="#">Samples</a>
CD74HC4511PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	<a href="#">Samples</a>
CD74HC4511PWT	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	<a href="#">Samples</a>
CD74HC4511PWTE4	ACTIVE	TSSOP	PW	16	250	Green (RoHS & no Sb/Br)	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4511	<a href="#">Samples</a>
CD74HCT4511E	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4511E	<a href="#">Samples</a>
CD74HCT4511EE4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT4511E	<a href="#">Samples</a>

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF CD54HC4511, CD74HC4511 :**

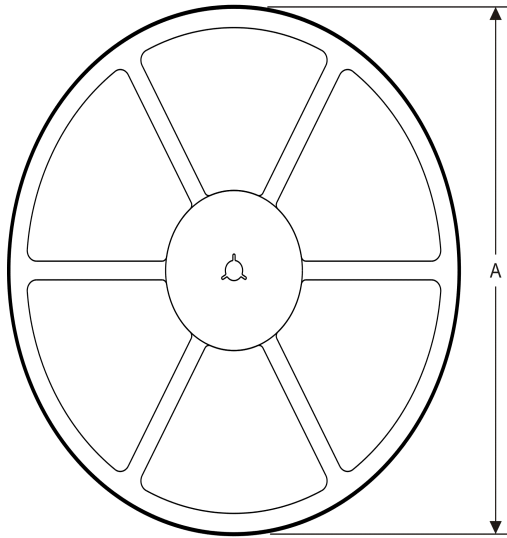
● Catalog: [CD74HC4511](#)

● Military: [CD54HC4511](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**TAPE AND REEL INFORMATION**

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4511M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC4511PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4511PWT	TSSOP	PW	16	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

## TAPE AND REEL BOX DIMENSIONS

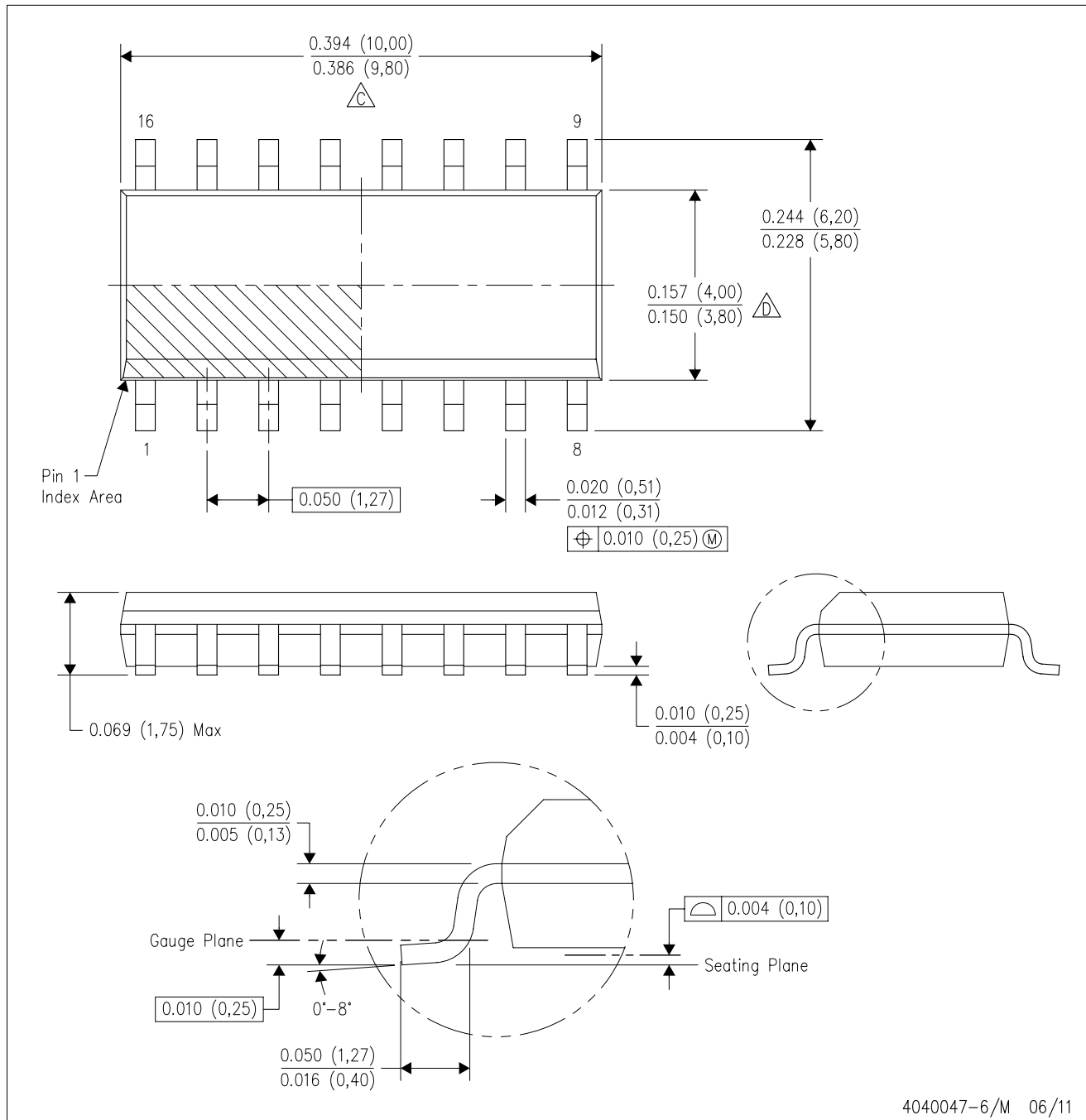


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4511M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HC4511PWR	TSSOP	PW	16	2000	367.0	367.0	35.0
CD74HC4511PWT	TSSOP	PW	16	250	367.0	367.0	35.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AC.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



4220204/A 02/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

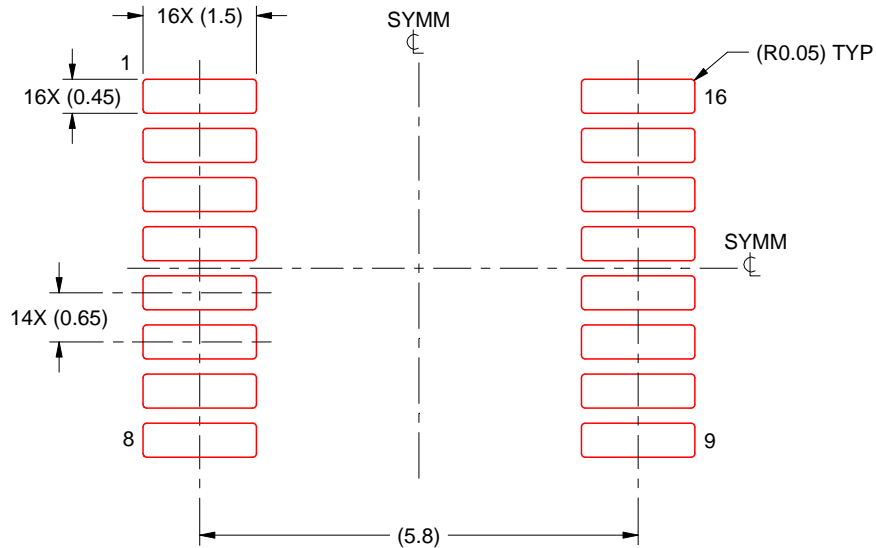
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

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