

High-Speed CMOS Logic 4-Bit Binary Full Adder with Fast Carry

Features

- Adds Two Binary Numbers
- Full Internal Lookahead
- Fast Ripple Carry for Economical Expansion
- Operates with Both Positive and Negative Logic
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range . . . -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL} , V_{OH}

Description

The 'HC283 and 'HCT283 binary full adders add two 4-bit binary numbers and generate a carry-out bit if the sum exceeds 15.

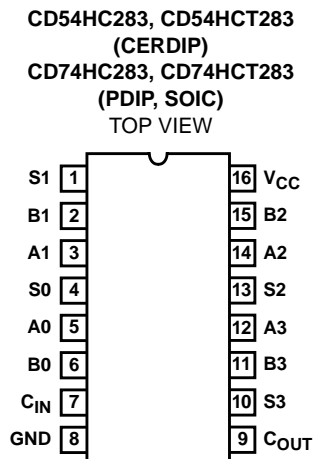
Because of the symmetry of the add function, this device can be used with either all active-high operands (positive logic) or with all active-low operands (negative logic). When using positive logic the carry-in input must be tied low if there is no carry-in.

Ordering Information

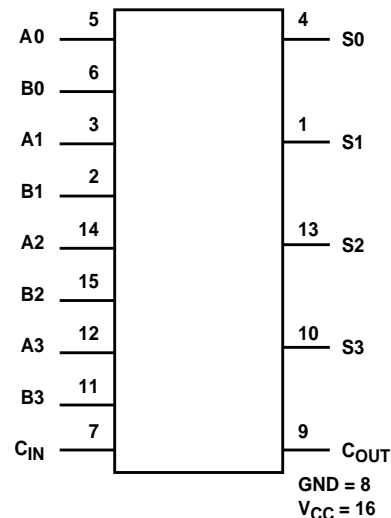
PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD54HC283F3A	-55 to 125	16 Ld CERDIP
CD54HCT283F3A	-55 to 125	16 Ld CERDIP
CD74HC283E	-55 to 125	16 Ld PDIP
CD74HC283M	-55 to 125	16 Ld SOIC
CD74HC283MT	-55 to 125	16 Ld SOIC
CD74HC283M96	-55 to 125	16 Ld SOIC
CD74HCT283E	-55 to 125	16 Ld PDIP
CD74HCT283M	-55 to 125	16 Ld SOIC
CD74HCT283MT	-55 to 125	16 Ld SOIC
CD74HCT283M96	-55 to 125	16 Ld SOIC

NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel. The suffix T denotes a small-quantity reel of 250.

Pinout



Functional Diagram



CD54HC283, CD74HC283, CD54HCT283, CD74HCT283

Absolute Maximum Ratings

DC Supply Voltage, V_{CC}	-0.5V to 7V
DC Input Diode Current, I_{IK}	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, I_{OK}	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, I_O	
For $-0.5V < V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC Output Source or Sink Current per Output Pin, I_O	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC V_{CC} or Ground Current, I_{CC}	$\pm 50mA$

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^{\circ}C/W$)
E (PDIP) Package	67
M (SOIC) Package	73
Maximum Junction Temperature	$150^{\circ}C$
Maximum Storage Temperature Range	$-65^{\circ}C$ to $150^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	$300^{\circ}C$ (SOIC - Lead Tips Only)

Operating Conditions

Temperature Range, T_A	$-55^{\circ}C$ to $125^{\circ}C$
Supply Voltage Range, V_{CC}	
HC Types	$.2V$ to $6V$
DC Input or Output Voltage, V_I, V_O	$0V$ to V_{CC}
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

- The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V_{CC} (V)	25 $^{\circ}C$			-40 $^{\circ}C$ TO 85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS	
		V_I (V)	I_O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX		
HC TYPES													
High Level Input Voltage	V_{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V	
				4.5	3.15	-	-	3.15	-	3.15	-	V	
				6	4.2	-	-	4.2	-	4.2	-	V	
Low Level Input Voltage	V_{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V	
				4.5	-	-	1.35	-	1.35	-	1.35	V	
				6	-	-	1.8	-	1.8	-	1.8	V	
High Level Output Voltage CMOS Loads	V_{OH}	V_{IH} or V_{IL}	-0.02	-0.02	2	1.9	-	-	1.9	-	1.9	-	V
			-0.02	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
			-0.02	-0.02	6	5.9	-	-	5.9	-	5.9	-	V
High Level Output Voltage TTL Loads	V_{OH}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V	
			-4	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
			-5.2	-5.2	6	5.48	-	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	V_{OL}	V_{IH} or V_{IL}	0.02	0.02	2	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
			0.02	0.02	6	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V_{OL}	V_{IH} or V_{IL}	-	-	-	-	-	-	-	-	-	V	
			4	4	4.5	-	-	0.26	-	0.33	-	0.4	V
			5.2	5.2	6	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I_I	V_{CC} or GND	-	6	-	-	± 0.1	-	± 1	-	± 1	μA	
Quiescent Device Current	I_{CC}	V_{CC} or GND	0	6	-	-	8	-	80	-	160	μA	

CD54HC283, CD74HC283, CD54HCT283, CD74HCT283

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	I _O (mA)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HCT Types												
High Level Input Voltage	V _{IH}	-	-	4.5 to 5.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5 to 5.5	-	-	0.8	-	0.8	-	0.8	V
High Level Output Voltage CMOS Loads	V _{OH}	V _{IL} or V _{IH}	-0.02	4.5	4.4	-	-	4.4	-	4.4	-	V
High Level Output Voltage TTL Loads	V _{OH}	V _{IL} or V _{IH}	-4	4.5	3.98	-	-	3.84	-	3.7	-	V
Low Level Output Voltage CMOS Loads	V _{OL}	V _{IH} or V _{IL}	0.02	4.5	-	-	0.1	-	0.1	-	0.1	V
Low Level Output Voltage TTL Loads	V _{OL}	V _{IH} or V _{IL}	4	4.5	-	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	I _I	V _{CC} to GND	-	5.5	-	-	±0.1	-	±1	-	±1	μA
Quiescent Device Current	ICC	V _{CC} or GND	-	5.5	-	-	8	-	80	-	160	μA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 2)	V _{CC} - 2.1	-	4.5 to 5.5	-	100	360	-	450	-	490	μA

NOTE:

- For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOADS
C _{IN}	1.5
B1, A1, A0	1
B0	0.4
B3, A3, A2, B2	0.5

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360μA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay C _{IN} to S0	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	160	-	200	-	240	ns
			4.5	-	-	32	-	40	-	48	ns
		C _L = 15pF	5	-	13	-	-	-	-	-	ns
			6	-	-	27	-	34	-	41	ns

CD54HC283, CD74HC283, CD54HCT283, CD74HCT283

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
C_{IN} to S1	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	180	-	225	-	270	ns
			4.5	-	-	36	-	45	-	54	ns
		$C_L = 15\text{pF}$	5	-	15	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	31	-	38	-	46	ns
C_{IN} to S2, C_{IN} to C_{OUT}	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	195	-	245	-	295	ns
			4.5	-	-	39	-	49	-	59	ns
		$C_L = 15\text{pF}$	5	-	16	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	33	-	42	-	50	ns
C_{IN} to S3	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	230	-	290	-	345	ns
			4.5	-	-	46	-	58	-	69	ns
		$C_L = 15\text{pF}$	5	-	19	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	39	-	49	-	59	ns
An, Bn to C_{OUT}	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	195	-	245	-	295	ns
			4.5	-	-	39	-	49	-	59	ns
		$C_L = 15\text{pF}$	5	-	16	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	33	-	42	-	50	ns
An, Bn to Sn	t_{PLH}, t_{PHL}	$C_L = 50\text{pF}$	2	-	-	210	-	265	-	315	ns
			4.5	-	-	42	-	53	-	63	ns
		$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	36	-	45	-	54	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	C_{IN}	$C_L = 50\text{pF}$	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance, (Notes 3, 4)	C_{PD}	-	5	-	70	-	-	-	-	-	pF

HCT TYPES

Propagation Delay C_{IN} to S0	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	13	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	31	-	39	-	47	ns
C_{IN} to S1	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	18	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	43	-	54	-	65	ns
C_{IN} to S2, C_{IN} to C_{OUT}	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	19	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	46	-	58	-	69	ns
C_{IN} to S3	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	22	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	53	-	66	-	80	ns
An, Bn to C_{OUT}	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	20	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	48	-	60	-	72	ns
An, Bn to Sn	t_{PLH}, t_{PHL}	$C_L = 15\text{pF}$	5	-	21	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	4.5	-	-	49	-	61	-	74	ns
Output Transition Time	t_{TLH}, t_{THL}	$C_L = 50\text{pF}$	4.5	-	-	15	-	19	-	22	ns

CD54HC283, CD74HC283, CD54HCT283, CD74HCT283

Switching Specifications Input t_r , $t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V_{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Input Capacitance	C_{IN}	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance, (Notes 3, 4)	C_{PD}	-	5	-	82	-	-	-	-	-	pF

NOTES:

3. C_{PD} is used to determine the dynamic power consumption, per package.
4. $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$ where: f_i = Input Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.

Test Circuits and Waveforms

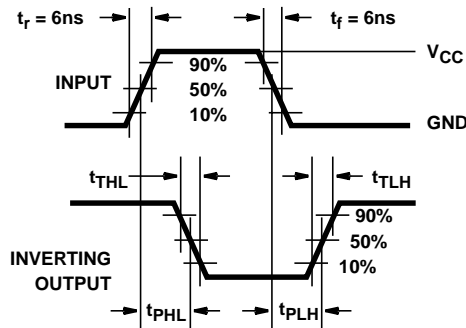


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

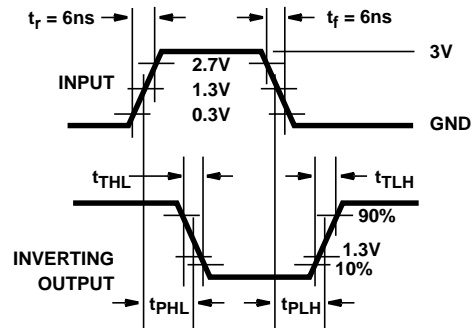


FIGURE 2. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962-8976501EA	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8976501EA CD54HC283F3A	Samples
CD54HC283F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	5962-8976501EA CD54HC283F3A	Samples
CD54HCT283F3A	ACTIVE	CDIP	J	16	1	Non-RoHS & Green	SNPB	N / A for Pkg Type	-55 to 125	CD54HCT283F3A	Samples
CD74HC283E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HC283E	Samples
CD74HC283M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC283M	Samples
CD74HC283M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC283M	Samples
CD74HC283ME4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC283M	Samples
CD74HC283MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC283M	Samples
CD74HCT283E	ACTIVE	PDIP	N	16	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-55 to 125	CD74HCT283E	Samples
CD74HCT283M	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT283M	Samples
CD74HCT283M96	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT283M	Samples
CD74HCT283M96G4	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT283M	Samples
CD74HCT283MG4	ACTIVE	SOIC	D	16	40	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT283M	Samples
CD74HCT283MT	ACTIVE	SOIC	D	16	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT283M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of ≤ 1000 ppm threshold. Antimony trioxide based flame retardants must also meet the ≤ 1000 ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF CD54HC283, CD54HCT283, CD74HC283, CD74HCT283 :

● Catalog: [CD74HC283](#), [CD74HCT283](#)

● Military: [CD54HC283](#), [CD54HCT283](#)

NOTE: Qualified Version Definitions:

● Catalog - TI's standard catalog product

● Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT283M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC283M96	SOIC	D	16	2500	333.2	345.9	28.6
CD74HCT283M96	SOIC	D	16	2500	333.2	345.9	28.6

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - $\triangle D$ The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4040047-6/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 -  C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 -  D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AC.

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



4211283-4/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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