

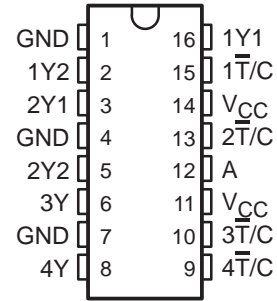
CDC329A

1-LINE TO 6-LINE CLOCK DRIVER WITH SELECTABLE POLARITY

SCAS328B – DECEMBER 1992 – REVISED OCTOBER 1998

- Low Output Skew for Clock-Distribution and Clock-Generation Applications
- TTL-Compatible Inputs and CMOS-Compatible Outputs
- Distributes One Clock Input to Six Clock Outputs
- Polarity Control Selects True or Complementary Outputs
- Distributed V_{CC} and GND Pins Reduce Switching Noise
- High-Drive Outputs (–32-mA I_{OH}, 32-mA I_{OL})
- State-of-the-Art EPIC-II B™ BiCMOS Design Significantly Reduces Power Dissipation
- Package Options Include Plastic Small-Outline (D)

**D PACKAGE
(TOP VIEW)**



description

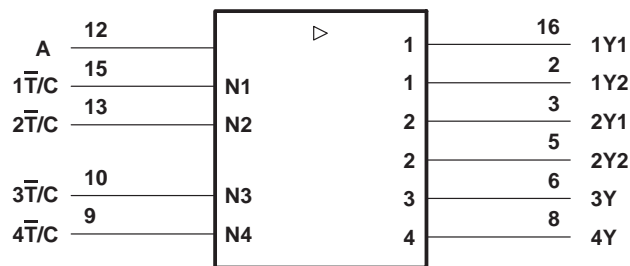
The CDC329A contains a clock-driver circuit that distributes one input signal to six outputs with minimum skew for clock distribution. Through the use of the polarity-control inputs (\bar{T}/C), various combinations of true and complementary outputs can be obtained.

The CDC329A is characterized for operation from –40°C to 85°C.

FUNCTION TABLE

| INPUTS | | OUTPUT |
|-------------|---|--------|
| \bar{T}/C | A | Y |
| L | L | L |
| L | H | H |
| H | L | H |
| H | H | L |

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.



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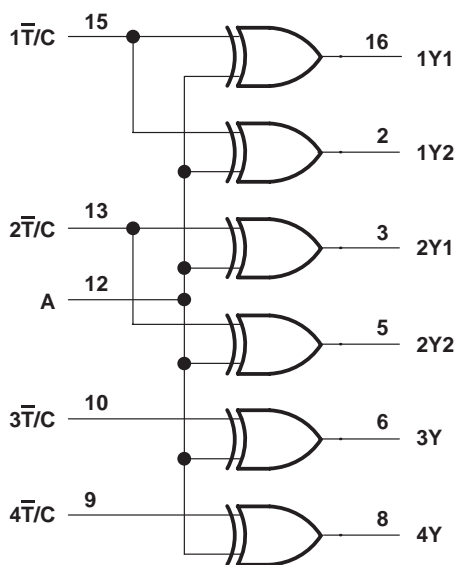


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logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

| | |
|---|--|
| Supply voltage range, V_{CC} | -0.5 V to 7 V |
| Input voltage range, V_I (see Note 1) | -0.5 V to 7 V |
| Voltage range applied to any output in the high state or power-off state, V_O (see Note 1) | -0.5 V to $V_{CC} + 0.5$ V |
| Current into any output in the low state, I_O | 64 mA |
| Input clamp current, I_{IK} ($V_I < 0$) | -18 mA |
| Output clamp current, I_{OK} ($V_O < 0$) | -50 mA |
| Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air) (see Note 2) | 0.77 W |
| Storage temperature range, T_{stg} | -65°C to 150°C |

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 300 mils. For more information, refer to the *Package Thermal Considerations* application note in the 1994 *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002B.



recommended operating conditions (see Note 3)

| | MIN | NOM | MAX | UNIT |
|---|------|-----|-----------------|------|
| V _{CC} Supply voltage | 4.75 | 5 | 5.25 | V |
| V _{IH} High-level input voltage | 2 | | | V |
| V _{IL} Low-level input voltage | | | 0.8 | V |
| V _I Input voltage | 0 | | V _{CC} | V |
| I _{OH} High-level output current | | | -32 | mA |
| I _{OL} Low-level output current | | | 32 | mA |
| Δt/Δv Input transition rise or fall rate | | | 5 | ns/V |
| f _{clock} Input clock frequency | | | 80 | MHz |
| T _A Operating free-air temperature | -40 | | 85 | °C |

NOTE 3: Unused inputs must be held high or low to prevent them from floating.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

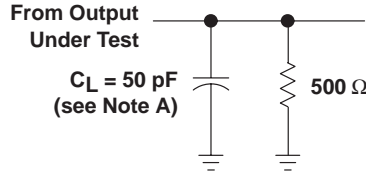
| PARAMETER | TEST CONDITIONS | | MIN | TYP† | MAX | UNIT |
|-----------------|---------------------------------|--|--------------|------|------|------|
| V _{IK} | V _{CC} = 4.75 V, | I _I = -18 mA | | | -1.2 | V |
| V _{OH} | V _{CC} = 4.75 V, | I _{OH} = -32 mA | 3.85 | | | V |
| V _{OL} | V _{CC} = 4.75 V, | I _{OL} = 32 mA | | | 0.55 | V |
| I _I | V _{CC} = 5.25 V, | V _I = V _{CC} or GND | | | ±1 | μA |
| I _{CC} | V _{CC} = 5.25 V, | V _I = V _{CC} or GND, I _O = 0, | Outputs high | | 10 | mA |
| | | | Outputs low | | 40 | |
| C _i | V _I = 2.5 V or 0.5 V | | | 3 | | pF |

† All typical values are at V_{CC} = 5 V, T_A = 25°C

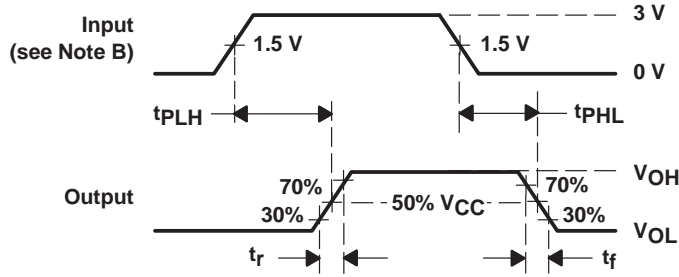
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figures 1 and 2)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | MIN | TYP | MAX | UNIT |
|--------------------|--------------|--------------------|-----|------|-----|------|
| t _{PLH} | A | Any Y | 2 | | 5.9 | ns |
| t _{PHL} | | | 1.7 | | 5.9 | |
| t _{PLH} | T̄/C | Any Y | 1.5 | | 5 | ns |
| t _{PHL} | | | 1.5 | | 5 | |
| t _{sk(o)} | A | Any Y (same phase) | | | 0.6 | ns |
| | | Any Y (any phase) | | | 1.5 | |
| t _r | | | | 1.3 | | ns |
| t _f | | | | 0.85 | | ns |

PARAMETER MEASUREMENT INFORMATION



LOAD CIRCUIT FOR OUTPUTS

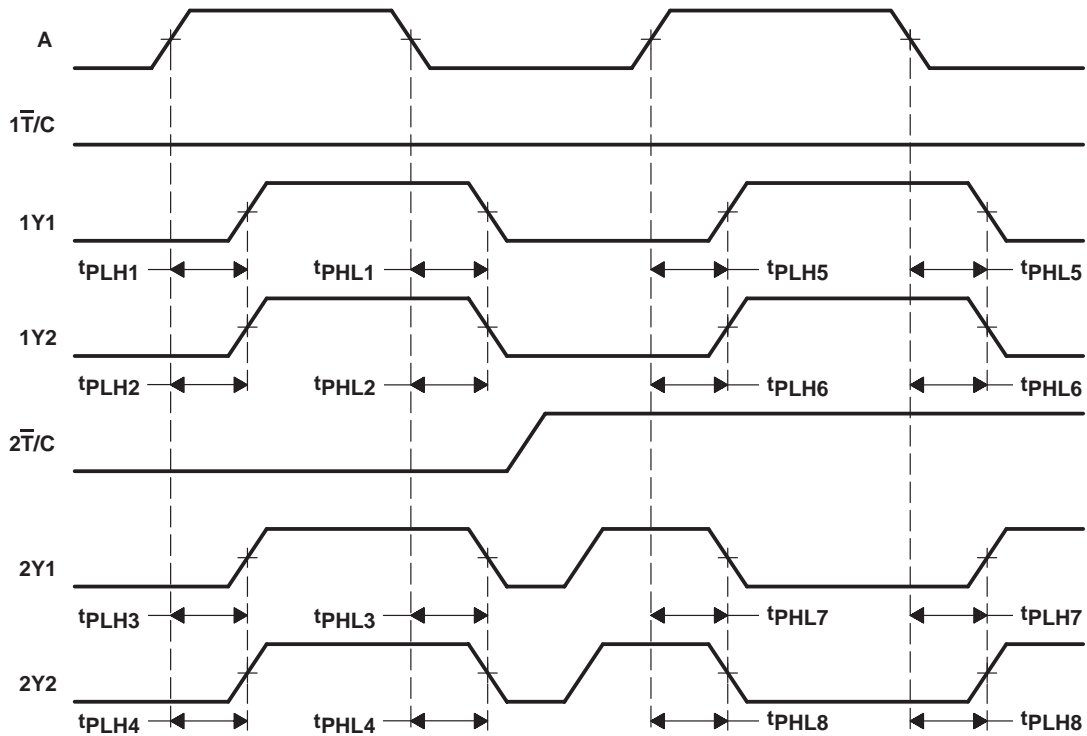


VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $t_r \leq 2.5$ ns, $t_f \leq 2.5$ ns.

Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. Output skew, $t_{sk(o)}$, from A to any Y (same phase), can be measured only between outputs for which the respective polarity-control inputs ($\overline{T/C}$) are at the same logic level. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PHL} from $A\downarrow$ to any Y (e.g., t_{PHLn} , $n = 1$ to 4; or t_{PHLn} , $n = 5$ to 6)
 - The difference between the fastest and slowest of t_{PHL} from $A\downarrow$ to any Y (e.g., t_{PHLn} , $n = 1$ to 4; or t_{PHLn} , $n = 5$ to 6)
 - The difference between the fastest and slowest of t_{PLH} from $A\downarrow$ to any Y (e.g., t_{PLHn} , $n = 7$ to 8)
 - The difference between the fastest and slowest of t_{PHL} from $A\uparrow$ to any Y (e.g., t_{PHLn} , $n = 7$ to 8)
- B. Output skew, $t_{sk(o)}$, from A to any Y (any phase), can be measured between outputs for which the respective polarity-control inputs ($\overline{T/C}$) are at the same or different logic levels. It is calculated as the greater of:
- The difference between the fastest and slowest of t_{PLH} from $A\uparrow$ to any Y or t_{PHL} from $A\uparrow$ to any Y (e.g., t_{PLHn} , $n = 1$ to 4; or t_{PLHn} , $n = 5$ to 6, and t_{PHLn} , $n = 7$ to 8)
 - The difference between the fastest and slowest of t_{PHL} from $A\downarrow$ to any Y or t_{PLH} from $A\downarrow$ to any Y (e.g., t_{PHLn} , $n = 1$ to 4; or t_{PHLn} , $n = 5$ to 6, and t_{PLHn} , $n = 7$ to 8)

Figure 2. Waveforms for Calculation of $t_{sk(o)}$

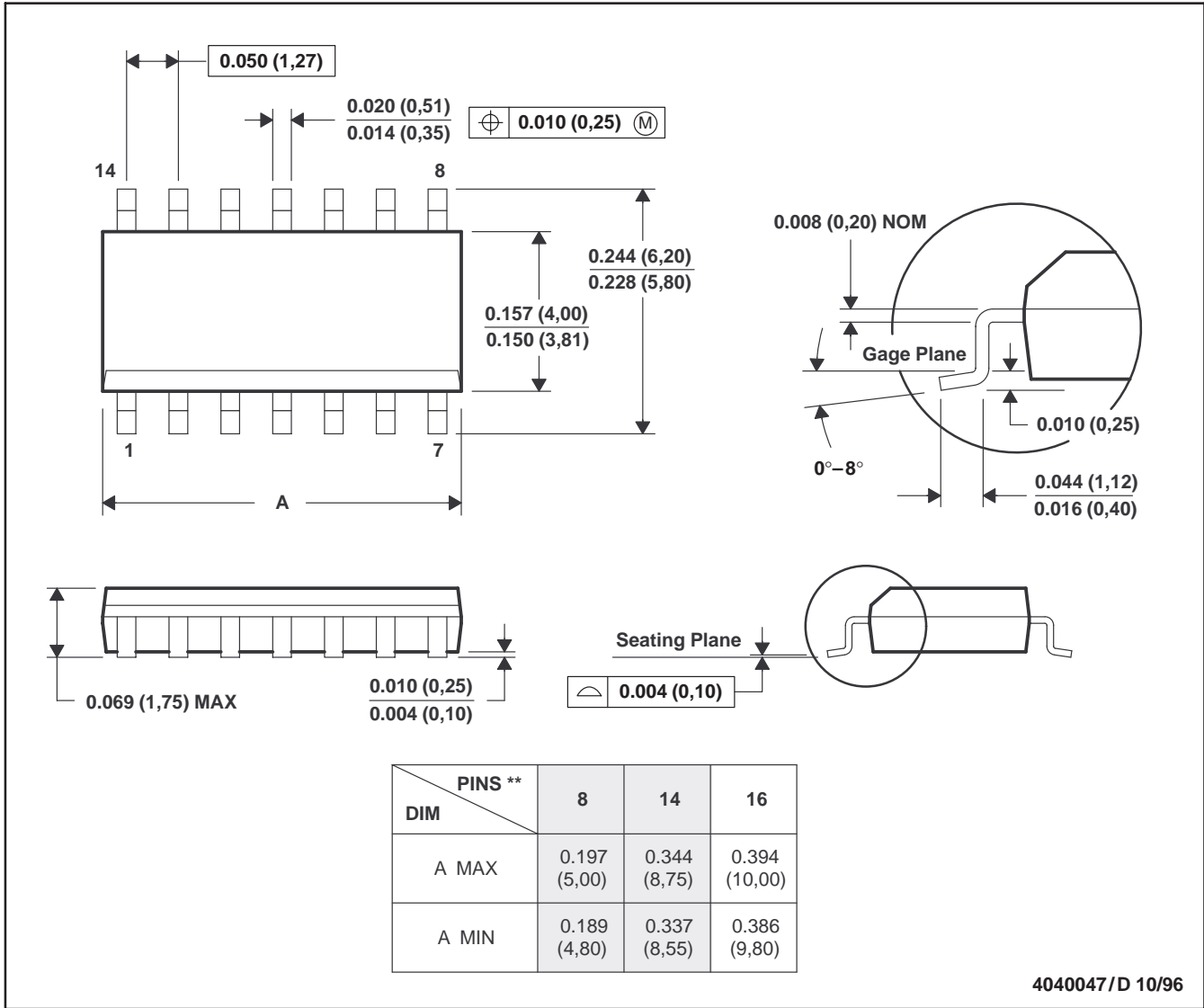
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MECHANICAL INFORMATION

D (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

14 PIN SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
 D. Falls within JEDEC MS-012

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---------------------------|---------------|----------------------|----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CDC329AD | Active | Production | SOIC (D) 16 | 40 TUBE | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDC329A |
| CDC329ADR | Active | Production | SOIC (D) 16 | 2500 LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | CDC329A |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

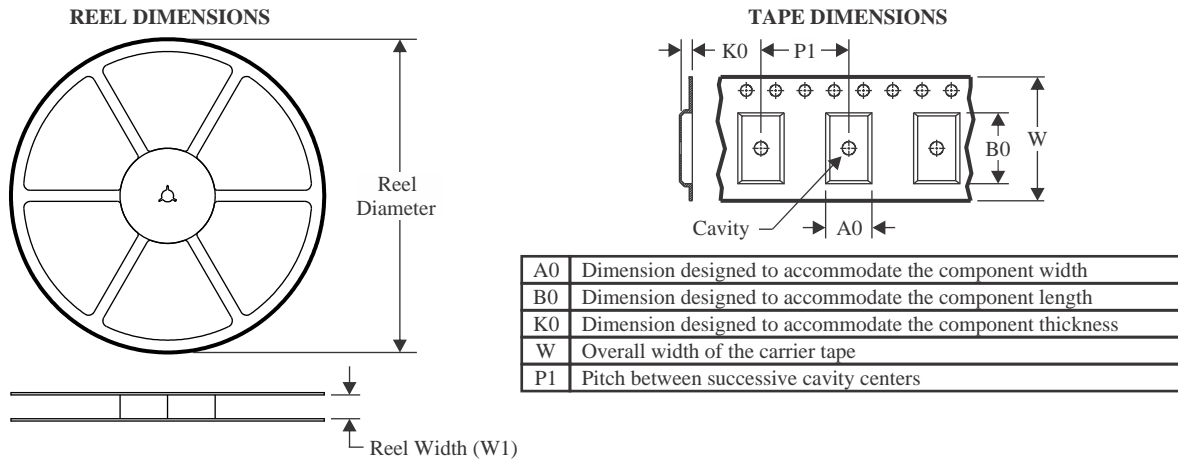
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDC329ADR | SOIC | D | 16 | 2500 | 330.0 | 16.4 | 6.5 | 10.3 | 2.1 | 8.0 | 16.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|-----------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDC329ADR | SOIC | D | 16 | 2500 | 350.0 | 350.0 | 43.0 |

TUBE


*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (μm) | B (mm) |
|------------|--------------|--------------|------|-----|--------|--------|--------|--------|
| CDC329AD | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |
| CDC329ADG4 | D | SOIC | 16 | 40 | 505.46 | 6.76 | 3810 | 4 |

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