

## Dual 1:6 Low Additive Jitter LVDS Buffer

Check for Samples: [CDCLVD2106](#)

### FEATURES

- Dual 1:6 Differential Buffer
- Low Additive Jitter: <math>\lt; 300\text{ fs rms}</math> in 10 kHz – 20 MHz
- Low Within Bank Output Skew of 45 ps (Max)
- Universal Inputs Accept LVDS, LVPECL, LVCMOS
- One Input Dedicated for Six Outputs
- Total of 12 LVDS Outputs, ANSI EIA/TIA-644A Standard Compatible
- Clock Frequency up to 800 MHz
- 2.375–2.625 V Device Power Supply
- LVDS Reference Voltage,  $V_{AC\_REF}$ , Available for Capacitive Coupled Inputs
- Industrial Temperature Range  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$
- Packaged in 6 mm x 6 mm 40-pin QFN (RHA)
- ESD Protection Exceeds 3-kV HBM, 1-kV CDM

### APPLICATIONS

- Telecommunications/Networking
- Medical Imaging
- Test and Measurement Equipment
- Wireless Communications
- General Purpose Clocking

### DESCRIPTION

The CDCLVD2106 clock buffer distributes two clock inputs (IN0, IN1) to a total of 12 pairs of differential LVDS clock outputs (OUT0, OUT11). Each buffer block consists of one input and 6 LVDS outputs. The inputs can either be LVDS, LVPECL, or LVCMOS.

The CDCLVD2106 is specifically designed for driving 50- $\Omega$  transmission lines. In case of driving the inputs in single ended mode, the appropriate bias voltage ( $V_{AC\_REF}$ ) should be applied to the unused negative input pin.

Using the control pin (EN), outputs can be either disabled or enabled. If the EN pin is left open two buffers with all outputs are enabled, if switched to a logical "0" both buffers with all outputs are disabled (static logical "0"), if switched to a logical "1", one buffer with six outputs is disabled and another buffer with six outputs is enabled. The part supports a fail safe function. It incorporates an input hysteresis, which prevents random oscillation of the outputs in absence of an input signal.

The device operates in 2.5V supply environment and is characterized from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$  (ambient temperature). The CDCLVD2106 is packaged in small 40-pin, 6-mm x 6-mm QFN package.

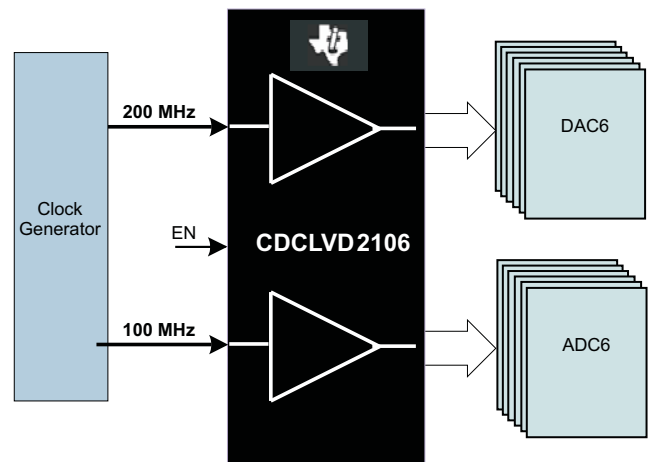


Figure 1. Application Example



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

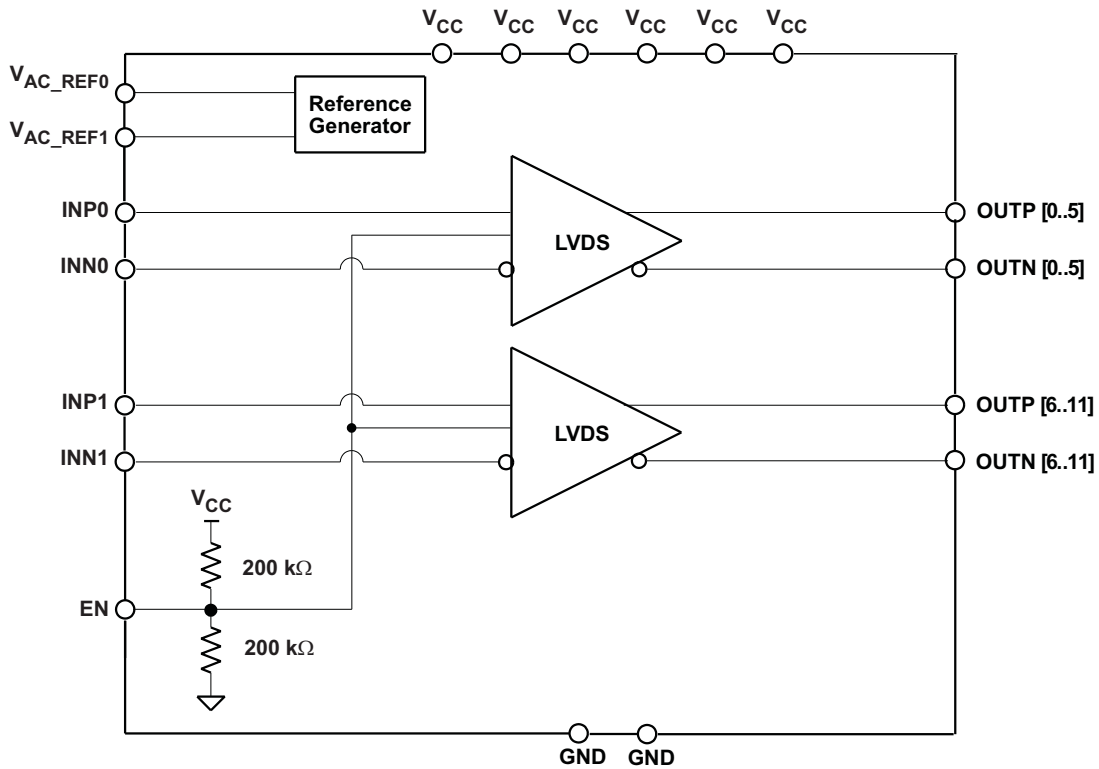
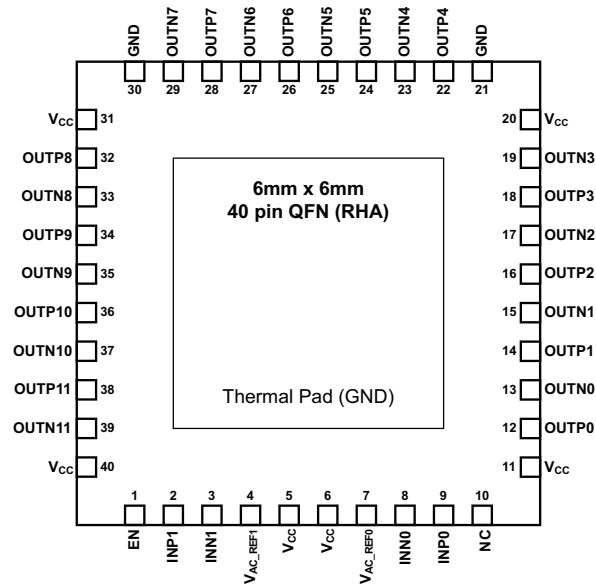


Figure 2. CDCLVD2106 Block Diagram



**PIN FUNCTIONS**

PIN			
NAME	NO.	TYPE	DESCRIPTION
V <sub>CC</sub>	5, 6, 11, 20, 31, 40	Power	2.5V supplies for the device
GND	21, 30	Ground	Device ground
INP0, INN0	9, 8	Input	Differential input pair or single ended input
INP1, INN1	2, 3	Input	Differential redundant input pair or single ended input
OUTP0, OUTN0	12, 13	Output	Differential LVDS output pair no. 0
OUTP1, OUTN1	14, 15	Output	Differential LVDS output pair no. 1
OUTP2, OUTN2	16, 17	Output	Differential LVDS output pair no. 2
OUTP3, OUTN3	18, 19	Output	Differential LVDS output pair no. 3
OUTP4, OUTN4	22, 23	Output	Differential LVDS output pair no. 4
OUTP5, OUTN5	24, 25	Output	Differential LVDS output pair no. 5
OUTP6, OUTN6	26, 27	Output	Differential LVDS output pair no. 6
OUTP7, OUTN7	28, 29	Output	Differential LVDS output pair no. 7
OUTP8, OUTN8	32, 33	Output	Differential LVDS output pair no. 8
OUTP9, OUTN9	34, 35	Output	Differential LVDS output pair no. 9
OUTP10, OUTN10	36, 37	Output	Differential LVDS output pair no. 10
OUTP11, OUTN11	38, 39	Output	Differential LVDS output pair no. 11
V <sub>AC_REF0</sub>	7	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin.
V <sub>AC_REF1</sub>	4	Output	Bias voltage output for capacitive coupled inputs. If used, it is recommended to use a 0.1µF to GND on this pin.
NC	10		No connect
EN	1	Input with internal 200kΩ pull-up and pull-down	Control pin – enables or disables the outputs (See <a href="#">Table 1</a> ).
Thermal Pad		Ground	Device ground. Thermal pad must be soldered to ground. See thermal management recommendations.

**Table 1. Output Control Table**

EN	CLOCK OUTPUTS
0	All outputs disabled (static "0")
Open	All outputs enabled
1	OUT0 to OUT5 enabled and OUT6 to OUT11 disabled (static "0")

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	VALUE	UNIT
Supply voltage range, $V_{CC}$	–0.3 to 2.8	V
Input voltage range, $V_I$	–0.2 to ( $V_{CC} + 0.2$ )	V
Output voltage range, $V_O$	–0.2 to ( $V_{CC} + 0.2$ )	V
Driver short circuit current, $I_{OSD}$	See note <sup>(2)</sup>	
Electrostatic discharge (HBM, 1.5 k $\Omega$ , 100 pF)	>3000	V

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) The outputs can handle permanent short.

## RECOMMENDED OPERATING CONDITIONS

	MIN	TYP	MAX	UNIT
Device supply voltage, $V_{CC}$	2.375	2.5	2.625	V
Ambient temperature, $T_A$	–40		85	°C

## THERMAL INFORMATION

THERMAL METRIC <sup>(1)</sup>		CDCLVD2106	UNITS
		RHA (40 PINS)	
$\theta_{JA}$	Junction-to-ambient thermal resistance	31.0	°C/W
$\theta_{JC(top)}$	Junction-to-case(top) thermal resistance	28.7	
$\theta_{JB}$	Junction-to-board thermal resistance	9.3	
$\psi_{JT}$	Junction-to-top characterization parameter	0.4	
$\psi_{JB}$	Junction-to-board characterization parameter	9.3	
$\theta_{JC(bottom)}$	Junction-to-case(bottom) thermal resistance	3.1	

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## ELECTRICAL CHARACTERISTICS

At  $V_{CC} = 2.375V$  to  $2.625V$ ,  $T_A = -40^\circ C$  to  $85^\circ C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>EN CONTROL INPUT CHARACTERISTICS</b>						
$V_{dI3}$	3 State	Open		$0.5 \times V_{CC}$		V
$V_{dIH}$	Input high voltage		$0.7 \times V_{CC}$			V
$V_{dIL}$	Input low voltage			$0.2 \times V_{CC}$		V
$I_{dIH}$	Input high current	$V_{CC} = 2.625 V$ , $V_{IH} = 2.625 V$			30	$\mu A$
$I_{dIL}$	Input low current	$V_{CC} = 2.625 V$ , $V_{IL} = 0 V$			–30	$\mu A$
$R_{pull(EN)}$	Input pull-up/ pull-down resistor			200		k $\Omega$
<b>2.5V LVC MOS (see Figure 7) INPUT CHARACTERISTICS</b>						
$f_{IN}$	Input frequency				200	MHz
$V_{th}$	Input threshold voltage	External threshold voltage applied to complementary input	1.1		1.5	V
$V_{IH}$	Input high voltage		$V_{th} + 0.1$		$V_{CC}$	V
$V_{IL}$	Input low voltage		0		$V_{th} - 0.1$	V
$I_{IH}$	Input high current	$V_{CC} = 2.625 V$ , $V_{IH} = 2.625 V$			10	$\mu A$
$I_{IL}$	Input low current	$V_{CC} = 2.625 V$ , $V_{IL} = 0 V$			–10	$\mu A$
$\Delta V/\Delta T$	Input edge rate	20%–80%	1.5			V/ns
$C_{IN}$	Input capacitance			2.5		pF

**ELECTRICAL CHARACTERISTICS (continued)**

 At  $V_{CC} = 2.375V$  to  $2.625V$ ,  $T_A = -40^{\circ}C$  to  $85^{\circ}C$  (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>DIFFERENTIAL INPUT CHARACTERISTICS</b>						
$f_{IN}$	Input frequency	Clock input			800	MHz
$V_{IN, DIFF}$	Differential input voltage peak-to-peak	$V_{ICM} = 1.25 V$	0.3		1.6	$V_{PP}$
$V_{ICM}$	Input common mode voltage range	$V_{IN, DIFF, PP} > 0.4 V$	1.0		$V_{CC} - 0.3$	V
$I_{IH}$	Input high current	$V_{CC} = 2.625 V$ , $V_{IH} = 2.625 V$			10	$\mu A$
$I_{IL}$	Input low current	$V_{CC} = 2.625$ , $V_{IL} = 0 V$			-10	$\mu A$
$\Delta V/\Delta T$	Input edge rate	20%–80%	0.75			V/ns
$C_{IN}$	Input capacitance			2.5		pF
<b>LVDS OUTPUT CHARACTERISTICS</b>						
$ V_{OD} $	Differential output voltage magnitude		250		450	mV
$\Delta V_{OD}$	Change in differential output voltage magnitude	$V_{IN, DIFF, PP} = 0.3V$ , $R_L = 100 \Omega$	-15		15	mV
$V_{OC(SS)}$	Steady-state common mode output voltage		1.1		1.375	V
$\Delta V_{OC(SS)}$	Steady-state common mode output voltage	$V_{IN, DIFF, PP} = 0.6V$ , $R_L = 100 \Omega$	-15		15	mV
$V_{ring}$	Output overshoot and undershoot	Percentage of output amplitude $V_{OD}$			10%	
$V_{OS}$	Output ac common mode	$V_{IN, DIFF, PP} = 0.6V$ , $R_L = 100 \Omega$		40	70	$mV_{P-P}$
$I_{OS}$	Short-circuit output current	$V_{OD} = 0 V$			$\pm 24$	mA
$t_{PD}$	Propagation delay	$V_{IN, DIFF, PP} = 0.3 V$		1.5	2.5	ns
$t_{SK, PP}$	Part-to-part skew				600	ps
$t_{SK,O\_WB}$	Within bank output skew				45	ps
$t_{SK,O\_BB}$	Bank-to-bank output skew	Both inputs are phase aligned			75	ps
$t_{SK,P}$	Pulse skew(with 50% duty cycle input)	Crossing-point-to-crossing-point distortion	-50		50	ps
$t_{RJIT}$	Random additive jitter (with 50% duty cycle input)	Edge speed = 0.75 V/ns, 10 kHz – 20 MHz			0.3	ps, RMS
$t_R/t_F$	Output rise/fall time	20% to 80%, 100 $\Omega$ , 5 pF	50		300	ps
$I_{CCSTAT}$	Static supply current	Outputs unterminated, $f = 0$ Hz		27	45	mA
$I_{CC100}$	Supply current	All outputs enabled; $R_L = 100 \Omega$ , $f = 100$ MHz		97	133	mA
$I_{CC800}$	Supply current	All outputs enabled; $R_L = 100 \Omega$ , $f = 800$ MHz		137	177	mA
<b><math>V_{AC\_REF}</math> CHARACTERISTICS</b>						
$V_{AC\_REF}$	Reference output voltage	$V_{CC} = 2.5 V$ , $I_{load} = 100 \mu A$	1.1	1.25	1.35	V

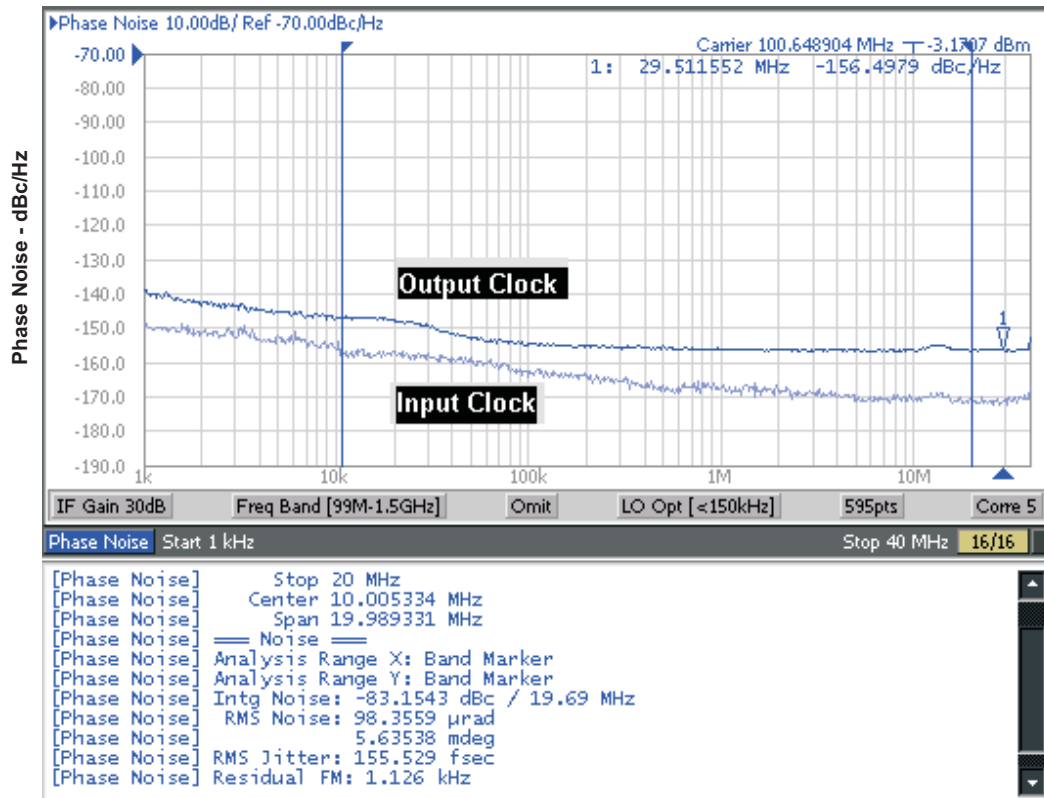
### Typical Additive Phase Noise Characteristics for 100 MHz Clock

PARAMETER		MIN	TYP	MAX	UNIT
phn <sub>100</sub>	Phase noise at 100 Hz offset		-132.9		dBc/Hz
phn <sub>1k</sub>	Phase noise at 1 kHz offset		-138.8		dBc/Hz
phn <sub>10k</sub>	Phase noise at 10 kHz offset		-147.4		dBc/Hz
phn <sub>100k</sub>	Phase noise at 100 kHz offset		-153.6		dBc/Hz
phn <sub>1M</sub>	Phase noise at 1 MHz offset		-155.2		dBc/Hz
phn <sub>10M</sub>	Phase noise at 10 MHz offset		-156.2		dBc/Hz
phn <sub>20M</sub>	Phase noise at 20 MHz offset		-156.6		dBc/Hz
t <sub>RJIT</sub>	Random additive jitter from 10 kHz to 20 MHz		171		fs, RMS

### Typical Additive Phase Noise Characteristics for 737.27 MHz Clock

PARAMETER		MIN	TYP	MAX	UNIT
phn <sub>100</sub>	Phase noise at 100 Hz offset		-80.2		dBc/Hz
phn <sub>1k</sub>	Phase noise at 1 kHz offset		-114.3		dBc/Hz
phn <sub>10k</sub>	Phase noise at 10 kHz offset		-138		dBc/Hz
phn <sub>100k</sub>	Phase noise at 100 kHz offset		-143.9		dBc/Hz
phn <sub>1M</sub>	Phase noise at 1 MHz offset		-145.2		dBc/Hz
phn <sub>10M</sub>	Phase noise at 10 MHz offset		-146.5		dBc/Hz
phn <sub>20M</sub>	Phase noise at 20 MHz offset		-146.6		dBc/Hz
t <sub>RJIT</sub>	Random additive jitter from 10 kHz to 20 MHz		65		fs, RMS

**TYPICAL CHARACTERISTICS**  
**INPUT- AND OUTPUT-CLOCK PHASE NOISES**  
 vs  
**FREQUENCY FROM the CARRIER**  
 (T<sub>A</sub> = 25°C and V<sub>CC</sub> = 2.5V)



Input clock RMS jitter is 32 fs from 10 kHz to 20 MHz and additive RMS jitter is 152 fs

**Figure 3. 100 MHz Input and Output Phase Noise Plots**

**TYPICAL CHARACTERISTICS (continued)**  
**DIFFERENTIAL OUTPUT VOLTAGE**  
**vs**  
**FREQUENCY**

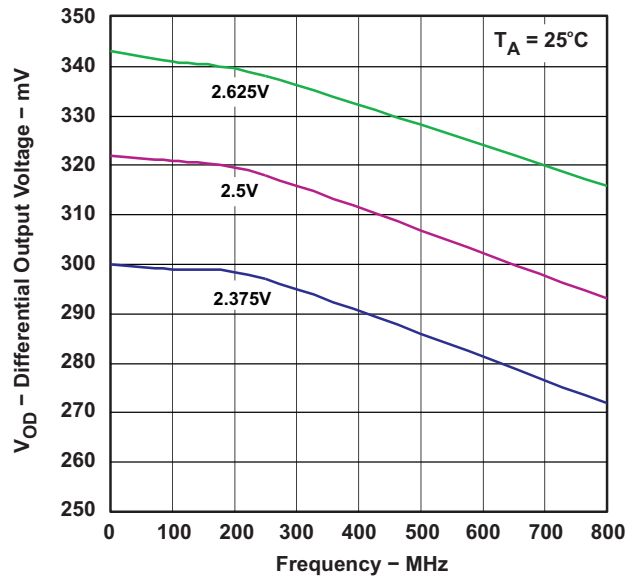


Figure 4. Differential Output Voltage vs Frequency

**TEST CONFIGURATIONS**

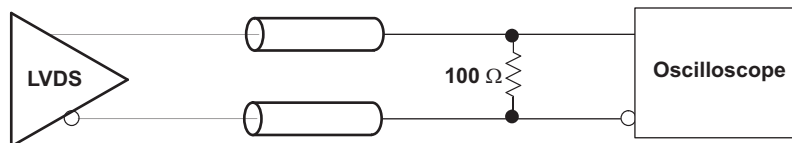


Figure 5. LVDS Output DC Configuration During Device Test

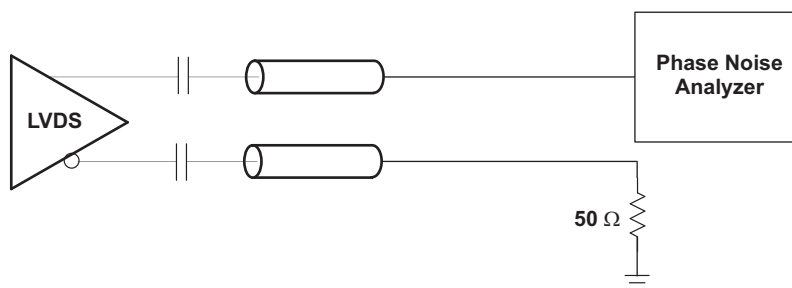


Figure 6. LVDS Output AC Configuration During Device Test



TYPICAL CHARACTERISTICS (continued)

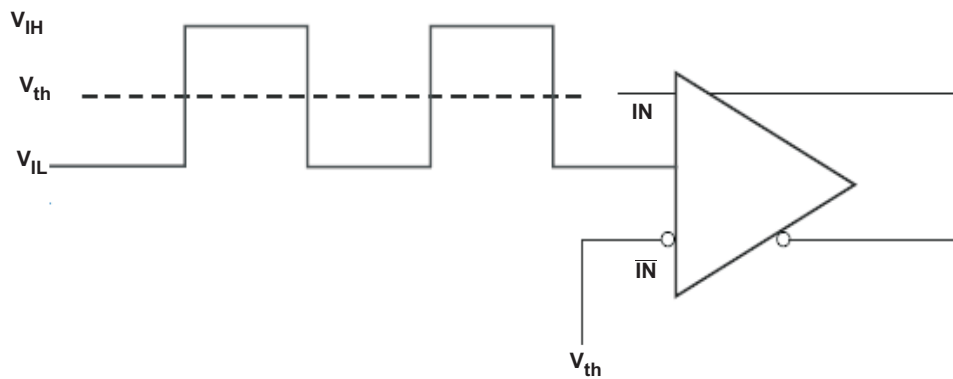


Figure 7. DC Coupled LVCMOS Input During Device Test

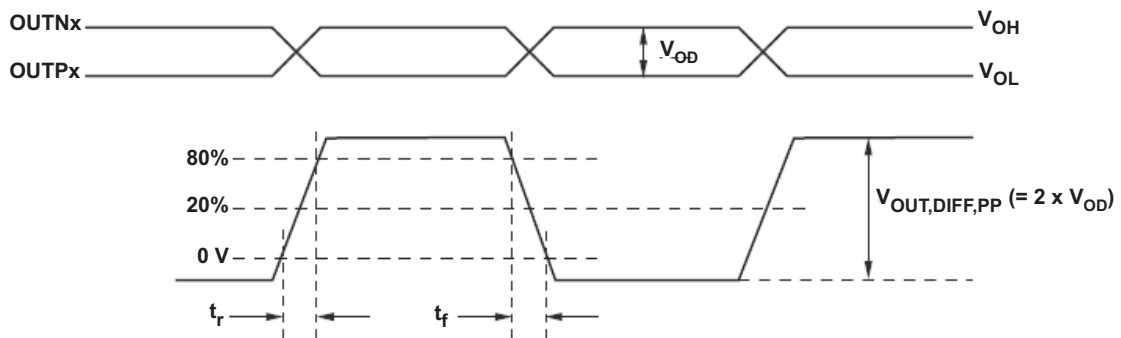
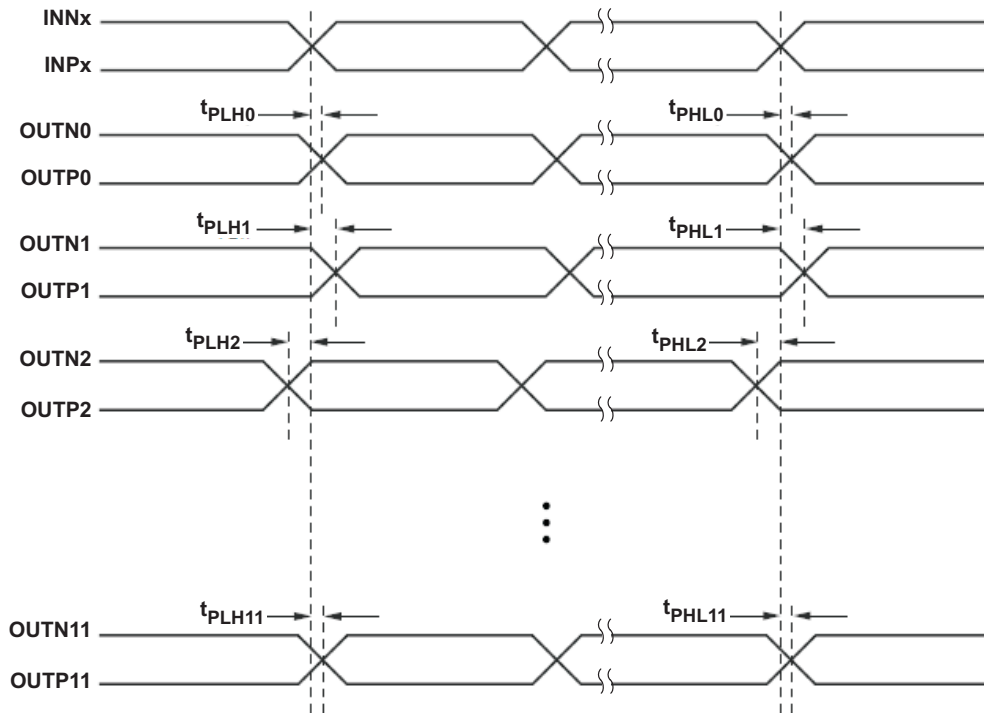


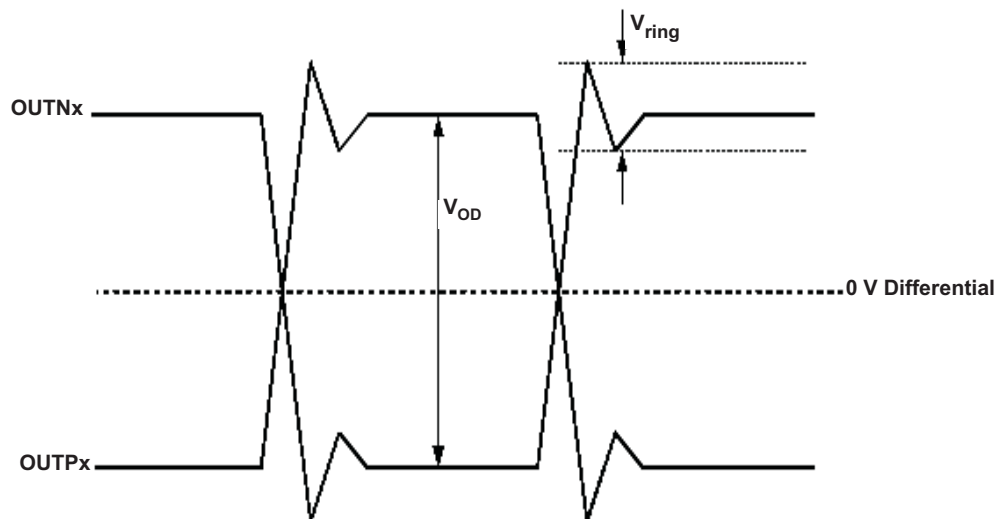
Figure 8. Output Voltage and Rise/Fall Time

**TYPICAL CHARACTERISTICS (continued)**



- A. Output skew is calculated as the greater of the following: As of the difference between the fastest and the slowest  $t_{PLHn}$  or the difference between the fastest and the slowest  $t_{PHLn}$  ( $n = 0, 1, 2, \dots, 11$ )
- B. Part to part skew is calculated as the greater of the following: As the difference between the fastest and the slowest  $t_{PLHn}$  or the difference between the fastest and the slowest  $t_{PHLn}$  across multiple devices ( $n = 0, 1, 2, \dots, 11$ )
- C. Both inputs (IN0 and IN1) are phase aligned

**Figure 9. Output Skew and Part-to-Part Skew**



**Figure 10. Output Overshoot and Undershoot**

TYPICAL CHARACTERISTICS (continued)

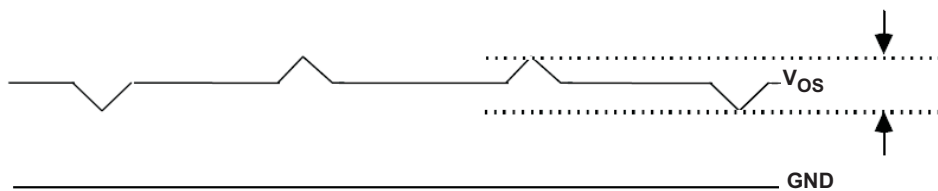


Figure 11. Output AC Common Mode

APPLICATION INFORMATION

THERMAL MANAGEMENT

For reliability and performance reasons, the die temperature should be limited to a maximum of 125°C.

The device package has an exposed pad that provides the primary heat removal path to the printed circuit board (PCB). To maximize the heat dissipation from the package, a thermal landing pattern including multiple vias to a ground plane must be incorporated into the PCB within the footprint of the package. The thermal pad must be soldered down to ensure adequate heat conduction to of the package. Check the mechanical data at the end of the data sheet for land and via pattern examples.

POWER SUPPLY FILTERING

High-performance clock buffers are sensitive to noise on the power supply, which can dramatically increase the additive jitter of the buffer. Thus, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to the application.

Filter capacitors are used to eliminate the low-frequency noise from the power supply, where the bypass capacitors provide the low impedance path for high-frequency noise and guard the power-supply system against the induced fluctuations. These bypass capacitors also provide instantaneous current surges as required by the device and should have low equivalent series resistance (ESR). To properly use the bypass capacitors, they must be placed very close to the power-supply pins and laid out with short loops to minimize inductance. It is recommended to add as many high-frequency (for example, 0.1 μF) bypass capacitors as there are supply pins in the package. It is recommended, but not required, to insert a ferrite bead between the board power supply and the chip power supply that isolates the high-frequency switching noises generated by the clock driver; these beads prevent the switching noise from leaking into the board supply. Choose an appropriate ferrite bead with very low dc resistance because it is imperative to provide adequate isolation between the board supply and the chip supply, as well as to maintain a voltage at the supply pins that is greater than the minimum voltage required for proper operation.

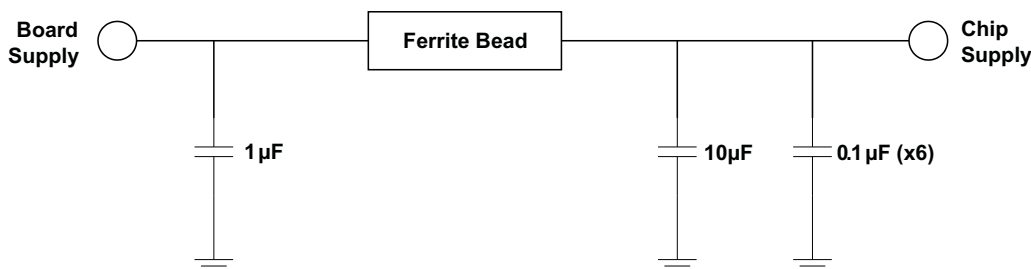
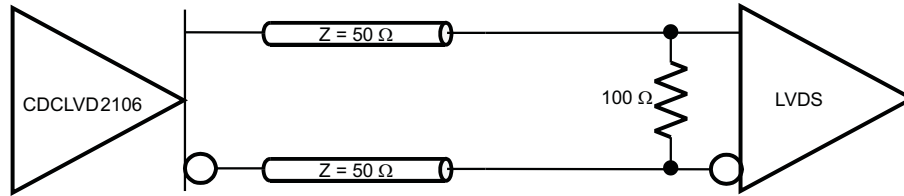


Figure 12. Power Supply Filtering

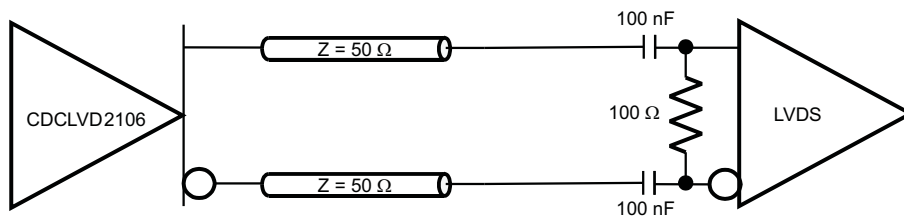
**LVDS OUTPUT TERMINATION**

The proper LVDS termination for signal integrity over two 50 Ω lines is 100 Ω between the outputs on the receiver end. Either dc-coupled termination or ac-coupled termination can be used for LVDS outputs. It is recommended to place termination resistor close to the receiver. If the receiver is internally biased to a voltage different than the output common mode voltage of the CDCLVD2106, ac-coupling should be used. If the LVDS receiver has internal 100 Ω termination, external termination must be omitted.

Unused outputs can be left open without connecting any trace to the output pins.



**Figure 13. LVDS Output DC Termination**



**Figure 14. LVDS Output AC Termination with Receiver Internally Biased**

## INPUT TERMINATION

The CDCLVD2106 inputs can be interfaced with LVDS, LVPECL, or LVCMOS drivers.

LVDS Driver can be connected to CDCLVD2106 inputs with dc or ac coupling as shown [Figure 15](#) and [Figure 16](#) respectively.

[Figure 17](#) shows how to connect LVPECL inputs to the CDCLVD2106. The series resistors are required to reduce the LVPECL signal swing if the signal swing is  $>1.6 V_{PP}$ .

[Figure 18](#) illustrates how to couple a 2.5 V LVCMOS clock input to the CDCLVD2106 directly. The series resistance ( $R_S$ ) should be placed close to the LVCMOS driver if needed. 3.3 V LVCMOS clock input swing needs to be limited to  $V_{IH} \leq V_{CC}$ .

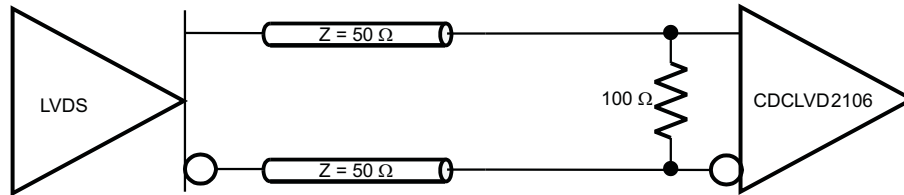


Figure 15. LVDS Clock Driver Connected to CDCLVD2106 Input (DC coupled)

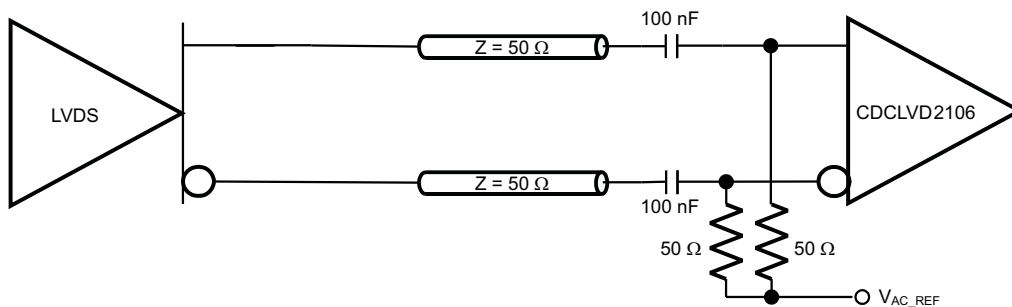


Figure 16. LVDS Clock Driver Connected to CDCLVD2106 Input (AC coupled)

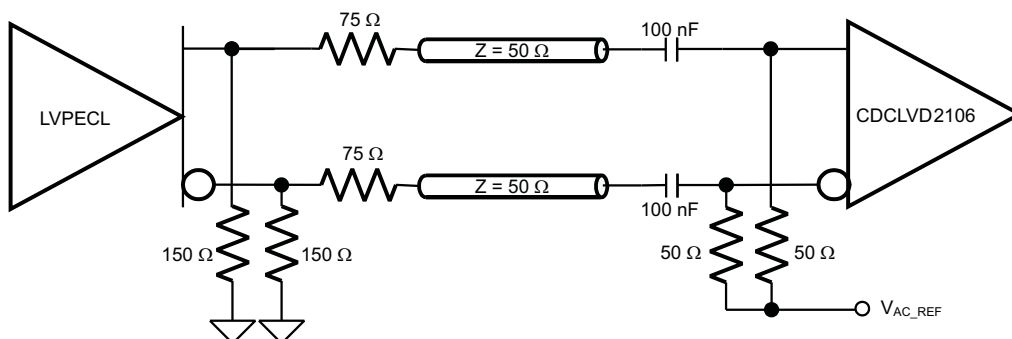
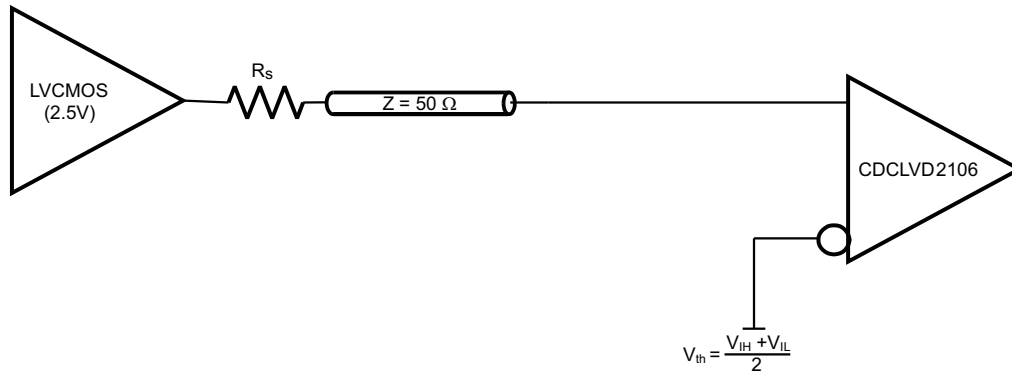


Figure 17. LVPECL Clock Driver Connected to CDCLVD2106 Input



**Figure 18. 2.5V LVC MOS Clock Driver Connected to CDCLVD2106 Input**

If one of the input buffers is used, then the other buffer should be disabled using the control pin EN; and, unused input pins should be grounded by 1-kΩ resistors.

**REVISION HISTORY**

Changes from Original (September 2010) to Revision A	Page
• Changed $t_{SK,O\_BB}$ Bank-to-bank output slew From: 170 ps (Max) To: 75 ps (Max) .....	5
• Deleted the Recommended PCB Layout illustration .....	11
Changes from Revision A (November 2010) to Revision B	Page
• Changed the device status From: Product Preview To: Production .....	1

**PACKAGING INFORMATION**

Orderable part number	Status (1)	Material type (2)	Package   Pins	Package qty   Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
<a href="#">CDCLVD2106RHAR</a>	Active	Production	VQFN (RHA)   40	2500   LARGE T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVD 2106
<a href="#">CDCLVD2106RHAT</a>	Active	Production	VQFN (RHA)   40	250   SMALL T&R	Yes	NIPDAU	Level-3-260C-168 HR	-40 to 85	CDCLVD 2106

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

**Important Information and Disclaimer:**The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCLVD2106RHAR	VQFN	RHA	40	2500	330.0	16.4	6.3	6.3	1.5	12.0	16.0	Q2



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCLVD2106RHAR	VQFN	RHA	40	2500	350.0	350.0	43.0

## GENERIC PACKAGE VIEW

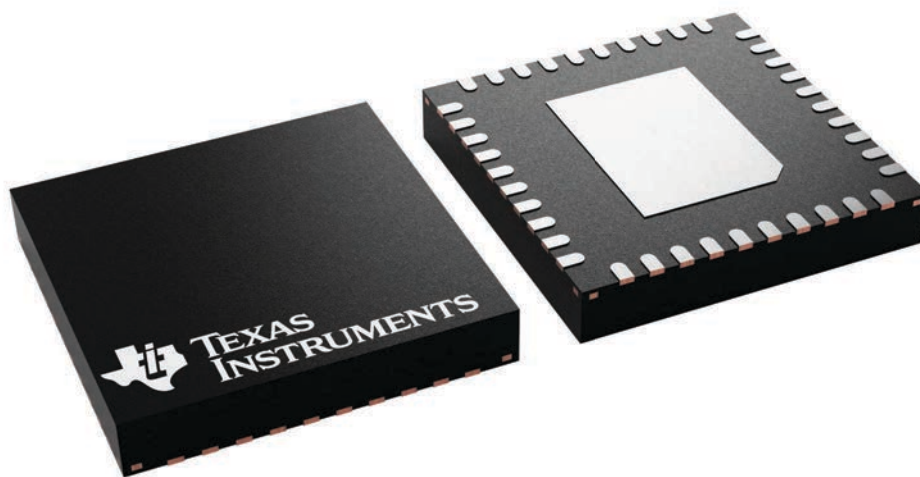
**RHA 40**

**VQFN - 1 mm max height**

6 x 6, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated