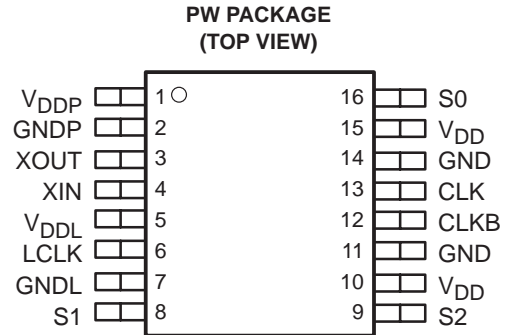


- **400-MHz Differential Clock Source for Direct Rambus Memory Systems for an 800-MHz Data Transfer Rate**
- **Operates From Two (3.3-V and 1.80-V) Power Supplies With 180 mW (Typ) at 400 MHz Total**
- **Packaged in a Thin Shrink Small-Outline Package (PW)**
- **External Crystal Required for Input**

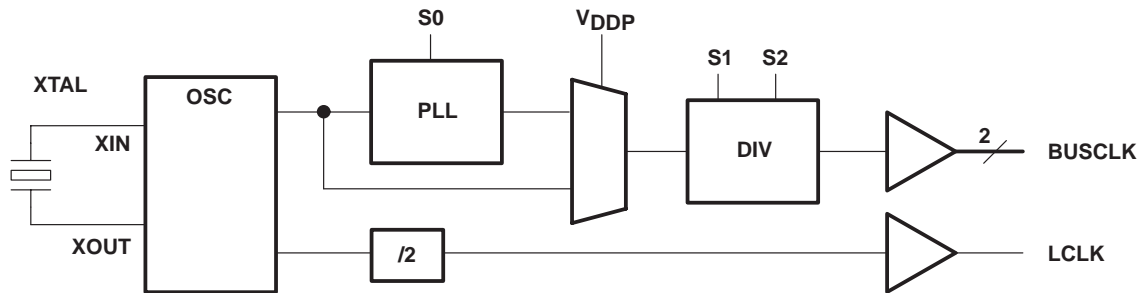


## description

The Direct Rambus clock generator – lite (DRCG-Lite) is an independent crystal clock generator. It performs clock multiplication using PLL, sourced by an internal crystal oscillator. It provides one differential, high-speed Rambus channel compatible output pair. Also, one single-ended output is available to deliver 1/2 of the crystal frequency. The Rambus channel operates at up to 400 MHz with an option to select 300 MHz as well. The desired crystal is a 18.75-MHz crystal in a series resonance fundamental application.

The CDCR61A is characterized for operation over free-air temperatures of 0°C to 85°C.

## functional block diagram



**BUSCLK FREQUENCY SETTINGS**

S0	M (PLL MULTIPLIER)
0	16
1 or Open	64/3

**FUNCTION TABLE**

VDDP	S1	S2	MODE	CLK	CLKB	LCLK
ON	0	0	Normal	CLK	CLKB	XIN divided by 2
ON	1	1	Normal	CLK	CLKB	XIN divided by 2
ON	0	1	Test	Divided by 2	Divided by 2	XIN divided by 2
ON	1	0	Test	Divided by 4	Divided by 4	XIN divided by 2
0 V	0	0	Test	XIN	XIN (invert)	XIN divided by 2
0 V	1	1	Test	XIN	XIN (invert)	XIN divided by 2
0 V	0	1	Test	XIN divided by 2	XIN (invert) divided by 2	XIN divided by 2
0 V	1	0	Test	XIN divided by 4	XIN (invert) divided by 4	XIN divided by 2



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# CDCR61A DIRECT RAMBUS™ CLOCK GENERATOR – LITE

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## Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
CLK	13	O	Output clock, connect to Rambus channel
CLKB	12	O	Output clock (complement), connect to Rambus channel
GNDP, GNDL, GND	2, 7, 11, 14		Ground
LCLK	6	O	LVC MOS output, 1/2 of crystal frequency
S0, S1, S2	16, 8, 9	I	LVTTTL level logic select terminal for function selection
VDD	10, 15		Power supply, 3.3 V
VDDP	1		Power supply for PLL, 3.3 V (0 V for Test mode)
VDDL	5		Power supply for LCLK, 1.8 V
XIN	4	I	Reference crystal input
XOUT	3	O	Reference crystal feedback

### absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

Supply voltage range, $V_{DD}$ or $V_{DDP}$ (see Note 1)	–0.5 V to 4 V
Supply voltage range, $V_{DDL}$ (see Note 1)	–0.5 V to 4 V
Input voltage range, $V_I$ , at any input terminal	–0.5 V to $V_{DD} + 0.5$ V
Output voltage range, $V_O$ , at any output terminal (CLK, CLKB)	–0.5 V to $V_{DD} + 0.5$ V
Output voltage range, $V_O$ , at any output terminal (LCLK)	–0.5 V to $V_{DDL} + 0.5$ V
ESD rating (MIL-STD 883C, Method 3015)	> 2 kV, Machine Model >200 V
Continuous total power dissipation	see Dissipation Rating Table
Operating free-air temperature range, $T_A$	0°C to 85°C
Storage temperature range, $T_{stg}$	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25^\circ\text{C}$ POWER RATING	DERATING FACTOR ABOVE $T_A = 25^\circ\text{C}^\ddagger$	$T_A = 85^\circ\text{C}$ POWER RATING
PW	1400 mW	11 mW/°C	740 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.



### recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V <sub>DD</sub>		3	3.3	3.6	V
LCLK supply voltage, V <sub>DDL</sub>		1.7	1.8	2.1	V
Low-level input voltage, V <sub>IL</sub>	S0	0.35×V <sub>DD</sub>			V
	S1, S2	0.35×V <sub>DD</sub>			
High-level input voltage, V <sub>IH</sub>	S0	0.65×V <sub>DD</sub>			V
	S1, S2	0.65×V <sub>DD</sub>			
Internal pullup resistance	S0	10	55	100	kΩ
	S1, S2	90	145	250	
Low-level output current, I <sub>OL</sub>	CLK, CLKB	16			mA
	LCLK	10			
High-level output current, I <sub>OH</sub>	CLK, CLKB	-16			mA
	LCLK	-10			
Input frequency at crystal input		14.0625	18.75		MHz
Input capacitance (CMOS), C <sub>I</sub> †	S0, S1, S2	2.5			pF
	XIN, XOUT	20			
Operating free-air temperature, T <sub>A</sub>		0		85	°C

† Capacitance measured at f = 1 MHz, dc bias = 0.9 V, and V<sub>AC</sub> < 100 mV

### timing requirements

	MIN	MAX	UNIT
Clock cycle time, t <sub>(cycle)</sub>	2.5	3.7	ns
Input slew rate, SR	0.5	4	V/ns
State transition latency (V <sub>DDX</sub> or S0 to CLKs – normal mode), t <sub>(STL)</sub>		3	ms

### crystal specifications

	MIN	MAX	UNIT
Frequency	14.0625	18.75	MHz
Frequency tolerance (at 25°C ±3°C)	-15	15	ppm
Equivalent resistance (C <sub>L</sub> = 10 pF)		100	Ω
Temperature drift (-10°C to 75°C)		10	ppm
Drive level	0.01	1500	μW
Motional inductance	20.7	25.3	mH
Insulation resistance	500		MΩ
Spurious attenuation ratio (at frequency ±500 kHz)	3		dB
Overtone spurious	8		dB

# CDCR61A DIRECT RAMBUS™ CLOCK GENERATOR – LITE

SCAS626 – FEBRUARY 2000

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V <sub>O(X)</sub>	Differential crossing-point output voltage	See Figures 1 and 7		1.25		1.85	V
V <sub>O(PP)</sub>	Peak-to-peak output voltage swing, single ended	V <sub>OH</sub> – V <sub>OL</sub>	See Figure 1	0.4		0.7	V
V <sub>IK</sub>	Input clamp voltage	V <sub>DD</sub> = 3 V,	I <sub>I</sub> = –18 mA			–1.2	V
R <sub>I</sub>	Input resistance	XIN, XOUT	V <sub>DD</sub> = 3.3 V, V <sub>I</sub> = V <sub>O</sub>		>50		kΩ
I <sub>IH</sub>	High-level input current	XOUT	V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 2 V			27	mA
		S0	V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = V <sub>DD</sub>			10	μA
		S1, S2	V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = V <sub>DD</sub>			10	μA
I <sub>IL</sub>	Low-level input current	XOUT	V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 0 V			–5.7	mA
		S0	V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = 0 V	–30		–100	μA
		S1, S2	V <sub>DD</sub> = 3.6 V, V <sub>I</sub> = 0 V	–10		–50	μA
V <sub>OH</sub>	High-level output voltage	CLK, CLKB	See Figure 1			2.1	V
			V <sub>DD</sub> = min to max, I <sub>OH</sub> = –1 mA	V <sub>DD</sub> – 0.1 V			
			V <sub>DD</sub> = 3 V, I <sub>OH</sub> = –16 mA	2.2			
		LCLK	V <sub>DDL</sub> = min to max, I <sub>OH</sub> = –10 mA	V <sub>DDL</sub> – 0.45 V	V <sub>DDL</sub>		
V <sub>OL</sub>	Low-level output voltage	CLK, CLKB	See Figure 1		1		V
			V <sub>DD</sub> = min to max, I <sub>OL</sub> = 1 mA		0.1		
			V <sub>DD</sub> = 3 V, I <sub>OL</sub> = 16 mA		0.5		
		LCLK	V <sub>DDL</sub> = min to max, I <sub>OL</sub> = 10 mA	0	0.45		
I <sub>OH</sub>	High-level output current	CLK, CLKB	V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1 V	–32	–52	mA	
			V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		–51		
			V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 3.135 V	–14.5	–21		
		LCLK	V <sub>DDL</sub> = 1.7 V, V <sub>O</sub> = 0.5 V	–11	–26		
			V <sub>DDL</sub> = 1.8 V, V <sub>O</sub> = 0.9 V		–28		
			V <sub>DDL</sub> = 2.1 V, V <sub>O</sub> = 1.6 V	–24.5	–35		
I <sub>OL</sub>	Low-level output current	CLK, CLKB	V <sub>DD</sub> = 3.135 V, V <sub>O</sub> = 1.95 V	43	61.5	mA	
			V <sub>DD</sub> = 3.3 V, V <sub>O</sub> = 1.65 V		65		
			V <sub>DD</sub> = 3.465 V, V <sub>O</sub> = 0.4 V	25.5	36		
		LCLK	V <sub>DDL</sub> = 1.7 V, V <sub>O</sub> = 1.2 V	11	27		
			V <sub>DDL</sub> = 1.8 V, V <sub>O</sub> = 0.9 V		30		
			V <sub>DDL</sub> = 2.1 V, V <sub>O</sub> = 0.5 V	28	38		
r <sub>OH</sub>	High-level dynamic output resistance§	ΔI <sub>O</sub> – 14.5 mA to ΔI <sub>O</sub> – 16.5 mA		12	25	40	Ω
r <sub>OL</sub>	Low-level dynamic output resistance§	ΔI <sub>O</sub> + 14.5 mA to ΔI <sub>O</sub> + 16.5 mA		12	17	40	Ω
C <sub>O</sub>	Output capacitance	CLK, CLKB				3	pF
		LCLK				3	

† V<sub>DD</sub> refers to any of the following; V<sub>DD</sub>, V<sub>DDL</sub>, and V<sub>DDP</sub>

‡ All typical values are at V<sub>DD</sub> = 3.3 V, V<sub>DDL</sub> = 1.8 V, T<sub>A</sub> = 25°C.

§ r<sub>O</sub> = ΔV<sub>O</sub>/ΔI<sub>O</sub>. This is defined at the output terminals, not at the measurement point of Figure 1.



**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)**

PARAMETER		TEST CONDITIONS†	MIN	TYP‡	MAX	UNIT
I <sub>DD</sub>	Static supply current	Outputs high or low (V <sub>DDP</sub> = 0 V)			6.5	mA
I <sub>DDL</sub>	Static supply current (LVCMOS)	Outputs high or low (V <sub>DDP</sub> = 0 V)			50	μA
I <sub>DD(NORMAL)</sub>	Supply current in normal state	300 MHz			39	mA
		400 MHz			50	mA
I <sub>DDL(NORMAL)</sub>	Supply current in normal state (LVCMOS)	400 MHz			8	mA

† V<sub>DD</sub> refers to any of the following; V<sub>DD</sub>, V<sub>DDL</sub>, and V<sub>DDP</sub>

‡ All typical values are at V<sub>DD</sub> = 3.3 V, V<sub>DDL</sub> = 1.8 V, T<sub>A</sub> = 25°C.

**switching characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
t <sub>(cycle)</sub>	Clock cycle time (CLK, CLKB)		2.5		3.7	ns
t <sub>cj</sub>	Total jitter over 1, 2, 3, 4, 5, or 6 clock cycles‡	300 MHz	See Figure 3		140	ps
		400 MHz			100	
t <sub>jL</sub>	Long-term jitter	300 MHz	See Figure 4		400	ps
		400 MHz			300	
t <sub>DC</sub>	Output duty cycle over 10,000 cycles	See Figure 5	45%		55%	
t <sub>DC,ERR</sub>	Output cycle-to-cycle duty cycle error	300 MHz	See Figure 6		70	ps
		400 MHz			55	
t <sub>r</sub> , t <sub>f</sub>	Output rise and fall times (measured at 20%-80% of output voltage)#	CLK, CLKB	See Figure 9,	160	400	ps
Δt	Difference between rise and fall times on a single device (20%–80%)  t <sub>f</sub> – t <sub>r</sub>  #		See Figure 9,		100	ps
t <sub>c(LCLK)</sub>	Clock cycle time (LCLK)		106.6		142.2	ns
t <sub>(cj)</sub>	LCLK cycle jitter§	See Figure 11	–0.2		0.2	ns
t <sub>(cj10)</sub>	LCLK 10-cycle jitter§¶	See Figure 11	–1.3 t <sub>(cj)</sub>		1.3 t <sub>(cj)</sub>	ns
t <sub>DC</sub>	Output duty cycle	LCLK	40%		60%	
t <sub>r</sub> , t <sub>f</sub>	Output rise and fall times (measured at 20%-80% of output voltage)	LCLK	See Figure 9		1	ns
PLL loop bandwidth		f <sub>mod</sub> = 50 kHz			–3	dB
		f <sub>mod</sub> = 8 MHz			–20	

† All typical values are at V<sub>DD</sub> = 3.3 V, T<sub>A</sub> = 25°C.

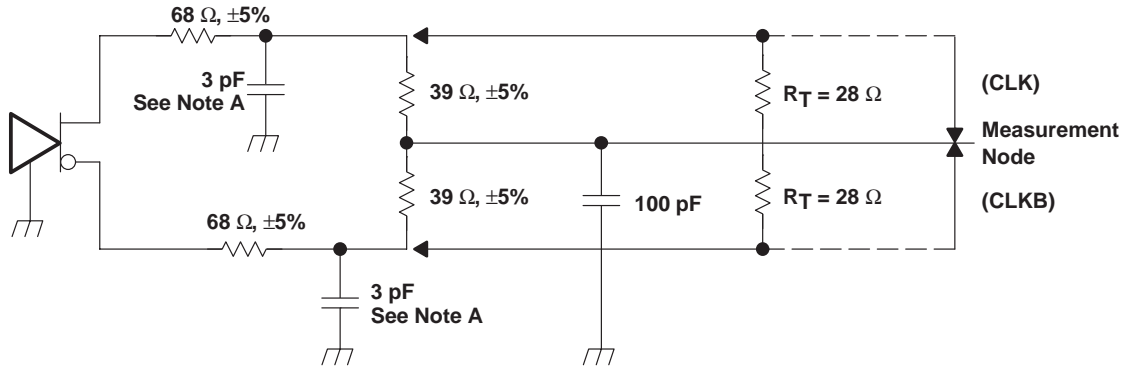
‡ Output short-term jitter specification is peak-to-peak (see Figure 9).

§ LCLK cycle jitter and 10-cycle jitter are defined as the difference between the measured period and the nominal period.

¶ LCLK 10-cycle jitter specification is based on the measured value of LCLK cycle jitter.

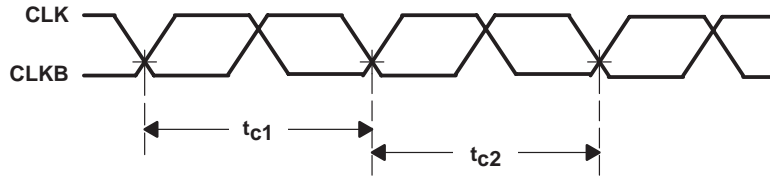
# V<sub>DD</sub> = 3.3 V

PARAMETER MEASUREMENT INFORMATION



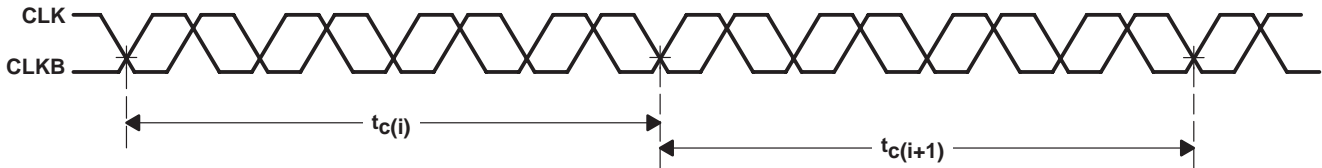
NOTE A: These capacitors represent parasitic capacitance. No discrete capacitors are used on the test board during device characterization.

Figure 1. Test Load and Voltage Definitions (V<sub>O(STOP)</sub>, V<sub>O(X)</sub>, V<sub>O</sub>, V<sub>OH</sub>, V<sub>OL</sub>)



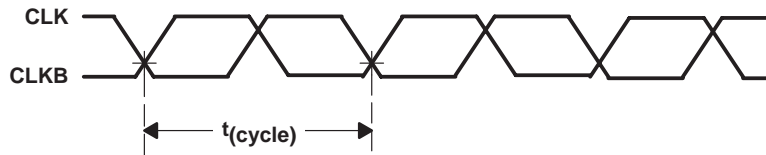
Cycle-to-cycle jitter = | t<sub>c1</sub> - t<sub>c2</sub> | over 10000 consecutive cycles

Figure 2. Cycle-to-Cycle Jitter



t<sub>c(i)</sub> = nominal expected time  
 Cycle-to-cycle jitter = | t<sub>c(i)</sub> - t<sub>c(i+1)</sub> | over 10000 consecutive cycles

Figure 3. Short-Term Cycle-to-Cycle Jitter over 2, 3, 4, or 6 Cycles



t<sub>JL</sub> = | t<sub>(cycle), max</sub> - t<sub>(cycle), min</sub> | over 10000 consecutive cycles

Figure 4. Long-Term Jitter

PARAMETER MEASUREMENT INFORMATION

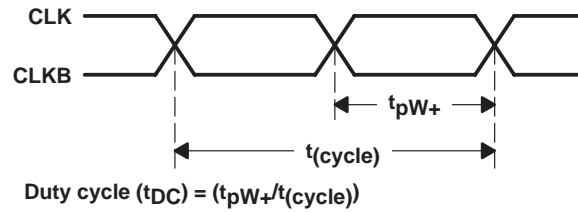


Figure 5. Output Duty Cycle

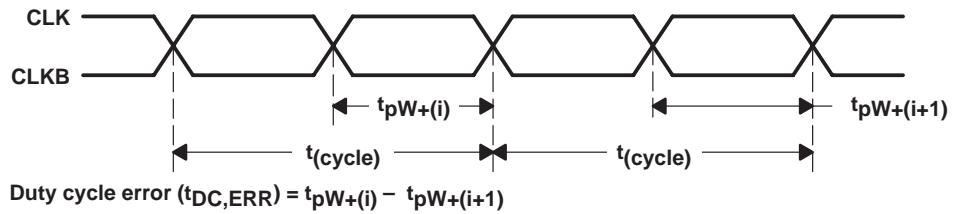


Figure 6. Duty Cycle Error (Cycle-to-Cycle)

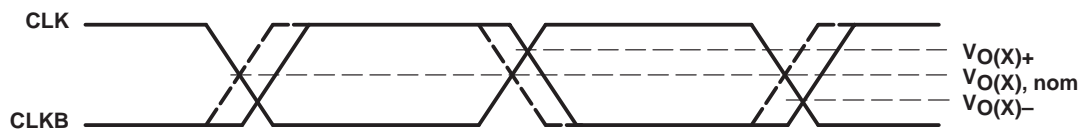


Figure 7. Crossing-Point Voltage

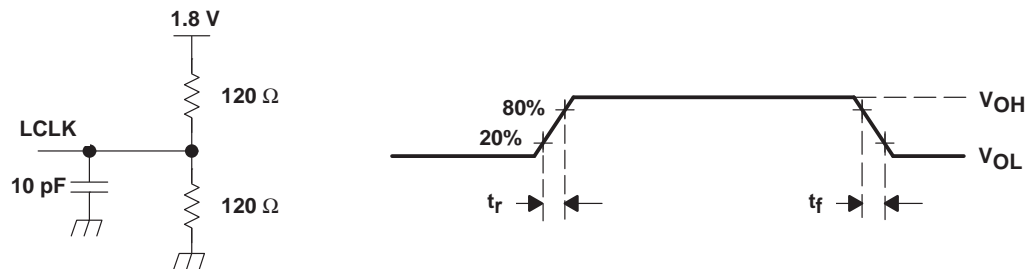


Figure 8. LCLK Test Load Circuit and Voltage Waveform for CLK/CLKB and LCLK

PARAMETER MEASUREMENT INFORMATION

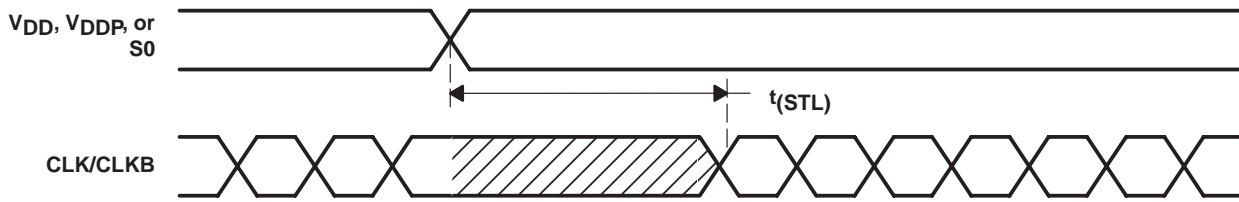


Figure 9. PLL Frequency Transition Timing

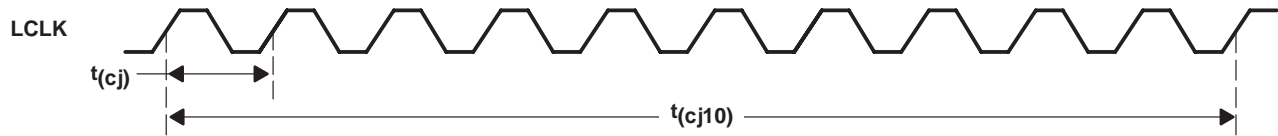


Figure 10. LCLK Jitter



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CDCR61APW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKR61A	<a href="#">Samples</a>
CDCR61APWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKR61A	<a href="#">Samples</a>
CDCR61APWRG4	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CKR61A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

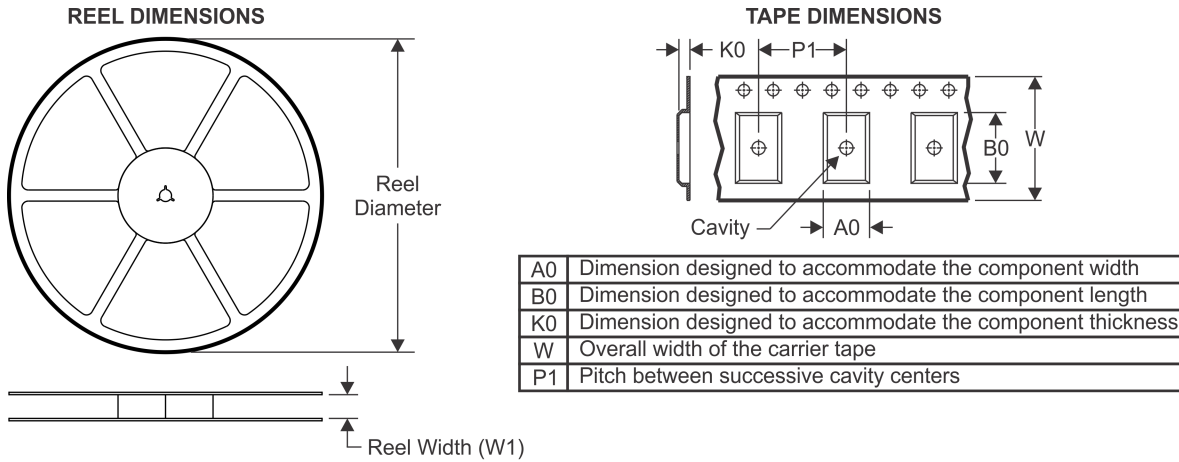
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CDCR61APWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CDCR61APWR	TSSOP	PW	16	2000	853.0	449.0	35.0



4220204/A 02/2017

**NOTES:**

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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