1 Features

- Ultra-low $C_{iss}$ and $C_{oss}$
- Ultra-low $Q_g$ and $Q_{gd}$
- Ultra-small footprint
  - 0.73 mm × 0.64 mm
- Ultra-low profile
  - 0.36-mm max height
- Integrated ESD protection diode
  - Rated > 4-kV HBM
  - Rated > 2-kV CDM
- Lead and halogen free
- RoHS compliant

2 Applications

- Optimized for load switch applications
- Optimized for general purpose switching applications
- Battery applications
- Handheld and mobile applications

3 Description

This 20-V, 990-mΩ, N-Channel FemtoFET™ MOSFET is designed and optimized to minimize the footprint in many handheld and mobile applications. Ultra-low capacitance improves switching speeds. When used in data line applications, the low capacitance minimizes noise coupling. This technology is capable of replacing standard small signal MOSFETs while providing a substantial reduction in footprint size.
Table of Contents

1 Features ................................................................. 1
2 Applications ............................................................. 1
3 Description ............................................................... 1
4 Revision History ....................................................... 2
5 Specifications ........................................................... 3
  5.1 Electrical Characteristics ......................................... 3
  5.2 Thermal Information ............................................... 3
  5.3 Typical MOSFET Characteristics ............................... 4
6 Device and Documentation Support ................................. 6
  6.1 Receiving Notification of Documentation Updates ............ 6
  6.2 Trademarks ........................................................... 6
7 Mechanical, Packaging, and Orderable Information .......... 7
  7.1 Mechanical Dimensions .......................................... 7
  7.2 Recommended Minimum PCB Layout ......................... 8
  7.3 Recommended Stencil Pattern ................................... 8

4 Revision History
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (July 2017) to Revision B (February 2022)  Page
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height ........................................ 1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm ........................................... 1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm ........................................... 7
• Added FemtoFET Surface Mount Guide note ................................................................. 8

Changes from Revision A (July 2017) to Revision B (November 2018)  Page
• Changed ultra-low profile bullet from 0.35 mm to 0.36 mm in height ........................................ 1
• Updated ultra-low profile image height from 0.35 mm to 0.36 mm ........................................... 1
• Changed ultra-low profile image height from 0.35 mm to 0.36 mm ........................................... 7
• Added FemtoFET Surface Mount Guide note ................................................................. 8
5 Specifications

5.1 Electrical Characteristics

\( T_A = 25^\circ\text{C} \) (unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>STATIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( BV_{DSS} ) Drain-to-source voltage</td>
<td>( V_{GS} = 0 \text{ V}, I_{DS} = 250 \mu\text{A} )</td>
<td>20</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( I_{DSS} ) Drain-to-Source leakage current</td>
<td>( V_{GS} = 0 \text{ V}, V_{DS} = 16 \text{ V} )</td>
<td>50</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( I_{GS} ) Gate-to-Source leakage current</td>
<td>( V_{DS} = 0 \text{ V}, V_{GS} = 10 \text{ V} )</td>
<td>25</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( V_{GS(th)} ) Gate-to-source threshold voltage</td>
<td>( V_{DS} = V_{GS}, I_{DS} = 2.5 \mu\text{A} )</td>
<td>0.85</td>
<td>1.10</td>
<td>1.35</td>
<td>V</td>
</tr>
<tr>
<td>( R_{DS(on)} ) Drain-to-source on-resistance</td>
<td>( V_{GS} = 2.5 \text{ V}, I_{DS} = 0.1 \text{ A} )</td>
<td>2220</td>
<td>4000</td>
<td></td>
<td>mΩ</td>
</tr>
<tr>
<td>( g_{fs} ) Transconductance</td>
<td>( V_{DS} = 2 \text{ V}, I_{DS} = 0.1 \text{ A} )</td>
<td>0.64</td>
<td></td>
<td></td>
<td>S</td>
</tr>
<tr>
<td><strong>DYNAMIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( C_{iss} ) Input capacitance</td>
<td>( V_{GS} = 0 \text{ V}, V_{DS} = 10 \text{ V}, f = 1 \text{ MHz} )</td>
<td>8.1</td>
<td>10.5</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_{oss} ) Output capacitance</td>
<td></td>
<td>5.9</td>
<td>7.7</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( C_{rss} ) Reverse transfer capacitance</td>
<td></td>
<td>0.13</td>
<td>0.17</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( R_G ) Series gate resistance</td>
<td></td>
<td>9.6</td>
<td></td>
<td></td>
<td>Ω</td>
</tr>
<tr>
<td>( Q_g ) Gate charge total (4.5 V)</td>
<td>( V_{DS} = 10 \text{ V}, I_{DS} = 0.1 \text{ A} )</td>
<td>0.216</td>
<td>0.281</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{gd} ) Gate charge gate-to-drain</td>
<td></td>
<td>0.027</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{gs} ) Gate charge gate-to-source</td>
<td></td>
<td>0.077</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Q_{g(th)} ) Gate charge at ( V_{th} )</td>
<td></td>
<td>0.048</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( t_{d(on)} ) Turnon delay time</td>
<td>( V_{DS} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_{DS} = 0.1 \text{ A}, R_G = 0 \text{ Ω} )</td>
<td>3</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_r ) Rise time</td>
<td></td>
<td>1</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_{d(off)} ) Turnoff delay time</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_f ) Fall time</td>
<td></td>
<td>7</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>DIODE CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{SD} ) Diode forward voltage</td>
<td>( I_{SD} = 0.1 \text{ A}, V_{GS} = 0 \text{ V} )</td>
<td>0.85</td>
<td>1</td>
<td></td>
<td>V</td>
</tr>
</tbody>
</table>

5.2 Thermal Information

\( T_A = 25^\circ\text{C} \) (unless otherwise stated)

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>TYPICAL VALUES</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{θJA} ) Junction-to-ambient thermal resistance(^{(1)})</td>
<td>90</td>
<td>°C/W</td>
</tr>
<tr>
<td>( R_{θJA} ) Junction-to-ambient thermal resistance(^{(2)})</td>
<td>255</td>
<td>°C/W</td>
</tr>
</tbody>
</table>

---

(1) Device mounted on FR4 material with 1-in\(^2\) (6.45-cm\(^2\)), 2-oz (0.071-mm) thick Cu.
(2) Device mounted on FR4 material with minimum Cu mounting area.
5.3 Typical MOSFET Characteristics

$T_A = 25^\circ C$ (unless otherwise stated)

![Saturation Characteristics](image1.png)

**Figure 5-1. Saturation Characteristics**

![Transfer Characteristics](image2.png)

**Figure 5-2. Transfer Characteristics**

![Transient Thermal Impedance](image3.png)

**Figure 5-3. Transient Thermal Impedance**

![Gate Charge](image4.png)

**Figure 5-4. Gate Charge**

![Capacitance](image5.png)

**Figure 5-5. Capacitance**
**Figure 5-6.** Threshold Voltage vs Temperature

**Figure 5-7.** On-State Resistance vs Gate-to-Source Voltage

**Figure 5-8.** Normalized On-State Resistance vs Temperature

**Figure 5-9.** Typical Diode Forward Voltage

**Figure 5-10.** Maximum Safe Operating Area

**Figure 5-11.** Maximum Drain Current vs Temperature
6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Trademarks

FemtoFET™ is a trademark of Texas Instruments.
All trademarks are the property of their respective owners.
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Mechanical Dimensions

A. All linear dimensions are in millimeters (dimensions and tolerancing per AME T14.5M-1994).
B. This drawing is subject to change without notice.
C. This package is a lead-free solder land design.

Table 7-1. Pin Configuration

<table>
<thead>
<tr>
<th>POSITION</th>
<th>DESIGNATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1</td>
<td>Gate</td>
</tr>
<tr>
<td>Pin 2</td>
<td>Source</td>
</tr>
<tr>
<td>Pin 3</td>
<td>Drain</td>
</tr>
</tbody>
</table>
7.2 Recommended Minimum PCB Layout

A. All dimensions are in millimeters.
B. For more information, see *FemtoFET Surface Mount Guide* (SLRA003D).

7.3 Recommended Stencil Pattern

A. All dimensions are in millimeters.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD15380F3</td>
<td>ACTIVE</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIAU Level-1-260C-UNLIM</td>
<td>55 to 150</td>
<td>6</td>
<td>Samples</td>
<td></td>
</tr>
<tr>
<td>CSD15380F3T</td>
<td>ACTIVE</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIAU Level-1-260C-UNLIM</td>
<td>55 to 150</td>
<td>6</td>
<td>Samples</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE:** Product device recommended for new designs.
- **LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "--" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

- Reel Diameter
- Reel Width (W1)

**TAPE DIMENSIONS**

- A0: Dimension designed to accommodate the component width
- B0: Dimension designed to accommodate the component length
- K0: Dimension designed to accommodate the component thickness
- W: Overall width of the carrier tape
- P1: Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**

- Pocket Quadrants
- Sprocket Holes
- User Direction of Feed

*All dimensions are nominal

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter (mm)</th>
<th>Reel Width W1 (mm)</th>
<th>A0 (mm)</th>
<th>B0 (mm)</th>
<th>K0 (mm)</th>
<th>P1 (mm)</th>
<th>W (mm)</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD15380F3</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>3000</td>
<td>180.0</td>
<td>8.4</td>
<td>1.94</td>
<td>0.79</td>
<td>0.44</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>CSD15380F3</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>3000</td>
<td>178.0</td>
<td>8.4</td>
<td>0.7</td>
<td>0.79</td>
<td>0.44</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>CSD15380F3T</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>250</td>
<td>180.0</td>
<td>8.4</td>
<td>1.94</td>
<td>0.79</td>
<td>0.44</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>CSD15380F3T</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>250</td>
<td>178.0</td>
<td>8.4</td>
<td>0.7</td>
<td>0.79</td>
<td>0.44</td>
<td>4.0</td>
<td>8.0</td>
<td>Q2</td>
</tr>
<tr>
<td>Device</td>
<td>Package Type</td>
<td>Package Drawing</td>
<td>Pins</td>
<td>SPQ</td>
<td>Length (mm)</td>
<td>Width (mm)</td>
<td>Height (mm)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>------------</td>
<td>--------------</td>
<td>-----------------</td>
<td>------</td>
<td>-----</td>
<td>-------------</td>
<td>------------</td>
<td>-------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSD15380F3</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>3000</td>
<td>182.0</td>
<td>182.0</td>
<td>20.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSD15380F3</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>3000</td>
<td>220.0</td>
<td>220.0</td>
<td>35.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSD15380F3T</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>250</td>
<td>182.0</td>
<td>182.0</td>
<td>20.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>CSD15380F3T</td>
<td>PICOSTAR</td>
<td>YJM</td>
<td>3</td>
<td>250</td>
<td>220.0</td>
<td>220.0</td>
<td>35.0</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is a Pb-free bump design. Bump finish may vary. To determine the exact finish, refer to the device datasheet or contact a local TI representative.
NOTES: (continued)

4. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.