



30-V, N-Channel NexFET™ Power MOSFETs

 Check for Samples: [CSD17552Q5A](#)

FEATURES

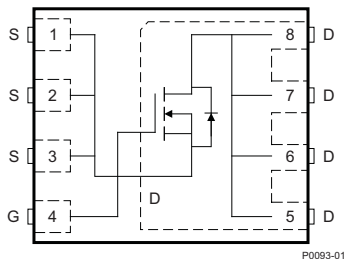
- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

APPLICATIONS

- Point of load Synchronous Buck in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

DESCRIPTION

The NexFET power MOSFET has been designed to minimize losses in power conversion applications.

Figure 1. Top View


PRODUCT SUMMARY

| | | | |
|--------------|-------------------------------|-----------------|--------|
| V_{DS} | Drain to Source Voltage | 30 | V |
| Q_g | Gate Charge Total (4.5V) | 9.0 | nC |
| Q_{gd} | Gate Charge Gate to Drain | 2.0 | nC |
| $R_{DS(on)}$ | Drain to Source On Resistance | $V_{GS} = 4.5V$ | 6.1 mΩ |
| | | $V_{GS} = 10V$ | 5.1 mΩ |
| $V_{GS(th)}$ | Threshold Voltage | 1.5 | V |

ORDERING INFORMATION

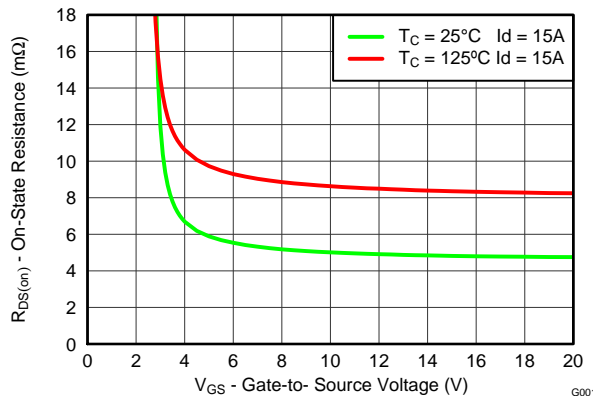
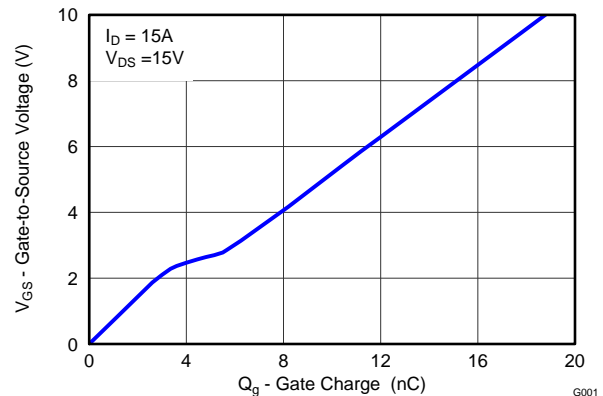
| Device | Package | Media | Qty | Ship |
|-------------|---------------------------------|--------------|------|---------------|
| CSD17552Q5A | SON 5-mm x 6-mm Plastic Package | 13-Inch Reel | 2500 | Tape and Reel |

ABSOLUTE MAXIMUM RATINGS

| $T_A = 25^\circ C$ unless otherwise stated | | VALUE | UNIT |
|--|--|------------|------------|
| V_{DS} | Drain to Source Voltage | 30 | V |
| V_{GS} | Gate to Source Voltage | ± 20 | V |
| I_D | Continuous Drain Current, $T_C = 25^\circ C$ | 60 | A |
| | Continuous Drain Current, Silicon Limited | 88 | A |
| | Continuous Drain Current, $T_A = 25^\circ C^{(1)}$ | 17 | A |
| I_{DM} | Pulsed Drain Current, $T_A = 25^\circ C^{(2)}$ | 106 | A |
| P_D | Power Dissipation ⁽¹⁾ | 3.0 | W |
| T_J, T_{STG} | Operating Junction and Storage Temperature Range | -55 to 150 | $^\circ C$ |
| E_{AS} | Avalanche Energy, single pulse $I_D = 30A, L = 0.1mH, R_G = 25\Omega$ | 45 | mJ |

(1) Typical $R_{\theta JA} = 40^\circ C/W$ on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\mu s$, duty cycle $\leq 2\%$

 $R_{DS(on)}$ vs V_{GS}

GATE CHARGE


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

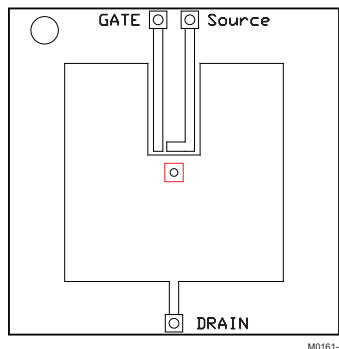
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|--------------------------------|----------------------------------|---|-----|------|------|------|
| Static Characteristics | | | | | | |
| B _V DSS | Drain to Source Voltage | V _{GS} = 0V, I _D = 250μA | 30 | | | V |
| I _{DSS} | Drain to Source Leakage Current | V _{GS} = 0V, V _{DS} = 24V | | | 1 | μA |
| I _{GSS} | Gate to Source Leakage Current | V _{DS} = 0V, V _{GS} = 20V | | | 100 | nA |
| V _{GS(th)} | Gate to Source Threshold Voltage | V _{DS} = V _{GS} , I _D = 250μA | 1.1 | 1.5 | 1.9 | V |
| R _{DS(on)} | Drain to Source On Resistance | V _{GS} = 4.5V, I _D = 15A | | 6.1 | 7.5 | mΩ |
| | | V _{GS} = 10V, I _D = 15A | | 5.1 | 6.2 | mΩ |
| g _{fs} | Transconductance | V _{DS} = 15V, I _D = 15A | | 77 | | S |
| Dynamic Characteristics | | | | | | |
| C _{iss} | Input Capacitance | V _{GS} = 0V, V _{DS} = 15V, f = 1MHz | | 1580 | 2050 | pF |
| C _{oss} | Output Capacitance | | | 385 | 500 | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 28 | 36 | pF |
| R _G | Series Gate Resistance | | | 0.9 | 1.8 | Ω |
| Q _g | Gate Charge Total (4.5V) | V _{DS} = 15V, I _D = 15A | | 9.0 | 12 | nC |
| Q _{gd} | Gate Charge Gate to Drain | | | 2.0 | | nC |
| Q _{gs} | Gate Charge Gate to Source | | | 3.6 | | nC |
| Q _{g(th)} | Gate Charge at V _{th} | | | 2.1 | | nC |
| Q _{oss} | Output Charge | V _{DS} = 15V, V _{GS} = 0V | | 11 | | nC |
| t _{d(on)} | Turn On Delay Time | V _{DS} = 15V, V _{GS} = 4.5V, I _D = 15A, R _G = 2Ω | | 7.6 | | ns |
| t _r | Rise Time | | | 11.4 | | ns |
| t _{d(off)} | Turn Off Delay Time | | | 12.2 | | ns |
| t _f | Fall Time | | | 3.6 | | ns |
| Diode Characteristics | | | | | | |
| V _{SD} | Diode Forward Voltage | I _{SD} = 11A, V _{GS} = 0V | | 0.8 | 1 | V |
| Q _{rr} | Reverse Recovery Charge | V _{DS} = 13V, I _F = 15A, di/dt = 300A/μs | | 20 | | nC |
| t _{rr} | Reverse Recovery Time | | | 18 | | ns |

THERMAL CHARACTERISTICS

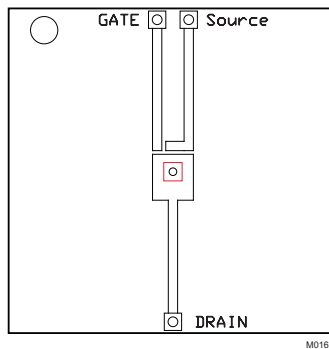
(T_A = 25°C unless otherwise stated)

| PARAMETER | | MIN | TYP | MAX | UNIT |
|------------------|--|-----|-----|-----|------|
| R _{θJC} | Thermal Resistance Junction to Case ⁽¹⁾ | | | 1.8 | °C/W |
| R _{θJA} | Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾ | | | 50 | °C/W |

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA} = 50^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2-
oz. (0.071-mm thick)
Cu.



Max $R_{\theta JA} = 125^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

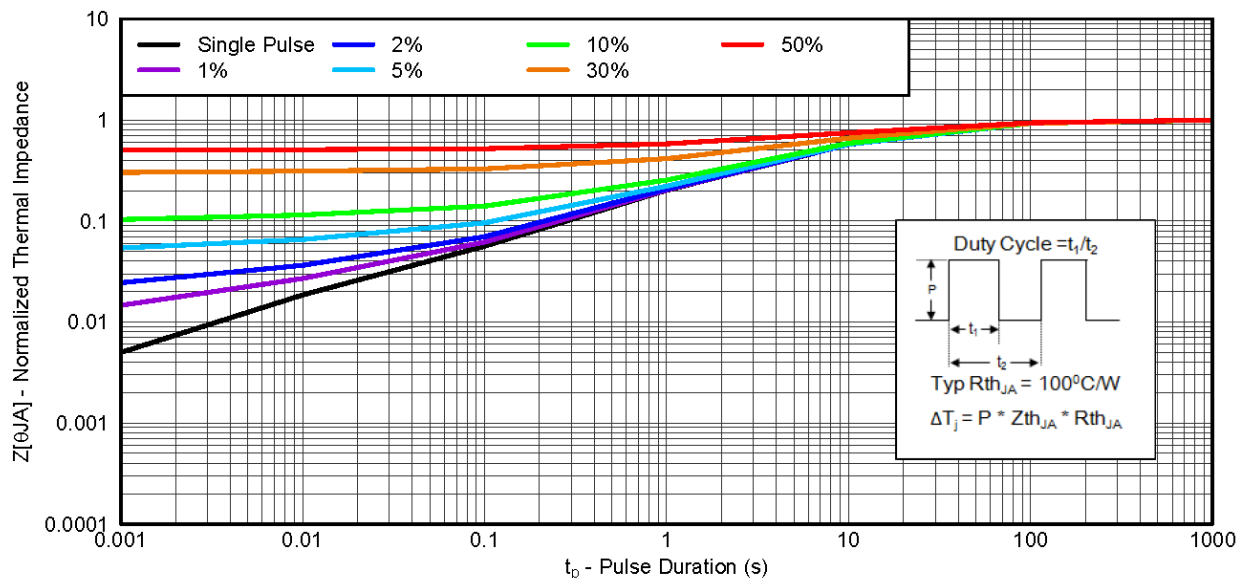


Figure 2. Transient Thermal Impedance

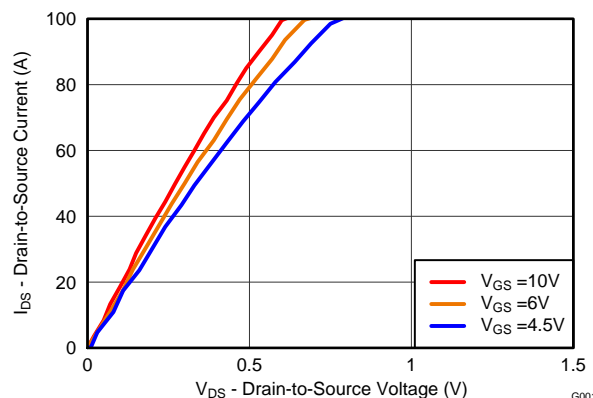


Figure 3. Saturation Characteristics

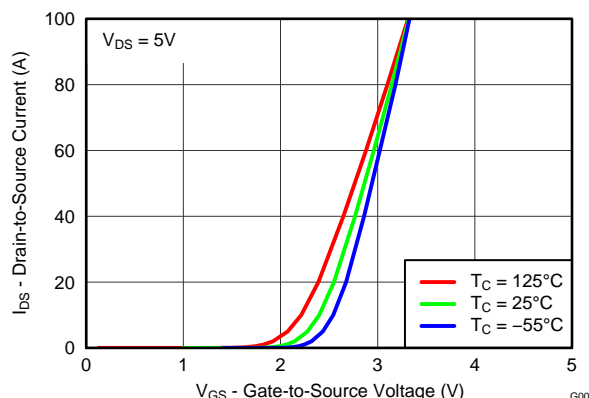


Figure 4. Transfer Characteristics

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

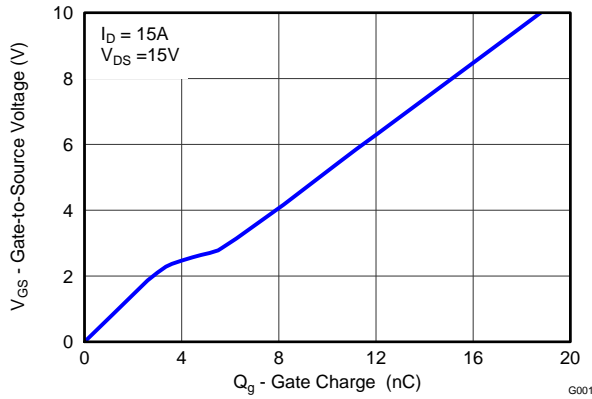


Figure 5. Gate Charge

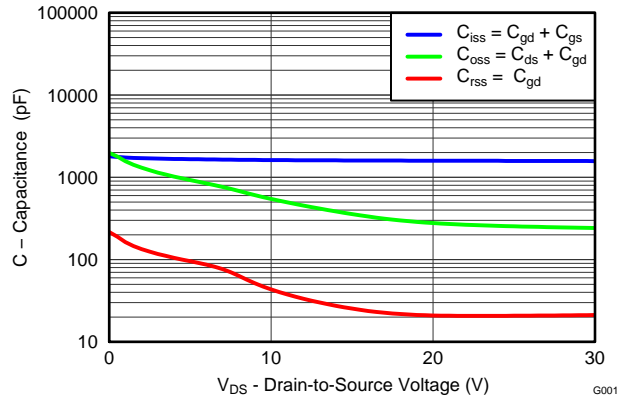


Figure 6. Capacitance

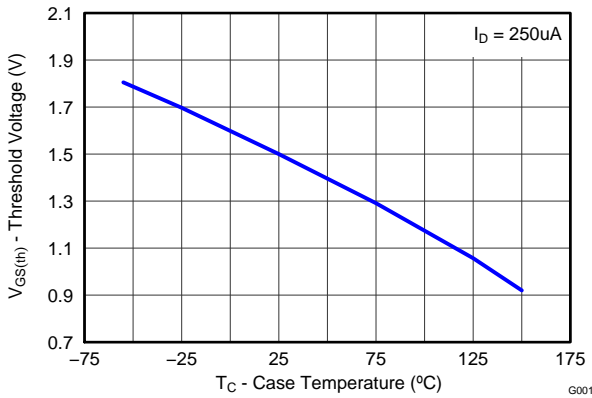


Figure 7. Threshold Voltage vs. Temperature

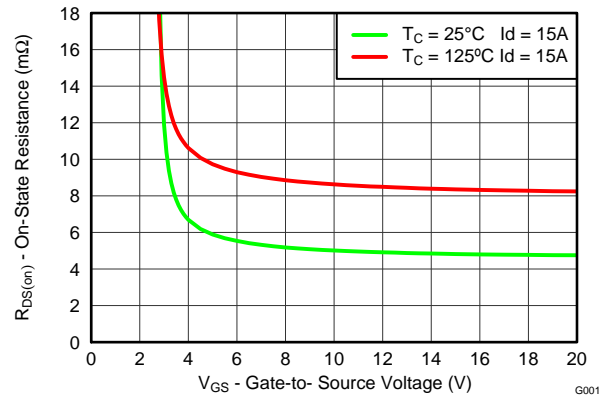


Figure 8. On-State Resistance vs. Gate-to-Source Voltage

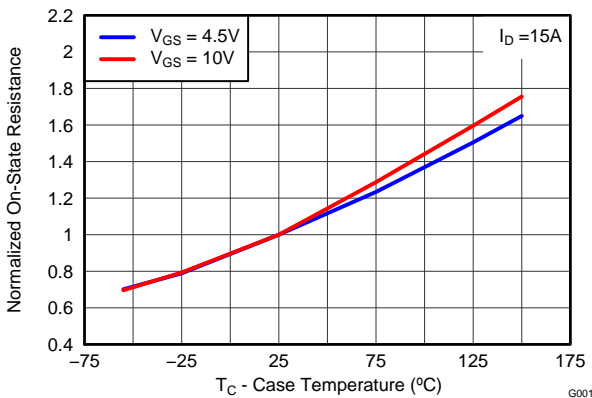


Figure 9. Normalized On-State Resistance vs. Temperature

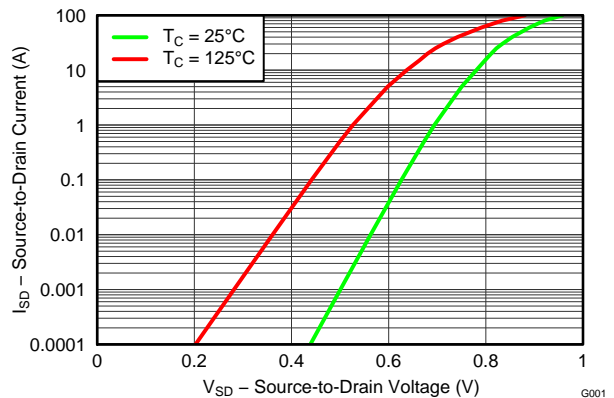


Figure 10. Typical Diode Forward Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

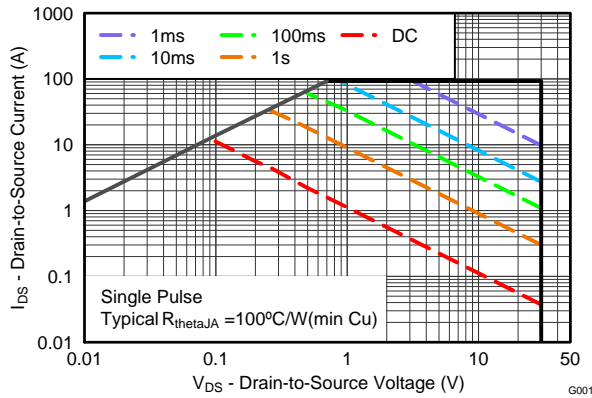


Figure 11. Maximum Safe Operating Area

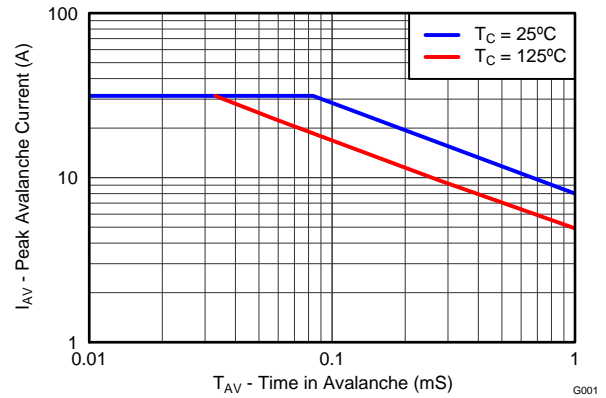


Figure 12. Single Pulse Unclamped Inductive Switching

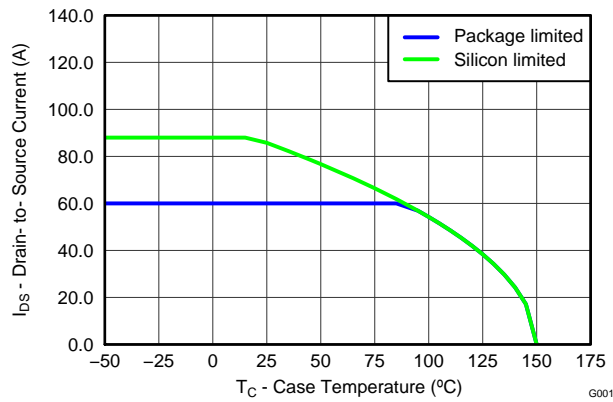


Figure 13. Maximum Drain Current vs. Temperature

MECHANICAL DATA

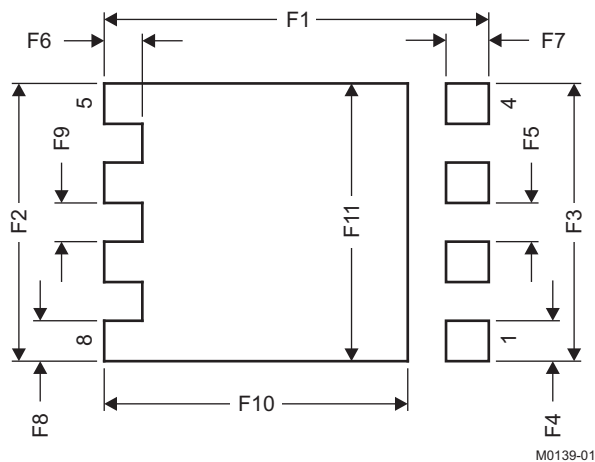
Q5A Package Dimensions



M0135-01

| DIM | MILLIMETERS | | |
|----------|-------------|------|------|
| | MIN | NOM | MAX |
| A | 0.90 | 1.00 | 1.10 |
| b | 0.33 | 0.41 | 0.51 |
| c | 0.20 | 0.25 | 0.34 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.61 | 3.81 | 4.02 |
| E | 5.90 | 6.00 | 6.10 |
| E1 | 5.70 | 5.75 | 5.80 |
| E2 | 3.38 | 3.58 | 3.78 |
| e | 1.17 | 1.27 | 1.37 |
| H | 0.41 | 0.56 | 0.71 |
| K | 1.10 | | |
| L | 0.51 | 0.61 | 0.71 |
| L1 | 0.06 | 0.13 | 0.20 |
| θ | 0° | | 12° |

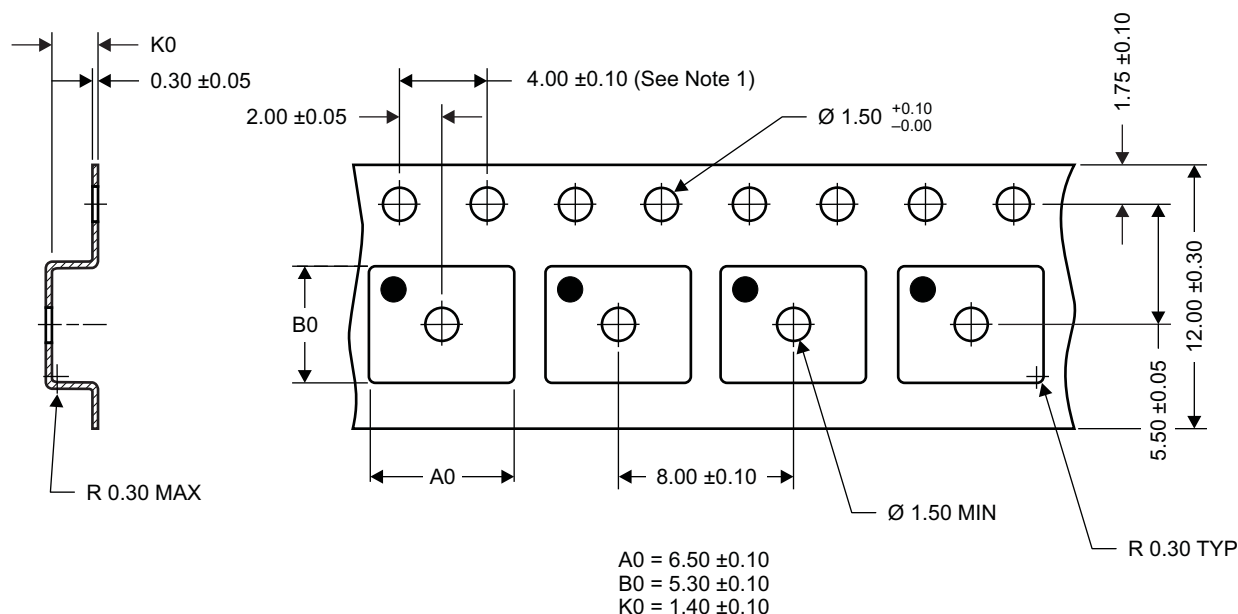
Figure 14. Recommended PCB Pattern



| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|-------|--------|-------|
| | MIN | MAX | MIN | MAX |
| F1 | 6.205 | 6.305 | 0.244 | 0.248 |
| F2 | 4.46 | 4.56 | 0.176 | 0.18 |
| F3 | 4.46 | 4.56 | 0.176 | 0.18 |
| F4 | 0.65 | 0.7 | 0.026 | 0.028 |
| F5 | 0.62 | 0.67 | 0.024 | 0.026 |
| F6 | 0.63 | 0.68 | 0.025 | 0.027 |
| F7 | 0.7 | 0.8 | 0.028 | 0.031 |
| F8 | 0.65 | 0.7 | 0.026 | 0.028 |
| F9 | 0.62 | 0.67 | 0.024 | 0.026 |
| F10 | 4.9 | 5 | 0.193 | 0.197 |
| F11 | 4.46 | 4.56 | 0.176 | 0.18 |

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q5A Tape and Reel Information



M0138-01

Notes:

- 10-sprocket hole-pitch cumulative tolerance ± 0.2
- Camber not to exceed 1mm in 100mm, noncumulative over 250mm
- Material: black static-dissipative polystyrene
- All dimensions are in mm (unless otherwise specified)
- A0 and B0 measured on a plane 0.3mm above the bottom of the pocket

PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package Pins | Package qty Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|-----------------------------|---------------|----------------------|-----------------|-----------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| CSD17552Q5A | Active | Production | VSONP (DQJ) 8 | 2500 LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -55 to 150 | CSD17552 |
| CSD17552Q5A.Z | Active | Production | VSONP (DQJ) 8 | 2500 LARGE T&R | ROHS Exempt | SN | Level-1-260C-UNLIM | -55 to 150 | CSD17552 |

(1) **Status:** For more details on status, see our [product life cycle](#).

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "-" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Copyright © 2025, Texas Instruments Incorporated