

# CSD18502Q5B 40 V N-Channel NexFET™ Power MOSFET

## 1 Features

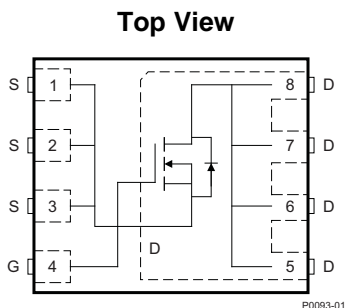
- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen-Free
- SON 5 mm x 6 mm Plastic Package

## 2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Motor Control

## 3 Description

This 40-V, 1.8-m $\Omega$ , 5 mm x 6 mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain to source voltage	40		V
$Q_g$	Gate charge total (4.5 V)	25		nC
$Q_{gd}$	Gate charge gate to drain	8.4		nC
$R_{DS(on)}$	Drain to source on resistance	$V_{GS} = 4.5\text{ V}$	2.5	m $\Omega$
		$V_{GS} = 10\text{ V}$	1.8	m $\Omega$
$V_{GS(th)}$	Threshold voltage	1.8		V

### Ordering Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18502Q5B	2500	13-Inch Reel	SON 5 mm x 6 mm Plastic Package	Tape and Reel
CSD18502Q5BT	250	7-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

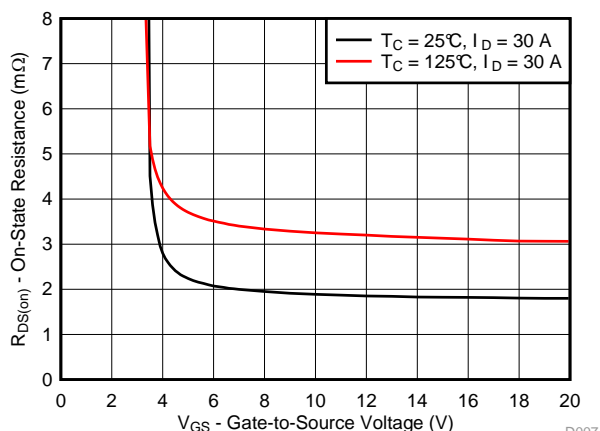
### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain to source voltage	40	V
$V_{GS}$	Gate to source voltage	$\pm 20$	V
$I_D$	Continuous drain current (package limited)	100	A
	Continuous drain current (silicon limited), $T_C = 25^\circ\text{C}$	204	
	Continuous drain current <sup>(1)</sup>	26	
$I_{DM}$	Pulsed drain current <sup>(2)</sup>	400	A
$P_D$	Power dissipation <sup>(1)</sup>	3.2	W
	Power dissipation, $T_C = 25^\circ\text{C}$	156	
$T_J$	Operating junction temperature	-55 to 150	$^\circ\text{C}$
$T_{stg}$	Storage temperature	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche energy, single pulse $I_D = 88\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\ \Omega$	387	mJ

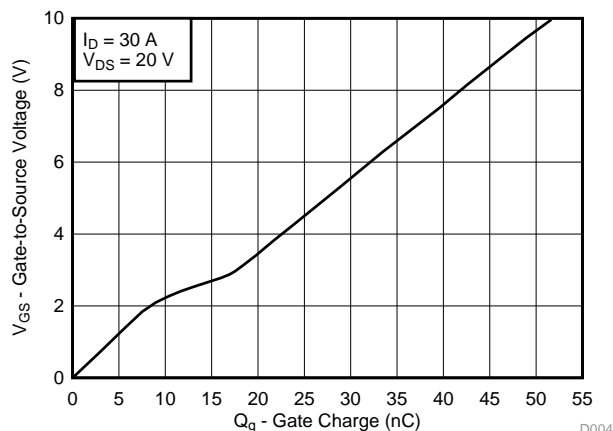
(1) Typical  $R_{\theta JA} = 40^\circ\text{C/W}$  on a 1 inch<sup>2</sup>, 2 oz. Cu pad on a 0.06 inch thick FR4 PCB.

(2) Max  $R_{\theta JC} = 0.8^\circ\text{C/W}$ , pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$

**$R_{DS(on)}$  vs  $V_{GS}$**



**Gate Charge**



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## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

<b>Changes from Revision A (May 2015) to Revision B</b>	<b>Page</b>
• Added <i>Receiving Notification of Documentation Updates</i> section. ....	<b>7</b>
• Changed the dimension between pads 3 and 4 from 0.028 inches: to 0.050 inches in the <i>Recommended PCB Pattern</i> section diagram .....	<b>9</b>

<b>Changes from Original (November 2012) to Revision A</b>	<b>Page</b>
• Added part number to title. ....	<b>1</b>
• Added 7-inch reel to <i>Ordering Information</i> . ....	<b>1</b>
• Added power dissipation at $T_C = 25^\circ\text{C}$ to <i>Absolute Maximum Ratings</i> . ....	<b>1</b>
• Updated pulsed drain current conditions in <i>Absolute Maximum Ratings</i> . ....	<b>1</b>
• Updated <a href="#">Figure 1</a> to normalized $R_{\theta\text{JC}}$ curves. ....	<b>4</b>
• Updated SOA in <a href="#">Figure 10</a> . ....	<b>6</b>
• Added <a href="#">Community Resources</a> . ....	<b>8</b>
• Updated mechanical drawings to show additional dimensions. ....	<b>8</b>

## 5 Specifications

### 5.1 Electrical Characteristics

(T<sub>A</sub> = 25°C unless otherwise stated)

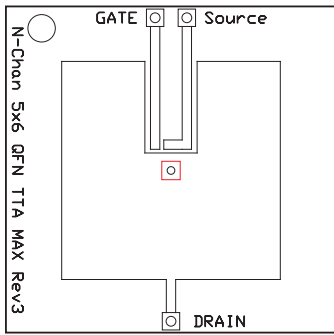
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT	
<b>STATIC CHARACTERISTICS</b>							
V <sub>DSS</sub>	Drain to source voltage	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V	
I <sub>DSS</sub>	Drain to source leakage current	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 32 V			1	μA	
I <sub>GSS</sub>	Gate to source leakage current	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = 20 V			100	nA	
V <sub>GS(th)</sub>	Gate to source threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	1.5	1.8	2.2	V	
R <sub>DS(on)</sub>	Drain to source on resistance	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 30 A		2.5	3.3	mΩ	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 30 A		1.8	2.3	mΩ	
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 30 A		143		S	
<b>DYNAMIC CHARACTERISTICS</b>							
C <sub>iss</sub>	Input capacitance	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 20 V, f = 1 MHz		3900	5070	pF	
C <sub>oss</sub>	Output capacitance			900	1170	pF	
C <sub>rss</sub>	Reverse transfer capacitance			21	27	pF	
R <sub>G</sub>	Series gate resistance			1.2	2.4	Ω	
Q <sub>g</sub>	Gate charge total (4.5 V)	V <sub>DS</sub> = 20 V, I <sub>D</sub> = 30 A		25	33	nC	
Q <sub>g</sub>	Gate charge total (10 V)			52	68	nC	
Q <sub>gd</sub>	Gate charge gate to drain			8.4		nC	
Q <sub>gs</sub>	Gate charge gate to source			10.3		nC	
Q <sub>g(th)</sub>	Gate charge at V <sub>th</sub>			6.9		nC	
Q <sub>oss</sub>	Output charge		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 0 V		59		nC
t <sub>d(on)</sub>	Turn on delay time		V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>DS</sub> = 30 A, R <sub>G</sub> = 0 Ω		5.3		ns
t <sub>r</sub>	Rise time			6.8		ns	
t <sub>d(off)</sub>	Turn off delay time			23		ns	
t <sub>f</sub>	Fall time			4		ns	
<b>DIODE CHARACTERISTICS</b>							
V <sub>SD</sub>	Diode forward voltage	I <sub>SD</sub> = 30 A, V <sub>GS</sub> = 0 V		0.8	1	V	
Q <sub>rr</sub>	Reverse recovery charge	V <sub>DS</sub> = 20 V, I <sub>F</sub> = 30 A, di/dt = 300 A/μs		88		nC	
t <sub>rr</sub>	Reverse recovery time			44		ns	

### 5.2 Thermal Information

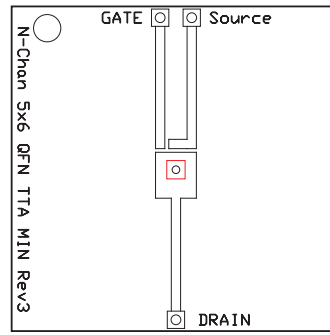
(T<sub>A</sub> = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R <sub>θJC</sub>	Junction-to-case (top of package) thermal resistance <sup>(1)</sup>			0.8	°C/W
R <sub>θJA</sub>	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			50	°C/W

- (1) R<sub>θJC</sub> is determined with the device mounted on a 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. R<sub>θJC</sub> is specified by design, whereas R<sub>θJA</sub> is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch<sup>2</sup> (6.45 cm<sup>2</sup>), 2 oz. (0.071 mm thick) Cu.



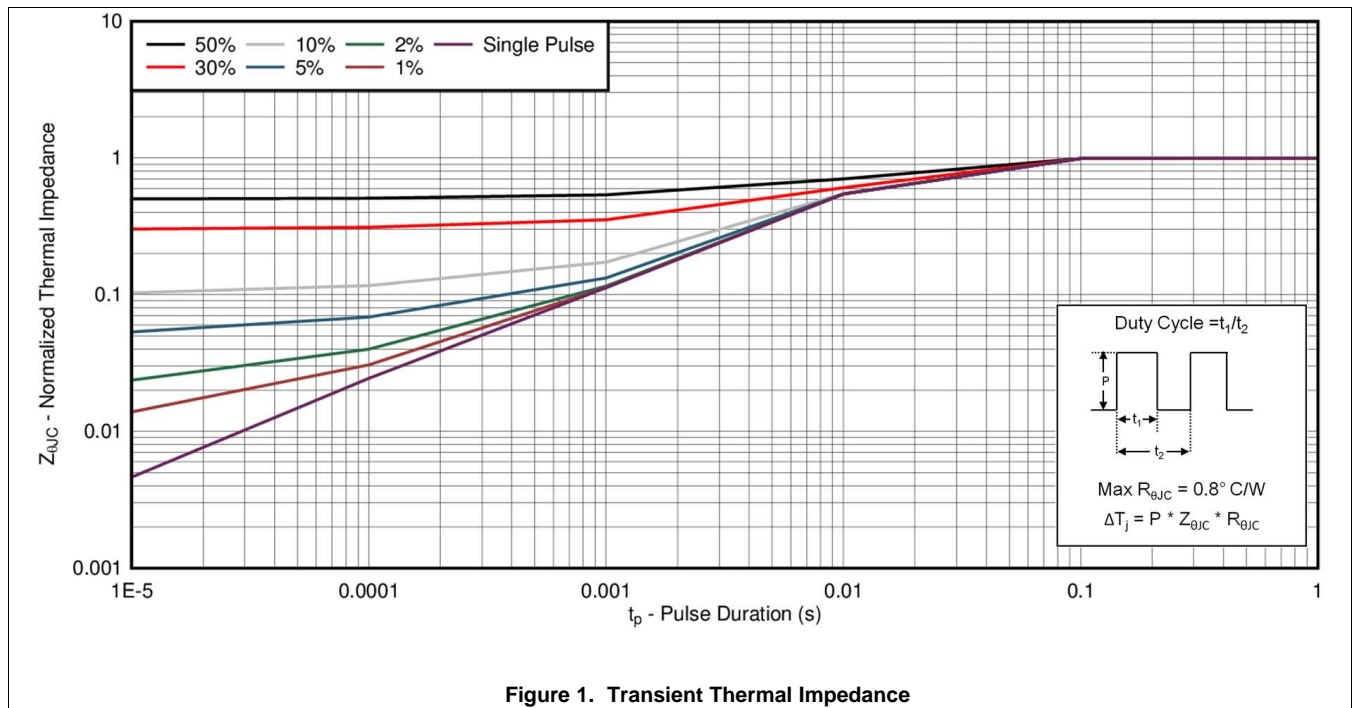
Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of 2  
oz. (0.071 mm thick)  
Cu.



Max  $R_{\theta JA} = 125^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of 2  
oz. (0.071 mm thick)  
Cu.

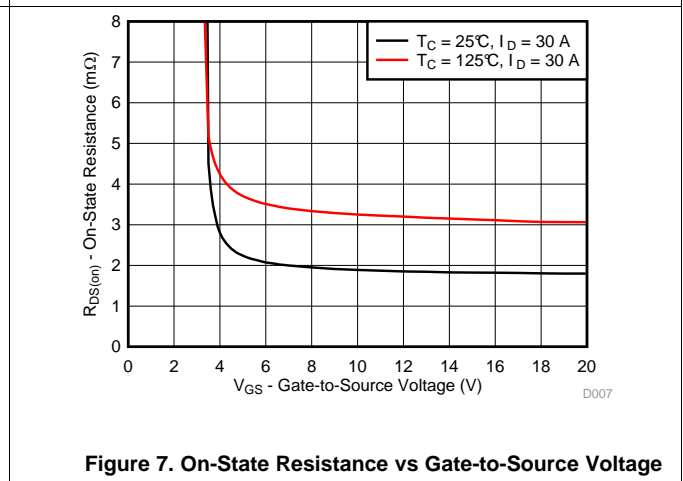
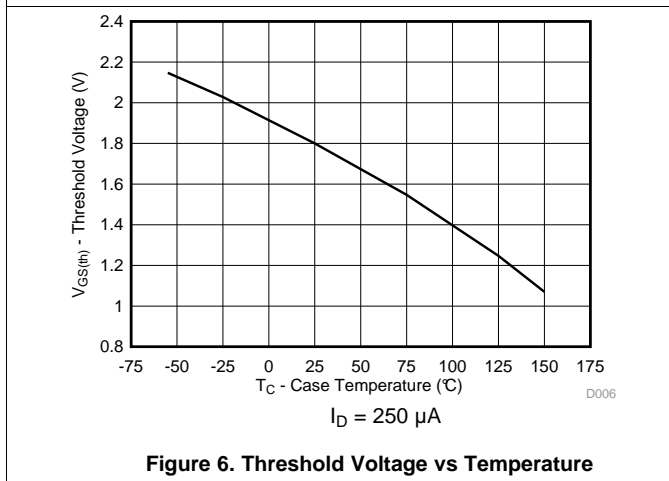
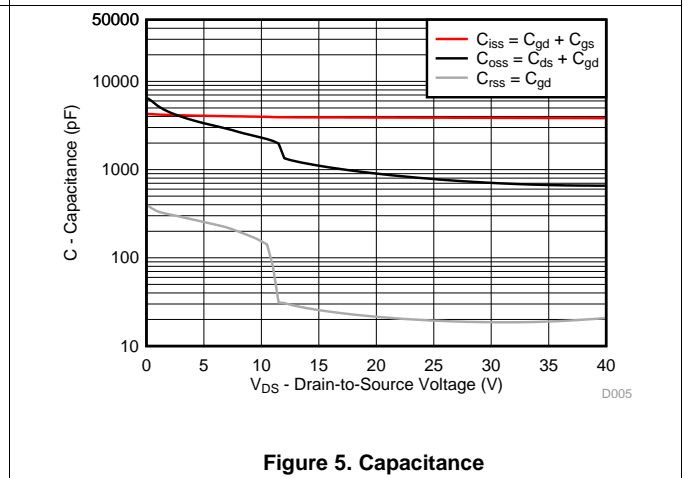
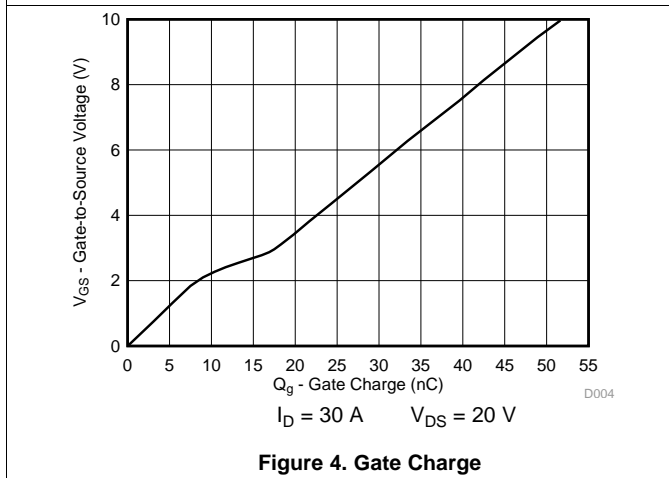
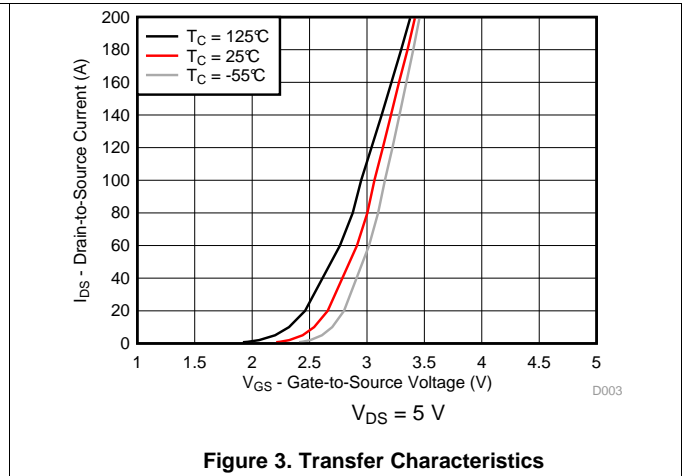
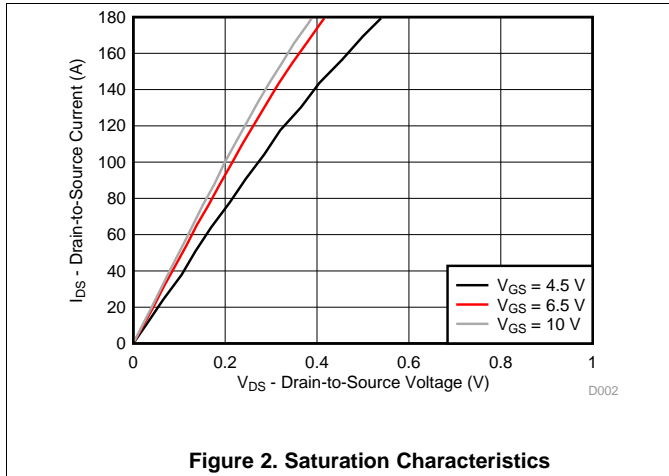
### 5.3 Typical MOSFET Characteristics

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)



Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

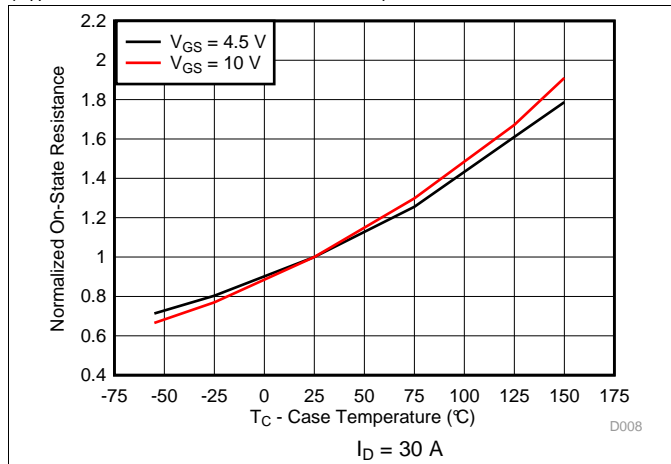


Figure 8. Normalized On-State Resistance vs Temperature

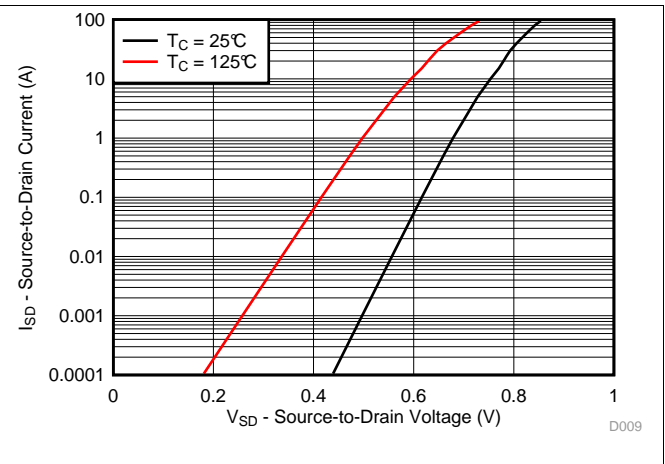


Figure 9. Typical Diode Forward Voltage

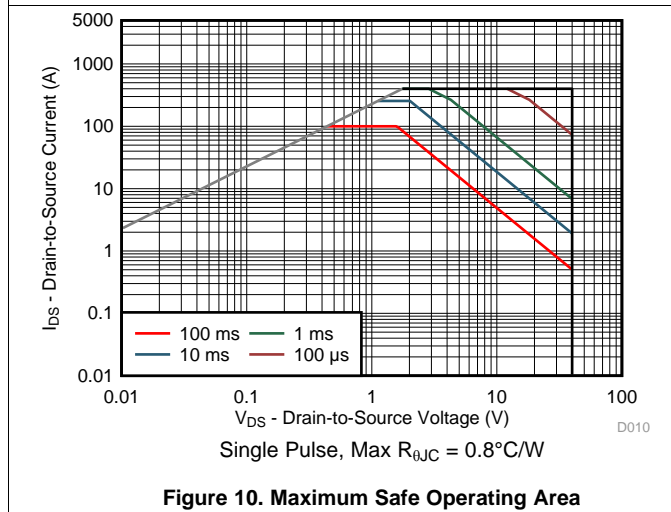


Figure 10. Maximum Safe Operating Area

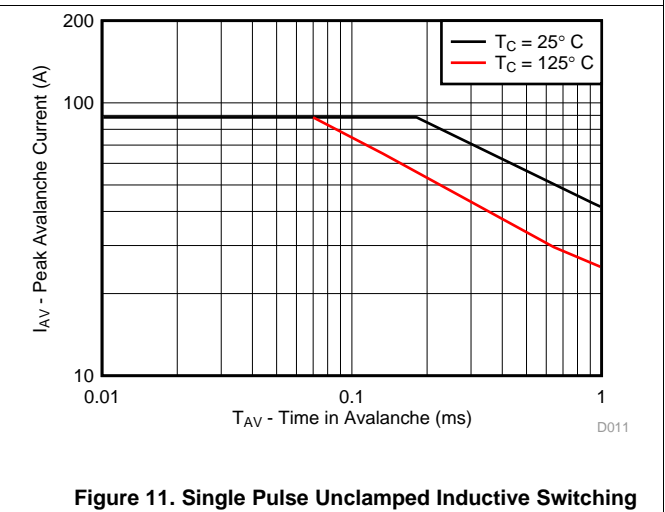


Figure 11. Single Pulse Unclamped Inductive Switching

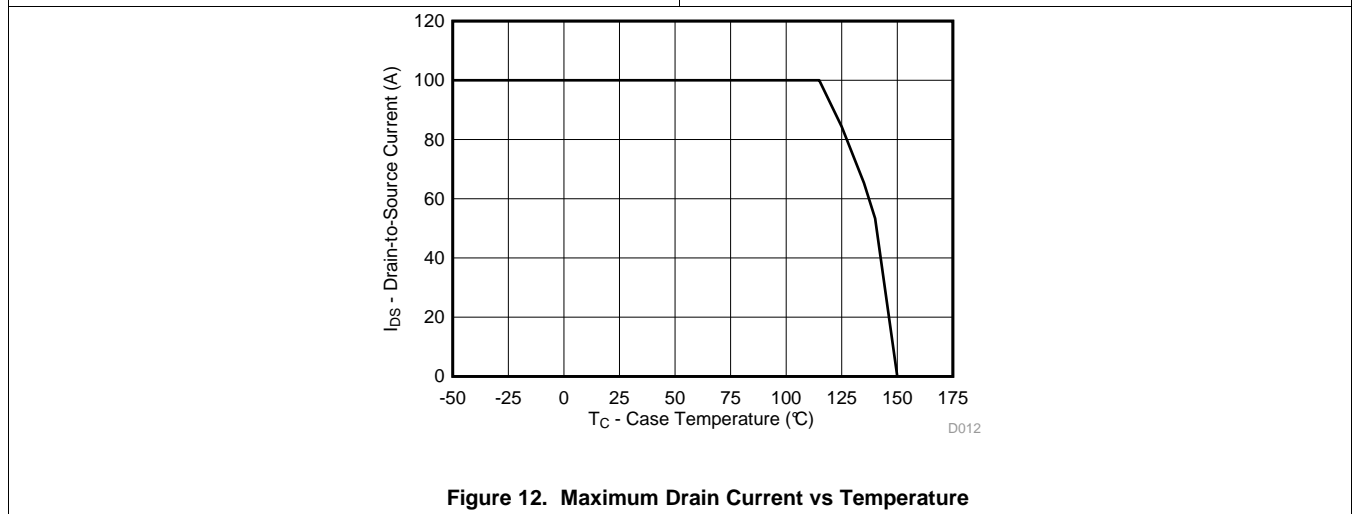


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

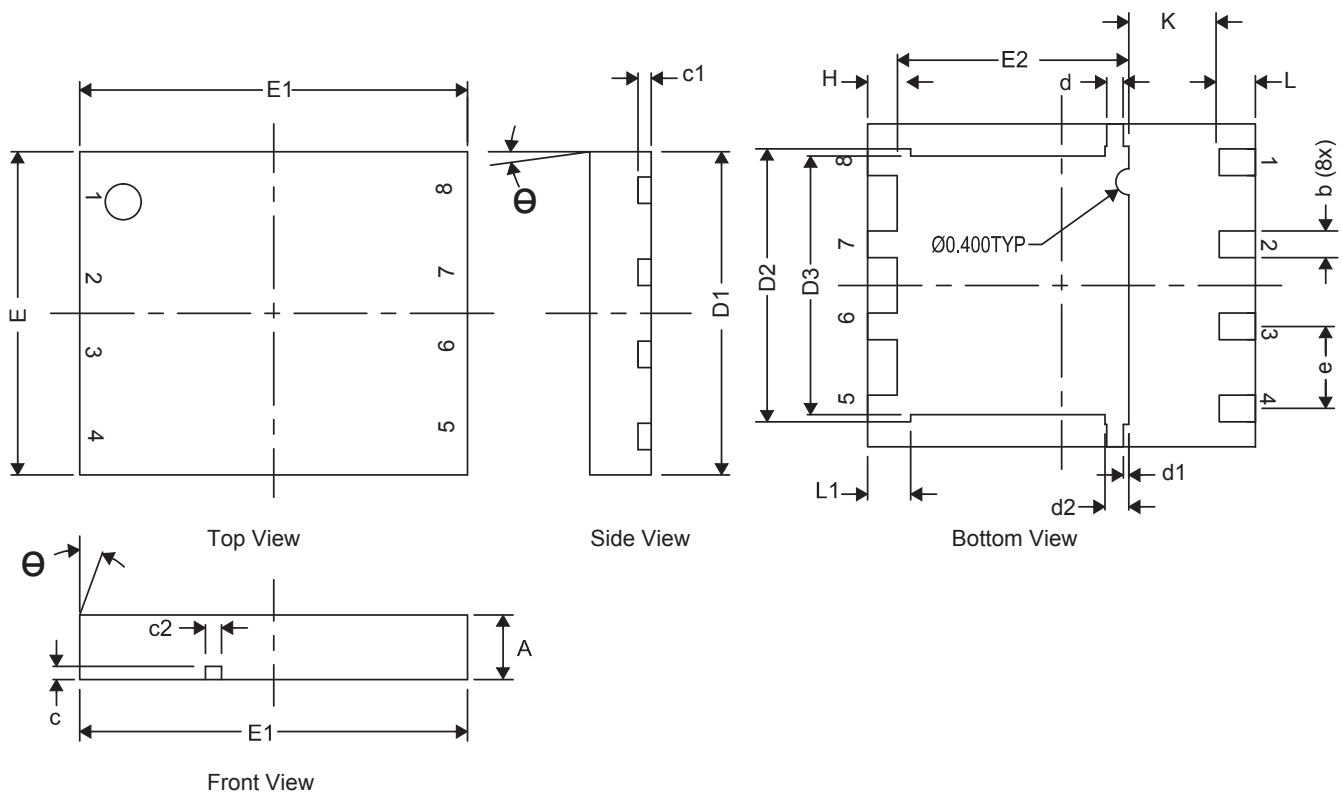
### 6.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

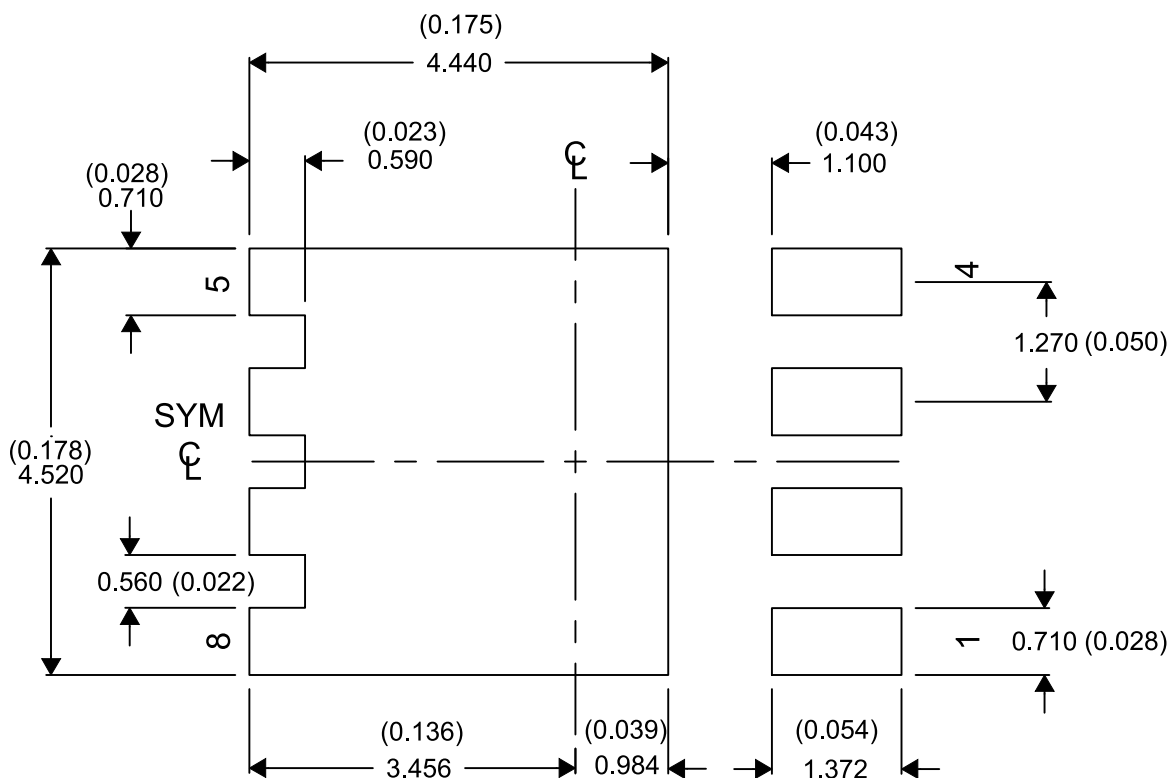
### 7.1 Q5B Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.95	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
d	0.20	0.25	0.30
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
L	0.46	0.56	0.66
$\theta$	0°	—	—
K	1.40 TYP		

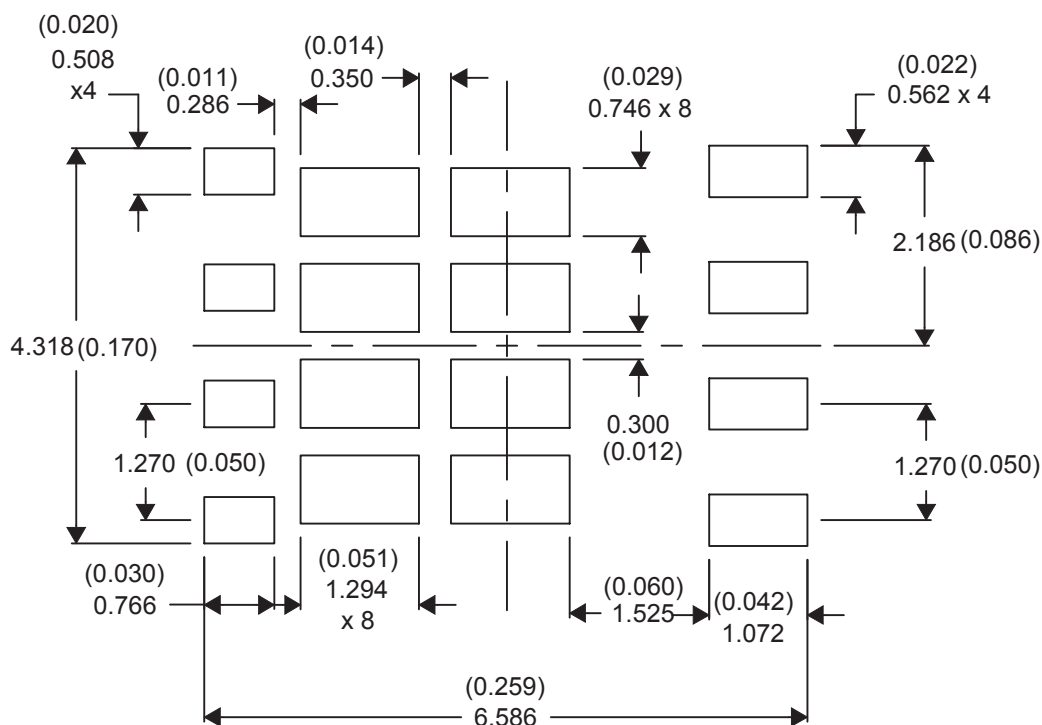


7.2 Recommended PCB Pattern

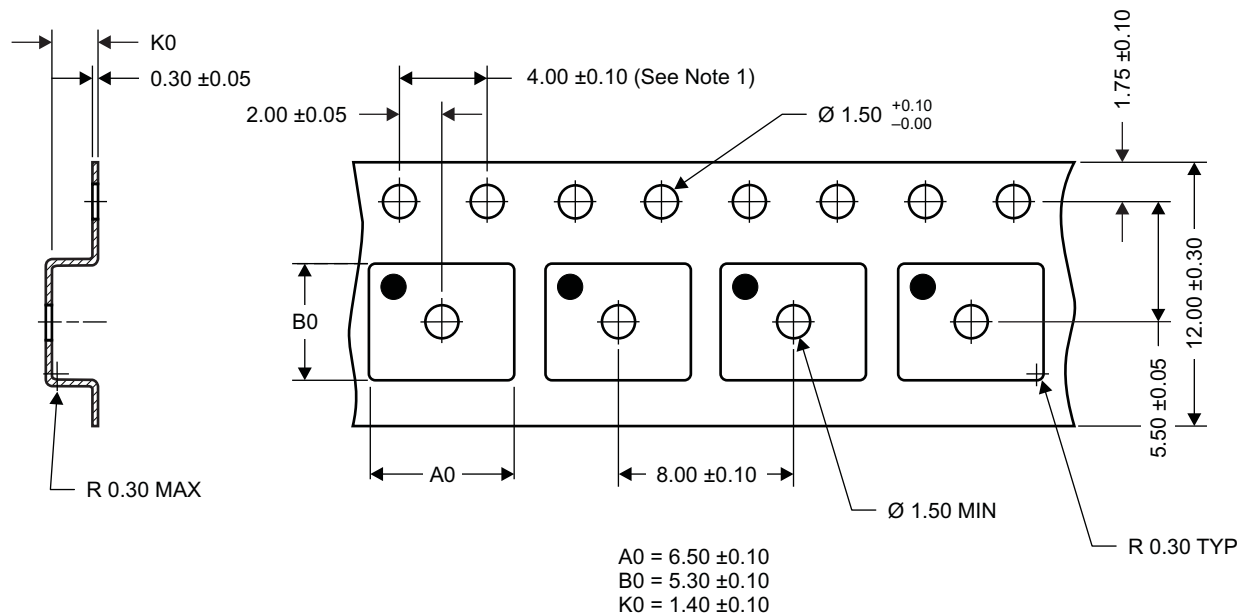


For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

7.3 Recommended Stencil Pattern



## 7.4 Q5B Tape and Reel Information



M0138-01

### Notes:

1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18502Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	RoHS-Exempt & Green	NIPDAU   SN	Level-1-260C-UNLIM		CSD18502	<a href="#">Samples</a>
CSD18502Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	RoHS-Exempt & Green	NIPDAU   SN	Level-1-260C-UNLIM	-55 to 150	CSD18502	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18502Q5B	VSON-CLIP	DNK	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18502Q5B	VSON-CLIP	DNK	8	2500	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18502Q5BT	VSON-CLIP	DNK	8	250	180.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1
CSD18502Q5BT	VSON-CLIP	DNK	8	250	178.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18502Q5B	VSON-CLIP	DNK	8	2500	335.0	335.0	32.0
CSD18502Q5B	VSON-CLIP	DNK	8	2500	367.0	367.0	35.0
CSD18502Q5BT	VSON-CLIP	DNK	8	250	182.0	182.0	20.0
CSD18502Q5BT	VSON-CLIP	DNK	8	250	210.0	210.0	52.0

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