1 Features
- Ultra-Low $Q_g$ and $Q_{gd}$
- Low $R_{DS(on)}$
- Low-Thermal Resistance
- Avalanche Rated
- Lead Free
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

2 Applications
- Solid State Relay Switch
- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Isolated Converter Primary Side Switch
- Motor Control

3 Description
This 60-V, 8.1-mΩ, SON 3.3-mm × 3.3-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.
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4 Revision History

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<th>REVISION</th>
<th>NOTES</th>
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<tbody>
<tr>
<td>December 2016</td>
<td>*</td>
<td>Initial release.</td>
</tr>
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</table>
5 Specifications

5.1 Electrical Characteristics

\(T_A = 25^\circ\text{C}\) (unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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<td><strong>STATIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{DSS}) Drain-to-source voltage</td>
<td>(V_{GS} = 0\ V, I_D = 250\ \mu\text{A})</td>
<td></td>
<td>60</td>
<td>60</td>
<td>V</td>
</tr>
<tr>
<td>(I_{DSS}) Drain-to-source leakage current</td>
<td>(V_{GS} = 0\ V, V_{DS} = 48\ V)</td>
<td></td>
<td>1</td>
<td>1</td>
<td>\mu\text{A}</td>
</tr>
<tr>
<td>(I_{GS}) Gate-to-source leakage current</td>
<td>(V_{DS} = 0\ V, V_{GS} = 20\ V)</td>
<td></td>
<td>100</td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>(V_{GS(th)}) Gate-to-source threshold voltage</td>
<td>(V_{GS} = V_{GS}, I_D = 250\ \mu\text{A})</td>
<td>1.5</td>
<td>2.0</td>
<td>2.7</td>
<td>V</td>
</tr>
<tr>
<td>(R_{DS(on)}) Drain-to-source on resistance</td>
<td>(V_{GS} = 4.5\ V, I_D = 12\ A)</td>
<td>12.0</td>
<td>15.6</td>
<td>18.0</td>
<td>\text{m}\Omega</td>
</tr>
<tr>
<td>(g_f) Transconductance</td>
<td>(V_{DS} = 6\ V, I_D = 12\ A)</td>
<td>40</td>
<td></td>
<td></td>
<td>S</td>
</tr>
<tr>
<td><strong>DYNAMIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(C_{iss}) Input capacitance</td>
<td>(V_{GS} = 0\ V, V_{DS} = 30\ V, f = 1\ \text{MHz})</td>
<td>885</td>
<td>1150</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(C_{oss}) Output capacitance</td>
<td>(V_{GS} = 0\ V, V_{DS} = 30\ V, f = 1\ \text{MHz})</td>
<td>168</td>
<td>218</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(C_{rss}) Reverse transfer capacitance</td>
<td>(V_{GS} = 0\ V, V_{DS} = 30\ V, f = 1\ \text{MHz})</td>
<td>4.8</td>
<td>6.2</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>(R_g) Series gate resistance</td>
<td>(V_{DS} = 30\ V, I_D = 12\ A)</td>
<td>0.5</td>
<td>1.0</td>
<td></td>
<td>\Omega</td>
</tr>
<tr>
<td>(Q_g) Gate charge total ((4.5\ V))</td>
<td>(V_{DS} = 30\ V, I_D = 12\ A)</td>
<td>5.6</td>
<td>7.3</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>(Q_{gs}) Gate charge total ((10\ V))</td>
<td>(V_{DS} = 30\ V, I_D = 12\ A)</td>
<td>11.1</td>
<td>14.5</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>(Q_{gd}) Gate charge gate-to-drain</td>
<td>(V_{DS} = 30\ V, I_D = 12\ A)</td>
<td>1.7</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>(Q_{ss}) Gate charge gate-to-source</td>
<td>(V_{DS} = 30\ V, I_D = 12\ A)</td>
<td>3.1</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>(Q_{g(th)}) Gate charge at (V_{th})</td>
<td>(V_{DS} = 30\ V, I_D = 12\ A)</td>
<td>2.0</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>(t_{(on)}) Turnon delay time</td>
<td>(V_{DS} = 30\ V, V_{GS} = 0\ V)</td>
<td>24</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>(t_r) Rise time</td>
<td>(V_{DS} = 30\ V, V_{GS} = 10\ V, I_{DS} = 12\ A, R_G = 0\ \Omega)</td>
<td>9</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(t_{(off)}) Turnoff delay time</td>
<td>(V_{DS} = 30\ V, V_{GS} = 0\ V)</td>
<td>18</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>(t_f) Fall time</td>
<td>(V_{DS} = 30\ V, I_{DS} = 12\ A)</td>
<td>8</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>DIODE CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>(V_{SD}) Diode forward voltage</td>
<td>(I_{SD} = 12\ A, V_{GS} = 0\ V)</td>
<td>0.8</td>
<td>1.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>(Q_{fr}) Reverse recovery charge</td>
<td>(V_{DS} = 30\ V, I_F = 12\ A)</td>
<td>37</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>(t_{fr}) Reverse recovery time</td>
<td>(dI/dt = 300\ A/\mu\text{s})</td>
<td>27</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

5.2 Thermal Information

\(T_A = 25^\circ\text{C}\) (unless otherwise stated)

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(R_{\text{JUC}}) Junction-to-case thermal resistance ((1))</td>
<td></td>
<td>1.9</td>
<td></td>
<td>^\circ\text{C}/\text{W}</td>
</tr>
<tr>
<td>(R_{\text{JUA}}) Junction-to-ambient thermal resistance ((1)(2))</td>
<td>55</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) \(R_{\text{JUC}}\) is determined with the device mounted on a 1-in\(^2\) \((6.45\text{-cm}^2)\), 2-oz (0.071-mm) thick Cu pad on a 1.5-in \times 1.5-in \((3.81\text{-cm} \times 3.81\text{-cm})\), 0.06-in (1.52-mm) thick FR4 PCB. \(R_{\text{JUC}}\) is specified by design, whereas \(R_{\text{JUA}}\) is determined by the user’s board design.

(2) Device mounted on FR4 material with 1-in\(^2\) \((6.45\text{-cm}^2)\), 2-oz (0.071-mm) thick Cu.
Max $R_{\text{JJA}} = 55^\circ\text{C/W}$ when mounted on 1 in$^2$ (6.45 cm$^2$) of 2-oz (0.071-mm) thick Cu.

Max $R_{\text{JJA}} = 160^\circ\text{C/W}$ when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

### 5.3 Typical MOSFET Characteristics

$T_A = 25^\circ\text{C}$ (unless otherwise stated)

---

**Figure 1. Transient Thermal Impedance**

Max $R_{\text{ijac}} = 1.9^\circ\text{C/W}$

$\Delta T_I = P \times Z_{\text{ijac}} \times R_{\text{ijac}}$

\[ Z_{\text{ijac}} = \text{Normalized Thermal Impedance} \]

\[ t_0 = \text{Pulse Duration (s)} \]

---

Product Folder Links: CSD18543Q3A
Typical MOSFET Characteristics (continued)

$T_A = 25^\circ C$ (unless otherwise stated)

**Figure 2. Saturation Characteristics**

**Figure 3. Transfer Characteristics**

**Figure 4. Gate Charge**

**Figure 5. Capacitance**

**Figure 6. Threshold Voltage vs Temperature**

**Figure 7. On-State Resistance vs Gate-to-Source Voltage**
Typical MOSFET Characteristics (continued)

\( T_A = 25^\circ C \) (unless otherwise stated)

**Figure 8. Normalized On-State Resistance vs Temperature**

**Figure 9. Typical Diode Forward Voltage**

**Figure 10. Maximum Safe Operating Area (SOA)**

**Figure 11. Single Pulse Unclamped Inductive Switching**

**Figure 12. Maximum Drain Current vs Temperature**
6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community** *TI’s Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI’s Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
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6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

SLYZ022 — *TI Glossary.*
This glossary lists and explains terms, acronyms, and definitions.
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q3A Package Dimensions

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. Metalized features are supplier options and may not be on the package.
5. All dimensions do not include mold flash or protrusions.

NOTE 4
EXPOSED THERMAL PAD

NOTE 3
1
4 5
8

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1. This package is designed to be soldered to a thermal pad on the board. For more information, see QFN/SON PCB Attachment (SLUA271).

2. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

For recommended circuit layout for PCB designs, see Reducing Ringing Through PCB Layout Techniques (SLPA005).
7.3 Q3A Recommended Stencil Pattern

1. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

7.4 Q3A Tape and Reel Information

Notes:
1. 10-sprocket hole-pitch cumulative tolerance ±0.2.
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
4. All dimensions are in mm, unless otherwise specified.
5. Thickness: 0.30 ±0.05 mm.
6. MSL1 260°C (IR and convection) PbF-reflow compatible.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (3)</th>
<th>MSL Peak Temp (4)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (5)</th>
<th>Samples</th>
</tr>
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<td>ACTIVE</td>
<td>VSONP</td>
<td>DNH</td>
<td>8</td>
<td>2500</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 150</td>
<td>18543</td>
<td>Samples</td>
</tr>
<tr>
<td>CSD18543Q3AT</td>
<td>ACTIVE</td>
<td>VSONP</td>
<td>DNH</td>
<td>8</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>SN</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 150</td>
<td>18543</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free". **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

(3) **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(4) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) **Device Marking** - Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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