

CSD19505KCS 80V N-Channel NexFET™ Power MOSFET

1 Features

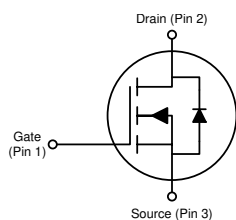
- Ultra-low Q_g and Q_{gd}
- Low thermal resistance
- Avalanche rated
- Pb-free terminal plating
- RoHS compliant
- Halogen Free
- TO-220 plastic package

2 Applications

- Secondary side synchronous rectifier
- Motor control

3 Description

This 80 V, 2.6 mΩ, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	80		V
Q_g	Gate Charge Total (10V)	76		nC
Q_{gd}	Gate Charge Gate to Drain	11		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 6\text{V}$	2.9	mΩ
		$V_{GS} = 10\text{V}$	2.6	mΩ
$V_{GS(th)}$	Threshold Voltage	2.6		V

Ordering Information⁽¹⁾

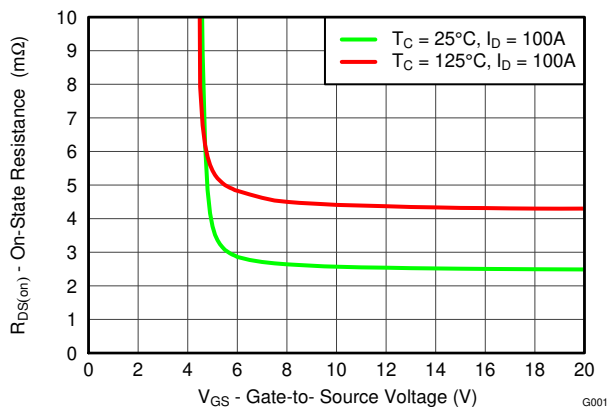
Device	Package	Media	Qty	Ship
CSD19505KCS	TO-220 Plastic Package	Tube	50	Tube

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

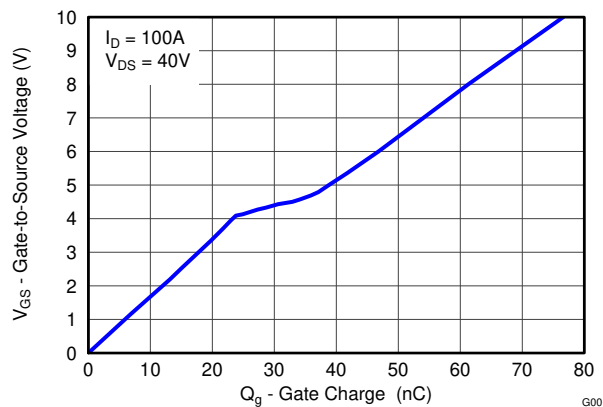
Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	80	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package limited)	150	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	208	
	Continuous Drain Current (Silicon limited), $T_C = 100^\circ\text{C}$	147	
I_{DM}	Pulsed Drain Current ⁽¹⁾	400	A
P_D	Power Dissipation	300	W
T_J, T_{stg}	Operating Junction and Storage Temperature Range	-55 to 175	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 101\text{A}, L = 0.1\text{mH}, R_G = 25\Omega$	510	mJ

- (1) Max $R_{\theta JC} = 0.5^\circ\text{C/W}$, pulse duration $\leq 100\mu\text{s}$, duty cycle $\leq 1\%$



$R_{DS(on)}$ vs V_{GS}



Gate Charge



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4 Specifications

4.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
B _V DSS	Drain-to-Source Voltage	V _{GS} = 0V, I _D = 250μA	80			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0V, V _{DS} = 64V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0V, V _{GS} = 20V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250μA	2.2	2.6	3.2	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 6V, I _D = 100A		2.9	3.8	mΩ
		V _{GS} = 10V, I _D = 100A		2.6	3.1	mΩ
g _{fs}	Transconductance	V _{DS} = 8V, I _D = 100A		262		S
DYNAMIC CHARACTERISTICS						
C _{iss}	Input Capacitance	V _{GS} = 0V, V _{DS} = 40V, f = 1MHz		6090	7820	pF
C _{oss}	Output Capacitance			1600	2080	pF
C _{rss}	Reverse Transfer Capacitance			26	34	pF
R _G	Series Gate Resistance			1.4	2.8	Ω
Q _g	Gate Charge Total (10V)	V _{DS} = 40V, I _D = 100A		76		nC
Q _{gd}	Gate Charge Gate to Drain			11		nC
Q _{gs}	Gate Charge Gate to Source			25		nC
Q _{g(th)}	Gate Charge at V _{th}			15		nC
Q _{oss}	Output Charge	V _{DS} = 40V, V _{GS} = 0V		214		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 50V, V _{GS} = 10V, I _{DS} = 100A, R _G = 0Ω		31		ns
t _r	Rise Time			16		ns
t _{d(off)}	Turn Off Delay Time			62		ns
t _f	Fall Time			6		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _{SD} = 100A, V _{GS} = 0V		0.9	1.1	V
Q _{rr}	Reverse Recovery Charge	V _{DS} = 40V, I _F = 100A,		400		nC
t _{rr}	Reverse Recovery Time	di/dt = 300A/μs		88		ns

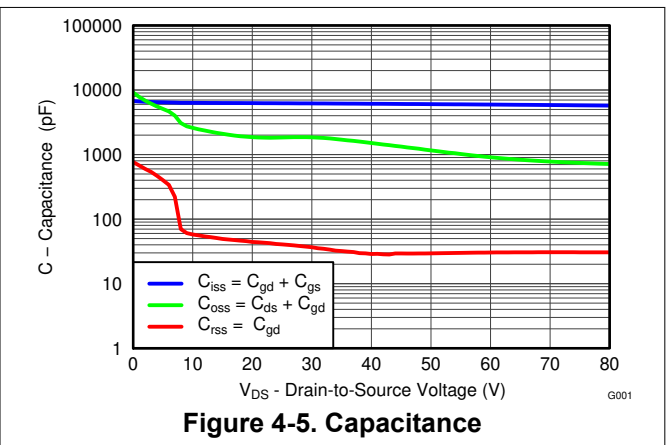
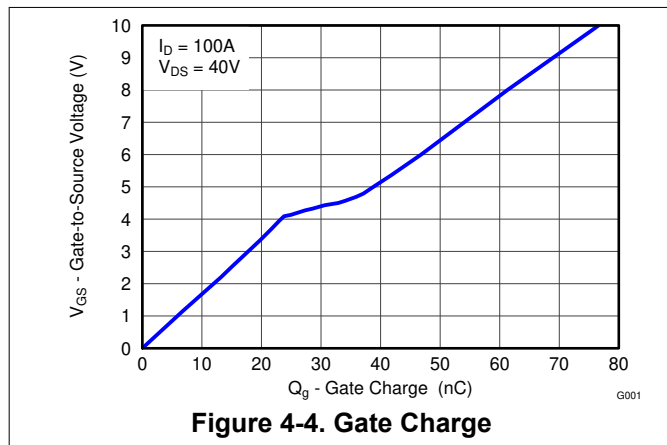
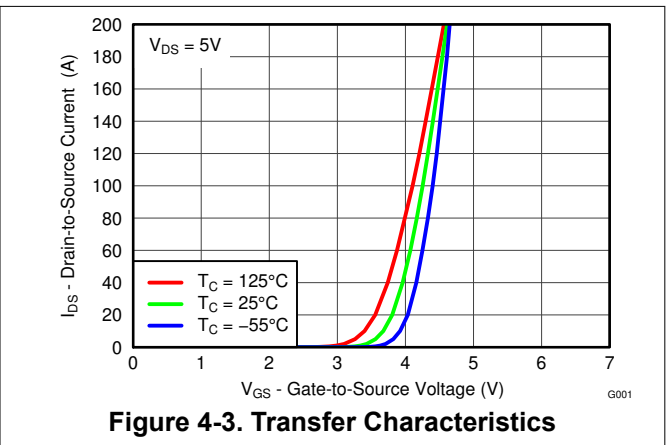
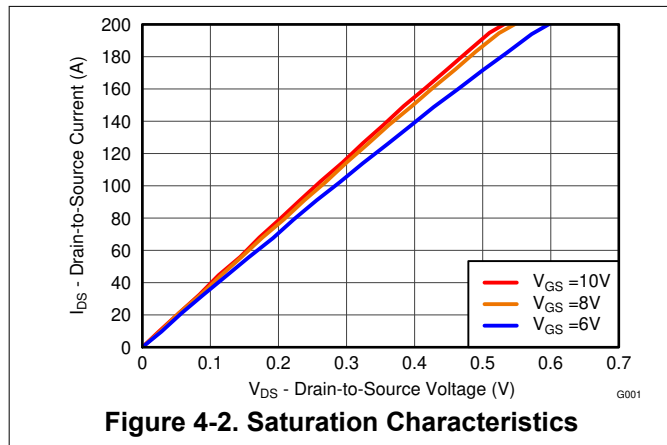
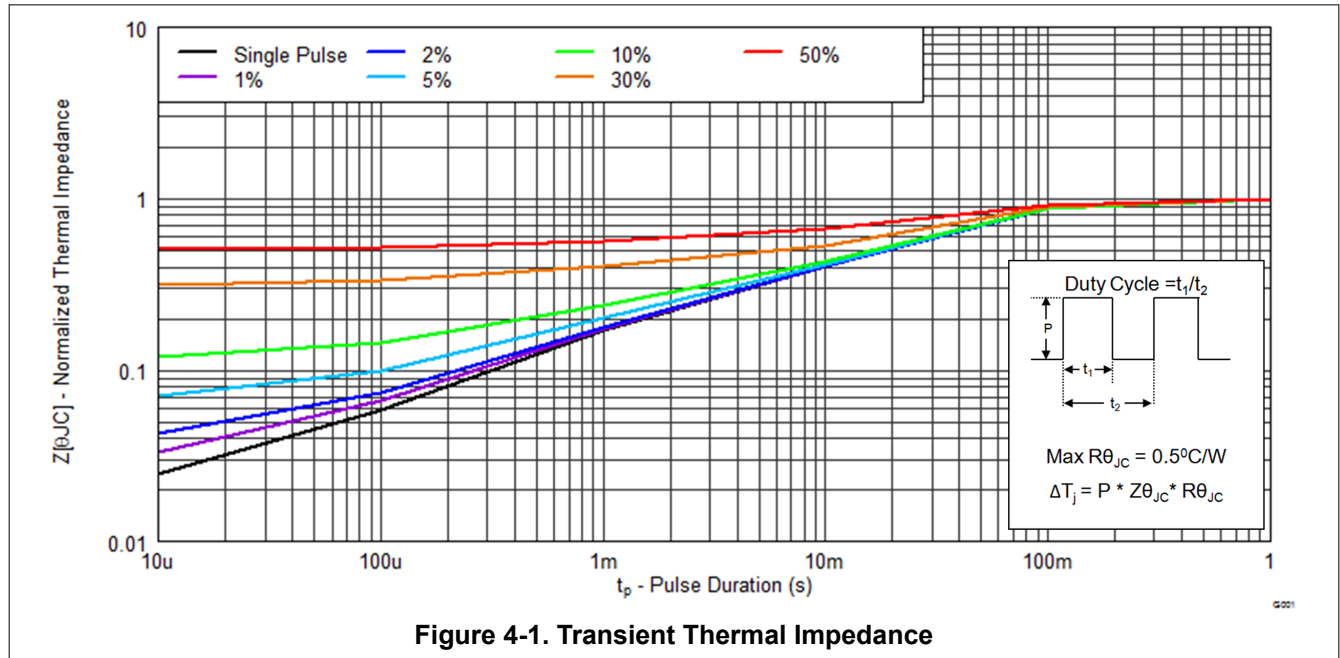
4.2 Thermal Information

(T_A = 25°C unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-Case Thermal Resistance			0.5	°C/W
R _{θJA}	Junction-to-Ambient Thermal Resistance			62	

4.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)



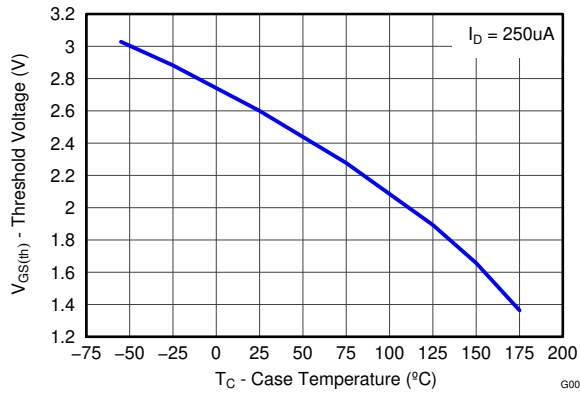


Figure 4-6. Threshold Voltage vs Temperature

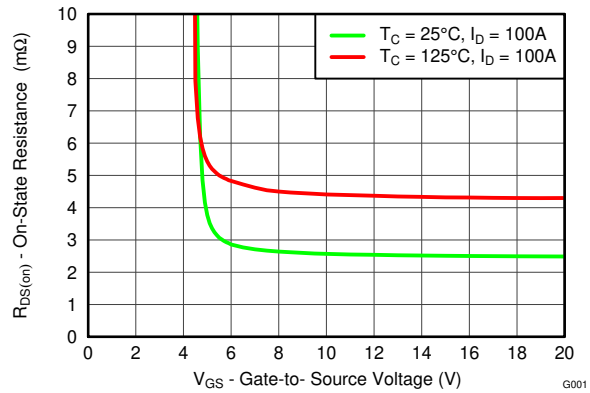


Figure 4-7. On-State Resistance vs Gate-to-Source Voltage

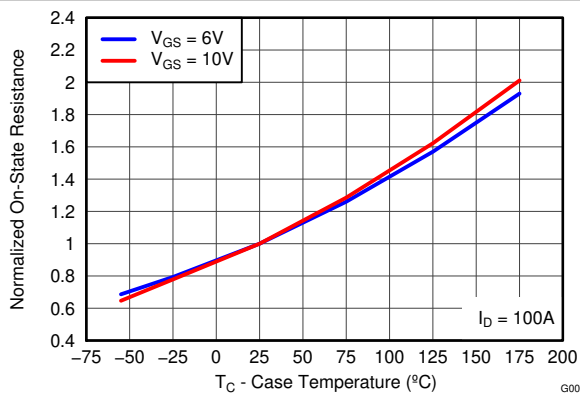


Figure 4-8. Normalized On-State Resistance vs Temperature

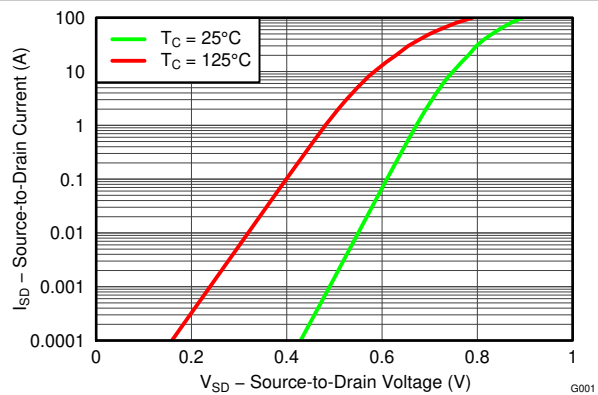


Figure 4-9. Typical Diode Forward Voltage

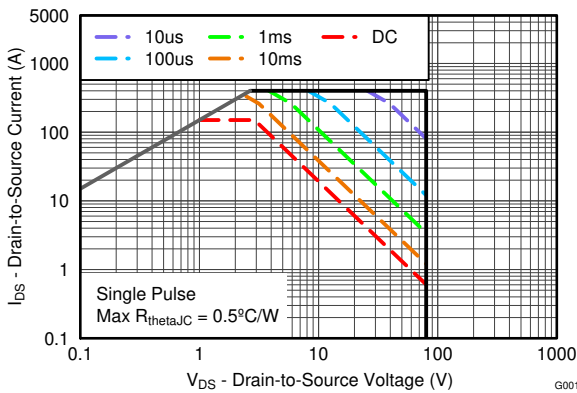


Figure 4-10. Maximum Safe Operating Area

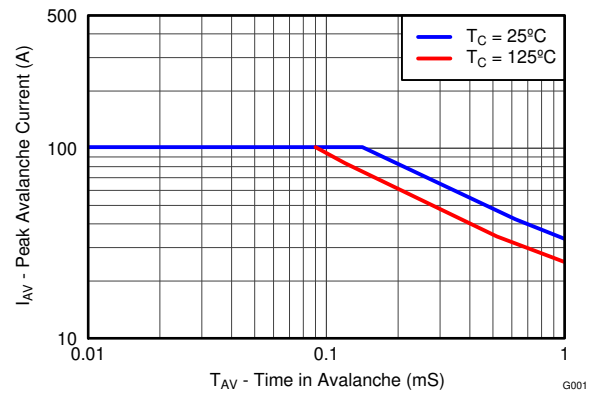


Figure 4-11. Single Pulse Unclamped Inductive Switching

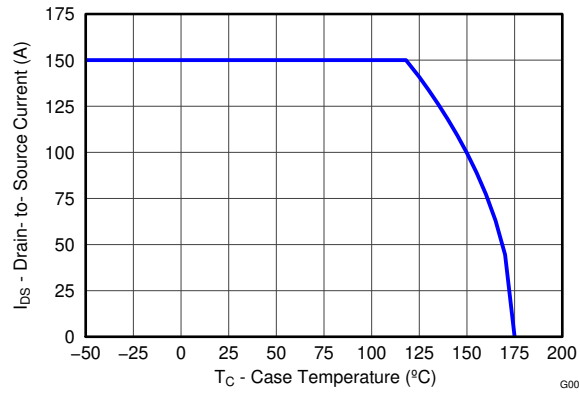


Figure 4-12. Maximum Drain Current vs Temperature

5 Device and Documentation Support

5.1 Third-Party Products Disclaimer

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5.2 Documentation Support

5.2.1 Related Documentation

5.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

5.4 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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5.5 Trademarks

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5.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

5.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

6 Revision History

Changes from Revision B (October 2014) to Revision C (April 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1

Changes from Revision A (January 2014) to Revision B (October 2014)	Page
• Updated Pulsed Drain Current Conditions	1
• Updated the SOA in Figure 4-10	4

Changes from Revision * (January 2014) to Revision A (February 2014)	Page
• Increased Pulsed Drain Current Limit	1
• Updated Figure 4-9	4

7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19505KCS	ACTIVE	TO-220	KCS	3	50	RoHS-Exempt & Green	SN	N / A for Pkg Type	-55 to 175	CSD19505KCS	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TUBE


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CSD19505KCS	KCS	TO-220	3	50	532	34.1	700	9.6
CSD19505KCS	KCS	TO-220	3	50	534.5	33	7000	3.4

KCS0003B



PACKAGE OUTLINE

TO-220 - 19.65 mm max height

TO-220



4222214/B 08/2018

EXAMPLE BOARD LAYOUT

KCS0003B

TO-220 - 19.65 mm max height

TO-220



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:15X

4222214/B 08/2018

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