1 Features
- Ultra-Low Q_g and Q_gd
- Low-Thermal Resistance
- Avalanche Rated
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

2 Applications
- Secondary Side Synchronous Rectifier
- Hot Swap Telecom
- Motor Control

3 Description
This 100-V, 6.4-mΩ, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

---

Product Summary

<table>
<thead>
<tr>
<th>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</th>
<th>TYPICAL VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;DS&lt;/sub&gt; Drain-to-Source Voltage</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>Q&lt;sub&gt;T&lt;/sub&gt; Gate Charge Total (10 V)</td>
<td>37</td>
<td>nC</td>
</tr>
<tr>
<td>Q&lt;sub&gt;gd&lt;/sub&gt; Gate Charge Gate-to-Drain</td>
<td>7.5</td>
<td>nC</td>
</tr>
<tr>
<td>R&lt;sub&gt;DS(on)&lt;/sub&gt; Drain-to-Source On Resistance</td>
<td>V&lt;sub&gt;DS&lt;/sub&gt; = 6 V 7.3</td>
<td>mΩ</td>
</tr>
<tr>
<td></td>
<td>V&lt;sub&gt;DS&lt;/sub&gt; = 10 V 6.4</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;GS(th)&lt;/sub&gt; Threshold Voltage</td>
<td>2.7</td>
<td>V</td>
</tr>
</tbody>
</table>

---

Device Information<sup>(1)</sup>

<table>
<thead>
<tr>
<th>DEVICE</th>
<th>PACKAGE</th>
<th>MEDIA</th>
<th>QTY</th>
<th>SHIP</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD19531KCS</td>
<td>TO-220 Plastic Package</td>
<td>Tube</td>
<td>50</td>
<td>Tube</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> For all available packages, see the orderable addendum at the end of the data sheet.

---

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>T&lt;sub&gt;A&lt;/sub&gt; = 25°C</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>V&lt;sub&gt;DS&lt;/sub&gt; Drain-to-Source Voltage</td>
<td>100</td>
<td>V</td>
</tr>
<tr>
<td>V&lt;sub&gt;GS&lt;/sub&gt; Gate-to-Source Voltage</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>I&lt;sub&gt;D&lt;/sub&gt; Continuous Drain Current (Package Limited)</td>
<td>100</td>
<td>A</td>
</tr>
<tr>
<td>I&lt;sub&gt;D&lt;/sub&gt; Continuous Drain Current (Silicon Limited), T&lt;sub&gt;C&lt;/sub&gt; = 25°C</td>
<td>110</td>
<td>A</td>
</tr>
<tr>
<td>I&lt;sub&gt;D&lt;/sub&gt; Continuous Drain Current (Silicon Limited), T&lt;sub&gt;C&lt;/sub&gt; = 100°C</td>
<td>78</td>
<td>A</td>
</tr>
<tr>
<td>I&lt;sub&gt;DM&lt;/sub&gt; Pulsed Drain Current&lt;sup&gt;(1)&lt;/sup&gt;</td>
<td>285</td>
<td>A</td>
</tr>
<tr>
<td>P&lt;sub&gt;D&lt;/sub&gt; Power Dissipation</td>
<td>214</td>
<td>W</td>
</tr>
<tr>
<td>T&lt;sub&gt;J&lt;/sub&gt; Operating Junction, Storage Temperature</td>
<td>−55 to 175</td>
<td>°C</td>
</tr>
<tr>
<td>E&lt;sub&gt;AS&lt;/sub&gt; Avalanche Energy, Single Pulse</td>
<td>180</td>
<td>mJ</td>
</tr>
</tbody>
</table>

<sup>(1)</sup> Max R<sub>θJC</sub> = 0.7°C/W, pulse duration ≤ 100 µs, duty cycle ≤ 1%.

---

R<sub>DS(on)</sub> vs V<sub>GS</sub>

Gate Charge

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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2 Applications .......................................................... 1
3 Description ............................................................ 1
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4 Revision History

Changes from Revision B (June 2014) to Revision C ................................................................. 7
• Added Receiving Notification of Documentation Updates section and Community Resources section to the Device and Documentation Support section ........................................................................................................................................ 7
• Changed package drawing in KCS Package Dimensions section ................................................................. 8

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• Added value for max $Q_g$ ............................................................................................................................................... 3

Changes from Original (September 2013) to Revision A ................................................................. 1
• Updated the silicon limited currents to reflect increase in device operating temperature range .............................. 1
• Increased pulsed current to reflect new conditions ........................................................................................................... 1
• Increased max power dissipation to reflect new conditions ........................................................................................................... 1
• Increased operating and junction temperature range to 175ºC ............................................................................................. 1
• Updated the pulsed drain current conditions .......................................................................................................................... 1
• Changed Figure 1 from a normalized $R_{thJA}$ curve to a normalized $R_{thJC}$ curve ................................................................. 4
• Updated Figure 6 to reflect increase in device operating temperature range ................................................................. 5
• Updated Figure 8 to reflect increase in device operating temperature range ................................................................. 5
• Updated Figure 10 to reflect measured SOA data ................................................................................................................ 6
• Updated Figure 12 to reflect increase in device operating temperature range ................................................................. 6
## 5 Specifications

### 5.1 Electrical Characteristics

\( T_A = 25^\circ C \) (unless otherwise stated)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>STATIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( BVDSS ) Drain-to-source voltage</td>
<td>( V_{GS} = 0 \ V, \ I_D = 250 \ \mu A )</td>
<td>100</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( IDSS ) Drain-to-source leakage current</td>
<td>( V_{GS} = 0 \ V, \ V_DS = 80 \ V )</td>
<td>1</td>
<td></td>
<td></td>
<td>\mu A</td>
</tr>
<tr>
<td>( IGSS ) Gate-to-source leakage current</td>
<td>( V_{DS} = 0 \ V, \ V_{GS} = 20 \ V )</td>
<td>100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>( VGS(th) ) Gate-to-source threshold voltage</td>
<td>( V_{DS} = V_{GS}, \ I_D = 250 \ \mu A )</td>
<td>2.2</td>
<td>2.7</td>
<td>3.3</td>
<td>V</td>
</tr>
<tr>
<td>( RDS(on) ) Drain-to-source on resistance</td>
<td>( V_{GS} = 6 \ V, \ I_D = 60 \ A )</td>
<td>7.3</td>
<td>8.8</td>
<td></td>
<td>m\Omega</td>
</tr>
<tr>
<td></td>
<td>( V_{GS} = 10 \ V, \ I_D = 60 \ A )</td>
<td>6.4</td>
<td>7.7</td>
<td></td>
<td></td>
</tr>
<tr>
<td>( gfs ) Transconductance</td>
<td>( V_{DS} = 10 \ V, \ I_D = 60 \ A )</td>
<td>137</td>
<td></td>
<td></td>
<td>S</td>
</tr>
<tr>
<td><strong>DYNAMIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( Ciss ) Input capacitance</td>
<td>( V_{GS} = 0 \ V, \ V_{DS} = 50 \ V, f = 1 \ MHz )</td>
<td>2980</td>
<td>3870</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( Coss ) Output capacitance</td>
<td>( V_{GS} = 0 \ V, \ V_{DS} = 50 \ V, f = 1 \ MHz )</td>
<td>560</td>
<td>728</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( Crss ) Reverse transfer capacitance</td>
<td>( V_{DS} = 50 \ V, \ I_D = 60 \ A )</td>
<td>13</td>
<td>17</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>( Rg ) Series gate resistance</td>
<td>( V_{DS} = 50 \ V, \ I_D = 60 \ A )</td>
<td>1.3</td>
<td>2.6</td>
<td></td>
<td>\Omega</td>
</tr>
<tr>
<td>( Qg ) Gate charge total (10 V)</td>
<td>( V_{DS} = 50 \ V, \ I_D = 60 \ A )</td>
<td>38</td>
<td>49</td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Qgd ) Gate charge gate-to-drain</td>
<td>( V_{DS} = 50 \ V, \ I_D = 60 \ A )</td>
<td>7.5</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Qgs ) Gate charge gate-to-source</td>
<td>( V_{DS} = 50 \ V, \ I_D = 60 \ A )</td>
<td>11.9</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Qg(th) ) Gate charge at ( V_{th} )</td>
<td>( V_{DS} = 50 \ V, \ I_D = 60 \ A )</td>
<td>7.3</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( Qoss ) Output charge</td>
<td>( V_{DS} = 50 \ V, \ V_{GS} = 0 \ V )</td>
<td>98</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( t_on ) Turnon delay time</td>
<td>( V_{DS} = 50 \ V, \ V_{GS} = 10 \ V, \ I_D = 60 \ A, \ R_G = 0 \ \Omega )</td>
<td>8.4</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( tr ) Rise Time</td>
<td>( V_{DS} = 50 \ V, \ V_{GS} = 10 \ V, \ I_D = 60 \ A, \ R_G = 0 \ \Omega )</td>
<td>7.2</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( t_off ) Turnoff delay time</td>
<td>( V_{DS} = 50 \ V, \ V_{GS} = 10 \ V, \ I_D = 60 \ A, \ R_G = 0 \ \Omega )</td>
<td>16</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>( tf ) Fall time</td>
<td>( V_{DS} = 50 \ V, \ V_{GS} = 10 \ V, \ I_D = 60 \ A, \ R_G = 0 \ \Omega )</td>
<td>4.1</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>DIODE CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>( V_{BD} ) Diode forward voltage</td>
<td>( I_{SD} = 60 \ A, \ V_{GS} = 0 \ V )</td>
<td>0.9</td>
<td>1</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>( Qr ) Reverse recovery charge</td>
<td>( V_{DS} = 50 \ V, \ I_F = 60 \ A, \ di/dt = 300 \ A/\mu s )</td>
<td>270</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>( tr ) Reverse recovery time</td>
<td>( V_{DS} = 50 \ V, \ I_F = 60 \ A, \ di/dt = 300 \ A/\mu s )</td>
<td>83</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

### 5.2 Thermal Information

\( T_A = 25^\circ C \) (unless otherwise stated)

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>( R_{JC} ) Junction-to-case thermal resistance</td>
<td>0.7</td>
<td></td>
<td></td>
<td>^C/W</td>
</tr>
<tr>
<td>( R_{JA} ) Junction-to-ambient thermal resistance</td>
<td>62</td>
<td></td>
<td></td>
<td>^C/W</td>
</tr>
</tbody>
</table>

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Submit Documentation Feedback

Product Folder Links: CSD19531KCS
5.3 Typical MOSFET Characteristics

\( T_A = 25^\circ C \) (unless otherwise stated)

![Graph showing typical MOSFET characteristics](image)

**Figure 1.** Transient Thermal Impedance

**Figure 2.** Saturation Characteristics

**Figure 3.** Transfer Characteristics
Typical MOSFET Characteristics (continued)

\( T_A = 25^\circ C \) (unless otherwise stated)

### Figure 4. Gate Charge

![Gate Charge Graph](#)

### Figure 5. Capacitance

![Capacitance Graph](#)

### Figure 6. Threshold Voltage vs Temperature

![Threshold Voltage Graph](#)

### Figure 7. On-State Resistance vs Gate-to-Source Voltage

![On-State Resistance Graph](#)

### Figure 8. Normalized On-State Resistance vs Temperature

![Normalized On-State Resistance Graph](#)

### Figure 9. Typical Diode Forward Voltage

![Diode Forward Voltage Graph](#)
Typical MOSFET Characteristics (continued)

$T_A = 25^\circ C$ (unless otherwise stated)

**Figure 10. Maximum Safe Operating Area**

**Figure 11. Single Pulse Unclamped Inductive Switching**

**Figure 12. Maximum Drain Current vs Temperature**
6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI’s views; see TI’s Terms of Use.

TI E2E™ Online Community  **TI’s Engineer-to-Engineer (E2E) Community**. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  **TI’s Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

**SLYZ022 — TI Glossary.**

This glossary lists and explains terms, acronyms, and definitions.
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 KCS Package Dimensions

![KCS Package Dimensions Diagram]

**Notes:**
1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-220.

**Table 1. Pin Configuration**

<table>
<thead>
<tr>
<th>POSITION</th>
<th>DESIGNATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>Pin 1</td>
<td>Gate</td>
</tr>
<tr>
<td>Pin 2 / Tab</td>
<td>Drain</td>
</tr>
<tr>
<td>Pin 3</td>
<td>Source</td>
</tr>
</tbody>
</table>
### PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD19531KCS</td>
<td>ACTIVE</td>
<td>TO-220</td>
<td>KCS</td>
<td>3</td>
<td>50</td>
<td>RoHS-Exempt &amp; Green</td>
<td>SN</td>
<td>N/A for Pkg Type</td>
<td>-55 to 175</td>
<td>CSD19531KCS</td>
</tr>
</tbody>
</table>

- **(1)** The marketing status values are defined as follows:
  - **ACTIVE**: Product device recommended for new designs.
  - **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
  - **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
  - **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
  - **OBSOLETE**: TI has discontinued the production of the device.

- **(2)** **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
  - **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
  - **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

- **(3)** **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

- **(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

- **(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

- **(6)** **Lead finish/Ball material** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**PACKAGE MATERIALS INFORMATION**

- **Device**: CSD19531KCS
  - **Package Name**: KCS
  - **Package Type**: TO-220
  - **Pins**: 3
  - **SPQ**: 50
  - **L (mm)**: 532
  - **W (mm)**: 34.1
  - **T (µm)**: 700
  - **B (mm)**: 9.6

- **Device**: CSD19531KCS
  - **Package Name**: KCS
  - **Package Type**: TO-220
  - **Pins**: 3
  - **SPQ**: 50
  - **L (mm)**: 532
  - **W (mm)**: 34.1
  - **T (µm)**: 700
  - **B (mm)**: 9.6

*All dimensions are nominal*
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