

# CSD19532Q5B 100 V N-Channel NexFET™ Power MOSFET

## 1 Features

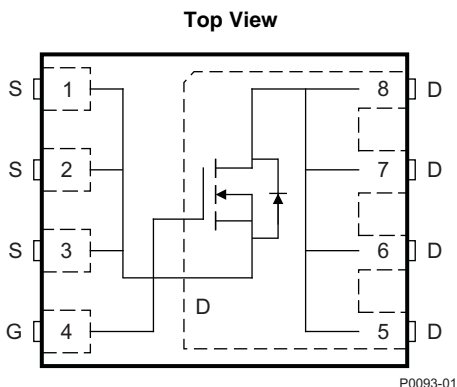
- Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm x 6-mm Plastic Package

## 2 Applications

- Synchronous Rectifier for Offline and Isolated DC-DC Converters
- Motor Control

## 3 Description

This 100 V, 4 mΩ, SON 5-mm x 6-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



### Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	100		V
$Q_g$	Gate Charge Total (10 V)	48		nC
$Q_{gd}$	Gate Charge Gate to Drain	8.7		nC
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}$	4.6	mΩ
		$V_{GS} = 10\text{ V}$	4	mΩ
$V_{GS(th)}$	Threshold Voltage	2.6		V

### Ordering Information<sup>(1)</sup>

Device	Media	Qty	Package	Ship
CSD19532Q5B	13-Inch Reel	2500	SON 5 x 6 mm Plastic Package	Tape and Reel
CSD19532Q5BT	13-Inch Reel	250		

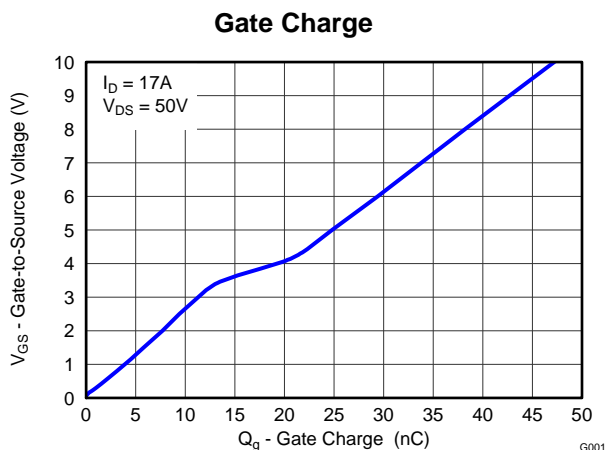
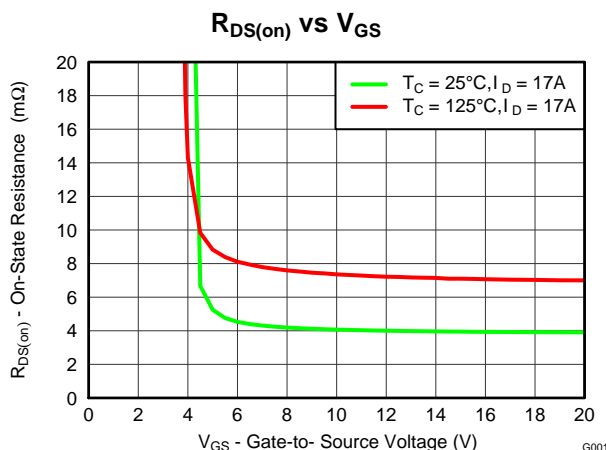
(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	100	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current (Package limited)	100	A
	Continuous Drain Current (Silicon limited), $T_C = 25^\circ\text{C}$	140	
	Continuous Drain Current <sup>(1)</sup>	17	
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	400	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.1	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	195	
$T_J, T_{stg}$	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, single pulse $I_D = 74\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	274	mJ

(1) Typical  $R_{\theta JA} = 40^\circ\text{C/W}$  on a 1-inch<sup>2</sup>, 2-oz. Cu pad on a 0.06-inch thick FR4 PCB.

(2) Max  $R_{\theta JC} = 0.8^\circ\text{C/W}$ , Pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$



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## 4 Revision History

### Changes from Revision A (June 2014) to Revision B

**Page**

- Added the *Receiving Notification of Documentation Updates* and *Community Resources* sections to *Device and Documentation Support*. ..... 7
- Changed the dimension between pads 3 and 4 from 0.028 inches: to 0.050 inches in the *Recommended PCB Pattern* section diagram ..... 9

### Changes from Original (December 2013) to Revision A

**Page**

- Added small reel option to ordering information table. .... 1
- Increased silicon limit for continuous drain current to 140 A. .... 1
- Increased max pulsed current to 400 A. .... 1
- Added max power rating when the case temperature is held to 25°C. .... 1
- Updated pulsed current conditions to specify Max  $R_{\theta JC}$ . .... 1
- Updated [Figure 10](#). .... 6
- Updated mechanical drawing. .... 8

## 5 Specifications

### 5.1 Electrical Characteristics

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$V_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	100			V
$I_{DSS}$	Drain-to-Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 80\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	2.2	2.6	3.2	V
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 6\text{ V}, I_D = 17\text{ A}$		4.6	5.7	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 17\text{ A}$		4	4.9	m $\Omega$
$g_{fs}$	Transconductance	$V_{DS} = 50\text{ V}, I_D = 17\text{ A}$		84		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 50\text{ V}, f = 1\text{ MHz}$		3700	4810	pF
$C_{oss}$	Output Capacitance			706	918	pF
$C_{rss}$	Reverse Transfer Capacitance			14	18	pF
$R_G$	Series Gate Resistance			1.2	2.4	$\Omega$
$Q_g$	Gate Charge Total (10 V)	$V_{DS} = 50\text{ V}, I_D = 17\text{ A}$		48	62	nC
$Q_{gd}$	Gate Charge Gate to Drain			8.7		nC
$Q_{gs}$	Gate Charge Gate to Source			13		nC
$Q_{g(th)}$	Gate Charge at $V_{th}$			9.5		nC
$Q_{oss}$	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		128		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 50\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 17\text{ A}, R_G = 0\ \Omega$		7		ns
$t_r$	Rise Time			6		ns
$t_{d(off)}$	Turn Off Delay Time			22		ns
$t_f$	Fall Time			6		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 17\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
$Q_{rr}$	Reverse Recovery Charge	$V_{DS} = 50\text{ V}, I_F = 17\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		249		nC
$t_{rr}$	Reverse Recovery Time			80		ns

### 5.2 Thermal Information

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-Case Thermal Resistance <sup>(1)</sup>			0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient Thermal Resistance <sup>(1)(2)</sup>			50	

- (1)  $R_{\theta JC}$  is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inches  $\times$  1.5-inches (3.81-cm  $\times$  3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



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Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on  
1 inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2-oz. (0.071-mm thick)  
Cu.

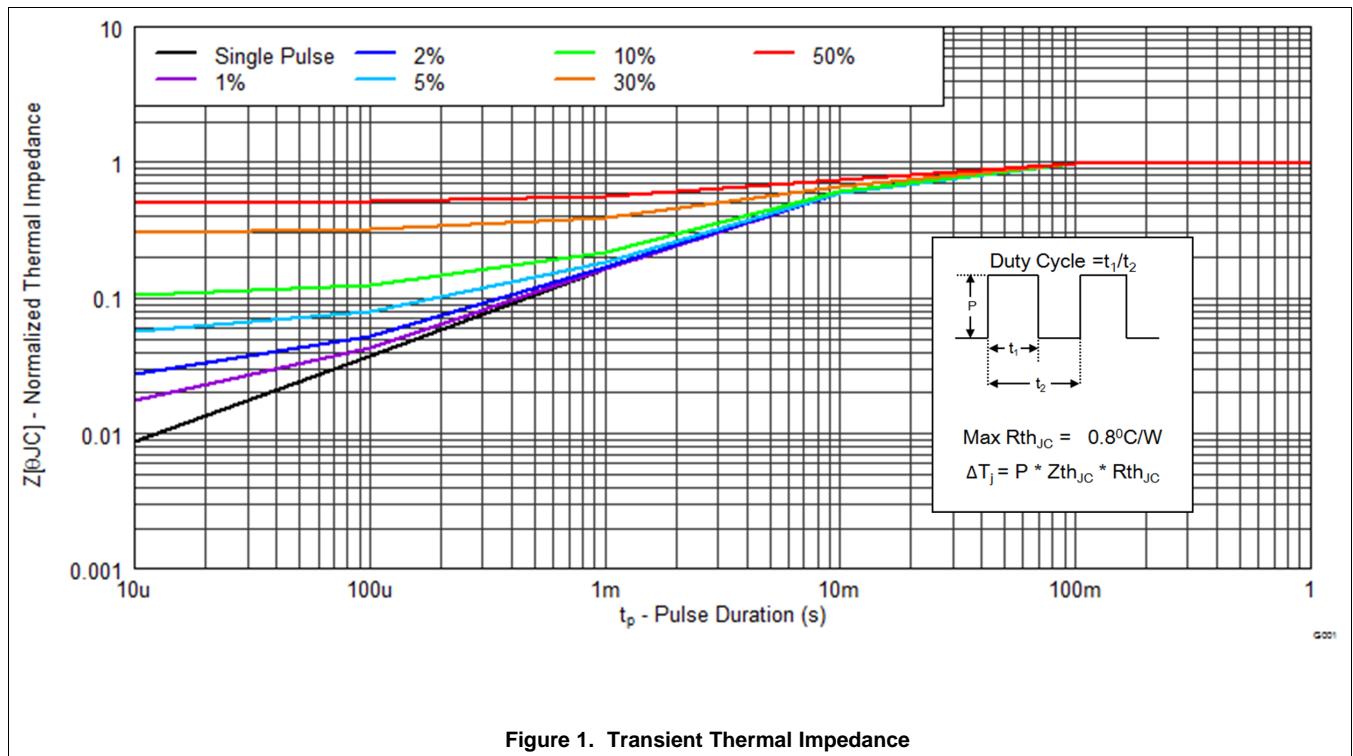


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Max  $R_{\theta JA} = 125^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

### 5.3 Typical MOSFET Characteristics

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)



Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

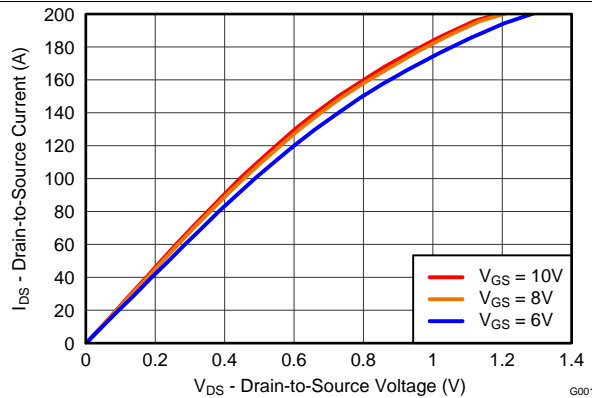


Figure 2. Saturation Characteristics

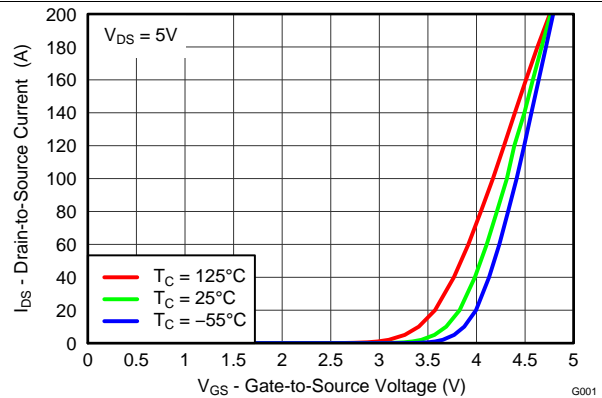


Figure 3. Transfer Characteristics

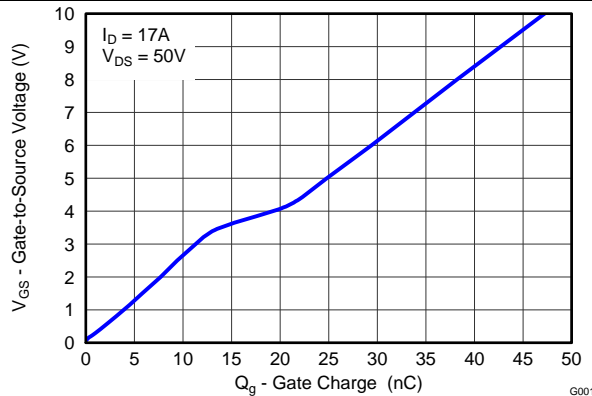


Figure 4. Gate Charge

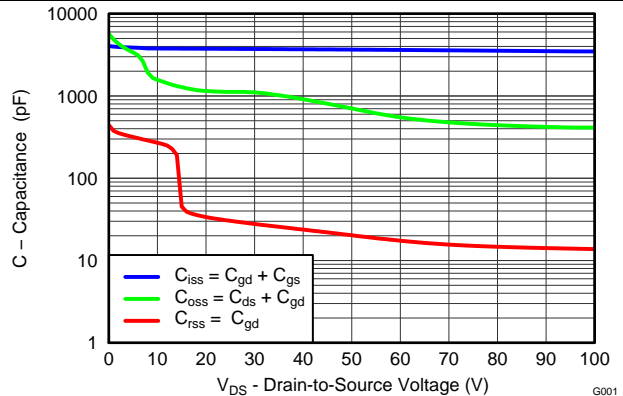


Figure 5. Capacitance

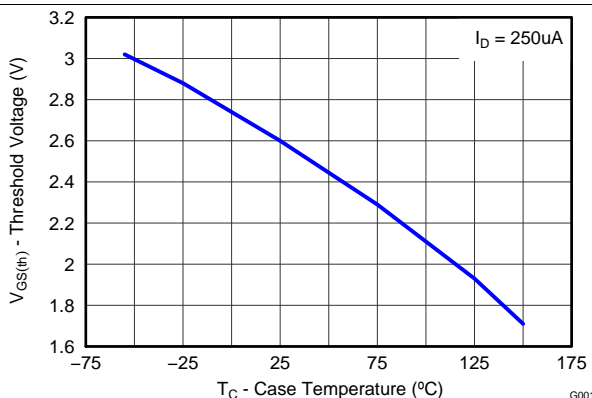


Figure 6. Threshold Voltage vs Temperature

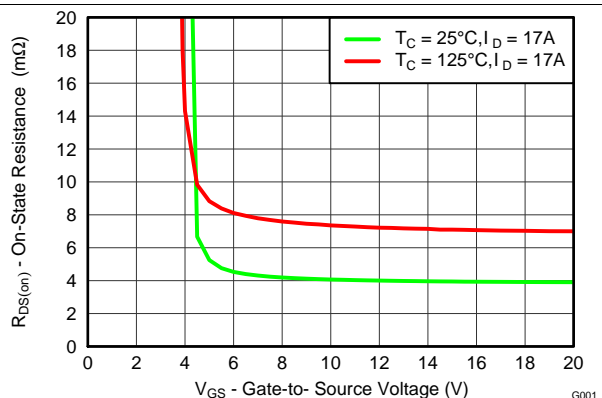


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

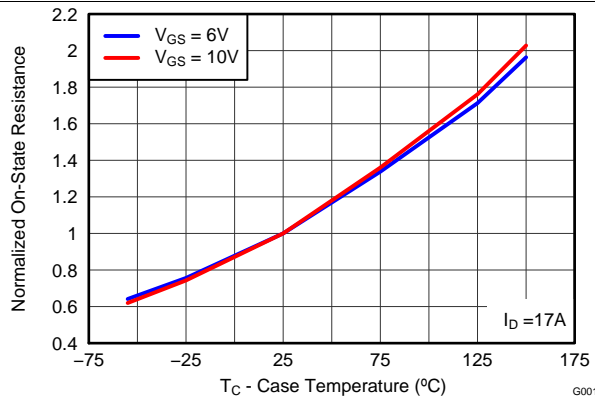


Figure 8. Normalized On-State Resistance vs Temperature

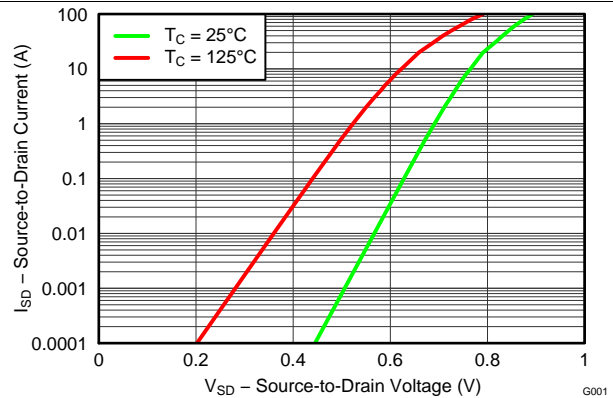


Figure 9. Typical Diode Forward Voltage

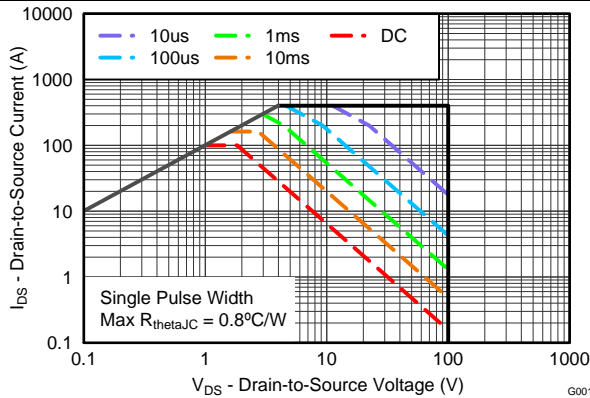


Figure 10. Maximum Safe Operating Area

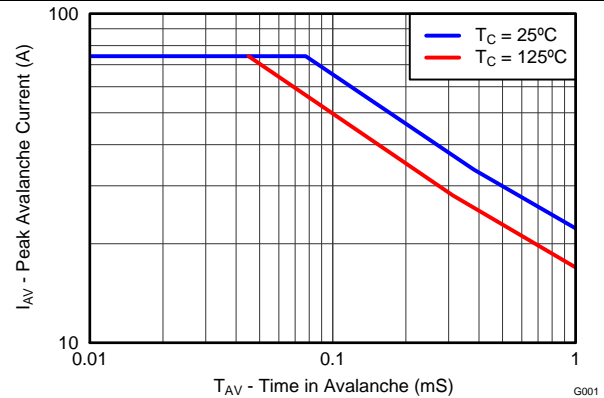


Figure 11. Single Pulse Unclamped Inductive Switching

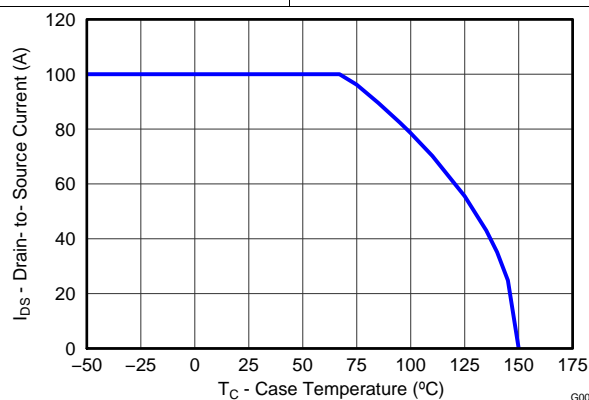


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.

### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

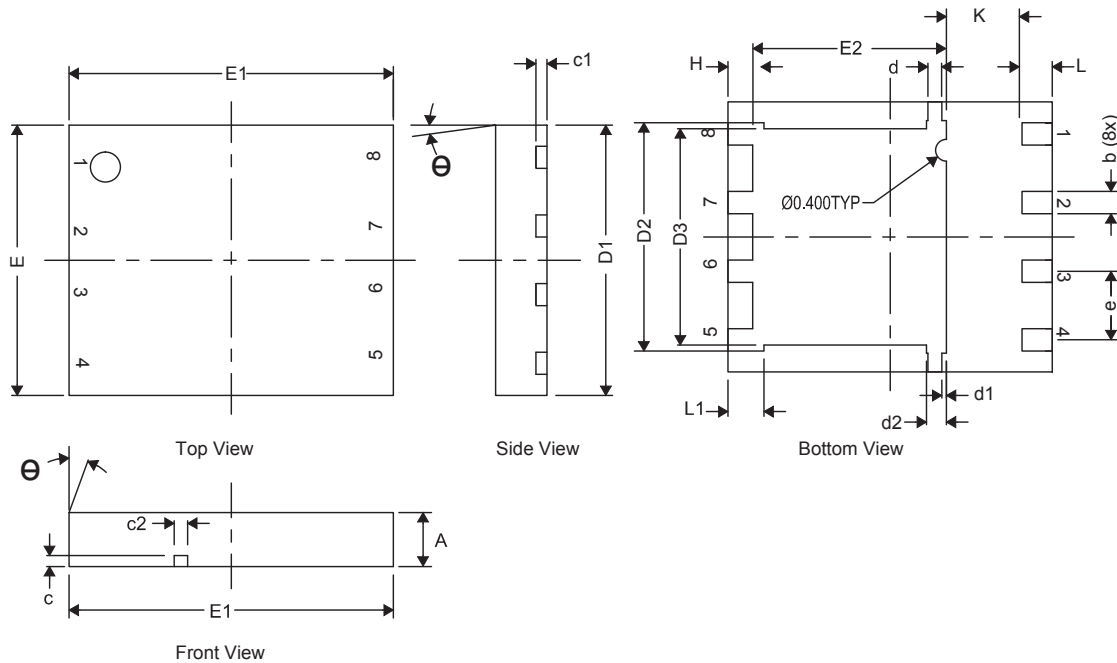
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

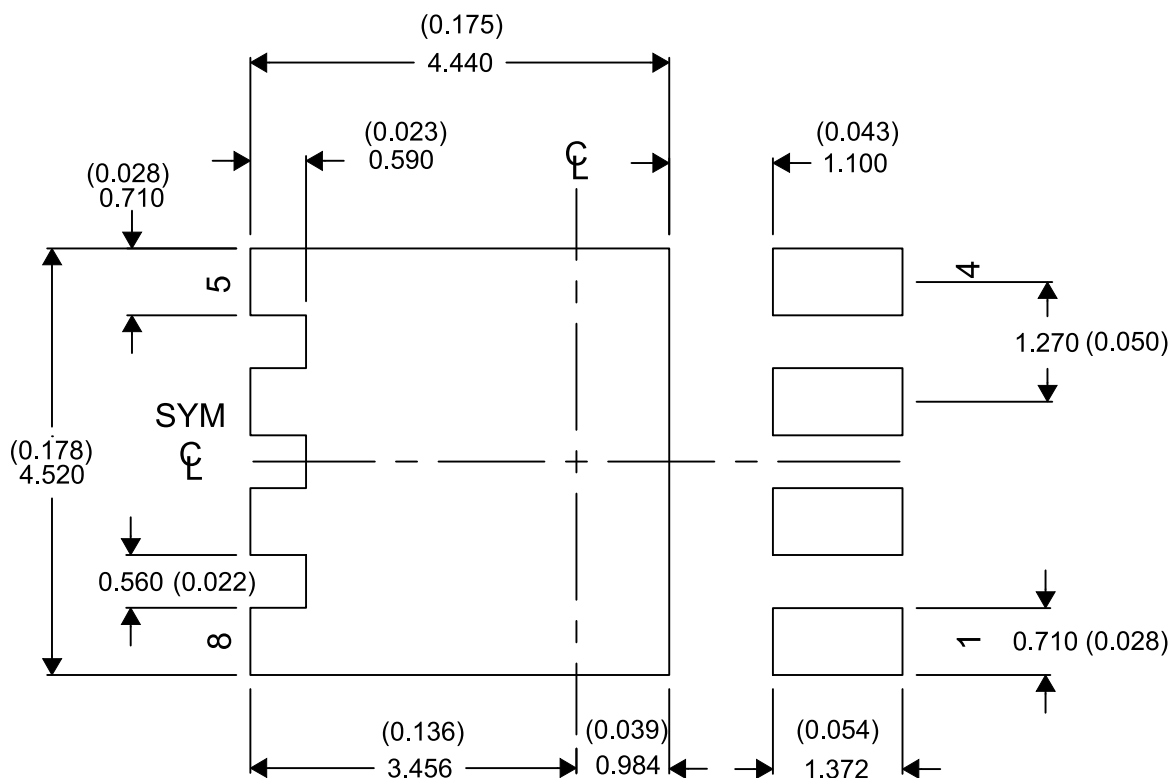
### 7.1 Q5B Package Dimensions



DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 TYP		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
$\theta$	0°	—	—
K	1.40 TYP		

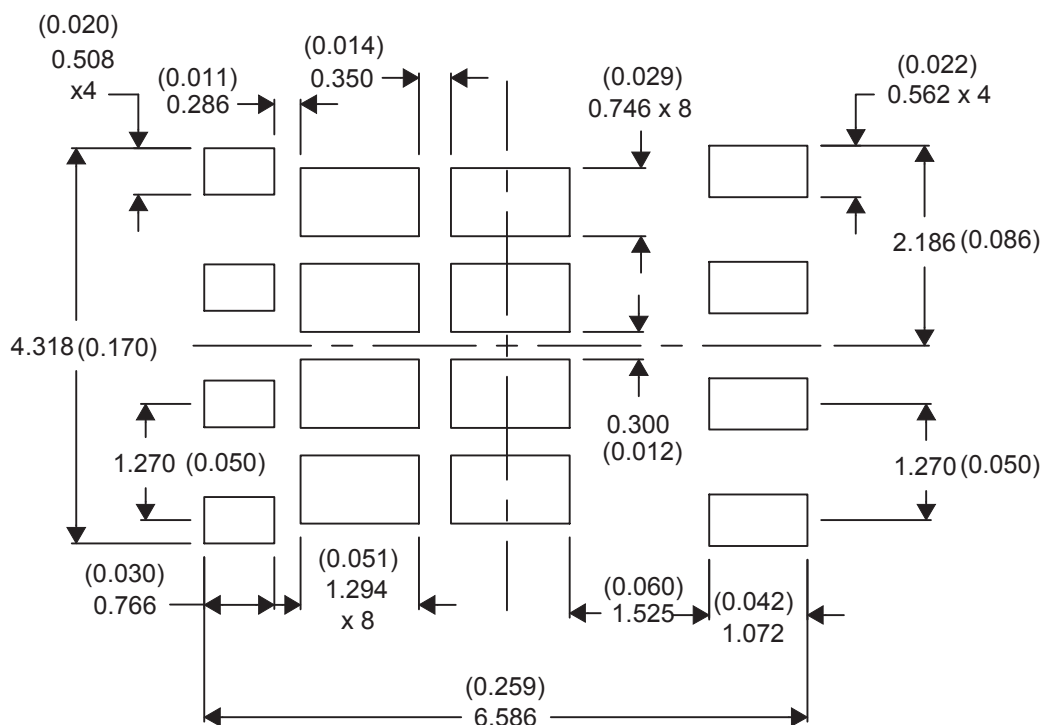


## 7.2 Recommended PCB Pattern

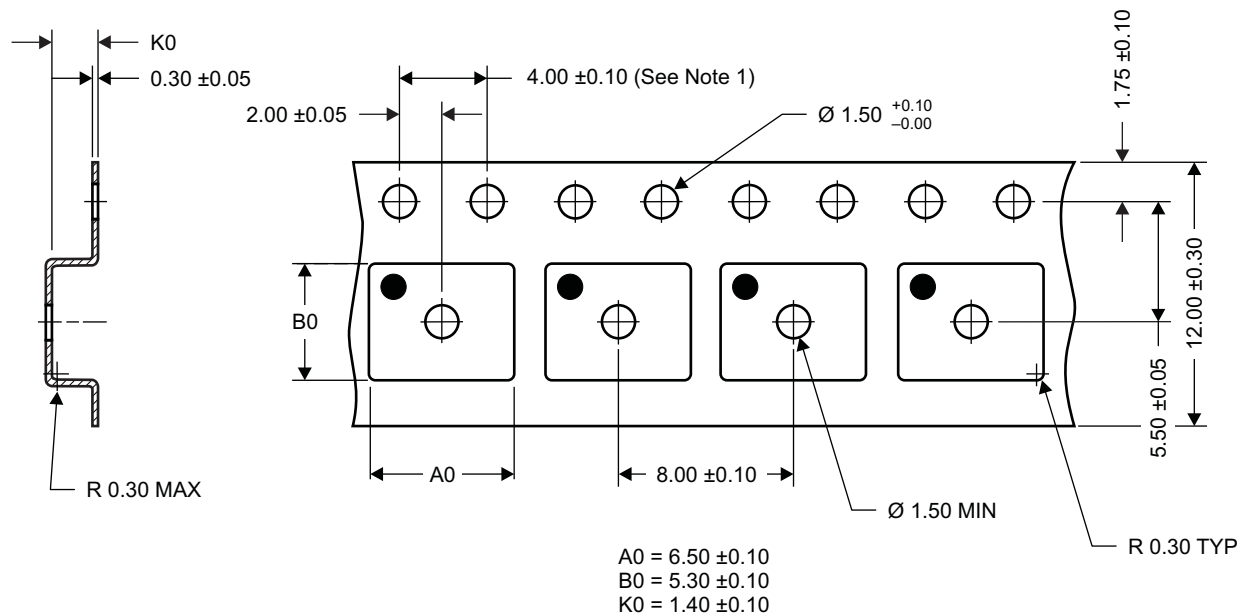


For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

## 7.3 Recommended Stencil Pattern



## 7.4 Q5B Tape and Reel Information



M0138-01

### Notes:

1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$ .
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static-dissipative polystyrene.
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD19532Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 150	CSD19532	<a href="#">Samples</a>
CSD19532Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	Green (RoHS & no Sb/Br)	SN	Level-1-260C-UNLIM	-55 to 150	CSD19532	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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