1 Features
- Ultra-Low Q_g and Q_{gd}
- Low-Thermal Resistance
- Avalanche Rated
- Lead Free
- RoHS Compliant
- Halogen Free
- SON 2-mm × 2-mm Plastic Package

2 Applications
- Power Over Ethernet (PoE)
- Power Sourcing Equipment (PSE)
- Motor Control

3 Description
This 100-V, 49-mΩ, SON 2-mm × 2-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.
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4 Revision History

Changes from Original (July 2016) to Revision A

<table>
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<th>Change Description</th>
<th>Page</th>
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<tbody>
<tr>
<td>Changed test voltage $V_{DS}$ from 100 V : to 50 V in Gate Charge curve.</td>
<td>1</td>
</tr>
<tr>
<td>Changed test voltage $V_{DS}$ from 100 V : to 50 V in Figure 4.</td>
<td>4</td>
</tr>
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5 Specifications

5.1 Electrical Characteristics

$T_A = 25^\circ C$ (unless otherwise stated)

<table>
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<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
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</thead>
<tbody>
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<td><strong>STATIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$BV_{DSS}$ (Drain-to-source voltage)</td>
<td>$V_{GS} = 0 \text{ V}, I_D = 250 \mu A$</td>
<td>100</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$I_{DSS}$ (Drain-to-source leakage current)</td>
<td>$V_{GS} = 0 \text{ V}, V_{DS} = 80 \text{ V}$</td>
<td></td>
<td>1</td>
<td></td>
<td>$\mu A$</td>
</tr>
<tr>
<td>$I_{GS}$ (Gate-to-source leakage current)</td>
<td>$V_{DS} = 0 \text{ V}, V_{GS} = 20 \text{ V}$</td>
<td></td>
<td></td>
<td>100</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{GS(th)}$ (Gate-to-source threshold voltage)</td>
<td>$V_{DS} = V_{GS}, I_D = 250 \mu A$</td>
<td></td>
<td>2.8</td>
<td>3.2</td>
<td>3.8 V</td>
</tr>
<tr>
<td>$R_{DS(on)}$ (Drain-to-source on resistance)</td>
<td>$V_{GS} = 6 \text{ V}, I_D = 5 \text{ A}$</td>
<td>58</td>
<td>72</td>
<td></td>
<td>m$\Omega$</td>
</tr>
<tr>
<td>$g_{m}$ (Transconductance)</td>
<td>$V_{DS} = 10 \text{ V}, I_D = 5 \text{ A}$</td>
<td>19</td>
<td></td>
<td></td>
<td>S</td>
</tr>
<tr>
<td><strong>DYNAMIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{iss}$ (Input capacitance)</td>
<td>$V_{GS} = 0 \text{ V}, V_{DS} = 50 \text{ V}, f = 1 \text{ MHz}$</td>
<td>349</td>
<td>454</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{oss}$ (Output capacitance)</td>
<td></td>
<td>69</td>
<td>90</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$C_{rss}$ (Reverse transfer capacitance)</td>
<td>$V_{DS} = 50 \text{ V}, I_D = 5 \text{ A}$</td>
<td>12.6</td>
<td>16.4</td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td>$R_G$ (Series gate resistance)</td>
<td></td>
<td>4.6</td>
<td>9.2</td>
<td></td>
<td>$\Omega$</td>
</tr>
<tr>
<td>$Q_g$ (Gate charge total (10 $V$))</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gd}$ (Gate charge gate-to-drain)</td>
<td>$V_{DS} = 50 \text{ V}, I_D = 5 \text{ A}$</td>
<td>0.8</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gs}$ (Gate charge gate-to-source)</td>
<td></td>
<td>1.6</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{g(th)}$ (Gate charge at $V_{th}$)</td>
<td></td>
<td>1.0</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{oss}$ (Output charge)</td>
<td>$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$</td>
<td>12.3</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$t_{d(on)}$ (Turnon delay time)</td>
<td></td>
<td>5</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{r}$ (Rise time)</td>
<td>$V_{DS} = 50 \text{ V}, V_{GS} = 10 \text{ V}$</td>
<td>3</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_{d(off)}$ (Turnoff delay time)</td>
<td>$I_D = 5 \text{ A}, R_G = 0 \text{ $\Omega$}$</td>
<td>7</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td>$t_f$ (Fall time)</td>
<td></td>
<td>2</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>DIODE CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{BD}$ (Diode forward voltage)</td>
<td>$I_D = 5 \text{ A}, V_{GS} = 0 \text{ V}$</td>
<td>0.85</td>
<td>1.0</td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$Q_r$ (Reverse recovery charge)</td>
<td>$V_{DS} = 50 \text{ V}, I_F = 5 \text{ A}$</td>
<td>94</td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$t_{rr}$ (Reverse recovery time)</td>
<td>$di/dt = 300 \text{ A}/\mu s$</td>
<td>32</td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

5.2 Thermal Information

$T_A = 25^\circ C$ (unless otherwise stated)

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JC}$ (Junction-to-case thermal resistance)</td>
<td>6.2</td>
<td></td>
<td></td>
<td>$^\circ C/\text{W}$</td>
</tr>
<tr>
<td>$R_{JA}$ (Junction-to-ambient thermal resistance)</td>
<td>65</td>
<td></td>
<td></td>
<td>$^\circ C/\text{W}$</td>
</tr>
</tbody>
</table>

(1) $R_{JC}$ is determined with the device mounted on a 1-in$^2$ (6.45-cm$^2$), 2-oz (0.071-mm) thick Cu pad on a 1.5-in $\times$ 1.5-in (3.81-cm $\times$ 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{JC}$ is specified by design, whereas $R_{JA}$ is determined by the user’s board design.

(2) Device mounted on FR4 material with 1-in$^2$ (6.45-cm$^2$), 2-oz (0.071-mm) thick Cu.
Max $R_{thA} = 65^\circ$C/W when mounted on 1 in$^2$ (6.45 cm$^2$) of 2-oz (0.071-mm) thick Cu.

Max $R_{thA} = 250^\circ$C/W when mounted on a minimum pad area of 2-oz (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

$T_A = 25^\circ$C (unless otherwise stated)

Figure 1. Transient Thermal Impedance
Typical MOSFET Characteristics (continued)

\(T_A = 25^\circ\text{C}\) (unless otherwise stated)

**Figure 2. Saturation Characteristics**

\(V_{DS} = 5\, \text{V}\)

**Figure 3. Transfer Characteristics**

**Figure 4. Gate Charge**

\(I_D = 5\, \text{A}\), \(V_{DS} = 50\, \text{V}\)

**Figure 5. Capacitance**

**Figure 6. Threshold Voltage vs Temperature**

\(I_D = 250\, \mu\text{A}\)

**Figure 7. On-State Resistance vs Gate-to-Source Voltage**
Typical MOSFET Characteristics (continued)

\[ T_A = 25^\circ \text{C} \] (unless otherwise stated)

- **Figure 8. Normalized On-State Resistance vs Temperature**
  - Graph showing normalized on-state resistance vs case temperature with two lines representing different voltage values: \( V_{GS} = 6 \text{ V} \) and \( V_{GS} = 10 \text{ V} \).
  - Single pulse, max \( R_{\text{JUC}} = 6.2^\circ \text{C/W} \).

- **Figure 9. Typical Diode Forward Voltage**
  - Graph showing diode forward voltage vs source-drain voltage with lines for different case temperatures: \( T_C = 25^\circ \text{C} \) and \( T_C = 125^\circ \text{C} \).

- **Figure 10. Maximum Safe Operating Area**
  - Graph showing peak avalanche current vs time in avalanche with different pulse durations: DC, 100 \( \mu \text{s} \), 10 ms, and 1 ms.

- **Figure 11. Single Pulse Unclamped Inductive Switching**
  - Graph showing drain current vs case temperature.

- **Figure 12. Maximum Drain Current vs Temperature**
  - Graph showing drain current vs case temperature for different pulse durations.

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CSD19538Q2
SLPSS82A – JULY 2016 – REVISED JANUARY 2017

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Product Folder Links: CSD19538Q2
6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

**TI E2E™ Online Community**  **TI's Engineer-to-Engineer (E2E) Community.** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support**  **TI's Design Support** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary

**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 Q2 Package Dimensions

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.
Q2 Package Dimensions (continued)

7.1.1 Recommended PCB Pattern

1. For recommended circuit layout for PCB designs, see *Reducing Ringing Through PCB Layout Techniques* (SLPA005).

2. This package is designed to be soldered to a thermal pad on the board. For more information, see *QFN/SON PCB Attachment* (SLUA271).
7.1.2 Recommended Stencil Pattern

1. All linear dimensions are in millimeters.
2. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7.2 Q2 Tape and Reel Information

Notes:
1. Measured from centerline of sprocket hole to centerline of pocket.
2. Cumulative tolerance of 10 sprocket holes is ±0.2.
3. Other material available.
4. Typical SR of form tape Max 10^9 OHM/SQ.
5. All dimensions are in mm, unless otherwise specified.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD19538Q2</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DQK</td>
<td>6</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 150</td>
<td>1958</td>
<td></td>
</tr>
<tr>
<td>CSD19538Q2T</td>
<td>ACTIVE</td>
<td>WSON</td>
<td>DQK</td>
<td>6</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>NIPDAU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 150</td>
<td>1958</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.
This image is a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
NOTES:  
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.  
B. This drawing is subject to change without notice.  
C. Small Outline No-Lead (SON) package configuration.  
⚠️ The package thermal pads must be soldered to the board for thermal and mechanical performance.
THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No-Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pads must be soldered to the printed circuit board for thermal and mechanical performance.
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
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