CSD75208W1015 Dual 20-V Common Source P-Channel NexFET™ Power MOSFET

1 Features
- Dual P-Channel MOSFETs
- Common Source Configuration
- Small Footprint 1 mm x 1.5 mm
- Gate-Source Voltage Clamp
- Gate ESD Protection –3 kV
- Pb Free
- RoHS Compliant
- Halogen Free

2 Applications
- Battery Management
- Load Switch
- Battery Protection

3 Description
This device is designed to deliver the lowest on-resistance and gate charge in the smallest outline possible with excellent thermal characteristics in an ultra-low profile. Low on-resistance coupled with the small footprint and low profile make the device ideal for battery operated space constrained applications.

Top View

R_D1D2(on) vs V_GS

R_DS(on) vs V_GS

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

Changes from Original (July 2014) to Revision A Page

- Changed Figure 1. ......................................................... 4
- Added Community Resources and Receiving Notification of Documentation Updates sections to Device and Documentation Support. ......................................................... 7
# 5 Specifications

## 5.1 Electrical Characteristics

$T_A = 25^\circ\text{C}$ unless otherwise stated

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<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>STATIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$BV_{DSS}$ Drain-to-Source Voltage</td>
<td>$V_{GS} = 0 \text{V}, I_{DS} = -250 \mu\text{A}$</td>
<td>$-20$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$BV_{GSS}$ Gate-to-Source Voltage</td>
<td>$V_{DS} = 0 \text{V}, I_{G} = -250 \mu\text{A}$</td>
<td></td>
<td>$-6.1$</td>
<td>$-7.2$</td>
<td>V</td>
</tr>
<tr>
<td>$I_{DSSS}$ Drain-to-Source Leakage Current</td>
<td>$V_{GS} = 0 \text{V}, V_{DS} = -16 \text{V}$</td>
<td></td>
<td></td>
<td>$-1$</td>
<td>(\mu\text{A})</td>
</tr>
<tr>
<td>$I_{GSS}$ Gate-to-Source Leakage Current</td>
<td>$V_{DS} = 0 \text{V}, V_{GS} = -6 \text{V}$</td>
<td></td>
<td></td>
<td>$-100$</td>
<td>nA</td>
</tr>
<tr>
<td>$V_{DS(th)}$ Gate-to-Source Threshold Voltage</td>
<td>$V_{DS} = V_{GS}, I_{DS} = -250 \mu\text{A}$</td>
<td>$-0.5$</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$R_{DS(on)}$ Drain-to-Source On-Resistance</td>
<td>$V_{GS} = -1.8 \text{V}, I_{D} = -1 \text{A}$</td>
<td>$100$</td>
<td></td>
<td></td>
<td>m(\Omega)</td>
</tr>
<tr>
<td></td>
<td>$V_{GS} = -2.5 \text{V}, I_{D} = -1 \text{A}$</td>
<td>$70$</td>
<td></td>
<td></td>
<td>m(\Omega)</td>
</tr>
<tr>
<td></td>
<td>$V_{GS} = -4.5 \text{V}, I_{D} = -1 \text{A}$</td>
<td>$56$</td>
<td></td>
<td></td>
<td>m(\Omega)</td>
</tr>
<tr>
<td>$R_{D1D2(on)}$ Drain-to-Drain On-Resistance</td>
<td>$V_{GS} = -1.8 \text{V}, I_{D1D2} = -1 \text{A}$</td>
<td>$190$</td>
<td></td>
<td></td>
<td>m(\Omega)</td>
</tr>
<tr>
<td></td>
<td>$V_{GS} = -2.5 \text{V}, I_{D1D2} = -1 \text{A}$</td>
<td>$120$</td>
<td></td>
<td></td>
<td>m(\Omega)</td>
</tr>
<tr>
<td></td>
<td>$V_{GS} = -4.5 \text{V}, I_{D1D2} = -1 \text{A}$</td>
<td>$90$</td>
<td></td>
<td></td>
<td>m(\Omega)</td>
</tr>
<tr>
<td>$g_f$ Transconductance</td>
<td>$V_{DS} = -2 \text{V}, I_{D} = -1 \text{A}$</td>
<td></td>
<td></td>
<td></td>
<td>S</td>
</tr>
<tr>
<td><strong>DYNAMIC CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{iss}$ Input Capacitance</td>
<td>$V_{GS} = 0 \text{V}, V_{DS} = -10 \text{V}, f = 1 \text{MHz}$</td>
<td></td>
<td>$315$</td>
<td>$410$</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{oss}$ Output Capacitance</td>
<td>$V_{DS} = 0 \text{V}, I_{DS} = -1 \text{A}$</td>
<td></td>
<td>$132$</td>
<td>$172$</td>
<td>pF</td>
</tr>
<tr>
<td>$C_{rss}$ Reverse Transfer Capacitance</td>
<td>$V_{DS} = -10 \text{V}, I_{DS} = -1 \text{A}$</td>
<td></td>
<td></td>
<td>$7.7$</td>
<td>pF</td>
</tr>
<tr>
<td>$Q_{dd}$ Gate Charge Total (–4.5 V)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gd}$ Gate Charge, Gate-to-Drain</td>
<td>$V_{DS} = -10 \text{V}, I_{DS} = -1 \text{A}$</td>
<td></td>
<td></td>
<td>$0.23$</td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{gs}$ Gate Charge, Gate-to-Source</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{g(th)}$ Gate Charge at $V_{th}$</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>nC</td>
</tr>
<tr>
<td>$Q_{oss}$ Output Charge</td>
<td>$V_{DS} = 0 \text{V}, V_{GS} = 0 \text{V}$</td>
<td></td>
<td></td>
<td>$2.1$</td>
<td>nC</td>
</tr>
<tr>
<td>$t_{(on)}$ Rise Time</td>
<td>$V_{DS} = -10 \text{V}, V_{GS} = -4.5 \text{V}, I_{DS} = -1 \text{A}, R_{G} = 0 \Omega$</td>
<td></td>
<td></td>
<td>$9$</td>
<td>ns</td>
</tr>
<tr>
<td>$t_{(off)}$ Fall Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
<tr>
<td><strong>DIODE CHARACTERISTICS</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$V_{BD}$ Diode Forward Voltage</td>
<td>$I_{DS} = -1 \text{A}, V_{GS} = 0 \text{V}$</td>
<td></td>
<td></td>
<td>$-0.75$</td>
<td>$-1$</td>
</tr>
<tr>
<td>$Q_f$ Reverse Recovery Charge</td>
<td>$V_{DD} = -10 \text{V}, I_{F} = -1 \text{A}, \text{di/dt} = 200 \text{A/\mu s}$</td>
<td></td>
<td></td>
<td>$4.3$</td>
<td>nC</td>
</tr>
<tr>
<td>$t_f$ Reverse Recovery Time</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>ns</td>
</tr>
</tbody>
</table>

## 5.2 Thermal Information

$T_A = 25^\circ\text{C}$ unless otherwise stated

<table>
<thead>
<tr>
<th>THERMAL METRIC</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{JA}$ Junction-to-Junction Temperature</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R_{JUA}$ Junction-to-Ambient Thermal Resistance</td>
<td>$165$</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
<tr>
<td>$R_{JUA}$ Junction-to-Ambient Thermal Resistance</td>
<td>$95$</td>
<td></td>
<td></td>
<td>°C/W</td>
</tr>
</tbody>
</table>

(1) Device mounted on FR4 material with minimum Cu mounting area
(2) Measured with both devices biased in a parallel condition.
(3) Device mounted on FR4 material with 1-inch\(^2\) (6.45-cm\(^2\)), 2-oz. (0.071-mm thick) Cu.
Typ $R_{	ext{JA}} = 95^\circ\text{C/W}$ when mounted on 1 inch$^2$ (6.45 cm$^2$) of 2-oz. (0.071-mm thick) Cu.

Typ $R_{	ext{JA}} = 165^\circ\text{C/W}$ when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^\circ\text{C}$ unless otherwise stated)

Figure 1. Transient Thermal Impedance
Typical MOSFET Characteristics (continued)

\((T_A = 25°C \text{ unless otherwise stated})\)

### Figure 2. Saturation Characteristics

- **Figure 3. Transfer Characteristics**

- **Figure 4. Gate Charge**

- **Figure 5. Capacitance**

- **Figure 6. Threshold Voltage vs Temperature**

- **Figure 7. On-State Drain-to-Drain Resistance vs Gate-to-Source Voltage**

\[V_{DS} = -5 \text{ V}\]

\[I_D = -1 \text{ A} \quad V_{DS} = -10 \text{ V}\]

\[V_{GS} = -4.5 \text{ V} \quad V_{GS} = -2.5 \text{ V} \quad V_{GS} = -1.8 \text{ V}\]

\[I_D = -250 \mu\text{A}\]

\[T_C = 25°C \quad T_C = 25°C \quad T_C = -55°C\]

\[C_{iss} = C_{gd} + C_{gs}\]

\[C_{oss} = C_{ds} + C_{gd}\]

\[C_{rss} = C_{gd}\]
Typical MOSFET Characteristics (continued)

\( T_A = 25^\circ C \) unless otherwise stated

**Figure 8. On-State Drain-to-Source Resistance vs Gate-to-Source Voltage**

**Figure 9. Normalized On-State Resistance vs Temperature**

**Figure 10. Typical Diode Forward Voltage**

**Figure 11. Maximum Safe Operating Area**

**Figure 12. Maximum Drain Current vs Temperature**
6 Device and Documentation Support

6.1 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

6.2 Community Resources
The following links connect to TI community resources. Linked contents are provided “AS IS” by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI’s Terms of Use.

**TI E2E™ Online Community** *TI’s Engineer-to-Engineer (E2E) Community.* Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI’s Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

6.3 Trademarks
NexFET, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

6.4 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.5 Glossary
**SLYZ022 — TI Glossary.**
This glossary lists and explains terms, acronyms, and definitions.
7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

7.1 CSD75208W1015 Package Dimensions

![Diagram of CSD75208W1015 package dimensions]

Table 1. Pinout

<table>
<thead>
<tr>
<th>POSITION</th>
<th>DESIGNATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>B1, B2</td>
<td>Source</td>
</tr>
<tr>
<td>C1</td>
<td>Gate1</td>
</tr>
<tr>
<td>C2</td>
<td>Drain1</td>
</tr>
<tr>
<td>A2</td>
<td>Gate2</td>
</tr>
<tr>
<td>A1</td>
<td>Drain2</td>
</tr>
</tbody>
</table>

NOTE: All dimensions are in mm (unless otherwise specified).
7.2 Recommended PCB Land Pattern

NOTE: All dimensions are in mm (unless otherwise specified).

7.3 Tape and Reel Information

NOTE: All dimensions are in mm (unless otherwise specified).
# PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>CSD75208W1015</td>
<td>ACTIVE</td>
<td>DSBGA</td>
<td>YZC</td>
<td>6</td>
<td>3000</td>
<td>RoHS &amp; Green</td>
<td>SNAGCU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 150</td>
<td>75208</td>
<td>Samples</td>
</tr>
<tr>
<td>CSD75208W1015T</td>
<td>ACTIVE</td>
<td>DSBGA</td>
<td>YZC</td>
<td>6</td>
<td>250</td>
<td>RoHS &amp; Green</td>
<td>SNAGCU</td>
<td>Level-1-260C-UNLIM</td>
<td>-55 to 150</td>
<td>75208</td>
<td>Samples</td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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