SBAS279D – AUGUST 2003 – REVISED JULY 2005

Dual, 12-Bit, 40MSPS Digital-to-Analog Converter

FEATURES

- **Dual, 12-Bit, 40MSPS Current Output DAC**
- **Four 12-Bit Voltage Output DACs—for Transmit Control**
- **Single +3V Operation**
- **Very Low Power: 29mW**
- **High SFDR: 75dB at f_{OUT} = 5MHz**
- **Low-Current Standby or Full Power-Down Modes**
- **Internal Reference**
- **Optional External Reference**
- **Adjustable Full-Scale Range: 0.5mA to 2mA**

APPLICATIONS

- **Transmit Channels**
  - **I and Q**
  - **PC Card Modems: GPRS, CDMA**
  - **Wireless Network Cards (NICs)**
- **Signal Synthesis (DDS)**
- **Portable Medical Instumentation**
- **Arbitrary Waveform Generation (AWG)**

DESCRIPTION

The DAC2932 is a dual 12-bit, current-output digital-to-analog converter (DAC) designed to combine the features of high dynamic range and very low power consumption. The DAC2932 converter supports update rates of up to 40MSPS. In addition, the DAC2932 features four 12-bit voltage output DACs, which can be used to perform system control functions.

The advanced segmentation architecture of the DAC2932 is optimized to provide a high spurious-free dynamic range (SFDR).

The DAC2932 has a high impedance (> 200kΩ) differential current output with a nominal range of 2mA and a compliance voltage of up to 0.8V. The differential outputs allow for either a differential or single-ended analog signal interface. The close matching of the current outputs ensures superior dynamic performance in the differential configuration, which can be implemented with a transformer. Using a small geometry CMOS process, the monolithic DAC2932 is designed to operate within a single-supply range of 2.7V to 3.3V. Low power consumption makes it ideal for portable and battery-operated systems. Further optimization by lowering the output current can be realized with the adjustable full-scale option. The full-scale output current can be adjusted over a span of 0.5mA to 2mA.

For noncontinuous operation of the DAC2932, a full power-down mode can reduce the power dissipation to as little as 25μW.

The DAC2932 is designed to operate with a single parallel data port. While it alternates the loading of the input data into separate input latches for both current output DACs (I-DACs), the updating of the analog output signal occurs simultaneously. The DAC2932 integrates a temperature compensated 1.22V bandgap reference. The DAC2932 also allows for additional flexibility of using an external reference.

The DAC2932 is available in a TQFP-48 package.

ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR(1)	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC2932	TQFP-48	PFB	–40°C to +85°C	DAC2932	DAC2932PFBT	Tape and Reel, 250
					DAC2932PFBR	Tape and Reel, 2000

(1) For the most current specification and package information, refer to our web site at www.ti.com.

ABSOLUTE MAXIMUM RATINGS

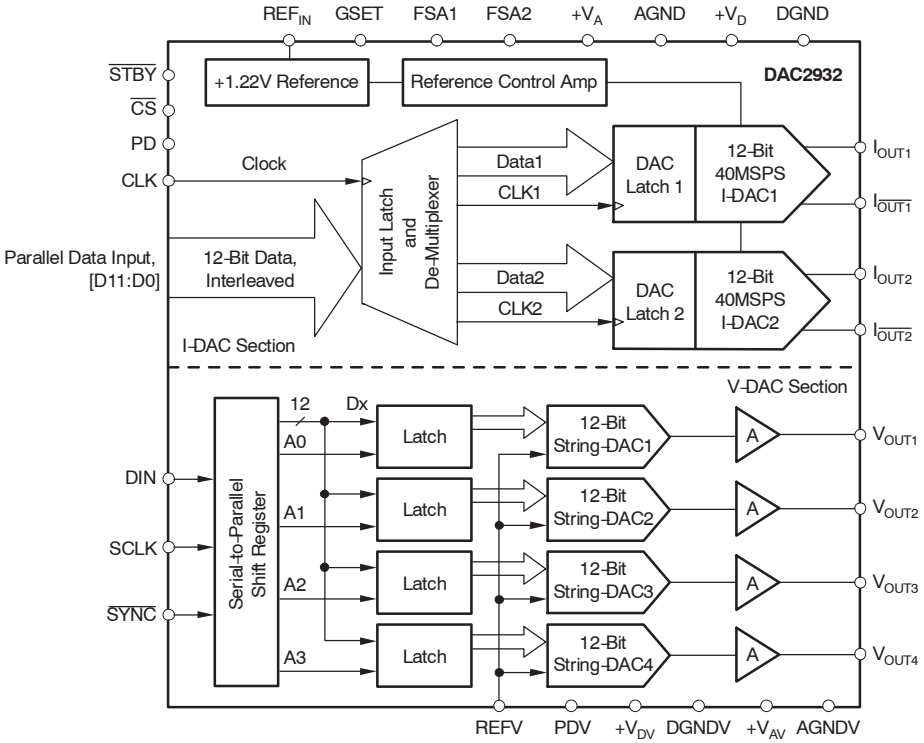
over operating free-air temperature range unless otherwise noted

	DAC2932	UNIT
$+V_A$ to AGND	–0.3 to +4	V
$+V_D$ to DGND	–0.3 to +4	V
AGND to DGND	–0.2 to +0.2	V
$+V_A$ to $+V_D$	–0.7 to +0.7	V
CLK, PD, $\overline{STBY}$, $\overline{CS}$ to DGND	–0.3 to V_D + 0.3	V
D0–D11 to DGND	–0.3 to V_D + 0.3	V
I_{OUT}, $I_{\overline{OUT}}$ to AGND	–0.5 to V_A + 0.3	V
REFV to AGNDV	–0.3 to V_{AV} + 0.3	V
GSET, REF_{IN}, FSA to AGND	–0.3 to V_A + 0.3	V
$V_{OUT}x$ to AGNDV	–0.3 to V_{AV} + 0.3	V
DIN to DGNDV	–0.3 to V_{DV} + 0.3	V
Junction temperature	+150	°C
Case temperature	+100	°C
Storage temperature range	–40 to +150	°C

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

FUNCTIONAL BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS: I-DAC

At $T_A = T_{MIN}$ to T_{MAX} (typical values are at T_A = 25°C), $+V_A$ = +3V, $+V_D$ = +3V, Update Rate = 40MSPS, I_{OUTFS} = 2mA, R_L = 250Ω, $C_L \le$ 10pF, GSET = H, and internal reference, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC2932 MIN	DAC2932 TYP	DAC2932 MAX	UNITS
Resolution			12		Bits
Output update rate (f_{CLOCK})			40		MSPS
Specified temperature range, operating	Ambient, T_A	–40		+85	°C
Static Accuracy(1)(2)					
Differential nonlinearity (DNL)		–3.5	±0.5	+3.5	LSB
Integral nonlinearity (INL)		–8	±1.5	+8	LSB
Dynamic Performance(3)					
Spurious-free dynamic range (SFDR)	To Nyquist, 0dBFS				
f_{OUT} = 0.2MHz, f_{CLOCK} = 20MSPS			68		dBc
f_{OUT} = 0.55MHz, f_{CLOCK} = 40MSPS			71		dBc
f_{OUT} = 1MHz, f_{CLOCK} = 25MSPS(4)		58	70		dBc
f_{OUT} = 2.2MHz, f_{CLOCK} = 40MSPS			72		dBc
f_{OUT} = 5MHz, f_{CLOCK} = 40MSPS			75		dBc
f_{OUT} = 10MHz, f_{CLOCK} = 40MSPS			69		dBc
f_{OUT} = 20MHz, f_{CLOCK} = 40MSPS			57		dBc
Spurious-free dynamic range within a window					
f_{OUT} = 2.2MHz, f_{CLOCK} = 40MSPS	1MHz span		76		dBc
f_{OUT} = 10MHz, f_{CLOCK} = 40MSPS	2MHz span		74		dBc
Total harmonic distortion (THD)					
f_{OUT} = 0.55MHz, f_{CLOCK} = 40MSPS			–70		dBc
f_{OUT} = 1MHz, f_{CLOCK} = 25MSPS(4)		–58	–69		dBc
f_{OUT} = 2.2MHz, f_{CLOCK} = 40MSPS			–70		dBc
Signal-to-noise and distortion (SINAD)					
f_{OUT} = 1MHz, f_{CLOCK} = 25MSPS(4)		52	61		dBc
Output settling time(1)	to 0.1%		20		ns
Output rise time(1)	10% to 90%		7.7		ns
Output fall time(1)	10% to 90%		7.4		ns
DC Accuracy					
Full-scale output range(5)(6) (FSR)	All bits high, I_{OUT1}, I_{OUT2}	0.5		2	mA
Output compliance range(7), V_{CO}		–0.5	+0.5	+0.8	V
Gain error (Full-Scale)		–2	±0.5	+2	%FSR
Gain error drift			70		ppmFSR/°C
Gain matching		–2.5	+0.6	+2.5	%FSR
Offset error			±0.001		%FSR
Power-supply rejection, $+V_A$	+3V, ±10%, at 25°C	–0.9	+0.5	+0.9	%FSR/V
Power-supply rejection, $+V_D$	+3V, ±10%, at 25°C	–0.12	+0.03	+0.12	%FSR/V
Output resistance			200		kΩ
Output capacitance	I_{OUT}, $\overline{I_{OUT}}$ to Ground		5		pF

(1) At output I_{OUT1}, I_{OUT2}, while driving a 250Ω load, transition from 000h to FFFh.
(2) Measured at f_{CLOCK} = 25MSPS and f_{OUT} = 1.0MHz.
(3) Differential, transformer (n = 4:1) coupled output, R_L = 400Ω.
(4) Differential outputs with a 250Ω load.
(5) Nominal full–scale output current is $I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}}$; with V_{REF} = 1.22V (typ) and R_{SET} = 19.6kΩ (1%)
(6) Ensured by design and characterization; not production tested.
(7) Gain error to remain ≤10% FSR over the full compliance range.
(8) Combined power dissipation of I-DAC and V-DAC.

ELECTRICAL CHARACTERISTICS: I-DAC (continued)

At T_A = T_{MIN} to T_{MAX} (typical values are at T_A = 25°C), $+V_A$ = +3V, $+V_D$ = +3V, Update Rate = 40MSPS, I_{OUTFS} = 2mA, R_L = 250Ω, C_L ≤ 10pF, GSET = H, and internal reference, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC2932 MIN	DAC2932 TYP	DAC2932 MAX	UNITS
Reference					
Voltage, V_{REF}		+1.14	+1.22	+1.26	V
Tolerance			±30		mV
Voltage drift			−40		ppm/°C
Output current			10		µA
Input resistance			1		MΩ
Input compliance range	External V_{REF}		+1.22		V
Small-signal bandwidth			0.1		MHz
Digital Inputs(6)					
Logic coding			Straight binary		
Logic high voltage, V_{IH}		+2	+3		V
Logic low voltage, V_{IL}			0	+0.8	V
Logic high current			±1		µA
Logic low current			±1		µA
Input capacitance			5		pF
Power Supply					
Analog supply voltage, $+V_A$, $+V_{AV}$		2.7	3	3.3	V
Digital supply voltage, $+V_D$, $+V_{DV}$		2.7	3	3.3	V
Analog supply current, I_{VA}	f_{CLOCK} = 25MSPS, digital inputs at 0		4.7		mA
I_{VA}	f_{CLOCK} = 40MSPS, f_{OUT} = 2.2MHz		5.4		mA
I_{VA}	Standby mode		0.4		mA
Digital supply current, I_{VD}	f_{CLOCK} = 25MSPS, digital inputs at 0		2		mA
I_{VD}	f_{CLOCK} = 40MSPS, f_{OUT} = 2.2MHz		4.3		mA
I_{VD}	Standby mode, clock off		0.02		mA
I_{VD}	Standby mode, $\overline{CS}$ = 0, f_{CLOCK} = 25MSPS		1.3		mA
Power dissipation, PD(8)	f_{CLOCK} = 25MSPS, digital inputs at 0		20	25	mW
PD	f_{CLOCK} = 40MSPS, f_{OUT} = 2.2MHz		29		mW
PD	Standby mode, f_{CLOCK} = 25MSPS		5.5	7	mW
PD	Power-down mode, clock off, digital inputs at 0		25		µW
Thermal resistance					
TQFP-48 θ_{JA}			97.5		°C/W
θ_{JC}			20		°C/W

(1) At output I_{OUT1}, I_{OUT2}, while driving a 250Ω load, transition from 000h to FFFh.
(2) Measured at f_{CLOCK} = 25MSPS and f_{OUT} = 1.0MHz.
(3) Differential, transformer (n = 4:1) coupled output, R_L = 400Ω.
(4) Differential outputs with a 250Ω load.
(5) Nominal full−scale output current is $I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}}$; with V_{REF} = 1.22V (typ) and R_{SET} = 19.6kΩ (1%)
(6) Ensured by design and characterization; not production tested.
(7) Gain error to remain ≤10% FSR over the full compliance range.
(8) Combined power dissipation of I-DAC and V-DAC.

ELECTRICAL CHARACTERISTICS: V-DAC

At $T_A = T_{MIN}$ to T_{MAX} (typical values are at $T_A = 25°C$), $+V_{AV} = +3V$, $+V_{DV} = +3V$, $R_L = 2k\Omega$ to GND, and $C_L = 40pF$, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC2932			UNITS
		MIN	TYP	MAX	
Static Performance(1)					
Resolution			12		Bits
Relative accuracy	At 25°C	–16	±8	+16	LSB
Differential nonlinearity, DNL	Tested; monotonic by design	–1	±0.2	+1	LSB
Zero code error(2)	All 0s loaded to DAC register		0.2	+0.8	%FSR
Full-scale error(2)	All 1s loaded to DAC register	–10	–3	+2	%FSR
Zero code error drift			5		µV/°C
Full-scale error drift			–15		ppmFSR/°C
Output Characteristics(3)					
Reference voltage setting, REFV		0		$+V_{AV}$	V
Output voltage settling time	1/4 scale to 3/4 scale change (400h to C00h)		3		µs
	$C_L = 470pF$		5		µs
Slew rate			1		V/µs
Capacitive load stability	$R_L = 2k\Omega$		470		pF
Code change glitch impulse	1LSB change around major carry		11		nV-s
Digital feedthrough			0.5		nV-s
DC output impedance			4		Ω
Short-circuit current			20		mA
Power-up time	Coming out of power-down mode		8		µs
Logic Inputs(3)					
Input current			±1		µA
Input low voltage, V_{IL}			0	0.8	V
Input high voltage, V_{IH}		2	3		V
Input capacitance			5		pF

(1) Linearity calculated using a reduced code range of 48 to 3976.
(2) Full-scale range (FSR) based on reference REFV = $+V_{AV}$ = +3.0V.
(3) Ensured by design and characterization; not production tested.

TIMING INFORMATION

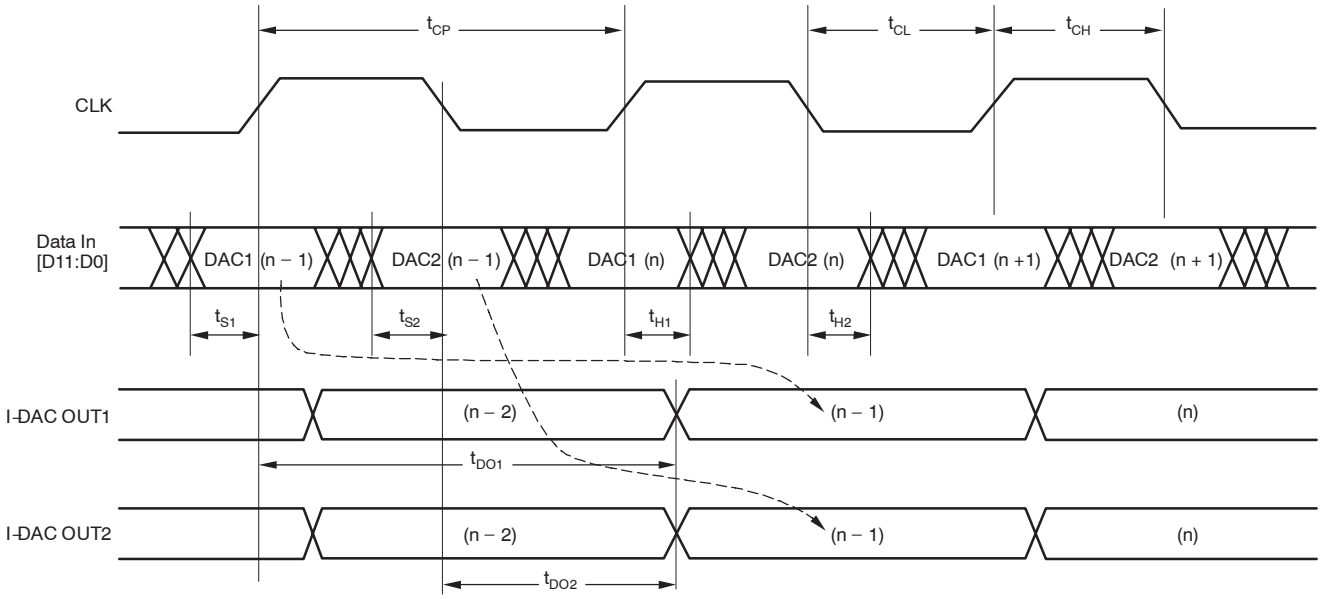


Figure 1. Timing Diagram of I-DAC

TIMING REQUIREMENTS(1,2): I-DAC

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{CP}	Clock cycle time (period)		25		ns
t_{CL}	Clock low time	10			ns
t_{CH}	Clock high time	10			ns
t_{S1}	Data setup time, I-DAC1	1	5		ns
t_{S2}	Data setup time, I-DAC2	1	5		ns
t_{H1}	Data hold time, I-DAC1	3.35	5		ns
t_{H2}	Data hold time, I-DAC2	3.35	5		ns
t_{DO1}(3)	Output delay time, I-DAC1		$t_{S1} + t_{CP}$		ns
t_{DO2}(3)	Output delay time, I-DAC2		$t_{S2}+(t_{CP}/2)$		ns
	$\overline{CS}$ hold time (pulse width)	2.49			ns
	$\overline{CS}$ to clock rising or falling edge setup time		0.52		ns
	$\overline{STBY}$ rise time to I_{OUT}		17		µs
	PD fall time to I_{OUT} (I-DAC coming out of power-down mode)		22		µs

(1) Based on design simulation and characterization; not production tested.
(2) All input signals are specified with $t_r = t_f \leq 2$ns (10% to 90% of $+V_{DV}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(3) Output delay time measured from 50% of rising clock edge to 50% point of full-scale transition.

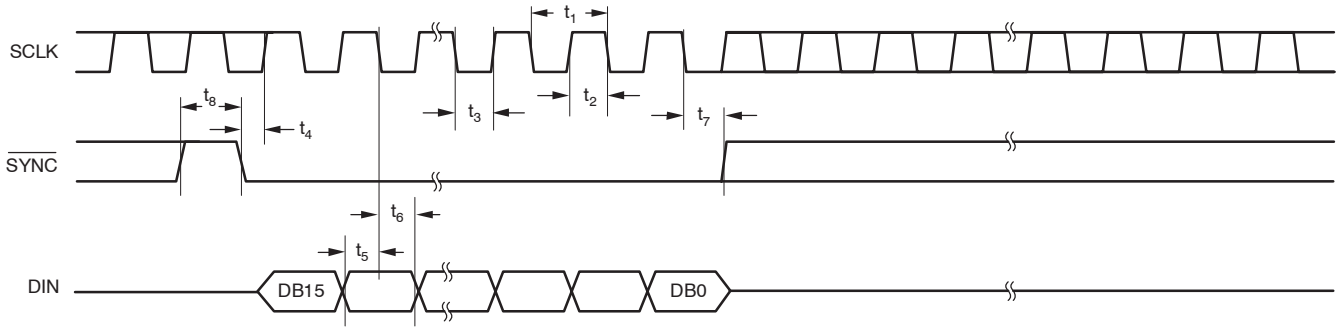


Figure 2. Serial Write Operation of V-DAC

TIMING REQUIREMENTS(1,2): V-DAC

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
t_1(3)	SCLK cycle time	50			ns
t_2	SCLK high time	13			ns
t_3	SCLK low time	22.5			ns
t_4	$\overline{\text{SYNC}}$ to SCLK rising edge setup time	0			ns
t_5	Data setup time	5	7.5		ns
t_6	Data hold time	1.5	2.5		ns
t_7	SCLK falling edge to $\overline{\text{SYNC}}$ rising edge	0	–6.0		ns
t_8	Minimum $\overline{\text{SYNC}}$ high time	50			ns
	PDV fall time to V_{OUT} (V-DAC coming out of power-down mode)		8		µs

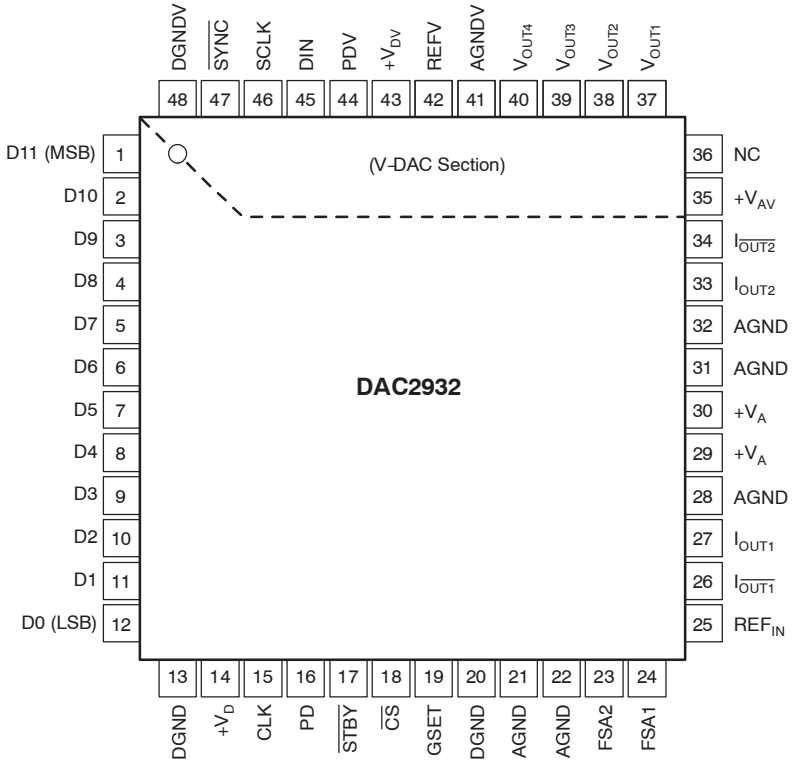
(1) All input signals are specified with $t_r = t_f \leq 2$ns (10% to 90% of $+V_{DV}$) and timed from a voltage level of $(V_{IL} + V_{IH})/2$.
(2) Based on design simulation and characterization; not production tested.
(3) Maximum SCLK frequency is 20MHz at $+V_{AV} = +V_{DV} = +2.7$V to 3.3V.

V–DAC: SERIAL DATA INPUT FORMAT

DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
A0 DAC1	**A1** DAC2	**A2** DAC3	**A3** DAC4	**D11** (MSB)	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0** (LSB)
Address Bits				12-Bit Data Word											

NOTE: A logic high in the address bit will select the corresponding V-DAC and write the data word into its register. If more than one address bit is set high, the selected V-DACs are updated with the same data word simultaneously.

PIN ASSIGNMENTS



Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
D11:D0	1:12	I	Parallel data input port for the dual I-DACs; MSB = D11, LSB = D0; interleaved operation.
DGND	13		Digital ground of I-DAC
$+V_D$	14		Digital supply of I-DAC; 2.7V to 3.3V
CLK	15	I	Clock input of I-DAC
PD	16	I	Power-down pin; active high; a logic high initiates power-down mode.
$\overline{STBY}$	17	I	Standby pin of I-DAC; active low; a logic low initiates Standby mode with PD = Low. A logic high configures the I-DAC for normal operation; pin will resume a high state if left open.
$\overline{CS}$	18	I	Chip select; active low; enables the parallel data port of the I–DACs; if used as chip select in applications using multiple DAC2932 devices, the parallel port data must be scrambled for proper functionality. Pin will resume a low state if left open.
GSET	19	I	Gain-setting mode. A logic high enables the use of two separate full-scale adjust resistors on pins FSA1 and FSA2. A logic low allows the use of a common full-scale adjust resistor connected to FSA1. The function of the FSA2 pin is disabled, and any remaining resistor has no effect. The value for the R_{SET} resistor remains the same for a given full-scale range, regardless of the selected GSET mode. Pin will resume a low state if left open.
DGND	20		Digital ground of I-DAC
AGND	21		Analog ground of I-DAC
AGND	22		Analog ground of I-DAC
FSA2	23	I	Full-scale adjust of I-DAC2; connect external gain setting resistor R_{SET2} = 19.6kΩ.
FSA1	24	I	Full-scale adjust of I-DAC1; connect external gain setting resistor R_{SET1} = 19.6kΩ.

Terminal Functions (continued)

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
REF_{IN}	25	I	External reference voltage input; internal reference voltage output; bypass with 0.1μF to AGND for internal reference operation.
$I_{\overline{OUT1}}$	26	O	Complementary current ouput of I-DAC1
I_{OUT1}	27	O	Current output of I-DAC1
AGND	28		Analog ground of I-DAC
$+V_A$	29		Analog supply of I-DAC; 2.7V to 3.3V
$+V_A$	30		Analog supply of I-DAC; 2.7V to 3.3V
AGND	31		Analog ground of I-DAC
AGND	32		Analog ground of I-DAC
I_{OUT2}	33	O	Current output of I-DAC2
$I_{\overline{OUT2}}$	34	O	Complementary current ouput of I-DAC2
$+V_{AV}$	35		Analog supply of V-DAC; 2.7V to 3.3V
NC	36		No internal connection
V_{OUT1}	37	O	Voltage output of V-DAC1
V_{OUT2}	38	O	Voltage output of V-DAC2
V_{OUT3}	39	O	Voltage output of V-DAC3
V_{OUT4}	40	O	Voltage output of V-DAC4
AGNDV	41		Analog ground of V-DAC
REFV	42	I	Reference voltage input for V-DACs; typically connected to supply ($+V_{AV}$)
$+V_{DV}$	43		Digital supply of V-DAC; 2.7V to 3.3V
PDV	44	I	Power-down of V-DACs; active high; a logic high initiates the power-down mode
DIN	45	I	Serial digital input for V–DAC; see timing and application sections for details
SCLK	46	I	Clock input of V-DAC
$\overline{SYNC}$	47	I	Frame synchronization signal for the serial data at DIN. Refer to timing section for details.
DGNDV	48		Digital ground of V-DAC.

TYPICAL CHARACTERISTICS

T_A = +25°C, $+V_A$ = $+V_{AV}$ = +3V, $+V_D$ = $+V_{DV}$ = +3V, I_{OUTFS} = 2mA, differential transformer-coupled output (n = 4:1), R_L = 400Ω on I-DAC, R_L = 2kΩ on V-DAC, and GSET = H unless otherwise noted.

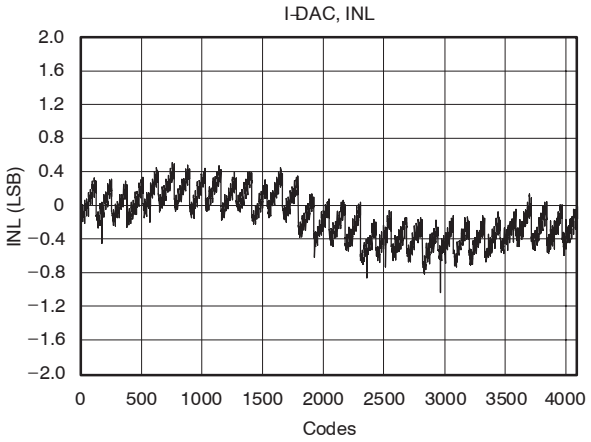


Figure 3

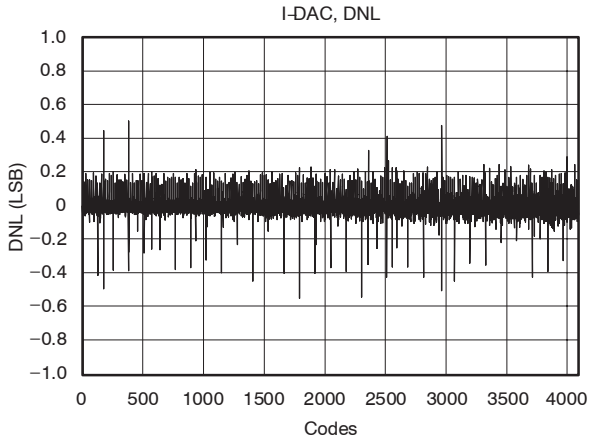


Figure 4

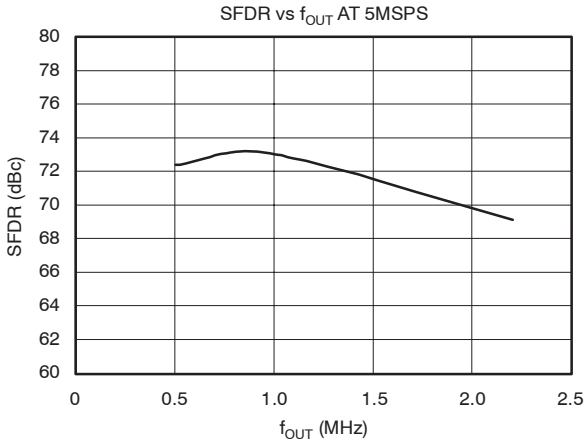


Figure 5

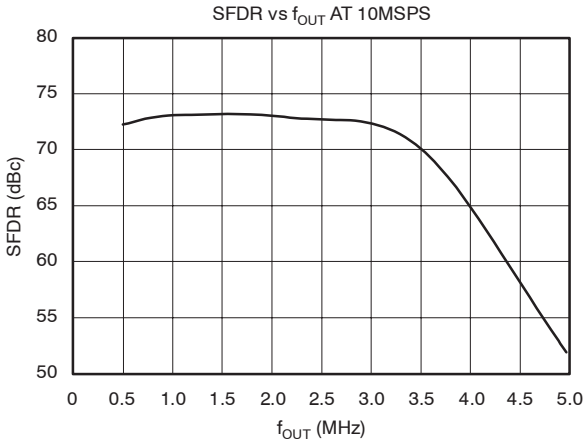


Figure 6

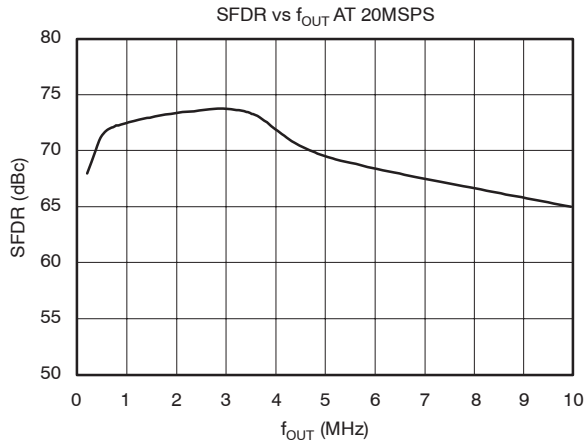


Figure 7

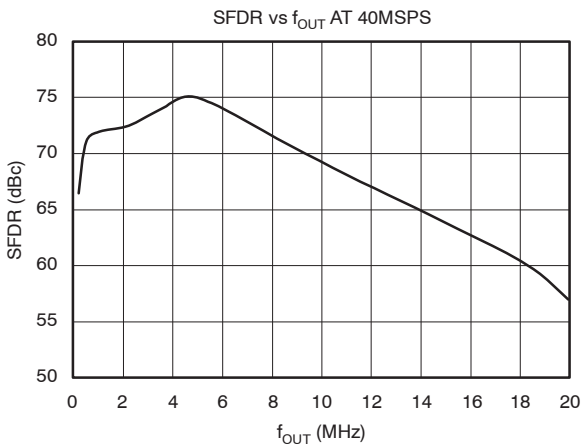


Figure 8

TYPICAL CHARACTERISTICS (continued)

T_A = +25°C, $+V_A$ = $+V_{AV}$ = +3V, $+V_D$ = $+V_{DV}$ = +3V, I_{OUTFS} = 2mA, differential transformer-coupled output (n = 4:1), R_L = 400Ω on I-DAC, R_L = 2kΩ on V-DAC, and GSET = H unless otherwise noted.

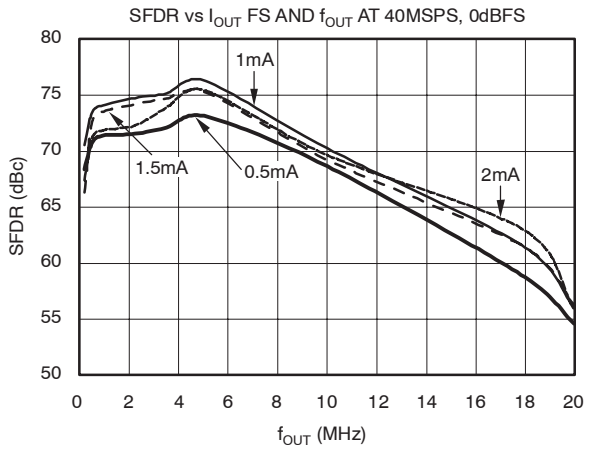


Figure 9

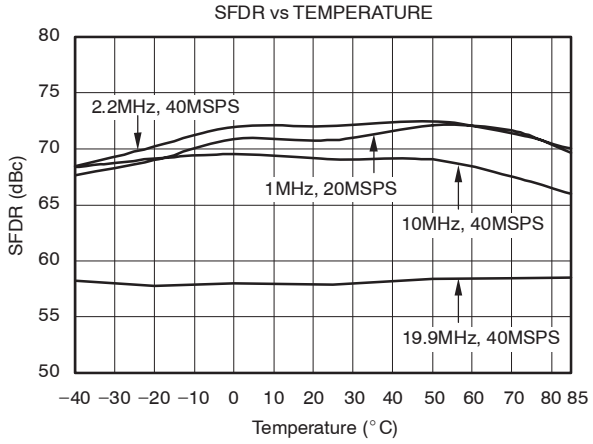


Figure 10

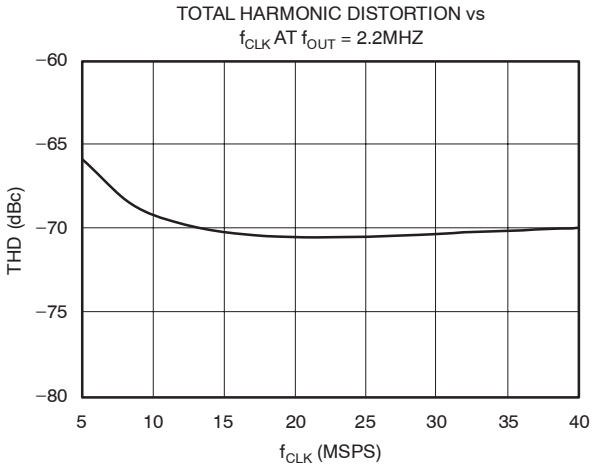


Figure 11

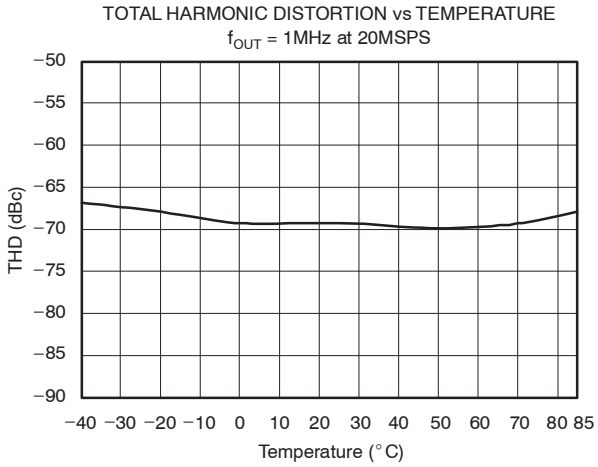


Figure 12

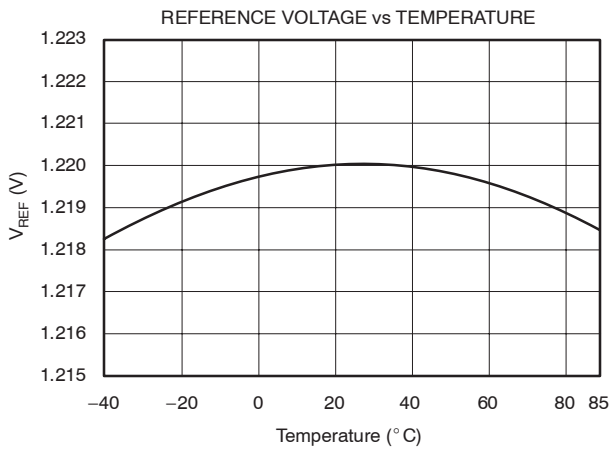


Figure 13

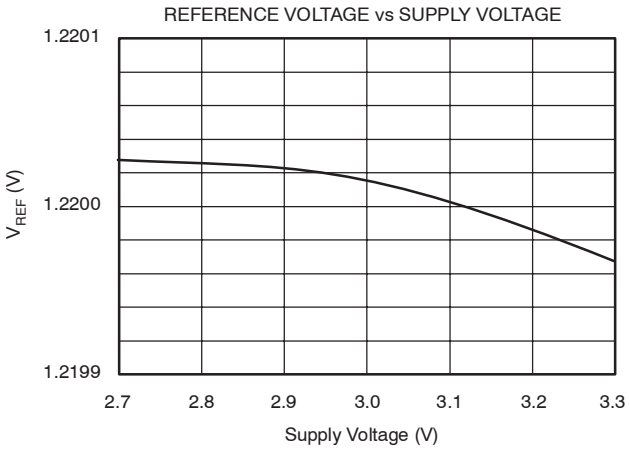


Figure 14

TYPICAL CHARACTERISTICS (continued)

T_A = +25°C, $+V_A$ = $+V_{AV}$ = +3V, $+V_D$ = $+V_{DV}$ = +3V, I_{OUTFS} = 2mA, differential transformer-coupled output (n = 4:1), R_L = 400Ω on I-DAC, R_L = 2kΩ on V-DAC, and GSET = H unless otherwise noted.

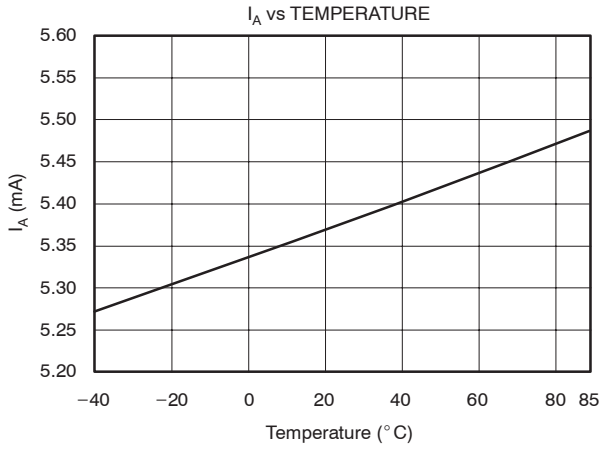


Figure 15

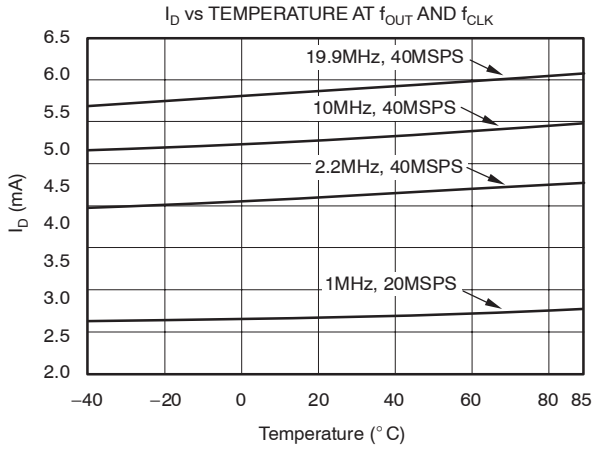


Figure 16

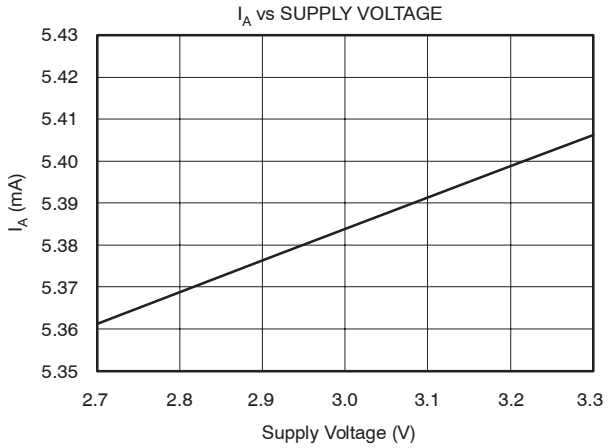


Figure 17

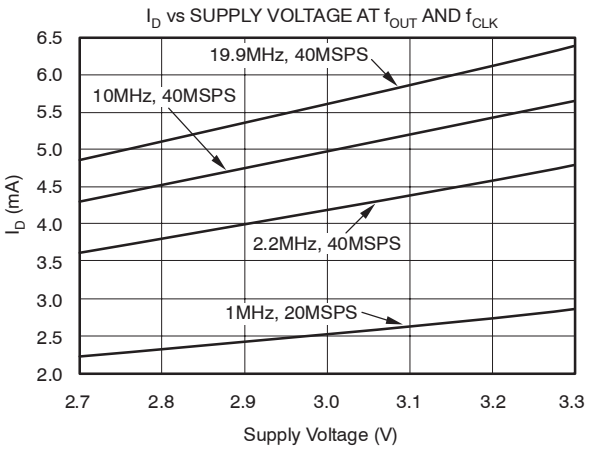


Figure 18

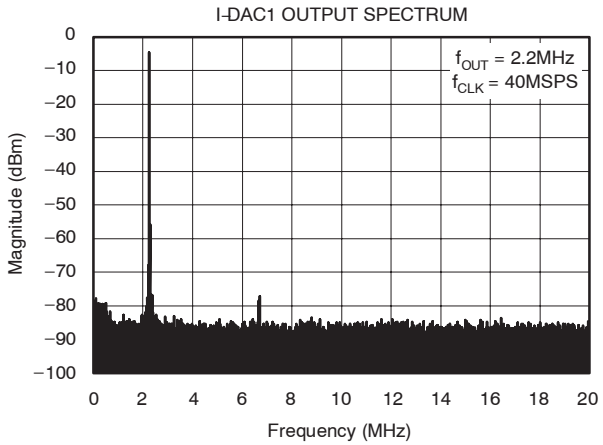


Figure 19

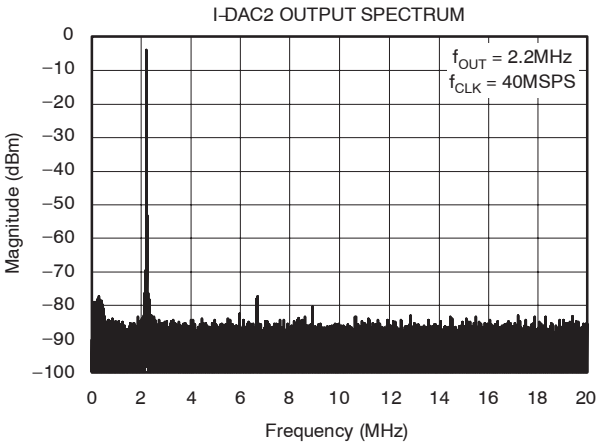


Figure 20

TYPICAL CHARACTERISTICS (continued)

T_A = +25°C, $+V_A$ = $+V_{AV}$ = +3V, $+V_D$ = $+V_{DV}$ = +3V, I_{OUTFS} = 2mA, differential transformer-coupled output (n = 4:1), R_L = 400Ω on I-DAC, R_L = 2kΩ on V-DAC, and GSET = H unless otherwise noted.

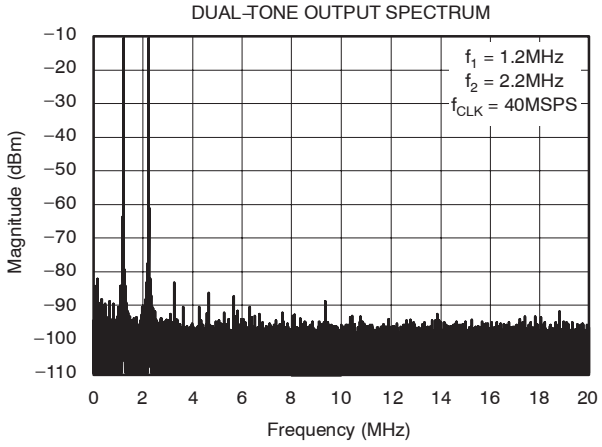


Figure 21

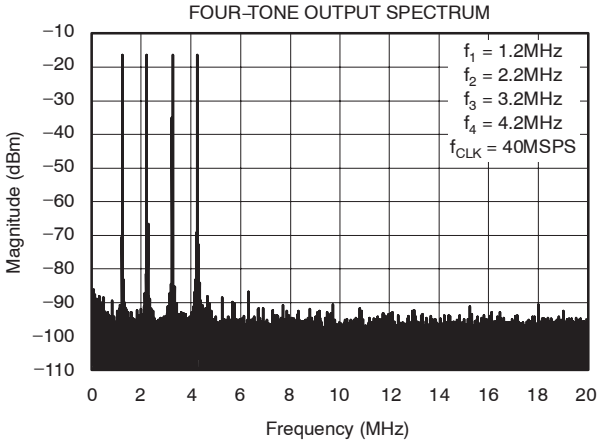


Figure 22

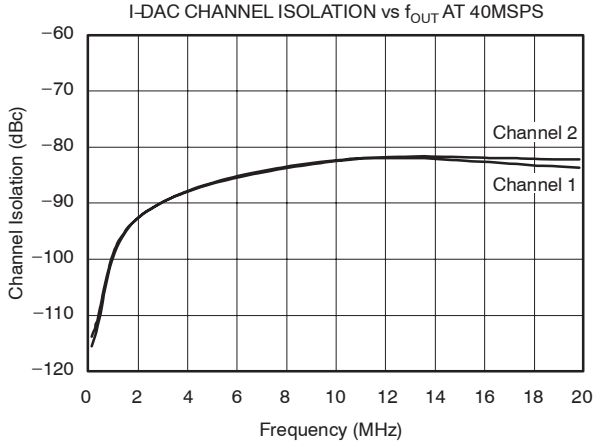


Figure 23

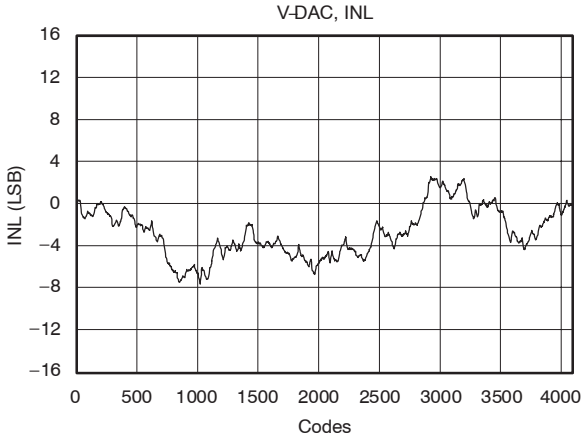


Figure 24

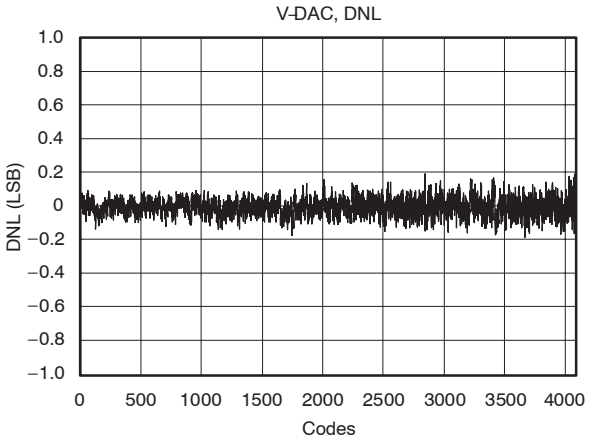


Figure 25

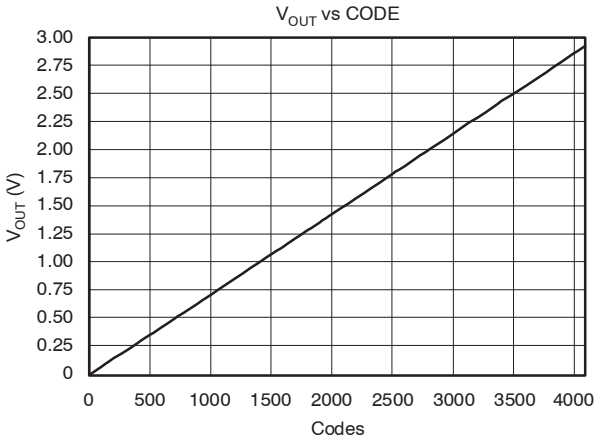


Figure 26

APPLICATION INFORMATION

THEORY OF OPERATION

The architecture of the DAC2932 uses the current steering technique to enable fast switching and a high update rate. The core element within the monolithic DAC is an array of segmented current sources that are designed to deliver a full-scale output current of up to 2mA, as shown in Figure 27. An internal decoder addresses the differential current switches each time the DAC is updated and a corresponding output current is formed by steering all currents to either output summing node, I_{OUT} or $I_{\overline{OUT}}$. The complementary outputs deliver a differential output signal, which improves the dynamic performance through reduction of even-order harmonics and common-mode signals (noise), and doubles the peak-to-peak output signal swing by a factor of two, compared to single-ended operation.

The segmented architecture results in a significant reduction of the glitch energy, and improves the dynamic performance (SFDR) and DNL. The current outputs maintain a very high output impedance of greater than 200kΩ.

The full-scale output current is determined by the ratio of the internal reference voltage (approximately +1.2V) and an external resistor, R_{SET}. The resulting I_{REF} is internally multiplied by a factor of 32 to produce an effective DAC output current that can range from 0.5mA to 2mA, depending on the value of R_{SET}.

The DAC2932 is split into a digital and an analog portion, each of which is powered through its own supply pin. The digital section includes edge-triggered input latches and the decoder logic, while the analog section comprises the current source array with its associated switches, and the reference circuitry.

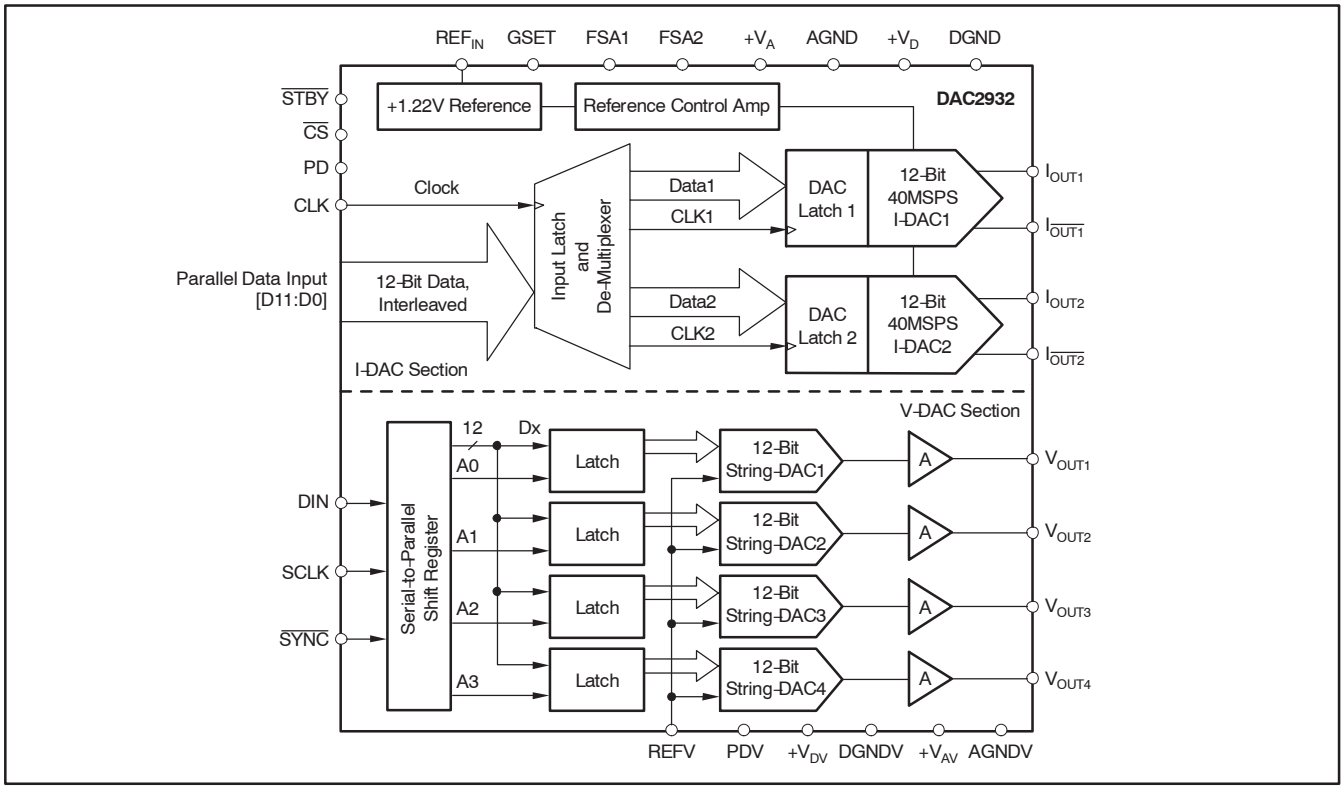


Figure 27. Block Diagram of the DAC2932

DAC TRANSFER FUNCTION

Each of the I-DACs in the DAC2932 has a complementary current output, I_{OUT1} and I_{OUT2}. The full-scale output current, I_{OUTFS}, is the summation of the two complementary output currents:

$$I_{OUTFS} = I_{OUT} + I_{\overline{OUT}} \quad (1)$$

The individual output currents depend on the DAC code and can be expressed as:

$$I_{OUT} = I_{OUTFS} \times (Code/4096) \quad (2)$$

$$I_{\overline{OUT}} = I_{OUTFS} \times (4095 - Code)/4096 \quad (3)$$

where Code is the decimal representation of the DAC data input word (0 to 4095).

Additionally, I_{OUTFS} is a function of the reference current I_{REF}, which is determined by the reference voltage and the external setting resistor, R_{SET}.

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (4)$$

In most cases, the complementary outputs will drive resistive loads or a terminated transformer. A signal voltage will develop at each output according to:

$$V_{OUT} = I_{OUT} \times R_{LOAD} \quad (5)$$

$$V_{\overline{OUT}} = I_{\overline{OUT}} \times R_{LOAD} \quad (6)$$

The value of the load resistance is limited by the output compliance specification of the DAC2932. To maintain optimum linearity performance, the compliance voltage at I_{OUT} and $I_{\overline{OUT}}$ should be limited to +0.5V or less.

The two single-ended output voltages can be combined to find the total differential output swing:

$$V_{OUTDIFF} = V_{OUT} - V_{\overline{OUT}} = \frac{(2 \times Code - 4095)}{4096} \times I_{OUTFS} \times R_{LOAD} \quad (7)$$

POWER-DOWN MODES

The DAC2932 has several modes of operation. Besides normal operation, the I-DAC section features a Standby mode and a full power-down mode, while the V-DAC section has one power-down mode. All modes are controlled by appropriate logic levels on the assigned pins of the DAC2932. Table 1 lists all pins and possible modes. The pins have internal pull-ups or pull-downs; if left open, all pins will resume logic levels that place the I-DAC and V-DAC in a normal operating mode (fully functional).

When in Standby mode the analog functions of the I-DAC section are powered down. The internal logic is still active and will consume some power if the clock remains applied. To further reduce the power in Standby mode the $\overline{CS}$ pin may be pulled high, which disables the internal logic from being clocked, even with the clock signal applied.

If $\overline{CS}$ remains low during the Standby mode and a running clock remains applied, any new data on the parallel data port will be latched into the DAC. The analog output, however, will not be updated as long as the I-DACs remain in Standby mode.

Table 1. Power-Down Modes

PD (16)	$\overline{STBY}$(17)	$\overline{CS}$ (18)	PDV (44)	DAC	MODE	DAC OUTPUTS
0	0	0	X	I-DAC enabled	Standby; data can still be written into the DACs with running clock applied	High-Z
0	0	1	X	I-DAC disabled	Standby; writing into DAC disabled—clock input disabled by $\overline{CS}$	High-Z
0	1	0	X	I-DAC enabled	Normal operation (return from Standby)	Last state prior to Standby
0	1	1	X	I-DAC disabled	Data input and clock input disabled; use when multiple devices on one bus	Last data held
1	X	X	X	I-DAC disabled	Full power-down; $\overline{STBY}$ and $\overline{CS}$ have no effect	High-Z
0	X	X	0	V-DAC enabled	V-DAC normal operation	
X	X	X	1	V-DAC disabled	V-DAC in power-down mode; independent operation of any I-DAC power-down configuration	All outputs; High-Z

NOTE: X = don't care.

CHIP SELECT OPERATION

The I–DAC clock is controlled by PD and $\overline{CS}$ through a digital clock interface that generates an internal clock which controls the data latches. Under normal operation PD and $\overline{CS}$ are kept low and the internal clock is just a delayed version of the clock signal present at the CLK pin. The data for channel 1 and channel 2 are latched by the rising and falling edges of CLK, respectively. The rising edge of CLK also causes the DAC to output the previously latched data pair.

The $\overline{CS}$ pin can be used to synchronize the latching of data from a single data bus connected to multiple DAC2932 devices, however in order for this operation to work correctly the data pairs on the bus have to be scrambled so that they are arranged correctly at the DAC outputs. The reason for this is explained in the following:

Figure 28 shows a timing diagram of the $\overline{CS}$ operation. When the $\overline{CS}$ pin is pulled high, the data in the parallel input port is not latched. The high condition on the $\overline{CS}$ pin is latched into the clock interface on the first rising edge of CLK following the $\overline{CS}$ edge; this holds the internal clock in a high condition, ignoring the CLK edges and thus not latching the bus data. In order to enable data latching, the $\overline{CS}$ pin must be returned to a low state. The change of state in $\overline{CS}$ is latched into the clock interface on the first rising CLK edge; this enables the internal clock which causes the data in channel 2 to be latched on the first falling edge of CLK. The next rising edge of CLK causes the DAC to output the old data from channel 1 and the new data just latched into channel 2 as well as to latch the new data into channel 1.

The operation previously described causes problems in those situations that have two or more DAC2932 devices sharing the same data bus with each DAC2932 reading every nth data pair. The (channel1, channel2) data pairs appearing at the DAC output correspond to (channel1 from the previous read cycle, channel2 data from the current read cycle) pairs. In order for the data bus pairs to be output correctly it is necessary to scramble the (channel1, channel2) data pairs so that the bus data corresponds to . . ., channel1, data for other DACs, channel2, . . . for each DAC2932.

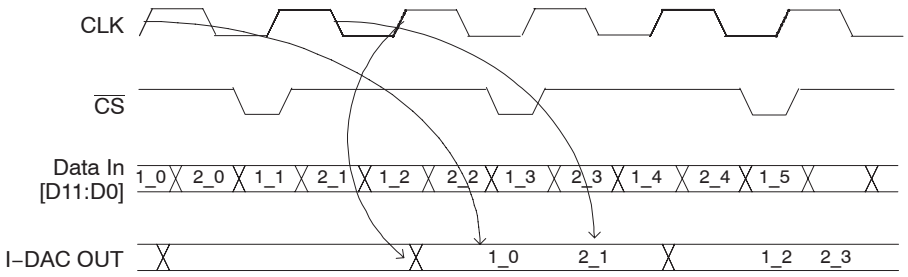


Figure 28. Timing Diagram of the $\overline{CS}$ Pin

ANALOG OUTPUTS

The DAC2932 provides two sets of complementary current outputs, I_{OUT} and $I_{\overline{OUT}}$. The simplified circuit of the analog output stage representing the differential topology is shown in Figure 29. The output impedance of I_{OUT} and $I_{\overline{OUT}}$ results from the parallel combination of the differential switches, along with the current sources and associated parasitic capacitances.

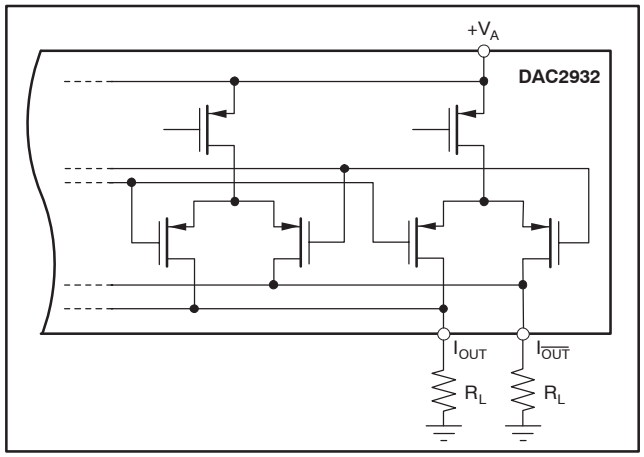


Figure 29. Equivalent Analog Output

The signal voltage swing that develops at the two outputs, I_{OUT} and $I_{\overline{OUT}}$, is limited by a negative and positive compliance. The negative limit of –0.5V is given by the breakdown voltage of the CMOS process, and exceeding it will compromise the reliability of the DAC2932, or even cause permanent damage. With the full-scale output set to 2mA, the positive compliance equals 0.8V, operating with an analog supply of $+V_A$ = 3V. To avoid degradation of the distortion performance and integral linearity, care must be taken so that the configuration of the DAC2932 does not exceed the compliance range.

Best distortion performance is typically achieved with the maximum full-scale output signal limited to approximately $0.5V_{PP}$. This is the case for a 250Ω load and a 2mA full-scale output current. A variety of loads can be adapted to the output of the DAC2932 by selecting a suitable transformer while maintaining optimum voltage levels at I_{OUT} and $I_{\overline{OUT}}$. Furthermore, using the differential output configuration in combination with a transformer is instrumental in achieving excellent distortion performance. Common-mode errors, such as even-order harmonics or noise, can be substantially reduced. This is particularly the case with high output frequencies.

For those applications requiring the optimum distortion and noise performance, it is recommended to select a full-scale output of 2mA. A lower full-scale range down to 0.5mA may be considered for applications that require low power consumption, but can tolerate a slightly reduced performance level.

The current-output DACs of the DAC2932 have a straight offset binary coding format. With all bits high, the full-scale output current (for example, 2mA) will be sourced at pins I_{OUT1} and I_{OUT2}, as shown in Table 2.

Table 2. Input Coding vs Analog Output Current

INPUT CODE (D11–D0)	I_{OUT} (mA)	$I_{\overline{OUT}}$ (mA)
1111 1111 1111	2	0
1000 0000 0000	1	1
0000 0000 0000	0	2

OUTPUT CONFIGURATIONS

As mentioned previously, utilizing the differential outputs of the converter yields the best dynamic performance. Such a differential output circuit may consist of an RF transformer or a differential amplifier configuration. The transformer configuration is ideal for most applications with ac coupling, while op amps are suitable for a dc-coupled configuration.

The single-ended configuration may be considered for applications requiring a unipolar output voltage. Connecting a resistor from either one of the outputs to ground converts the output current into a ground-referenced voltage signal. To improve on the dc linearity by maintaining a virtual ground, an I-to-V or op-amp configuration may be considered.

DIFFERENTIAL WITH TRANSFORMER

Using an RF transformer provides a convenient way of converting the differential output signal into a single-ended signal while achieving excellent dynamic performance (see Figure 3). The appropriate transformer should be carefully selected based on the output frequency spectrum and impedance requirements. The differential transformer configuration has the benefit of significantly reducing common-mode signals, thus improving the dynamic performance over a wide range of frequencies. Furthermore, by selecting a suitable impedance ratio (winding ratio), the transformer can be used to provide optimum impedance matching while controlling the compliance voltage for the converter outputs. The model shown, ADT16-6T (by Mini-Circuits), has a 16:1 ratio and may be used to interface the DAC2932 to a 50Ω load. This results in a 200Ω load for each of the outputs, I_{OUT} and $I_{\overline{OUT}}$. The output signals are ac coupled and inherently isolated by the transformer.

As shown in Figure 30, the transformer center tap is connected to ground. This forces the voltage swing on I_{OUT} and $I_{\overline{OUT}}$ to be centered at 0V. In this case the two resistors, R_L, may be replaced with one, R_{DIFF}, or omitted altogether. Alternatively, if the center tap is not connected, the signal swing will be centered at $R_L \times I_{OUTFS}/2$. However, in this case, the two resistors (R_L) must be used to enable the necessary dc-current flow for both outputs.

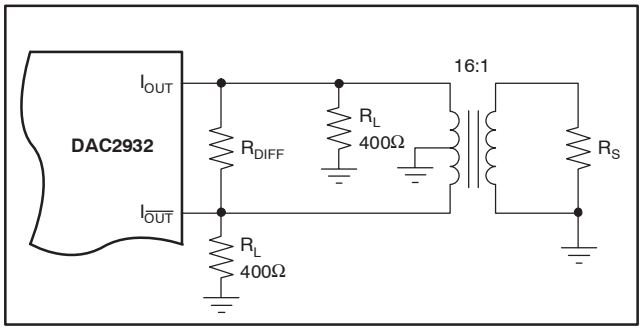


Figure 30. Differential Output Configuration Using an RF Transformer

DIFFERENTIAL CONFIGURATION USING AN OP AMP

If the application requires a dc–coupled output, a difference amplifier may be considered, as shown in Figure 31. Four external resistors are needed to configure the OPA690 voltage-feedback op amp as a difference amplifier performing the differential to single-ended conversion. Under the configuration shown, the DAC2932 generates a differential output signal of $0.5V_{PP}$ at the load resistors, R_L.

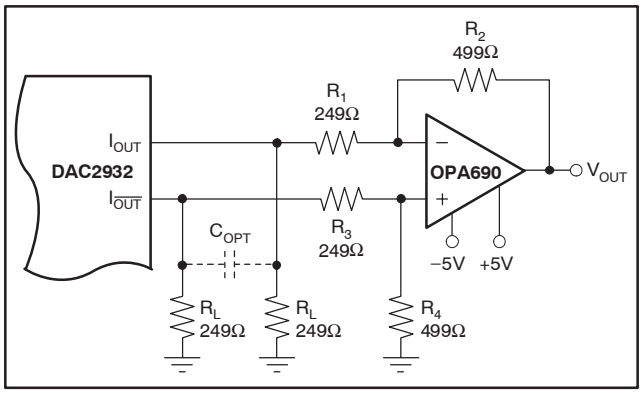


Figure 31. Difference Amplifier Provides Differential-to-Single-Ended Conversion and DC-Coupling

The OPA690 is configured for a gain of two. Therefore, operating the DAC2932 with a 2mA full-scale output produces a voltage output of ±1V. This requires the amplifier to operate from a dual power supply (±5V). The tolerance of the resistors typically sets the limit for the achievable common-mode rejection. An improvement can be obtained by fine tuning resistor R_4.

This configuration typically delivers a lower level of ac performance than the previously discussed transformer solution because the amplifier introduces another source of distortion. Suitable amplifiers should be selected based on their slew-rate, harmonic distortion, and output swing capabilities. A high-speed amplifier like the OPA690 may be considered. The ac performance of this circuit can be improved by adding a small capacitor (C_{DIFF}) between the outputs I_{OUT} and $I_{\overline{OUT}}$, as shown in Figure 31. This will introduce a real pole to create a low-pass filter in order to slew-limit the fast output signal steps of the DAC, which otherwise could drive the amplifier into slew-limitations or into an overload condition; both would cause excessive distortion. The difference amplifier can easily be modified to add a level shift for applications requiring the single-ended output voltage to be unipolar (that is, swing between 0V and +2V).

DUAL TRANSIMPEDANCE OUTPUT CONFIGURATION

The circuit example of Figure 32 shows the signal output currents connected into the summing junctions of the OPA2690 dual voltage-feedback op amp, which is set up as a transimpedance stage or I-to-V converter. With this circuit, the DAC output will be kept at a virtual ground, minimizing the effects of output impedance variations, which results in the best dc linearity (INL). As mentioned previously, care should be taken not to drive the amplifier into slew-rate limitations and produce unwanted distortion.

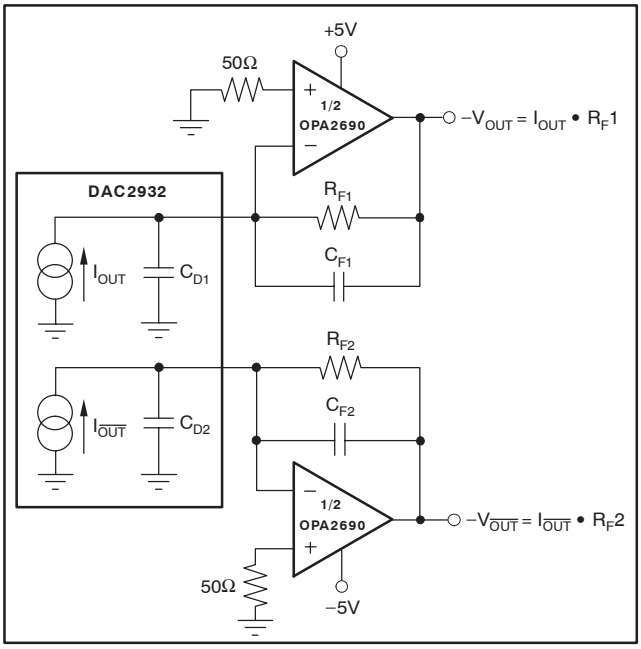


Figure 32. The OPA2690 Dual, Voltage-Feedback Amplifier Forms a Transimpedance Amplifier

The DC gain for this circuit is equal to feedback resistor R_F. At high frequencies, the DAC output impedance (C_{D1}, C_{D2}) produces a zero in the noise gain for the OPA2690 that can cause peaking in the closed-loop frequency response. C_F is added across R_F to compensate for this noise gain peaking. To achieve a flat transimpedance frequency response, the pole in each feedback network should be set to:

$$\frac{1}{2\pi R_F C_F} = \frac{\sqrt{GBP}}{4\pi R_F C_F} \quad (8)$$

where GBP = gain bandwidth product of the op amp, which gives a corner frequency f_{-3dB} of approximately:

$$f_{-3dB} = \frac{\sqrt{GBP}}{2\pi R_F C_D} \quad (9)$$

The full-scale output voltage is simply defined by the product of $I_{OUTFS} \bullet R_F$, and has a negative unipolar excursion. To improve on the ac performance of this circuit, adjustment of R_F and/or I_{OUTFS} should be considered. Further extensions of this application example may include adding a differential filter at the OPA2690 output followed by a transformer, in order to convert to a single-ended signal.

SINGLE-ENDED CONFIGURATION

Using a single load resistor connected to one of the DAC outputs, a simple current-to-voltage conversion can be accomplished. The circuit in Figure 33 shows a 250Ω resistor connected to I_{OUT}. Therefore, with a nominal output current of 2mA, the DAC produces a total signal swing of 0V to 0.5V.

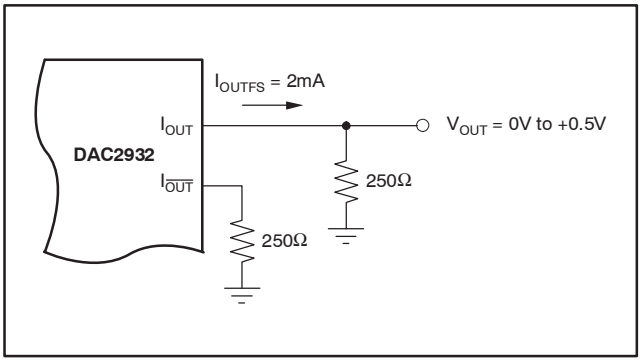


Figure 33. Differential Output Configuration Using an RF Transformer

Different load resistor values may be selected, as long as the output compliance range is not exceeded. Additionally, the output current (I_{OUTFS}) and the load resistor can be mutually adjusted to provide the desired output signal swing and performance.

INTERFACING ANALOG QUADRATURE MODULATORS

One of the main applications for the dual-channel DAC is baseband I- and Q-channel transmission for digital communications. In this application, the DAC is followed by an analog quadrature modulator, modulating an IF carrier with the baseband data, as shown in Figure 34. Often, the input stages of these quadrate modulators consist of npn-type transistors that require a dc bias (base) voltage of > 0.8V.

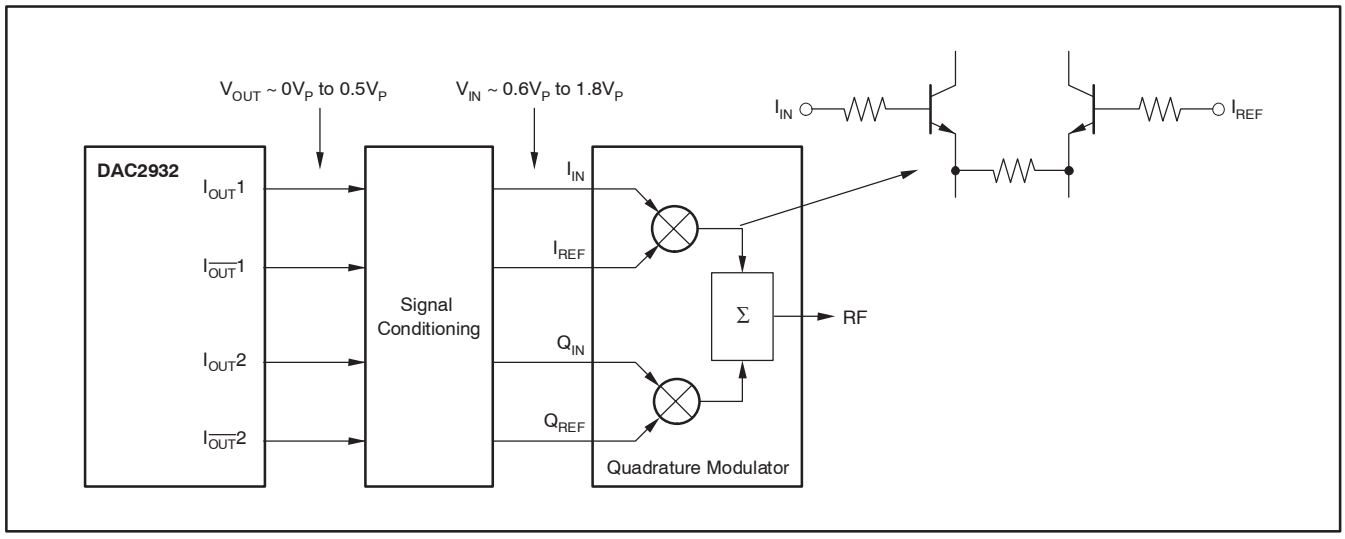


Figure 34. Generic Interface to a Quadrature Modulator. Signal conditioning (level shifting) may be required to ensure correct dc common-mode levels at the input of the quadrature modulator.

Figure 35 shows an example of a dc-coupled interface with dc level-shifting, using a precision resistor network. An ac-coupled interface, as shown in Figure 36, has the advantage in that the common-mode levels at the input of the modulator can be set independently of those at the output of the DAC. Furthermore, no voltage loss occurs in this setup.

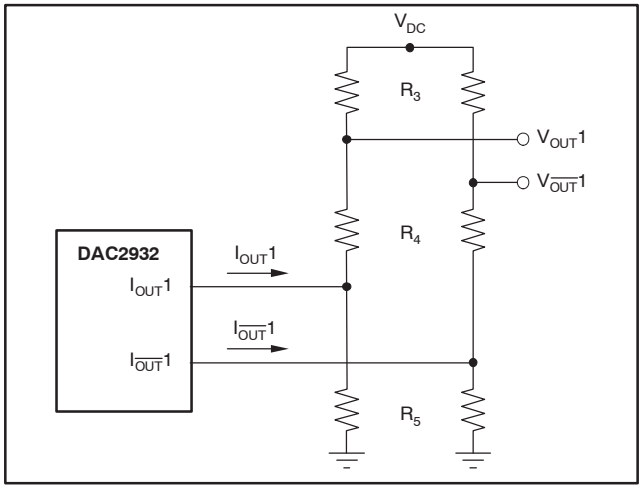


Figure 35. DC-Coupled Interface to a Quadrature Modulator Applying Level Shifting

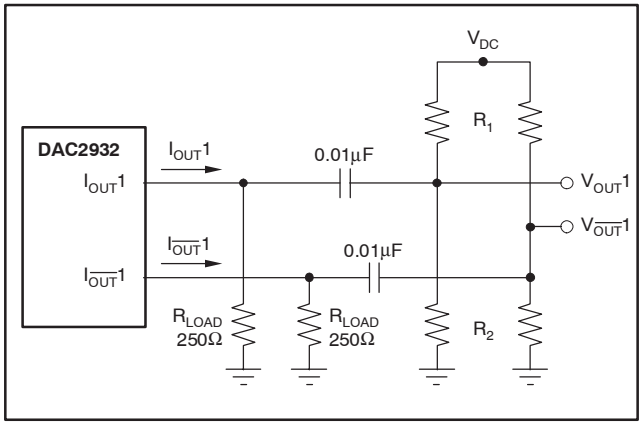


Figure 36. AC-Coupled Interface to a Quadrature Modulator Applying Level Shifting

INTERNAL REFERENCE OPERATION

The DAC2932 has an on-chip reference circuit that comprises a 1.22V bandgap reference and two control amplifiers, one for each DAC. The full-scale output current, I_{OUTFS}, of the DAC2932 is determined by the reference voltage, V_{REF}, and the value of resistor R_{SET}. I_{OUTFS} can be calculated by:

$$I_{OUTFS} = 32 \times I_{REF} = 32 \times \frac{V_{REF}}{R_{SET}} \quad (10)$$

The external resistor R_{SET} connects to the FSA pin (full-scale adjust) as shown in Figure 37. The reference control amplifier operates as a V-to-I converter producing a reference current, I_{REF}, which is determined by the ratio of V_{REF} and R_{SET}, as shown in Equation 10. The full-scale output current, I_{OUTFS}, results from multiplying I_{REF} by a fixed factor of 32.

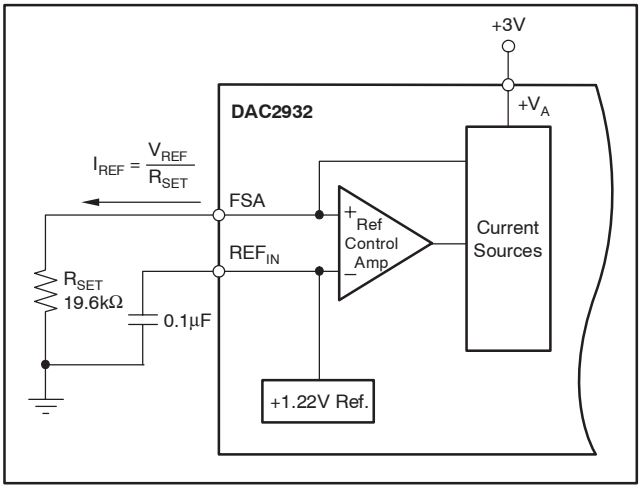


Figure 37. Internal Reference Configuration

Using the internal reference, a 19.6kΩ resistor value results in a full-scale output of approximately 2mA. Resistors with a tolerance of 1% or better should be considered. Selecting higher values, the output current can be adjusted from 2mA down to 0.5mA. Operating the DAC2932 at lower than 2mA output currents may be desirable for reasons of reducing the total power consumption or observing the output compliance voltage limitations for a given load condition.

It is recommended to bypass the REF_{IN} pin with a ceramic chip capacitor of 0.1µF or more. The control amplifier is internally compensated, and its small signal bandwidth is approximately 0.1MHz.

GAIN SETTING OPTIONS

The full-scale output current on the DAC2932 can be set two ways: either for each of the two DAC channels independently or for both channels simultaneously. For the independent gain set mode, GSET (pin 19) must be high (that is, connected to $+V_A$). In this mode, two external resistors are required—one R_{SET} connected to the FSA1 pin (pin 24) and the other to the FSA2 pin (pin 23). In this configuration, the user has the flexibility to set and adjust the full-scale output current for each DAC independently, allowing for the compensation of possible gain mismatches elsewhere within the transmit signal path.

Alternatively, bringing GSET low (that is, connected to AGND), switches the DAC2932 into the simultaneous gain set mode. Now the full-scale output current of both DAC channels is determined by only one external R_{SET} resistor connected to the FSA1 pin. The resistor at the FSA2 pin may be removed; however, this is not required since this pin is not functional in this mode and the resistor has no effect on the gain equation. The formula for deriving the correct R_{SET} remains unchanged. For example, R_{SET} = 19.6kΩ will result in a 2mA output for both DACs. The DAC2932 is specified with GSET being high and operating in inpendent gain mode. It should be noted that when using the simultaneous gain mode, the gain error and gain matching error will increase.

EXTERNAL REFERENCE OPERATION

The internal reference can be disabled by simply applying an external reference voltage into the REF_{IN} pin, which in this case functions as an input, as shown in Figure 38. The use of an external reference may be considered for applications that require higher accuracy and drift performance.

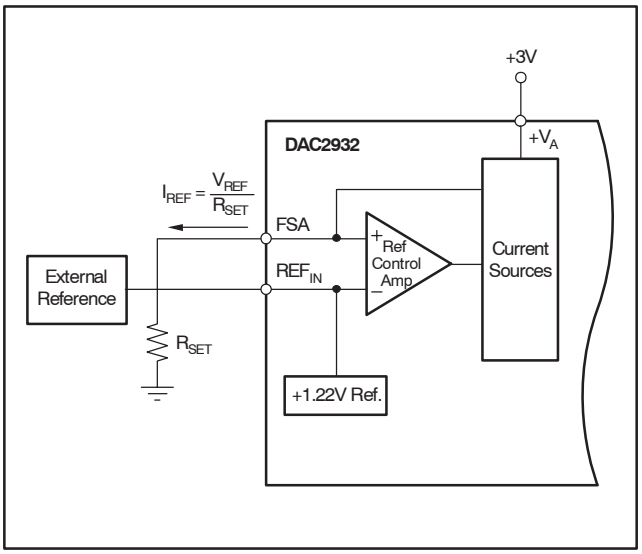


Figure 38. External Reference Configuration

While a 0.1μF capacitor is recommended for use with the internal reference, it is optional for the external reference operation. The reference input, REF_{IN}, has a high input impedance and can easily be driven by various sources.

V–DAC

The architecture consists of a resistor string DAC followed by an output buffer amplifier. Figure 39 shows a block diagram of the DAC architecture.

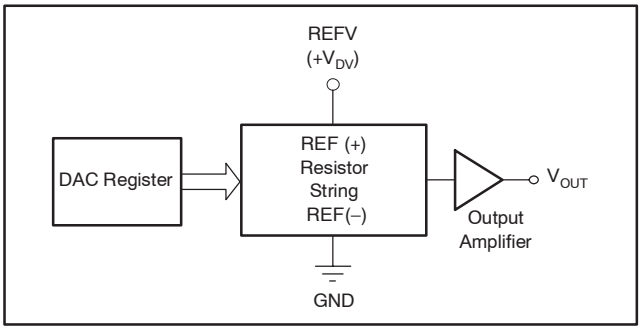


Figure 39. V-DAC Architecture

The input coding to the V-DAC is straight binary, so the ideal output voltage is given by:

$$V_{OUT} = REFV \times \frac{D}{4096} \quad (11)$$

where D = decimal equivalent of the binary code that is loaded to the DAC register; it can range from 0 to 4095.

SERIAL INTERFACE

The V–DACs have a three-wire serial interface ($\overline{SYNC}$, SCLK, and DIN), which is compatible with SPI, QSPI, and Microwire interface standards as well as most Digital Signal Processors (DSPs).

The write sequence begins by bringing the $\overline{SYNC}$ line low. Data from the DIN line is clocked into the 16-bit shift register on the falling edge of SCLK. The serial clock frequency can be as high as 20MHz, making the V-DACs compatible with high-speed DSPs. On the 16th falling edge of the serial clock, the last data bit is clocked in and the programmed function is executed (that is, a change in DAC register contents and/or a change in the mode of operation).

At this point, the $\overline{SYNC}$ line may be kept low or brought high. In either case, it must be brought high for a minimum of 50ns before the next write sequence so that a falling edge of $\overline{SYNC}$ can initiate the next write sequence. Since the $\overline{SYNC}$ buffer draws more current when the $\overline{SYNC}$ signal is high than it does when it is low, $\overline{SYNC}$ should be idled low between write sequences for lowest power operation of the part. As mentioned above, however, it must be brought high again just before the next write sequence.

INPUT SHIFT REGISTER

The input shift register is 16 bits wide. The first four bits are the address bits to the four V-DACs. The next 12 bits are the data bits. These are transferred to the DAC register on the 16th falling edge of the clock (SCLK).

SYNC INTERRUPT

In a normal write sequence, the $\overline{\text{SYNC}}$ line is kept low for at least 16 falling edges of SCLK and the DAC is updated on the 16th falling edge. However, if $\overline{\text{SYNC}}$ is brought high before the 16th falling edge, this acts as an interrupt to the write sequence. The shift register is reset and the write sequence is seen as invalid. Neither an update of the DAC register contents nor a change in the operating mode occurs, as shown in Figure 40.

POWER-ON RESET

The V-DACs contain a power-on reset circuit that controls the output voltage during power-up. On power-up, the DAC register is filled with zeros and the output voltage is 0V; it remains there until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up.

GROUNDING, DECOUPLING, AND LAYOUT INFORMATION

Proper grounding and bypassing, short lead length, and the use of ground planes are particularly important for high-frequency designs. Multilayer printed circuit boards (PCBs) are recommended for best performance since they offer distinct advantages such as minimization of ground impedance, separation of signal layers by ground layers, etc.

The DAC2932 uses separate pins for its analog and digital supply and ground connections. The placement of the decoupling capacitor should be such that the analog supply ($+V_A$) is bypassed to the analog ground (AGND), and the digital supply bypassed to the digital ground (DGND). In most cases, 0.1μF ceramic chip capacitors at each supply pin are adequate to provide a low impedance decoupling path. Keep in mind that their effectiveness largely depends on the proximity to the individual supply and ground pins. Therefore, they should be located as close as physically possible to those device leads. Whenever possible, the capacitors should be located immediately under each pair of supply/ground pins on the reverse side of the PCB. This layout approach minimizes the parasitic inductance of component leads and PCB runs.

Further supply decoupling with surface-mount tantalum capacitors (1μF to 4.7μF) can be added as needed in proximity of the converter.

Low noise is required for all supply and ground connections to the DAC2932. It is recommended to use a multilayer PCB with separate power and ground planes. Mixed signal designs require particular attention to the routing of the different supply currents and signal traces. Generally, analog supply and ground planes should only extend into analog signal areas, such as the DAC output signal and the reference signal. Digital supply and ground planes must be confined to areas covering digital circuitry, including the digital input lines connecting to the converter, as well as the clock signal. The analog and digital ground planes should be joined together at one point underneath the DAC. This can be realized with a short track of approximately 1/8” (3mm).

The power to the DAC2932 should be provided through the use of wide PCB runs or planes. Wide runs present a lower trace impedance, further optimizing the supply decoupling. The analog and digital supplies for the converter should only be connected together at the supply connector of the PCB. In the case of only one supply voltage being available to power the DAC, ferrite beads along with bypass capacitors can be used to create an LC filter. This will generate a low-noise analog supply voltage that can then be connected to the $+V_A$ supply pin of the DAC2932.

While designing the layout, it is important to keep the analog signal traces separated from any digital line, in order to prevent noise coupling onto the analog signal path.

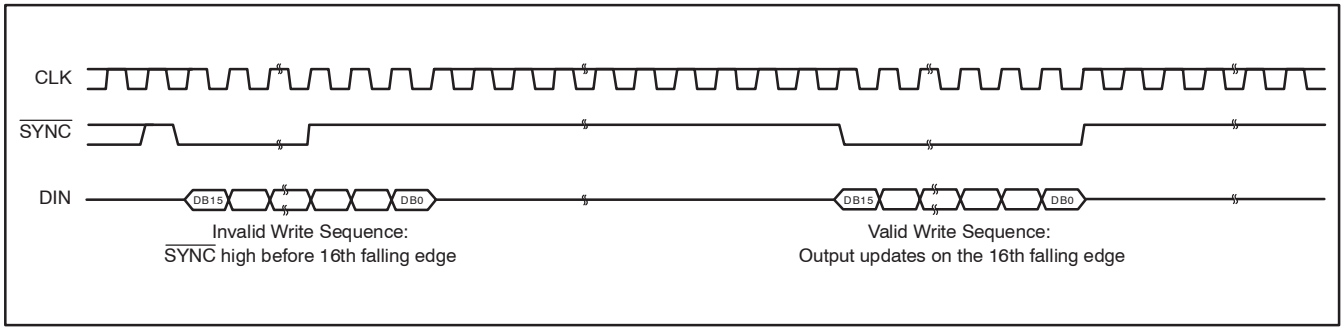


Figure 40. $\overline{\text{SYNC}}$ Interrupt Facility

Revision History

DATE	REV	PAGE	SECTION	DESCRIPTION
JUL 05	D	6	Timing Requirements	Changed tS1, tS2, tH1, tH2 min values, $\overline{CS}$ hold time (pulse width) min value, and $\overline{CS}$ to clock rising or falling edge setup time typ value.
		8	Pin Assignments	Changed pin names for pins 1 – 12
		8	Terminal Functions	Changed $\overline{CS}$ description.
		15	Power–Down Modes	In Table 1, changed column 1 row 7 from X to 0.
		16	Chip Select Operation	Added Chip Select Operation section with figure
		17	Differential With Transformer	Changed ratio and load in first paragraph. Changed ratio and load in Figure 30.
AUG 03	*	—	—	Original version

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC2932PFBR	ACTIVE	TQFP	PFB	48	2000	RoHS & Green	NIPDAU	Level-2A-260C-4 WKS	-40 to 85	DAC2932PFB	Samples
DAC2932PFBT	ACTIVE	TQFP	PFB	48	250	RoHS & Green	NIPDAU	Level-2A-260C-4 WKS	-40 to 85	DAC2932PFB	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

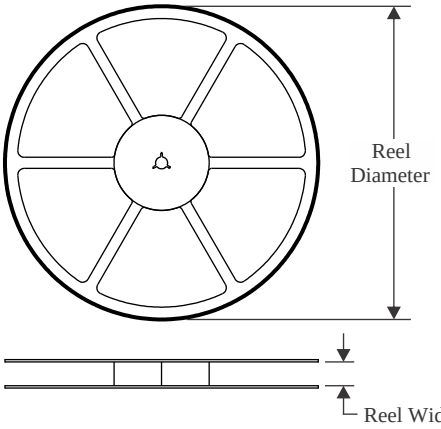
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

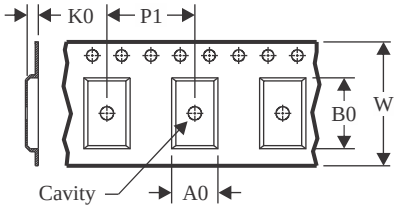
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

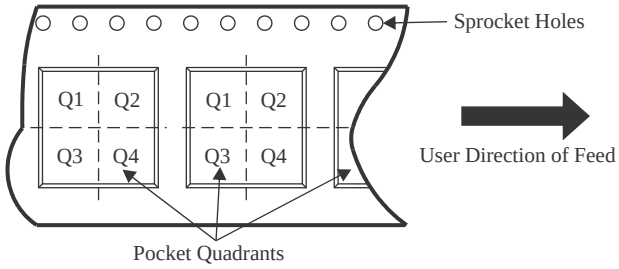


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

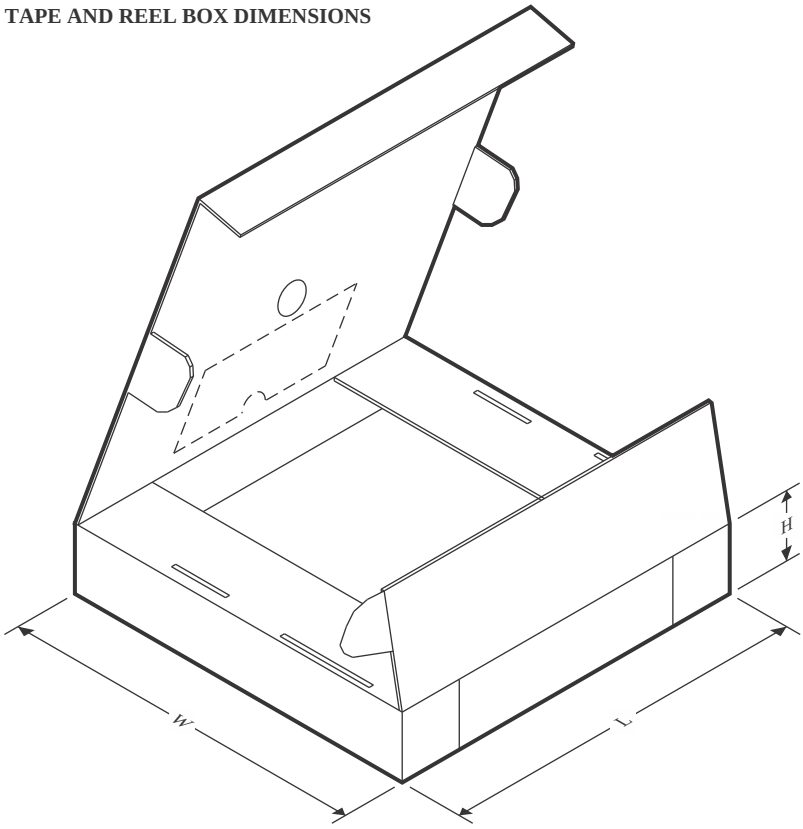
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC2932PFBR	TQFP	PFB	48	2000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	Q2

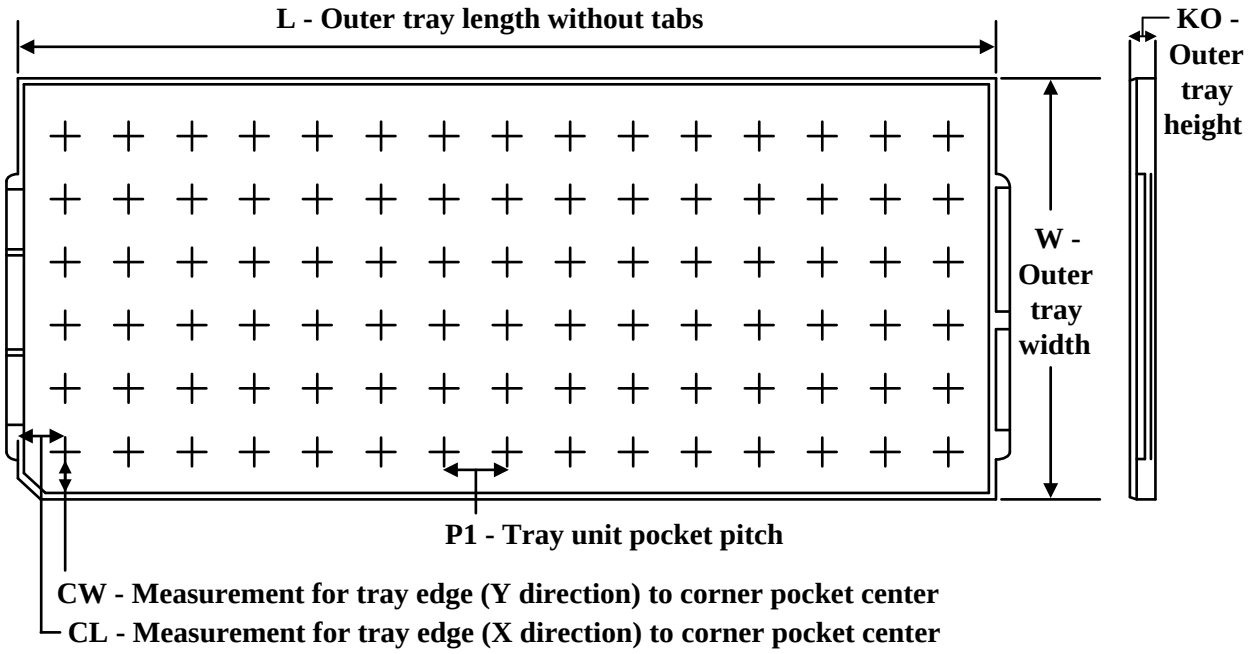
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC2932PFBR	TQFP	PFB	48	2000	350.0	350.0	43.0

TRAY



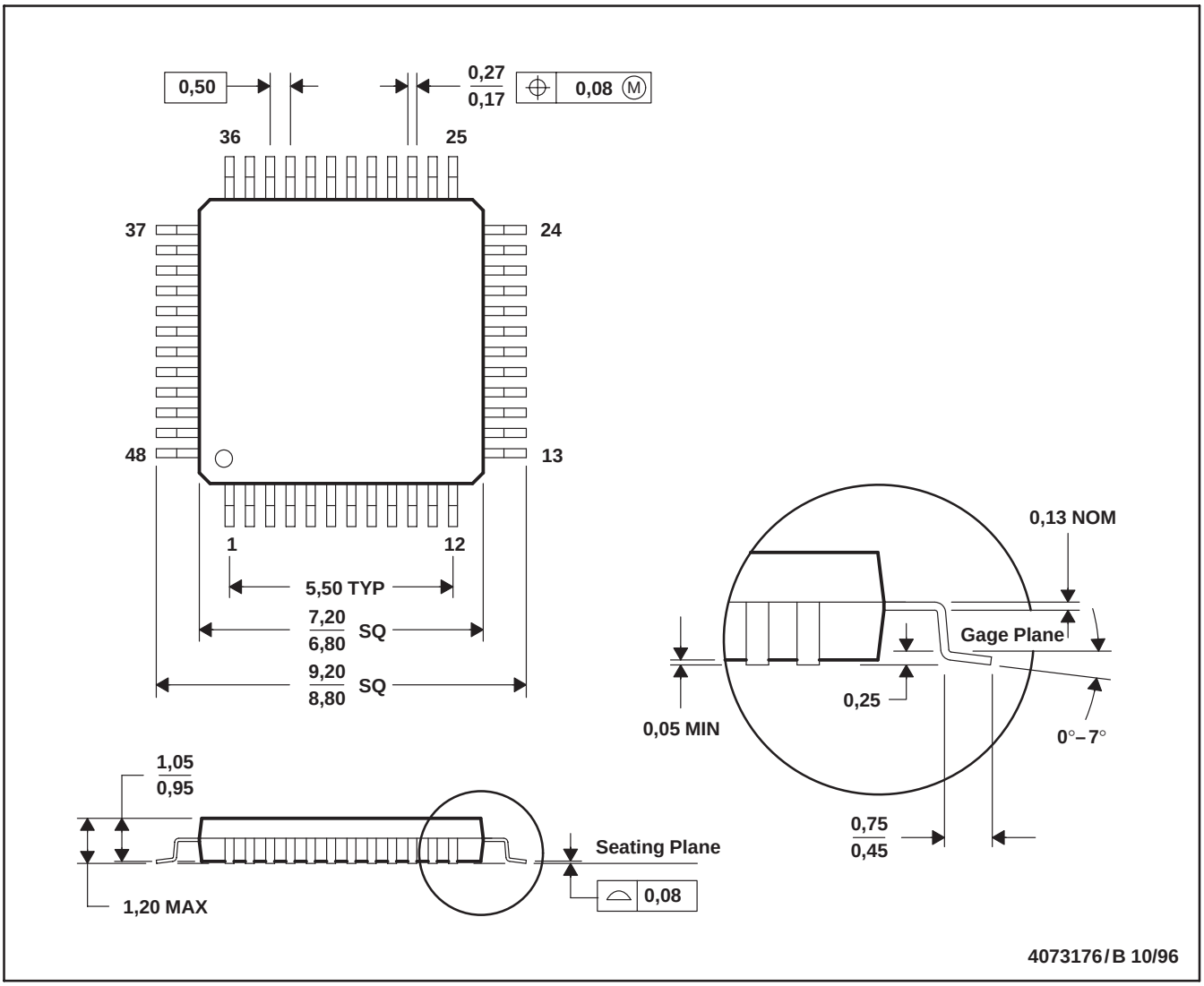
Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
DAC2932PFBR	PFB	TQFP	48	2000	10 x 25	150	315	135.9	7620	12.2	11.1	11.25
DAC2932PFBT	PFB	TQFP	48	250	10 x 25	150	315	135.9	7620	12.2	11.1	11.25

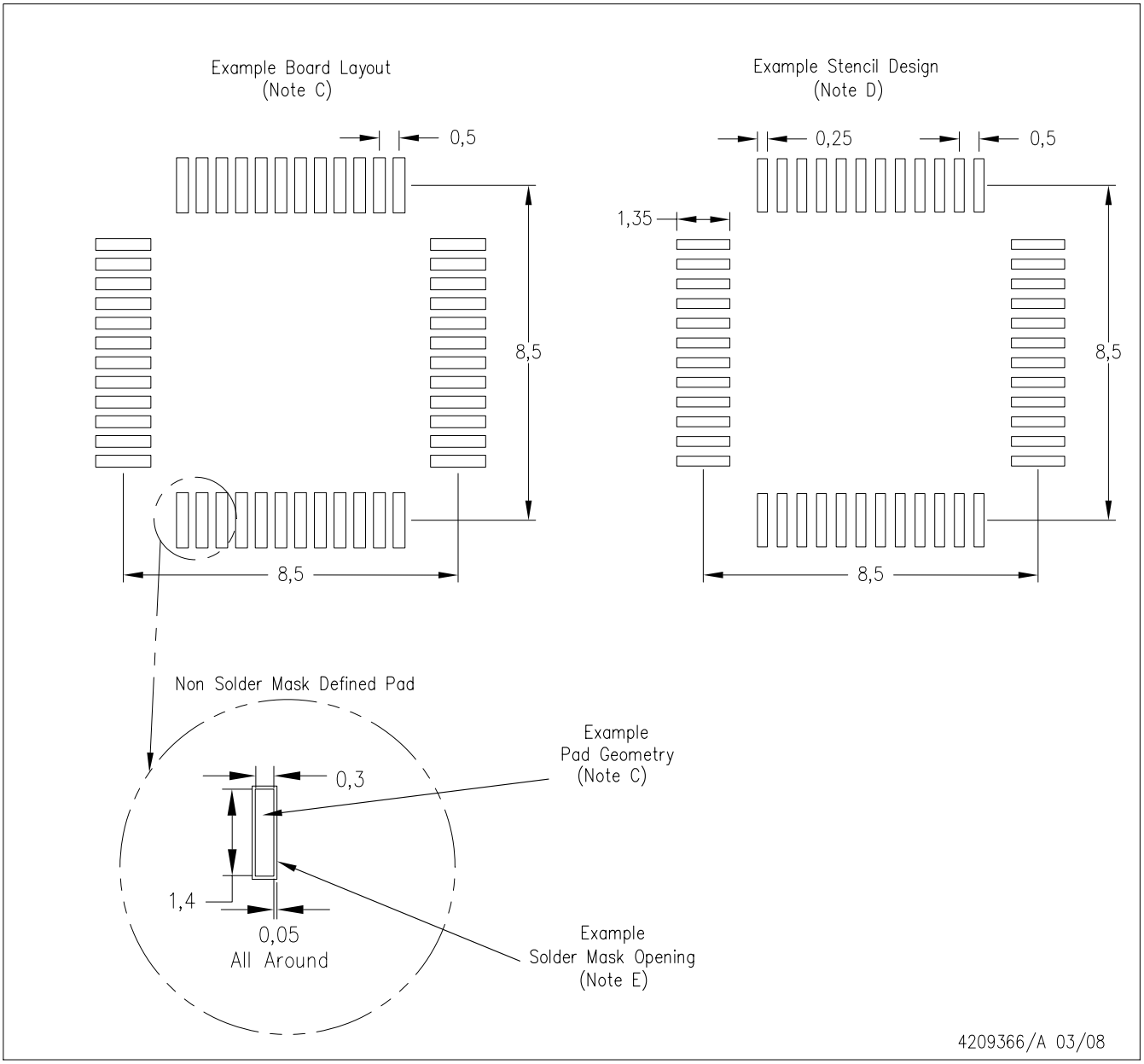
MTQF019A – JANUARY 1995 – REVISED JANUARY 1998

PFB (S-PQFP-G48) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

PFB (S–PQFP–G48)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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