



# 16-Bit, Single Channel DIGITAL-TO-ANALOG CONVERTER With Internal Reference and Parallel Interface

## FEATURES

- LOW POWER: 150mW Maximum
- +10V INTERNAL REFERENCE
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 5 $\mu$ s to  $\pm 0.003\%$  FSR
- 16-BIT MONOTONICITY,  $-40^{\circ}\text{C}$  TO  $+85^{\circ}\text{C}$
- $\pm 10\text{V}$ ,  $\pm 5\text{V}$  OR  $+10\text{V}$  CONFIGURABLE VOLTAGE OUTPUT
- RESET TO MIN-SCALE OR MID-SCALE
- DOUBLE-BUFFERED DATA INPUT
- INPUT REGISTER DATA READBACK
- SMALL LQFP-48 PACKAGE
- SUPPORTS TRANSPARENT DATA INPUT OPERATION

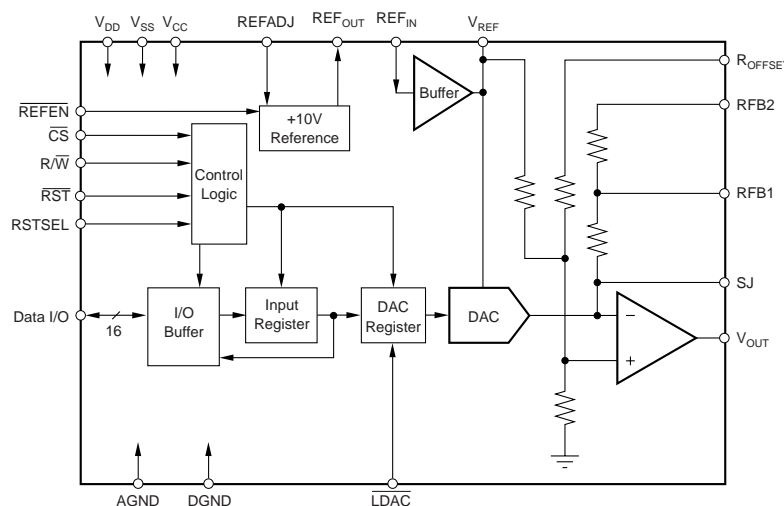
## APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS
- CLOSED-LOOP SERVO CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

## DESCRIPTION

The DAC7742 is a 16-bit Digital-to-Analog Converter (DAC) that provides 16 bits of monotonic performance over the specified operating temperature range and offers a +10V, low-drift internal reference. Designed for automatic test equipment and industrial process control applications, the DAC7742 output swing can be configured in a  $\pm 10\text{V}$ ,  $\pm 5\text{V}$ , or  $+10\text{V}$  range. The flexibility of the output configuration allows the DAC7742 to provide both unipolar and bipolar operation by pin strapping. The DAC7742 includes a high-speed output amplifier with a maximum settling time of 5 $\mu$ s to  $\pm 0.003\%$  FSR for a 20V full-scale change and only consumes 100mW (typical) of power.

The DAC7742 features a standard 16-bit parallel interface with double buffering to allow asynchronous updates of the analog output, and data read-back to support data integrity verification prior to an update. A user-programmable reset control allows the DAC output to reset to min-scale (FFFF<sub>H</sub>) or mid-scale (7FFF<sub>H</sub>) overriding the DAC register values. The DAC7742 is available in an LQFP-48 package and three performance grades specified to operate from  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ .



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

$V_{CC}$ to $V_{SS}$ .....	-0.3V to +32V
$V_{CC}$ to AGND .....	-0.3V to +16V
$V_{SS}$ to AGND .....	-16V to +0.3V
AGND to DGND .....	-0.3V to +0.3V
REF <sub>IN</sub> to AGND .....	0V to $V_{CC} - 1.4V$
$V_{DD}$ to DGND .....	-0.3V to +6V
Digital Input Voltage to DGND .....	-0.3V to $V_{DD} + 0.3V$
Digital Output Voltage to DGND .....	-0.3V to $V_{DD} + 0.3V$
Operating Temperature Range .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	+150°C

NOTE: (1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION

PRODUCT	LINEARITY ERROR (LSB)	DIFFERENTIAL NONLINEARITY (LSB)	PACKAGE-LEAD	PACKAGE DESIGNATOR <sup>(1)</sup>	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	TRANSPORT MEDIA, QUANTITY
DAC7742	±6	±4	LQFP-48	PT	-40°C to +85°C	DAC7742Y/250	DAC7742Y	Tape and Reel, 250
"	"	"	"	"	"	DAC7742Y/2K	"	Tape and Reel, 2000
DAC7742	±4	±2	LQFP-48	PT	-40°C to +85°C	DAC7742YB/250	DAC7742YB	Tape and Reel, 250
"	"	"	"	"	"	DAC7742YB/2K	"	Tape and Reel, 2000
DAC7742	±3	±1	LQFP-48	PT	-40°C to +85°C	DAC7742YC/250	DAC7742YC	Tape and Reel, 250
"	"	"	"	"	"	DAC7742YC/2K	"	Tape and Reel, 2000

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).

## ELECTRICAL CHARACTERISTICS

All specifications at  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{DD} = +5V$ , Internal reference enabled, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7742Y			DAC7742YB			DAC7742YC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>ACCURACY</b>											
Linearity Error (INL)	$T_A = 25^\circ C$			±6			±4			±3	LSB
Differential Linearity Error (DNL)				±5			±3			±2	LSB
Monotonicity		14		±4	15		±2	16		±1	LSB
Offset Error				±0.1			*			*	% of FSR
Offset Error Drift			±2			*		*		*	ppm/°C
Gain Error	With Internal REF			±0.4			±0.25			±0.2	% of FSR
	With External REF			±0.25			±0.1			*	% of FSR
Gain Error Drift	With Internal REF		±15			±10			±7		ppm/°C
PSRR ( $V_{CC}$ or $V_{SS}$ )	At Full-Scale		50	200		*	*		*	*	ppm/V
<b>ANALOG OUTPUT<sup>(1)</sup></b>											
Voltage Output <sup>(2)</sup>	+11.4/-4.75		0 to 10			*			*		V
	+11.4/-11.4		±10			*			*		V
	+11.4/-6.4		±5			*			*		V
Output Current		±5			*			*			mA
Output Impedance			0.1			*		*			Ω
Maximum Load Capacitance			200			*		*			pF
Short-Circuit Current			±15			*		*			mA
Short-Circuit Duration	AGND		Indefinite			*		*			
<b>REFERENCE</b>											
Reference Output		9.96	10	10.04	9.975	*	10.025	*	*	*	V
REF <sub>OUT</sub> Impedance			400			*		*	*		Ω
REF <sub>OUT</sub> Voltage Drift			±15			±10			±7		ppm/°C
REF <sub>OUT</sub> Voltage Adjustment <sup>(3)</sup>		±25			*		*	*			mV
REF <sub>IN</sub> Input Range <sup>(4)</sup>		4.75		$V_{CC} - 1.4$	*		*	*		*	V
REF <sub>IN</sub> Input Current			10			*		*	*		nA
REFADJ Input Range	Absolute Max Value that can be applied is $V_{CC}$	0		10	*		*	*	*		V
REFADJ Input Impedance			50			*		*	*		kΩ
$V_{REF}$ Output Current		-2		+2	*		*	*	*		mA
$V_{REF}$ Impedance			1			*		*	*		Ω

# ELECTRICAL CHARACTERISTICS (Cont.)

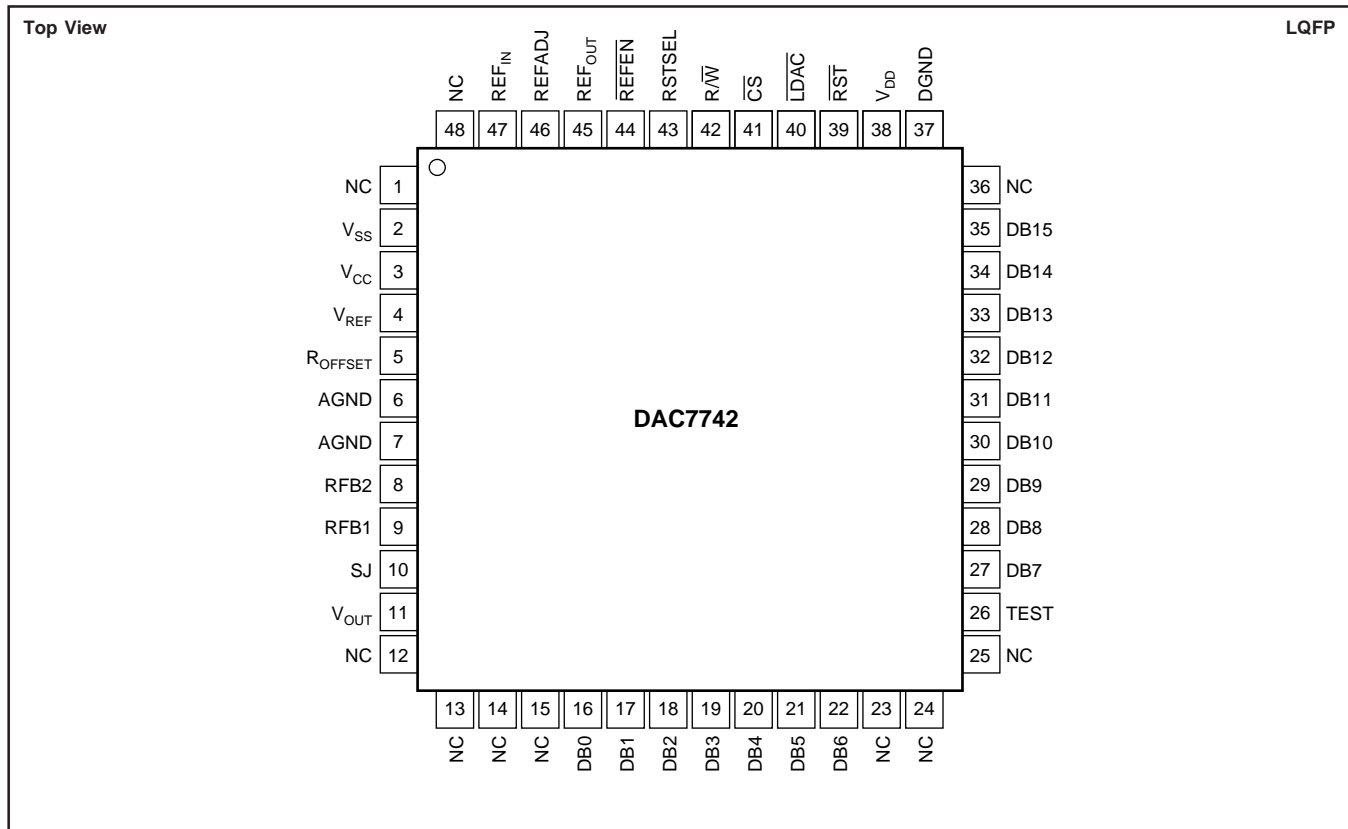
All specifications at  $T_A = T_{MIN}$  to  $T_{MAX}$ ,  $V_{CC} = +15V$ ,  $V_{SS} = -15V$ ,  $V_{DD} = +5V$ , Internal reference enabled, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7742Y			DAC7742YB			DAC7742YC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
<b>DYNAMIC PERFORMANCE</b> Settling Time to $\pm 0.003\%$	20V Output Step $R_L = 5k\Omega$ , $C_L = 200pF$ , with external $REF_{OUT}$ to $REF_{IN}$ filter <sup>(5)</sup>		3	4		*	*		*	*	$\mu s$
Digital Feedthrough Output Noise Voltage	at 10kHz		2 100			*	*		*	*	$\frac{nV \cdot s}{nV/\sqrt{Hz}}$
<b>DIGITAL INPUT</b> $V_{IH}$ $V_{IL}$ Input Coding	$ I_{IH}  < 10\mu A$ $ I_{IL}  < 10\mu A$	$0.7 \cdot V_{DD}$		$0.3 \cdot V_{DD}$	*		*	*		*	V V
		See Table III				*			*		
<b>DIGITAL OUTPUT</b> $V_{OH}$ $V_{OL}$	$I_{OH} = -0.8mA$ $I_{OL} = 1.6mA$	3.6		0.4	*		*	*		*	V V
<b>POWER SUPPLY</b> $V_{DD}$ $V_{CC}$ $V_{SS}$ $I_{DD}$ $I_{CC}$ $I_{SS}$ Power	Bipolar Operation Unipolar Operation  Unloaded Unloaded No Load, Ext. Reference No Load, Int. Reference	+4.75 +11.4 -15.75 -15.75	+5.0	+5.25 +15.75 -11.4 -4.75	*	*	*	*	*	*	V V V V $\mu A$ mA mA mW mW
<b>TEMPERATURE RANGE</b> Specified Performance		-40		+85	*		*	*		*	$^{\circ}C$

\* Specifications same as DAC7742Y.

NOTES: (1) With minimum  $V_{CC}/V_{SS}$  requirements, internal reference enabled. (2) Please refer to the "Theory of Operation" section for more information with respect to output voltage configurations. (3) See Figure 7 for gain and offset adjustment connection diagrams when using the internal reference. (4) The minimum value for  $REF_{IN}$  must be equal to the greater of  $V_{SS} + 14V$  and  $+4.75V$ , where  $+4.75V$  is the minimum voltage allowed. (5) Reference low-pass filter values:  $100k\Omega$ ,  $1.0\mu F$  (See Figure 10).

## PIN CONFIGURATION

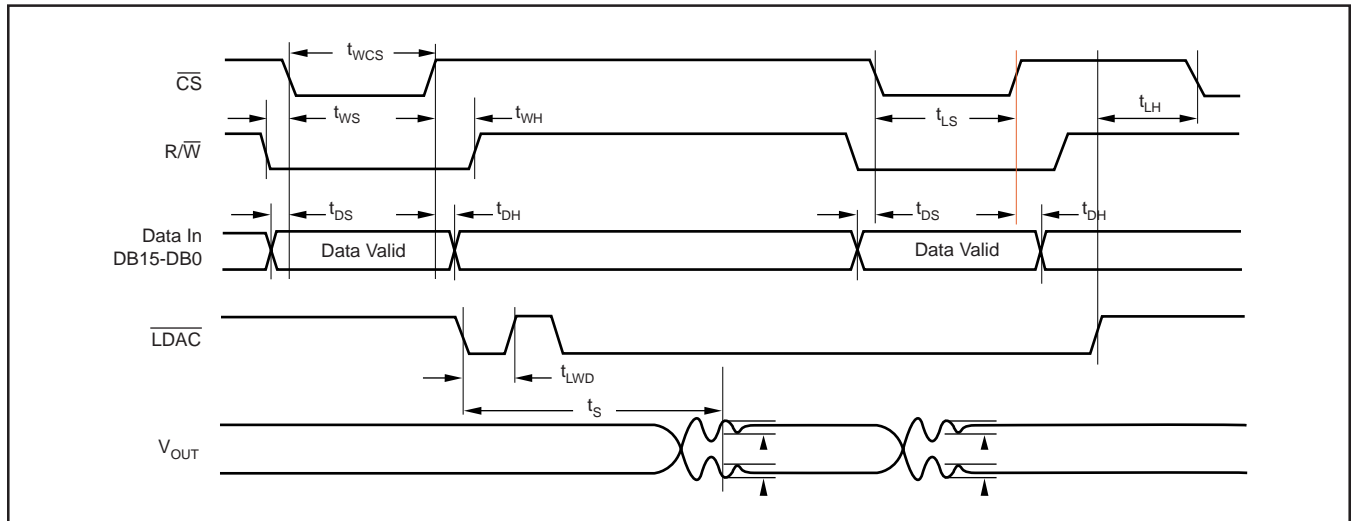


## PIN DESCRIPTIONS

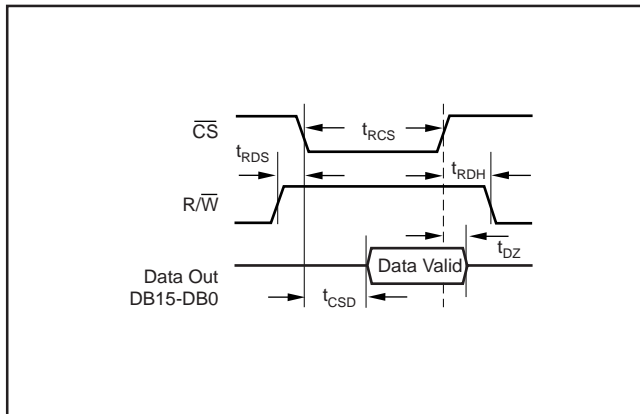
PIN	NAME	DESCRIPTION	PIN	NAME	DESCRIPTION
1	NC	No Connection	28	DB8	Data Bit 8
2	V <sub>SS</sub>	Negative Analog Power Supply	29	DB9	Data Bit 9
3	V <sub>CC</sub>	Positive Analog Power Supply	30	DB10	Data Bit 10
4	V <sub>REF</sub>	Buffered Output from REF <sub>IN</sub> ; can be used to drive external devices. Internally, this pin directly drives the DAC's circuitry.	31	DB11	Data Bit 11
5	R <sub>OFFSET</sub>	Offsetting Resistor	32	DB12	Data Bit 12
6	AGND	Analog Ground (Must be tied to analog ground.)	33	DB13	Data Bit 13
7	AGND	Analog Ground (Must be tied to analog ground.)	34	DB14	Data Bit 14
8	RFB2	Feedback Resistor 2, used to configure DAC output range.	35	DB15	Data Bit 15 (MSB)
9	RFB1	Feedback Resistor 1, used to configure DAC output range.	36	NC	No Connection
10	SJ	Summing Junction of the Output Amplifier	37	DGND	Digital Ground
11	V <sub>OUT</sub>	DAC Voltage Output	38	V <sub>DD</sub>	Digital Power Supply
12	NC	No Connection	39	R <sub>ST</sub>	V <sub>OUT</sub> reset; active LOW, depending on the state of RSTSEL, the DAC register is either reset to mid-scale or min-scale.
13	NC	No Connection	40	LDAC	DAC register load control, active LOW. Data is loaded from the input register to the DAC register.
14	NC	No Connection	41	CS	Chip Select, Active LOW
15	NC	No Connection	42	R/W	Enabled by CS, controls data read (HIGH) and write (LOW) from or to the input register.
16	DB0	Data Bit 0 (LSB)	43	RSTSEL	Reset Select; determines the action of RST. If HIGH, RST will reset the DAC register to mid-scale. If LOW, RST will reset the DAC register to min-scale.
17	DB1	Data Bit 1	44	REFEN	Enables internal +10V reference (REF <sub>OUT</sub> ), active LOW.
18	DB2	Data Bit 2	45	REF <sub>OUT</sub>	Internal Reference Output
19	DB3	Data Bit 3	46	REFADJ	Internal Reference Trim. (Acts as a gain adjustment input when the internal reference is used.)
20	DB4	Data Bit 4	47	REF <sub>IN</sub>	Reference Input
21	DB5	Data Bit 5	48	NC	No Connection
22	DB6	Data Bit 6			
23	NC	No Connection			
24	NC	No Connection			
25	NC	No Connection			
26	TEST	Reserved, Connect to DGND			
27	DB7	Data Bit 7			

# TIMING DIAGRAMS

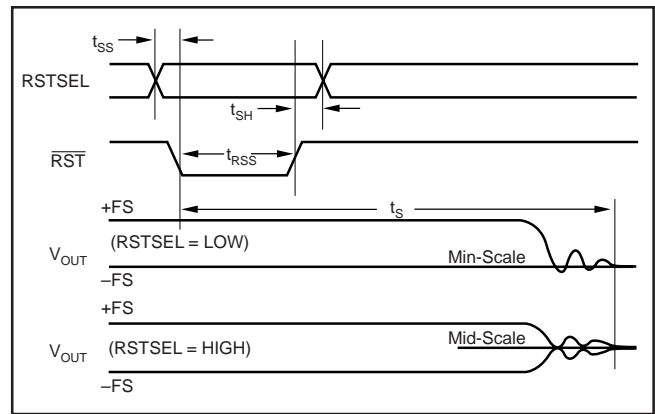
## DATA WRITE CYCLE



## READ CYCLE



## RESET TIMING

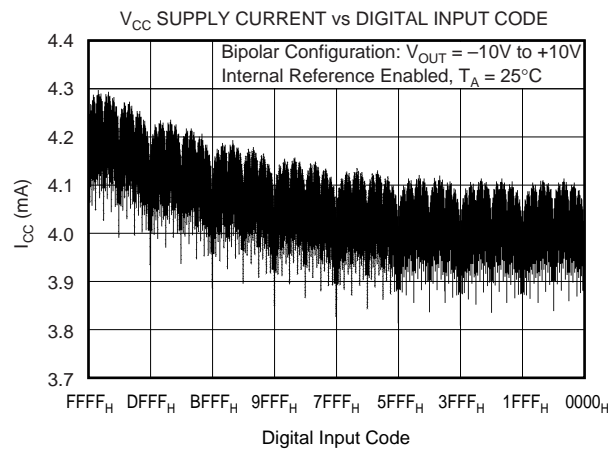
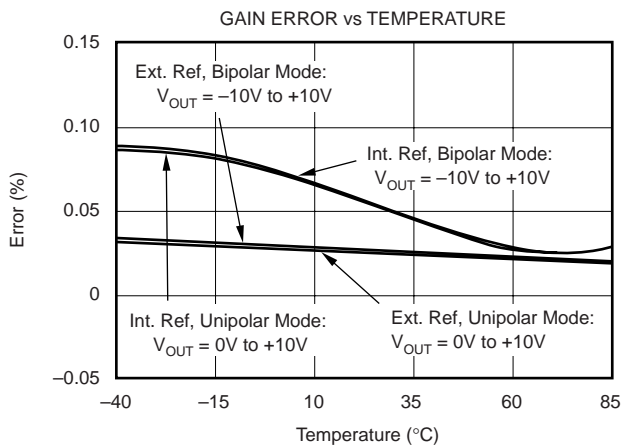
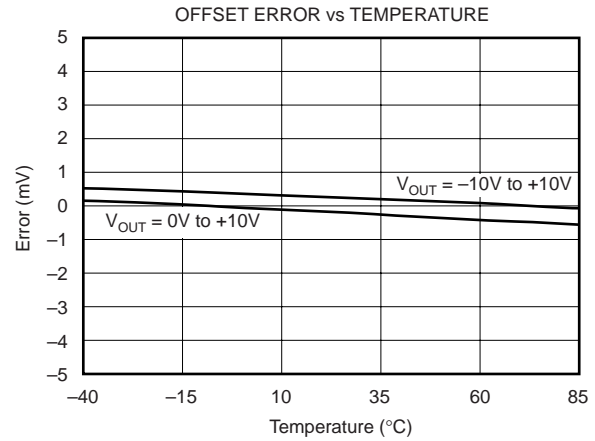
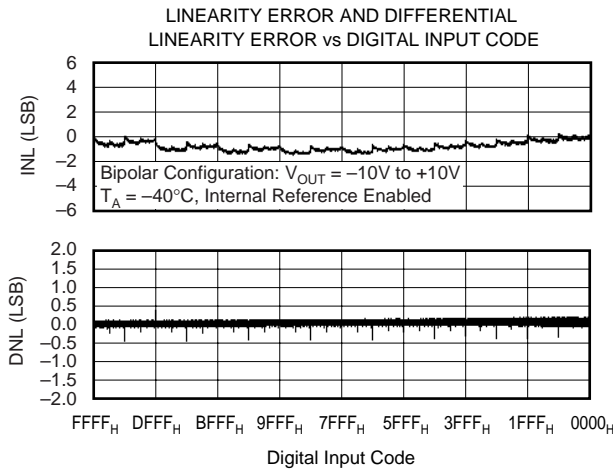
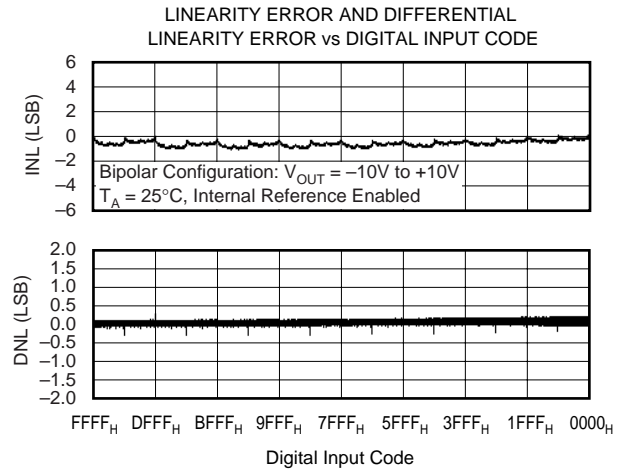
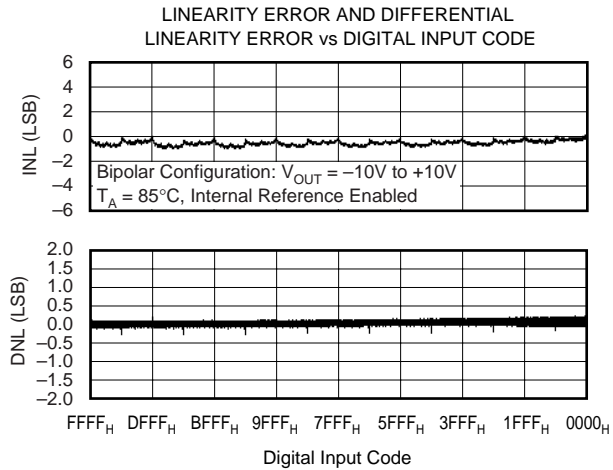


## TIMING CHARACTERISTICS

PARAMETER	DESCRIPTION	DAC7742Y			UNITS
		MIN	TYP	MAX	
<b>READ</b>					
$t_{RCS}$	$\overline{CS}$ LOW for Read	90			ns
$t_{RDS}$	$\overline{R/\overline{W}}$ HIGH to $\overline{CS}$ LOW	10			ns
$t_{RDH}$	$\overline{R/\overline{W}}$ HIGH After $\overline{CS}$ HIGH	10			ns
$t_{DZ}$	$\overline{CS}$ HIGH to Data Bus High Impedance	10		70	ns
$t_{CSD}$	$\overline{CS}$ LOW to Data Bus Valid		70	100	ns
<b>WRITE</b>					
$t_{ws}$	$\overline{R/\overline{W}}$ LOW to $\overline{CS}$ LOW	10			ns
$t_{wh}$	$\overline{R/\overline{W}}$ LOW After $\overline{CS}$ HIGH	10			ns
$t_{wCS}$	$\overline{CS}$ LOW for Write	25			ns
$t_{LWD}$	$\overline{LDAC}$ LOW for Write	20			ns
$t_{LS}$	$\overline{CS}$ LOW to $\overline{LDAC}$ HIGH for Direct Update	30			ns
$t_{LH}$	$\overline{CS}$ LOW After $\overline{LDAC}$ HIGH	0			ns
$t_{DS}$	Data Valid to $\overline{CS}$ LOW	0			ns
$t_{DH}$	Data Valid After $\overline{CS}$ HIGH	20			ns
<b>RESET</b>					
$t_{RSS}$	$\overline{RST}$ LOW	30			ns
$t_{SS}$	$\overline{RSTSEL}$ Valid Before $\overline{RST}$ LOW	0			ns
$t_{SH}$	$\overline{RSTSEL}$ Valid After $\overline{RST}$ HIGH	10			ns
<b>ANALOG</b>					
$t_s$	Voltage Output Settling Time			5	$\mu$ s

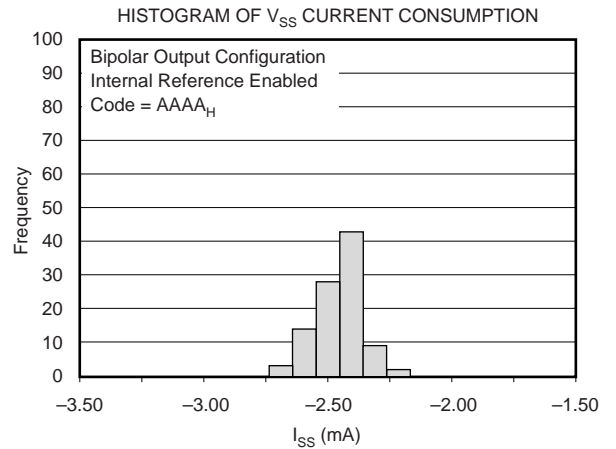
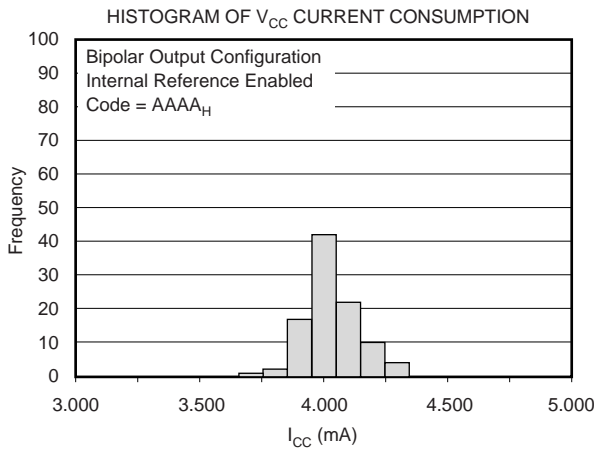
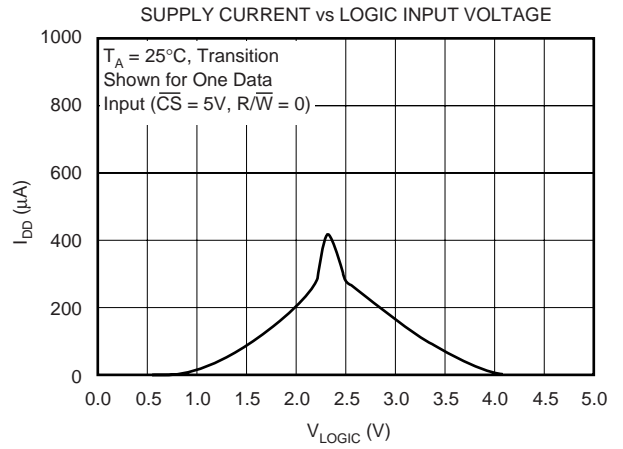
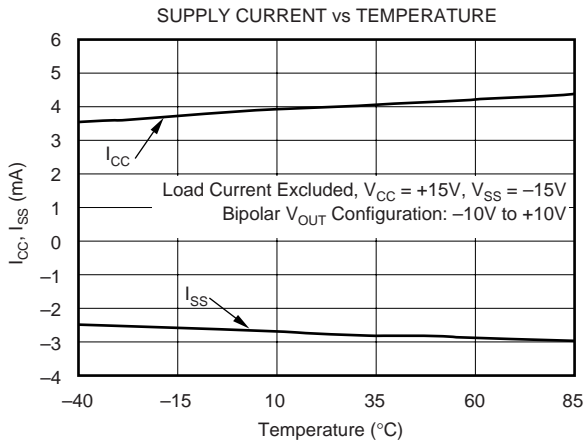
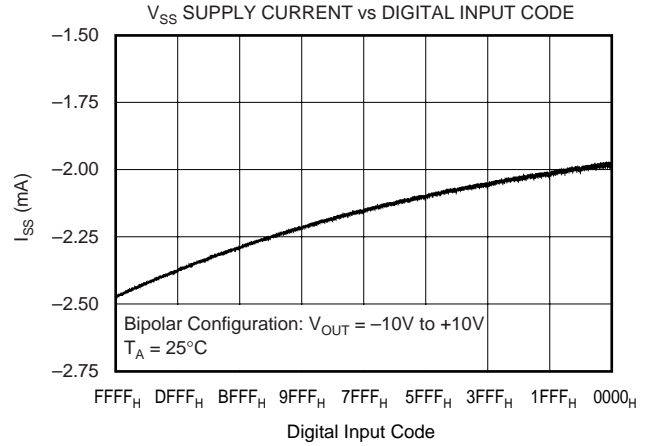
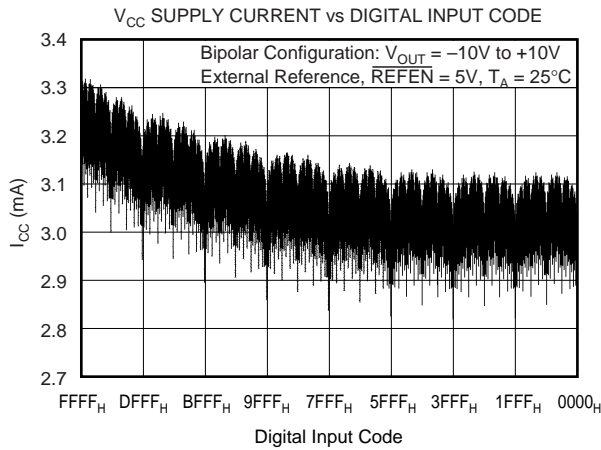
# TYPICAL CHARACTERISTICS

$T_A = +25^\circ\text{C}$  (unless otherwise noted).



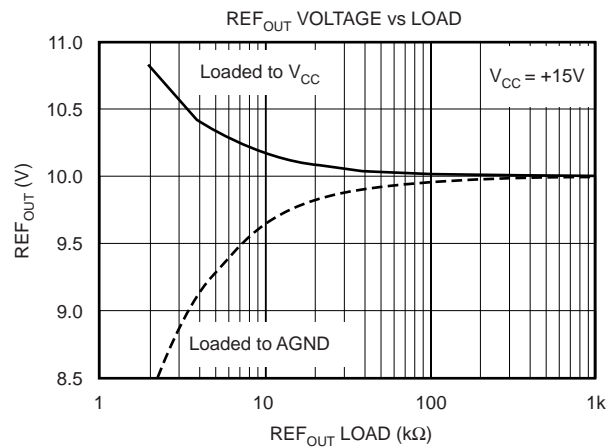
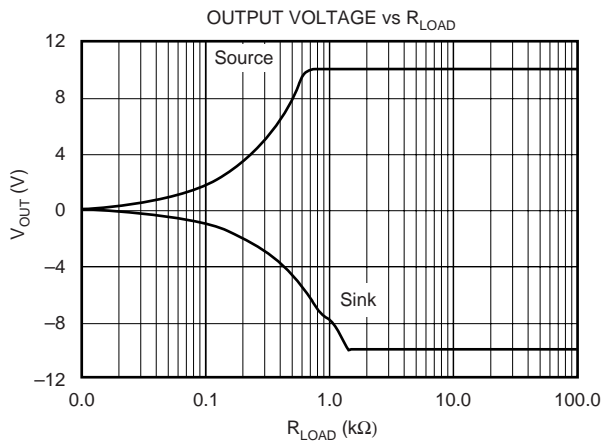
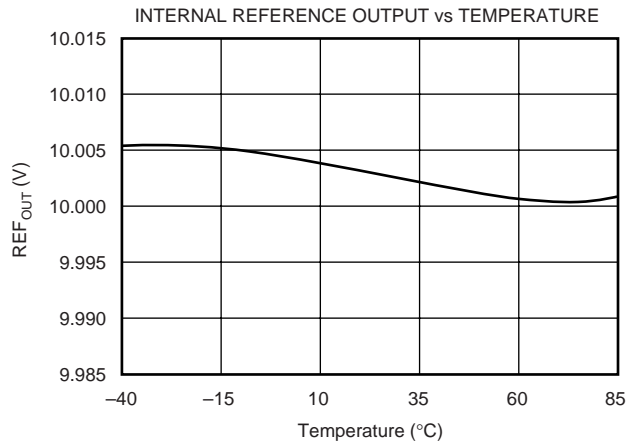
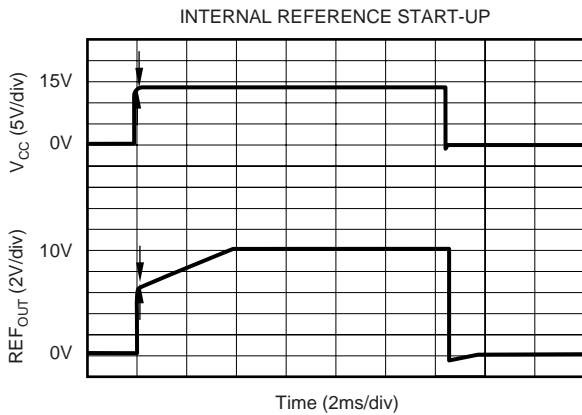
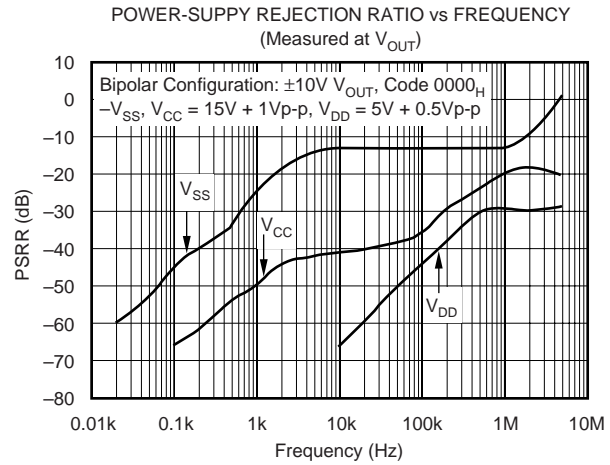
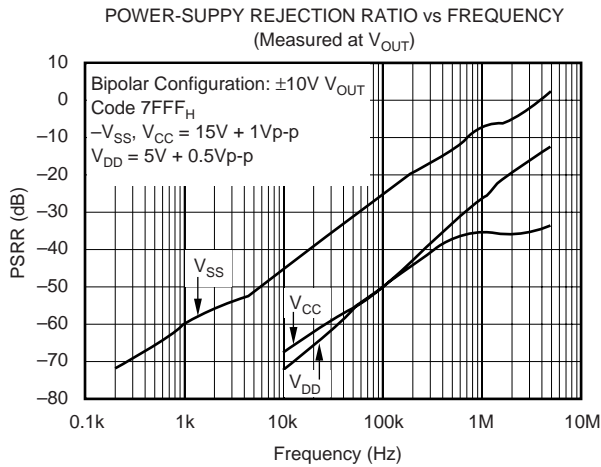
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# TYPICAL CHARACTERISTICS (Cont.)

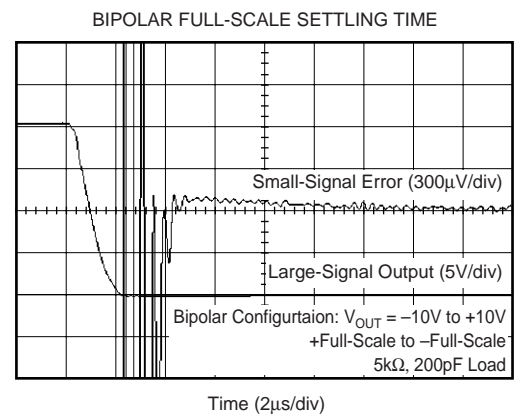
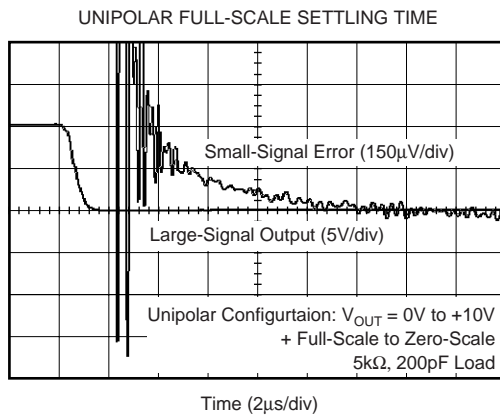
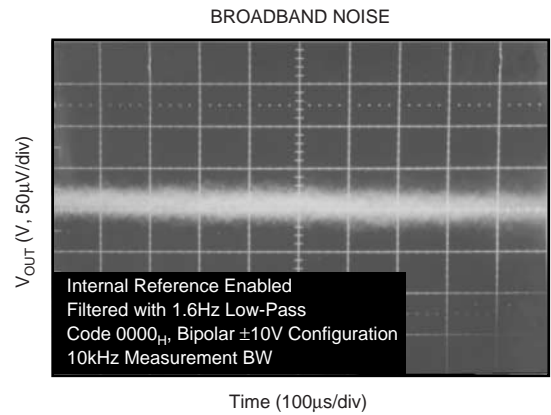
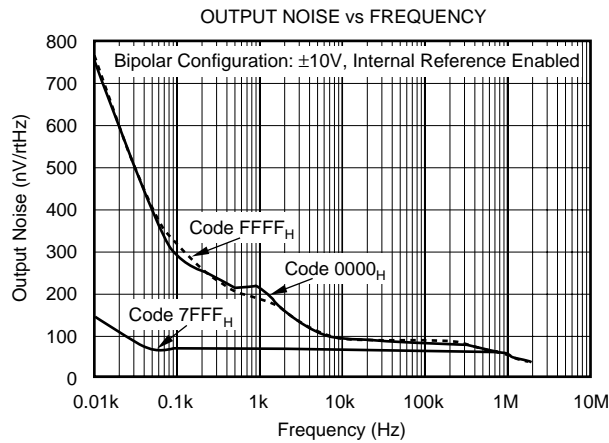
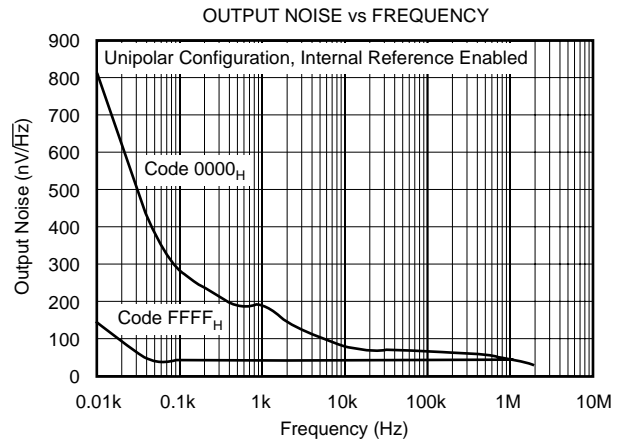
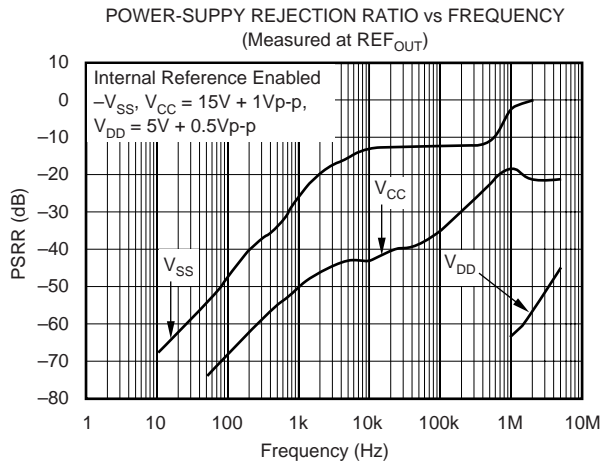
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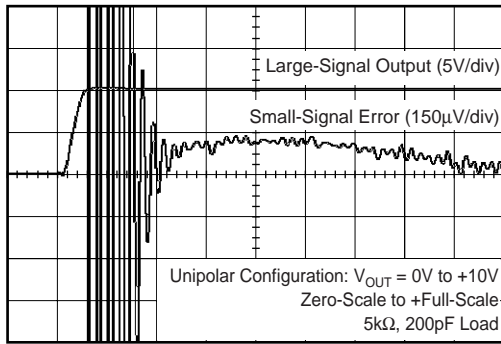
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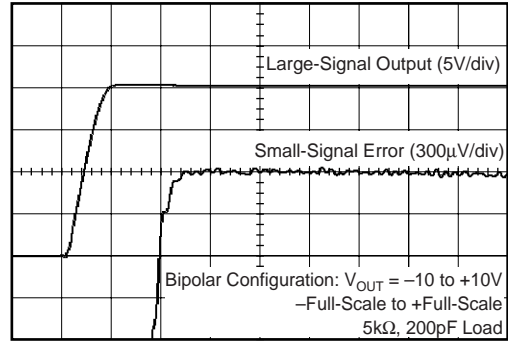
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UNIPOLAR FULL-SCALE SETTLING TIME



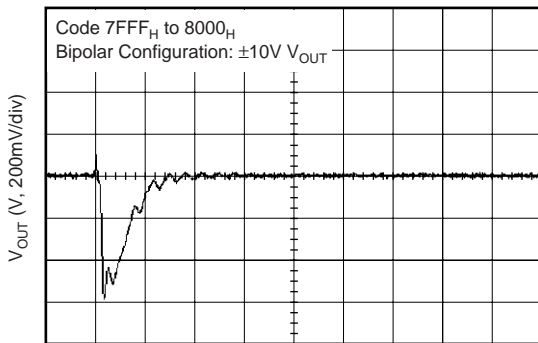
Time (2µs/div)

BIPOLAR FULL-SCALE SETTLING TIME



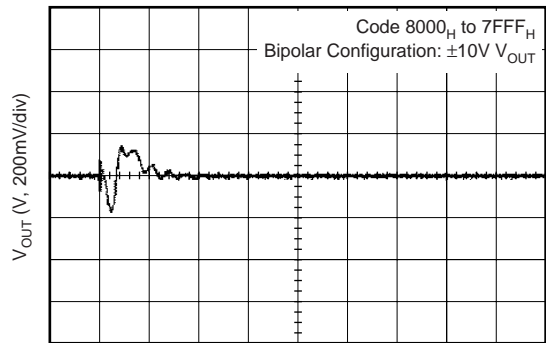
Time (2µs/div)

MID-SCALE GLITCH



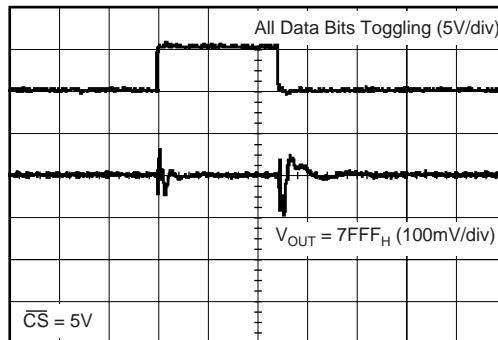
Time (1µs/div)

MID-SCALE GLITCH



Time (1µs/div)

DIGITAL FEEDTHROUGH



Time (200ns/div)

# THEORY OF OPERATION

The DAC7742 is a voltage output, 16-bit DAC with a +10V built-in internal reference. The architecture is an R-2R ladder configuration with the three MSBs segmented, followed by an operational amplifier that serves as a buffer, as shown in Figure 1. The output buffer is designed to allow user-configurable output adjustments giving the DAC7742 output voltage ranges of 0V to +10V, -5V to +5V, or -10V to +10V. Please refer to Figures 2, 3, and 4 for pin configuration information.

The digital input is a parallel word made up of the 16-bit DAC code and is loaded into the DAC register using the  $\overline{\text{LDAC}}$  input pin. The converter can be powered from  $\pm 12\text{V}$  to  $\pm 15\text{V}$  dual analog supplies and a +5V logic supply. The device offers a reset function, which immediately sets the DAC output voltage and DAC register to min-scale (code FFFF<sub>H</sub>) or mid-scale (code 7FFF<sub>H</sub>). The data I/O and reset functions are discussed in more detail in the following sections.

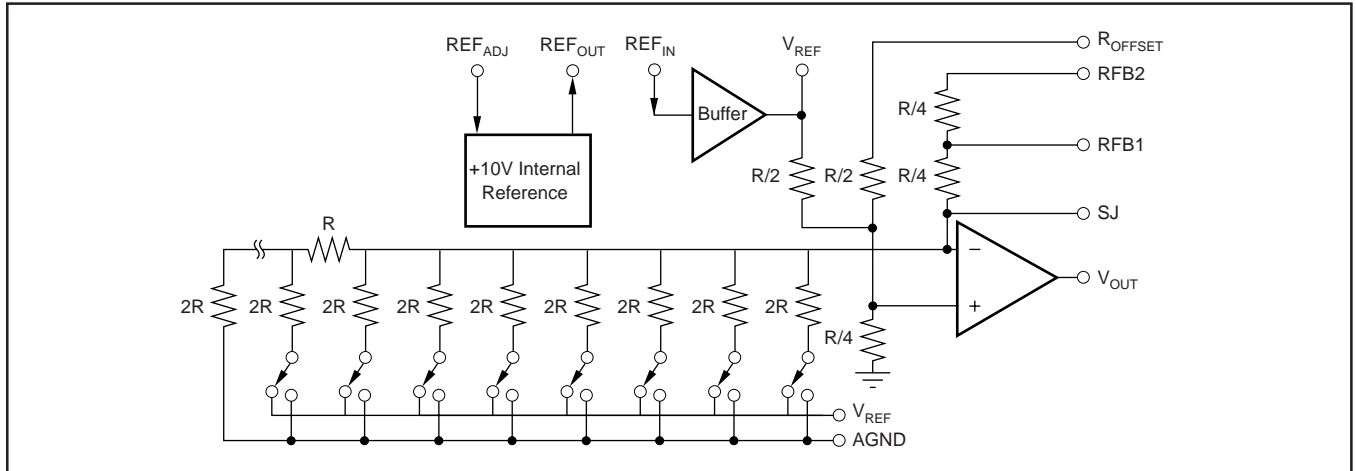


FIGURE 1. DAC7742 Architecture.

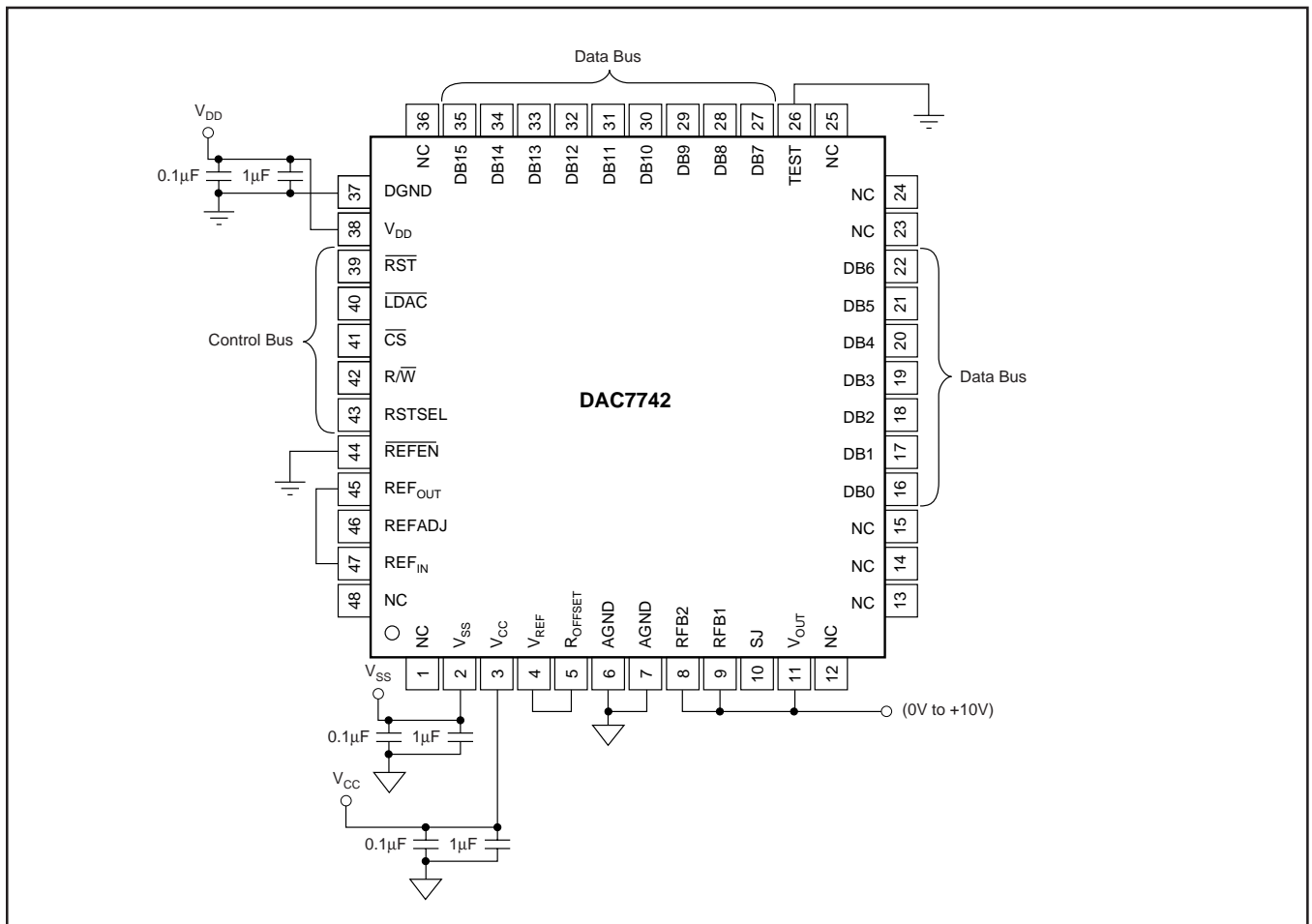


FIGURE 2. Basic Operation:  $V_{\text{OUT}} = 0\text{V}$  to +10V.

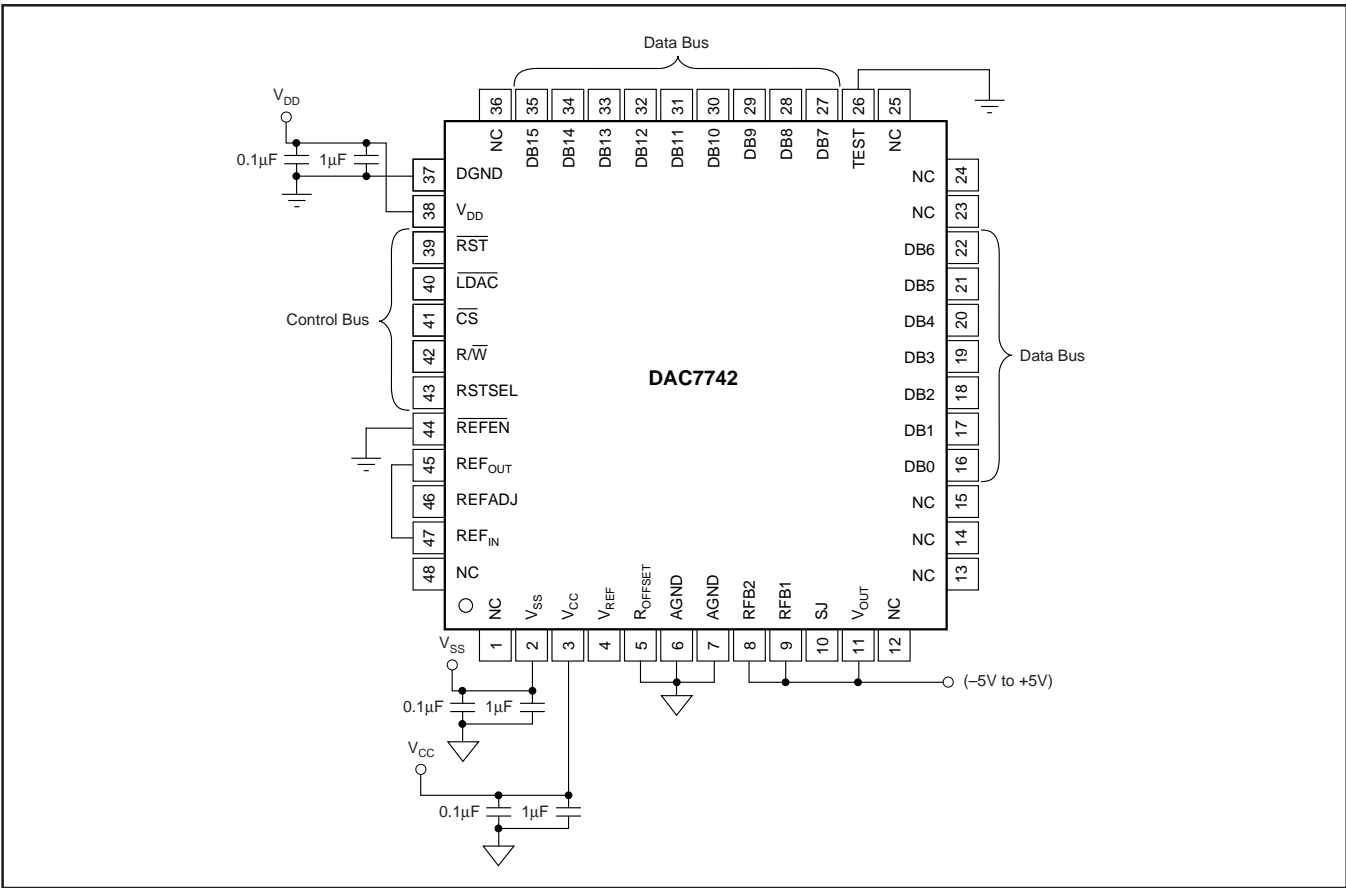


FIGURE 3. Basic Operation:  $V_{OUT} = -5V$  to  $+5V$ .

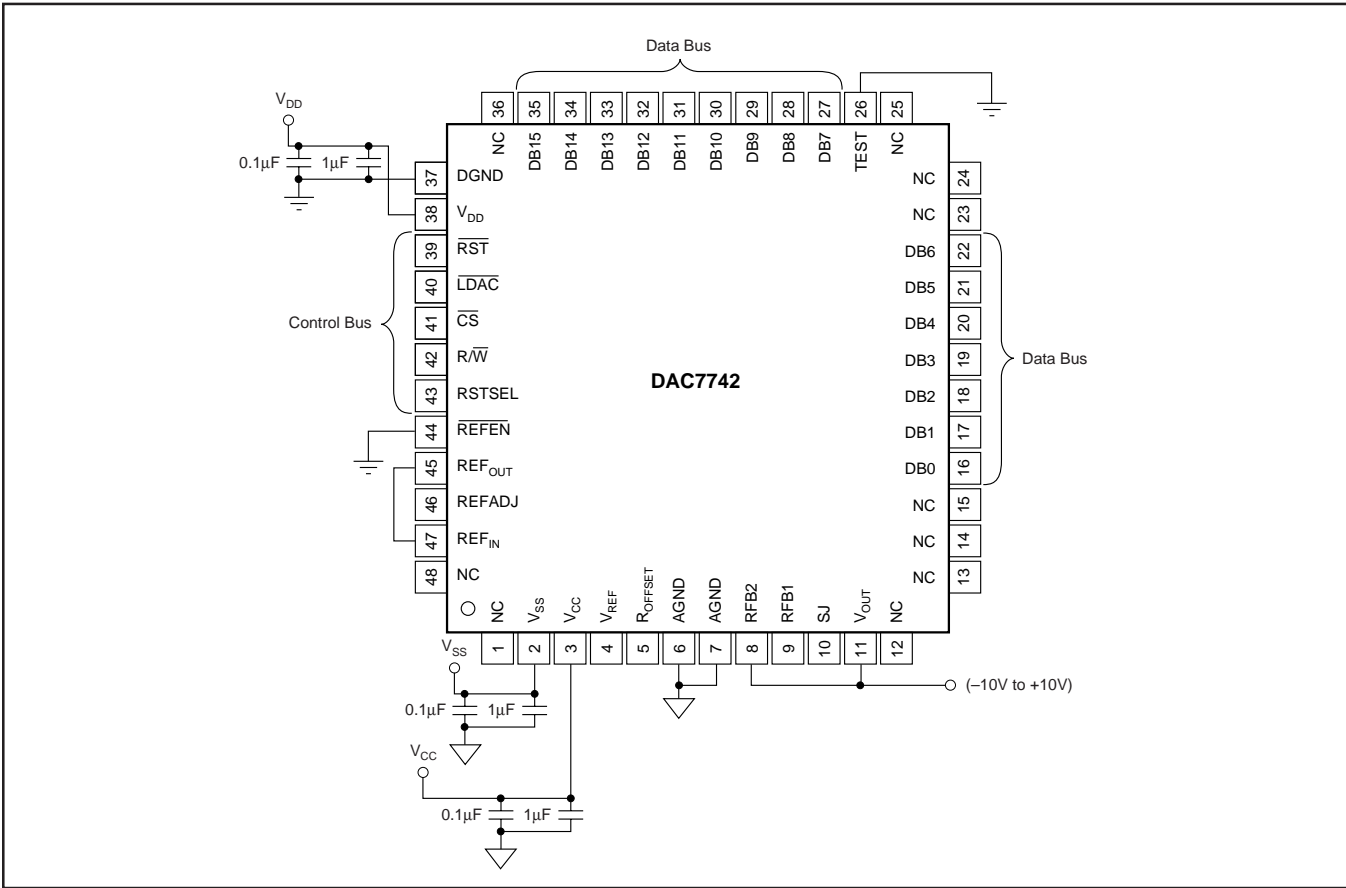


FIGURE 4. Basic Operation:  $V_{OUT} = -10V$  to  $+10V$ .

## ANALOG OUTPUTS

The output amplifier can swing to within 1.4V of the supply rails, specified over the  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  temperature range. This allows for a  $\pm 10\text{V}$  DAC voltage output operation from  $\pm 12\text{V}$  supplies with a typical 5% tolerance.

When the DAC7742 is configured for a unipolar, 0V to 10V output, a negative voltage supply is required. This is due to internal biasing of the output stage. Please refer to the “Electrical Characteristics” table for more information.

The minimum and maximum voltage output values are dependent upon the output configuration implemented and reference voltage applied to the DAC7742. Please note that  $V_{SS}$  (the negative power supply) must be in the range of  $-4.75\text{V}$  to  $-15.75\text{V}$  for unipolar operation. The voltage on  $V_{SS}$  sets several bias points within the converter and is required in all modes of operation. If  $V_{SS}$  is not in one of these two configurations, the bias values may be in error and proper operation of the device is not ensured.

Supply sequence is important in establishing correct startup of the DAC.

The digital supply ( $V_{DD}$ ) needs to establish correct bias conditions before the analog supplies ( $V_{CC}$ ,  $V_{SS}$ ) are brought up. If the digital supply cannot be brought up first, it must come up before either analog supply ( $V_{CC}$  or  $V_{SS}$ ), with the preferred sequence of:  $V_{SS}$  (device substrate),  $V_{DD}$ , and then  $V_{CC}$ .

## REFERENCE INPUTS

The DAC7742 provides a built-in +10V voltage reference and on-chip buffer to allow external component reference drive. To use the internal reference,  $\overline{\text{REFEN}}$  must be LOW, enabling the reference circuitry of the DAC7742 (as shown in Table I) and the  $\text{REF}_{\text{OUT}}$  pin must be connected to  $\text{REF}_{\text{IN}}$ . This is the input to the on-chip reference buffer. The buffer’s output is provided

REFEN	ACTION
1	Internal Reference disabled; $\text{REF}_{\text{OUT}} = \text{High Impedance}$
0	Internal Reference enabled; $\text{REF}_{\text{OUT}} = +10\text{V}$

TABLE I.  $\overline{\text{REFEN}}$  Action.

at the  $V_{\text{REF}}$  pin. In this configuration,  $V_{\text{REF}}$  is used to setup the DAC7742 output amplifier into one of three voltage output modes as discussed earlier.  $V_{\text{REF}}$  can also be used to drive other system components requiring an external reference.

The internal reference of the DAC7742 can be disabled when use of an external reference is desired. When using an external reference, the reference input,  $\text{REF}_{\text{IN}}$ , can be any voltage between 4.75V (or  $V_{SS} + 14\text{V}$ , whichever is greater) and  $V_{CC} - 1.4\text{V}$ .

## DIGITAL INTERFACE

Table III shows the data format for the DAC7742 and Table II illustrates the basic control logic of the device. The interface consists of a chip select input ( $\overline{\text{CS}}$ ), read/write control input ( $\overline{\text{R}/\overline{\text{W}}}$ ), data inputs (DB0-DB15), and a load DAC input ( $\overline{\text{LDAC}}$ ). An asynchronous reset input ( $\overline{\text{RST}}$ ) which is active LOW, is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select ( $\text{RSTSEL}$ ) signal. The DAC code is provided via a 16-bit parallel interface, as shown in Table II. The input word makes up the DAC code to be loaded into the data input register of the device. The data is latched into the input register on rising  $\overline{\text{CS}}$  and is loaded into the DAC register upon reception of a LOW level on the  $\overline{\text{LDAC}}$  input. This action updates the analog output,  $V_{\text{OUT}}$ , to the desired value.  $\overline{\text{LDAC}}$  inputs of multiple DAC7742s can be connected when a synchronized update of numerous DAC outputs is desired. Please refer to the timing section for more detailed data I/O information.

DIGITAL INPUT	ANALOG OUTPUT	
	Unipolar Configuration	Bipolar Configuration
	Complementary Straight Binary	Complementary Offset Binary
0xFFFF	Zero (0V)	-Full-Scale ( $-V_{\text{REF}}$ or $-V_{\text{REF}}/2$ )
0xFFFE	Zero + 1LSB	-Full-Scale + 1LSB
:	:	:
0x7FFF	1/2 Full-Scale	Bipolar Zero
0x7FFE	1/2 Full-Scale + 1LSB	Bipolar Zero + 1LSB
:	:	:
0x0000	Full-Scale ( $V_{\text{REF}} - 1\text{LSB}$ )	+Full-Scale ( $+V_{\text{REF}} - 1\text{LSB}$ or $+V_{\text{REF}}/2 - 1\text{LSB}$ )

TABLE III. DAC7742 Data Format.

CONTROL STATUS					COMMAND		
$\overline{\text{R}/\overline{\text{W}}}$	$\overline{\text{CS}}$	$\overline{\text{RST}}$	$\text{RSTSEL}$	$\overline{\text{LDAC}}$	Input Register	DAC Register	Mode
L	L	H	X	H	Write	Hold	Write Data to Input Register
X	H	H	X	L	Hold	Write	Update DAC Register with Data from Input Register
L	L	H	X	L	Transparent	Write	Write DAC Register Directly from Data Bus
H	L	H	X	H, L	Read	Hold	Read Data in Input Register
X	H	H	X	H	Hold	Hold	No Change
X	X	L	L	X	Reset to Min-Scale	Reset to Min-Scale	Reset to Input and DAC Register (FFFF <sub>H</sub> ) Min-Scale
X	X	L	H	X	Reset to Mid-Scale	Reset to Mid-Scale	Reset to Input and DAC Register (7FFF <sub>H</sub> ) Mid-Scale

TABLE II. DAC7742 Logic Truth Table.

## DAC RESET

The  $\overline{\text{RST}}$  and RSTSEL inputs control the reset of the analog output. The reset command is level triggered by a LOW signal on  $\overline{\text{RST}}$ . Once  $\overline{\text{RST}}$  is LOW, the DAC output will begin settling to the mid-scale or min-scale code depending on the state of the RSTSEL input. A HIGH value on RSTSEL will cause  $V_{\text{OUT}}$  to reset to the mid-scale code (7FFF<sub>H</sub>) and a LOW value will reset  $V_{\text{OUT}}$  to min-scale (FFFF<sub>H</sub>). A change in the state of the RSTSEL input while  $\overline{\text{RST}}$  is LOW will cause a corresponding change in the reset command selected internally and consequently change the output value of  $V_{\text{OUT}}$  of the DAC. Note that a valid reset signal also resets the input register of the DAC to the value specified by the state of RSTSEL.

## GAIN AND OFFSET CALIBRATION

The architecture of the DAC7742 is designed in such a way as to allow for easily configurable offset and gain calibration using a minimum of external components. The DAC7742 has built-in feedback resistors and output amplifier summing points brought out of the package in order to make the absolute calibration possible. Figures 5 and 6 illustrate the relationship of offset and gain adjustments for the DAC7742 in a unipolar configuration and in a bipolar configuration, respectively.

When calibrating the DAC's output, offset should be adjusted first to avoid 1st-order interaction of adjustments. In unipolar mode, the DAC7742's offset is adjusted from code FFFF<sub>H</sub> and for either bipolar mode, offset adjustments are made at code 7FFF<sub>H</sub>. Gain adjustment can then be made at code 0000<sub>H</sub> for each configuration, where the output of the DAC should be at +10V for the 0V to +10V – 1LSB or ±10V output range and +5V – 1LSB for the ±5V output range. Figure 7 shows the generalized external offset and gain adjustment circuitry using potentiometers.

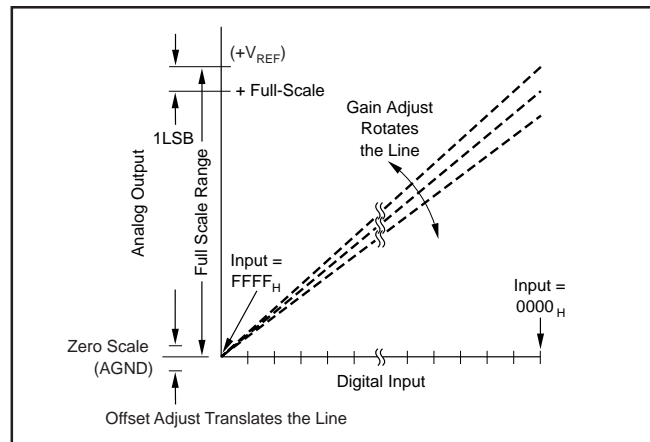


FIGURE 5. Relationship of Offset and Gain Adjustments for  $V_{\text{OUT}} = 0\text{V}$  to +10V Output Configuration.

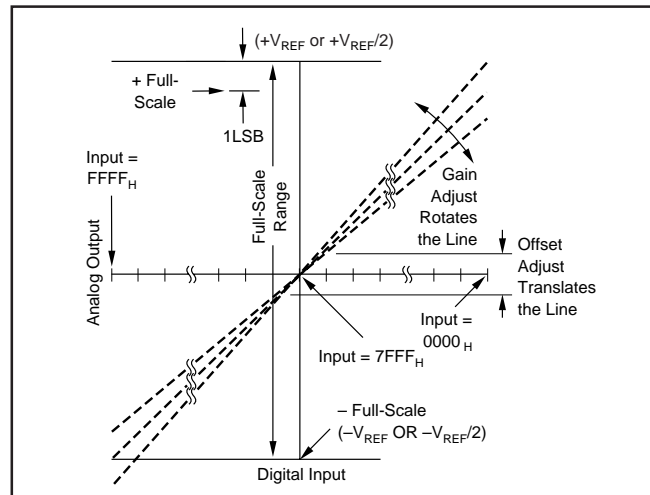


FIGURE 6. Relationship of Offset and Gain Adjustments for  $V_{\text{OUT}} = -10\text{V}$  to +10V Output Configuration. (Same Theory Applies for  $V_{\text{OUT}} = -5\text{V}$  to +5V.)

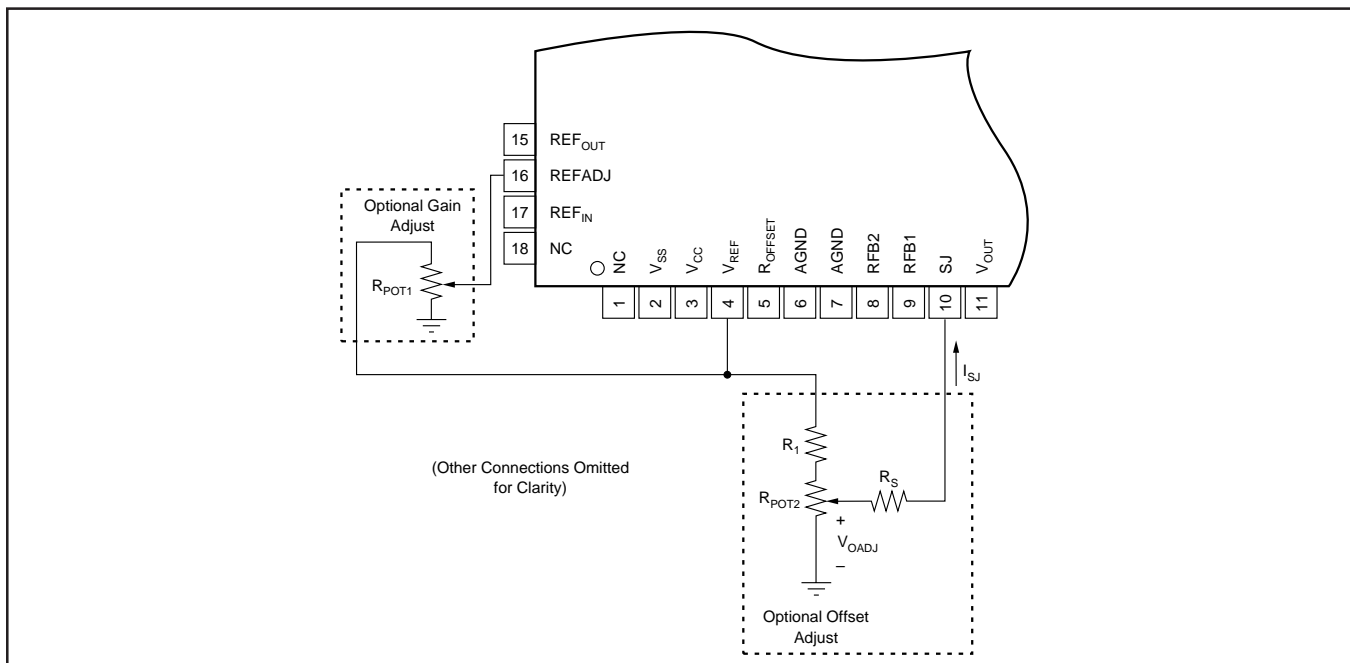


FIGURE 7. Generalized External Calibration Circuitry for Gain and Symmetrical Offset Adjustment.

## OFFSET ADJUSTMENT

Offset adjustment is accomplished by introducing a small current into the summing junction (SJ) of the DAC7742. The voltage at SJ, or  $V_{SJ}$ , is dependent on the output configuration of the DAC7742. Table IV shows the required pin strapping for a given configuration and the nominal values of  $V_{SJ}$  for each output range.

REFERENCE CONFIGURATION	OUTPUT CONFIGURATION	PIN STRAPPING			$V_{SJ}^{(1)}$
		R <sub>OFFSET</sub>	RFB1	RFB2	
Internal Reference	0V to +10V	to V <sub>REF</sub>	to V <sub>OUT</sub>	to V <sub>OUT</sub>	+5V
	-10V to +10V	NC	NC	to V <sub>OUT</sub>	+3.333V
	-5V to +5V	to AGND	to V <sub>OUT</sub>	to V <sub>OUT</sub>	+2.5V
External Reference	0V to V <sub>REF</sub>	to V <sub>REF</sub>	to V <sub>OUT</sub>	to V <sub>OUT</sub>	V <sub>REF</sub> /2
	-V <sub>REF</sub> to V <sub>REF</sub>	NC	NC	to V <sub>OUT</sub>	V <sub>REF</sub> /3
	-V <sub>REF</sub> /2 to V <sub>REF</sub> /2	to AGND	to V <sub>OUT</sub>	to V <sub>OUT</sub>	V <sub>REF</sub> /4

NOTE: (1) Voltage measured at  $V_{SJ}$  for a given configuration.

TABLE IV. Nominal  $V_{SJ}$  vs  $V_{OUT}$  and Reference Configuration.

The current level required to adjust the DAC7742's offset can be created by using a potentiometer divider, see Figure 7. Another alternative is to use a unipolar DAC in order to apply a voltage,  $V_{OAJ}$ , to the resistor  $R_S$ . A  $\pm 1.2\mu\text{A}$  current range applied to SJ will ensure offset adjustment coverage of the  $\pm 0.1\%$  maximum offset specification of the DAC7742.

When in a unipolar configuration ( $V_{SJ} = 5\text{V}$ ), only a single resistor,  $R_S$ , is needed for symmetrical offset adjustment with a 0V to 10V  $V_{OAJ}$  range. When in one of the two bipolar configurations,  $V_{SJ}$  is either +3.333v ( $\pm 10\text{V}$  range) or +2.5V ( $\pm 5\text{V}$  range), and circuit values chosen to match those given in Table V will provide symmetrical offset adjust. Please refer to Figure 7 for component configuration.

OUTPUT CONFIGURATION	R <sub>POT2</sub>	R <sub>1</sub>	R <sub>S</sub>	I <sub>SJ</sub> RANGE	NOMINAL OFFSET ADJUSTMENT
0V to +10V	10k	0	2.5M	$\pm 2\mu\text{A}$	$\pm 25\text{mV}$
-10V to +10V	10k	5k	1.5M	$\pm 2.2\mu\text{A}$	$\pm 55\text{mV}$
-5V to +5V	10k	10k	1.5M	$\pm 1.7\mu\text{A}$	$\pm 21\text{mV}$

TABLE V. Recommended External Component Values for Symmetrical Offset Adjustment ( $V_{REF} = 10\text{V}$ ).

Figure 8 illustrates the typical and minimum offset adjustment ranges provided by forcing a current at SJ for a given output voltage configuration.

## GAIN ADJUSTMENT

When using the internal reference of the DAC7742, gain adjustment is performed by adjusting the device's internal reference voltage via the reference adjust pin, REFADJ. The effect of a reference voltage change on the gain of the DAC output can be seen in the generic equation (for unipolar configuration):

$$V_{OUT} = V_{REFIN} \cdot \left( \frac{65535 - N}{65536} \right)$$

Where N is represented in decimal format and ranges from 0 to 65535.

REFADJ can be driven by a low impedance voltage source such as a unipolar, 0V to +10V DAC or a potentiometer (less than 100k $\Omega$ ), see Figure 7. Since the input impedance of REFADJ is typically 50k $\Omega$ , the smaller the resistance of the potentiometer, the more linear the adjustment will be. A 10k $\Omega$  potentiometer is suggested if linearity of the reference adjustment is of concern.

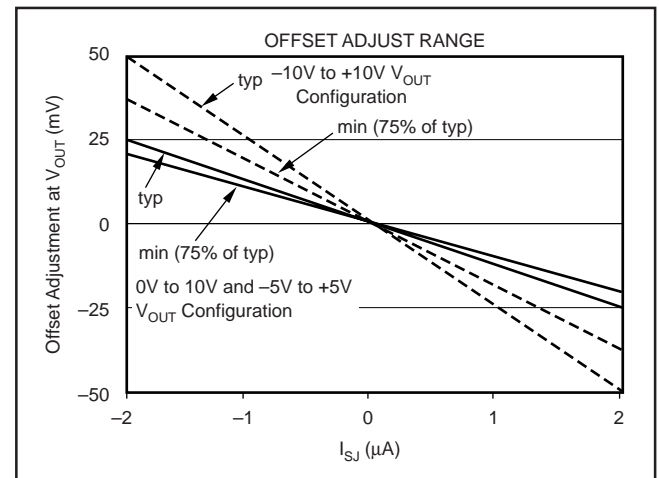


FIGURE 8. Offset Adjustment Transfer Characteristic.

When the DAC7742's internal reference is not used, gain adjustments can be made via trimming the external reference applied to the DAC at REF<sub>IN</sub>. This can be accomplished through using a potentiometer, unipolar DAC, or other means of precision voltage adjustment to control the voltage presented to the DAC7742 by the external reference. Figure 9 and Table VI summarize the range of adjustment of the internal reference via REFADJ.

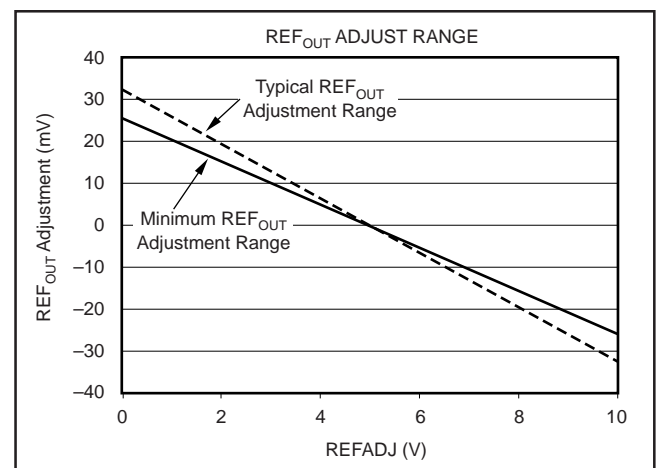


FIGURE 9. Internal Reference Adjustment Transfer Characteristic.

VOLTAGE AT REFADJ	REF <sub>OUT</sub> VOLTAGE
REFADJ = 0V	10V + 25mV (min)
REFADJ = 5V or NC <sup>(1)</sup>	10V
REFADJ = 10V	10V - 25mV (max)

NOTE: "NC" is "Not Connected".

TABLE VI. Minimum Internal Reference Adjustment Range.

## NOISE PERFORMANCE

Increased noise performance of the DAC output can be achieved by filtering the voltage reference input to the DAC7742. Figure 10 shows a typical internal reference filter schematic. A low-pass filter applied between the REF<sub>OUT</sub> and REF<sub>IN</sub> pins can increase noise immunity at the DAC and output amplifier. The REF<sub>OUT</sub> pin can source a maximum of 50µA so care should be taken in order to avoid overloading the internal reference output.

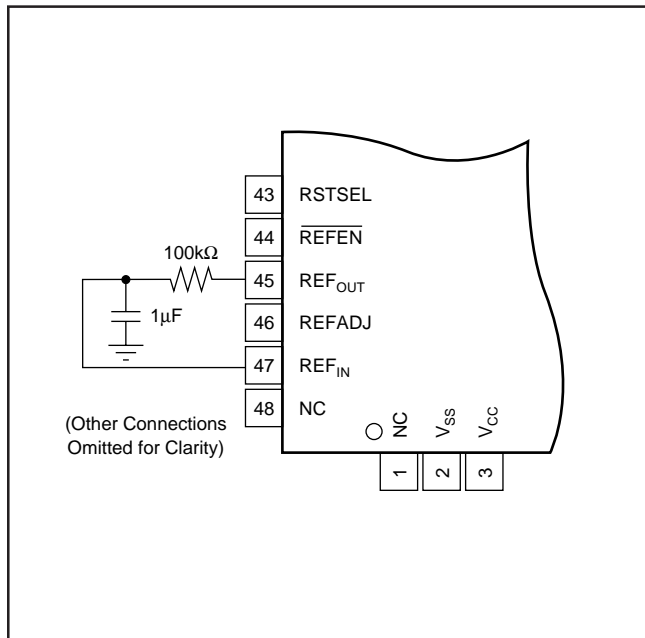


FIGURE 10. Internal Reference Filter.

## LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC7742 offers separate digital and analog supplies, as it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more important it will become to separate the analog and digital ground and supply planes at the device.



Since the DAC7742 has both analog and digital ground pins, return currents can be better controlled and have less effect on the DAC output error. Ideally, AGND would be connected directly to an analog ground plane and DGND to the digital ground plane. The analog ground plane would be separate from the ground connection for the digital components until they were connected at the power entry point of the system.

The voltages applied to V<sub>CC</sub> and V<sub>SS</sub> should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

In addition, a 1µF to 10µF bypass capacitor in parallel with a 0.1µF bypass capacitor is strongly recommended for each supply input. In some situations, additional bypassing may be required, such as a 100µF electrolytic capacitor or even a "Pi" filter made up of inductors and capacitors—all designed to essentially low-pass filter the analog supplies, removing any high frequency noise components.



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7742YB/250	ACTIVE	LQFP	PT	48	250	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7742Y B	
DAC7742YC/250	ACTIVE	LQFP	PT	48	250	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7742Y C	

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

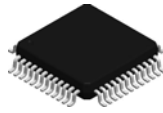
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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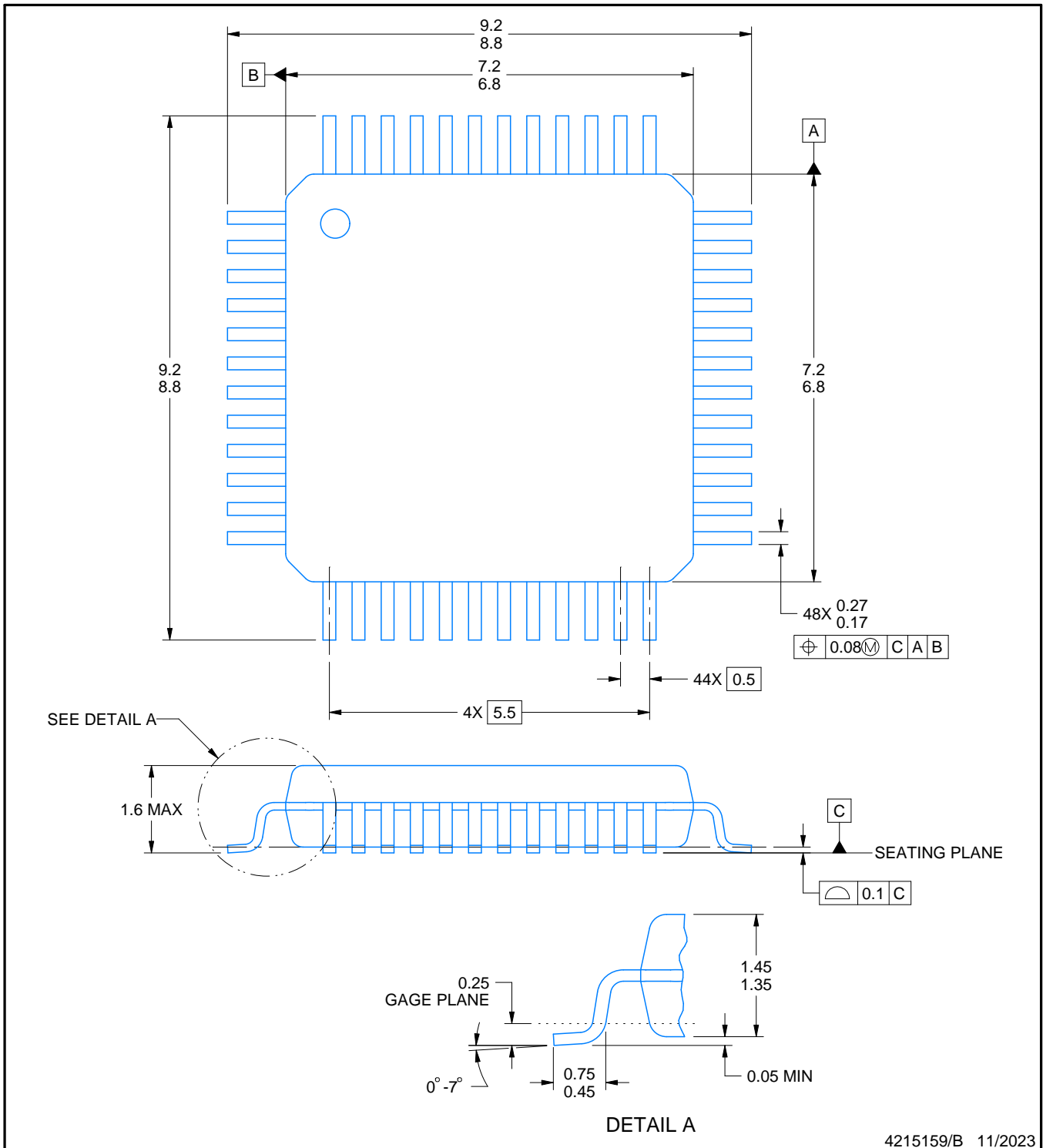
PT0048A



# PACKAGE OUTLINE

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



4215159/B 11/2023

## NOTES:

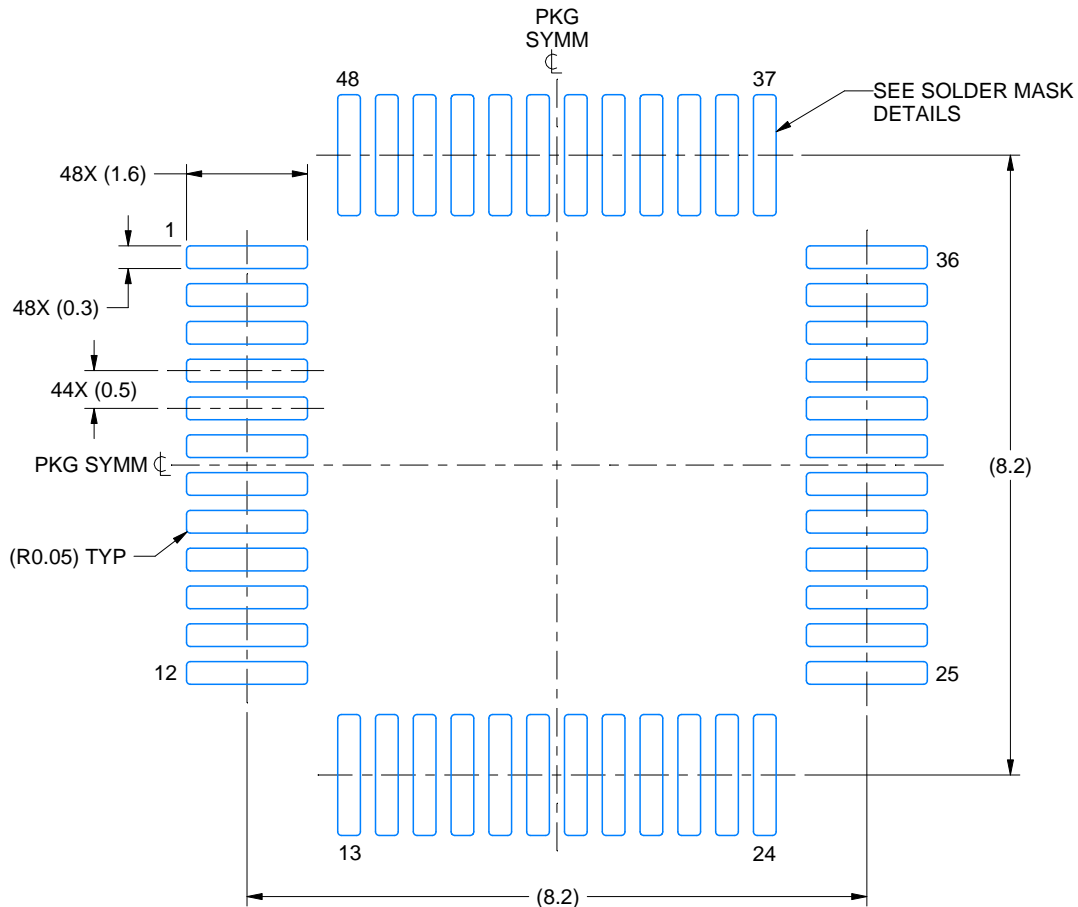
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads connected to the die pads.

# EXAMPLE BOARD LAYOUT

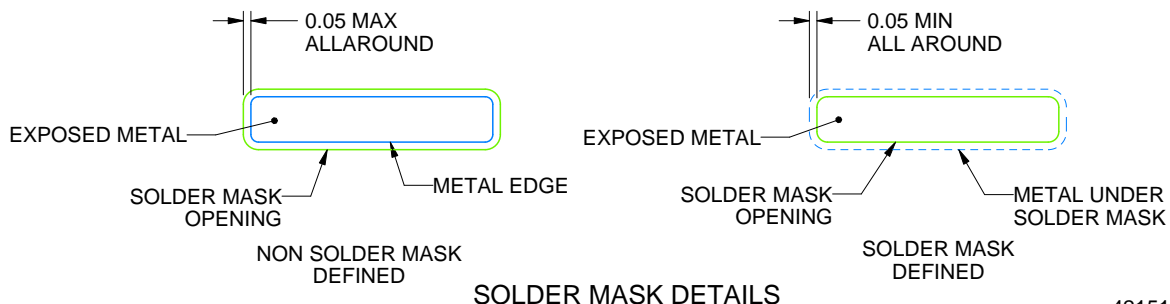
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE 10.000



SOLDER MASK DETAILS

4215159/B 11/2023

NOTES: (continued)

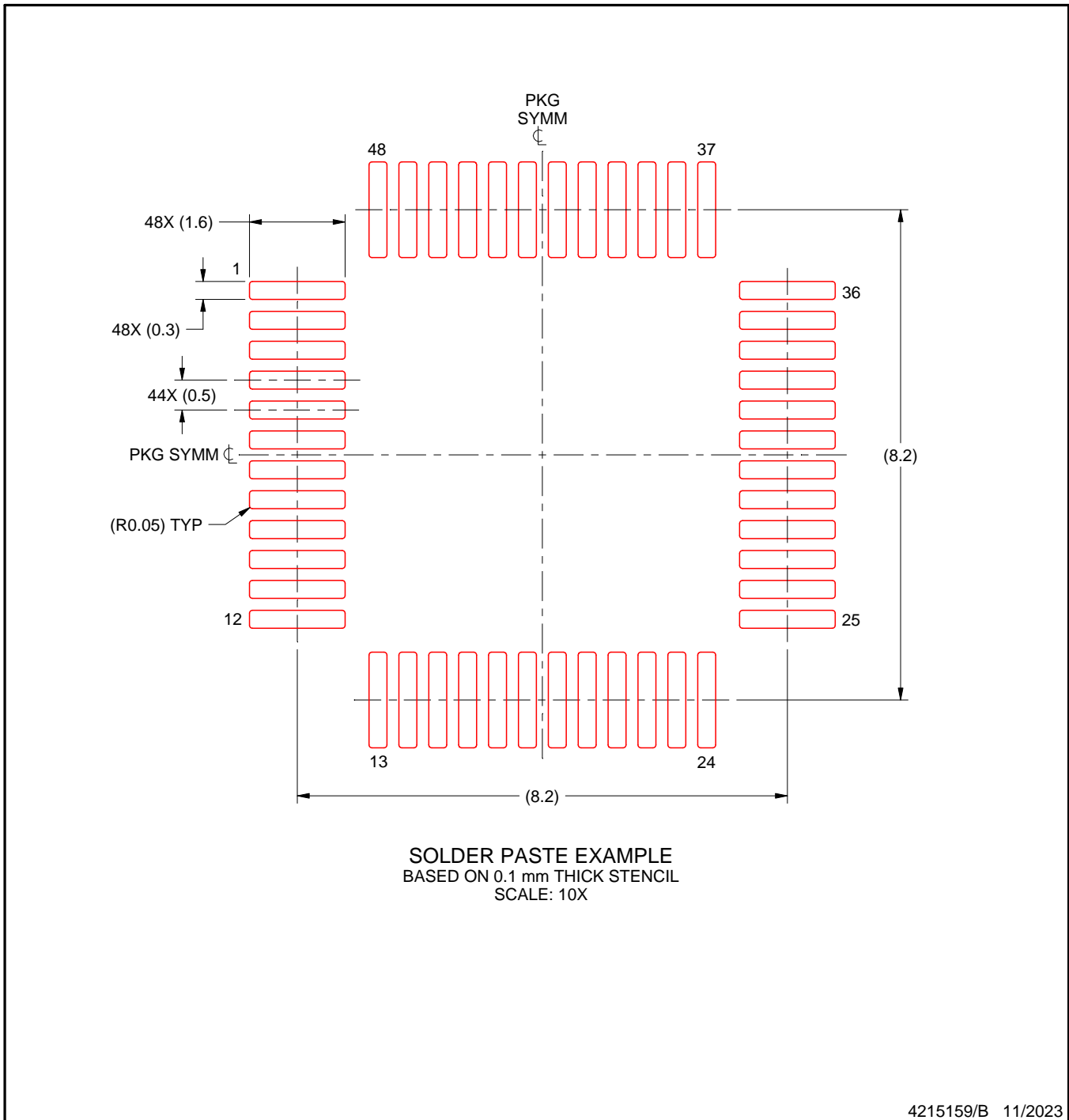
- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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