DCH01 Series, 1-W, 3000-V<sub>DC</sub> Isolated, Unregulated DC/DC Converter Modules

1 Features
- 3-kVDC Isolation (operational): 1-second test
- Continuous voltage applied across isolation barrier: 60 VDC / 42.5 VAC
- UL60950 certified product
- Industry standard footprint
- JEDEC 7-pin SIP package
- Input voltage: 5 V ±10%
- Output voltage: ±5 V, ±12 V, or ±15 V
- Supports series operation for higher output voltage
- Supports parallel operation for higher output power
- Up to 78% efficiency

2 Applications
- Point-of-use power conversion
- Ground loop elimination
- Data acquisition
- Industrial control and instrumentation
- Test equipment

3 Description
The DCH010505, DCH010512, and DCH010515 devices are a family of miniature, 1-W, 3-kV isolated DC/DC converters. Featured in an industry standard 7-pin SIP package, the DCH01 series requires minimal external components, reducing board space. The DCH01 series provides both single and dual split-supply outputs.

The use of a highly integrated package design results in highly reliable products with high power densities. High performance and small size makes the DCH01 suitable for a wide range of applications including signal chain applications and ground loop elimination.

WARNING: This product has operational isolation and is intended for signal isolation only. It must not be used as a part of a safety isolation circuit requiring reinforced isolation. See definitions in Feature Description.

Device Information<sup>(1)</sup>

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>PACKAGE</th>
<th>BODY SIZE (NOM)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCH0105xx</td>
<td>EDJ-Single (7)</td>
<td>19.50 mm × 10.00 mm</td>
</tr>
<tr>
<td></td>
<td>EDJ-Dual (7)</td>
<td>19.50 mm × 10.00 mm</td>
</tr>
</tbody>
</table>

(1) For all available packages, see the orderable addendum at the end of the data sheet.

---

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.
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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (November 2016) to Revision J Page

• Added links to Applications .................................................... 1

Changes from Revision H (January 2009) to Revision I Page

• Added ESD Ratings table, Feature Description section, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section ................................................................. 1
• Changed Ordering Information to Device Comparison Tables ................................................................. 3
• Deleted Wave soldering temperature (260°C maximum) from Absolute Maximum Ratings table ................................................................. 4
• Added Thermal Information table ................................................................. 4
• Added Isolation subsection to the Feature Description ................................................................. 10
5 Device Comparison Tables

Table 1. DCH01 Products

<table>
<thead>
<tr>
<th>MODEL</th>
<th>INPUT VOLTAGE (V)</th>
<th>OUTPUT VOLTAGE (V)</th>
<th>OUTPUT CURRENT (mA)</th>
<th>OUTPUT POWER (W)</th>
<th>ISOLATION VOLTAGE (kVDC)</th>
<th>PACKAGE-LEAD</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCH010505S</td>
<td>5 ± 10%</td>
<td>5</td>
<td>200</td>
<td>1</td>
<td>3</td>
<td>SIP-7</td>
</tr>
<tr>
<td>DCH010512S</td>
<td>5 ± 10%</td>
<td>12</td>
<td>83</td>
<td>1</td>
<td>3</td>
<td>SIP-7</td>
</tr>
<tr>
<td>DCH010515S</td>
<td>5 ± 10%</td>
<td>15</td>
<td>67</td>
<td>1</td>
<td>3</td>
<td>SIP-7</td>
</tr>
<tr>
<td>DCH010505D</td>
<td>5 ± 10%</td>
<td>±5</td>
<td>±100</td>
<td>1</td>
<td>3</td>
<td>SIP-7</td>
</tr>
<tr>
<td>DCH010512D</td>
<td>5 ± 10%</td>
<td>±12</td>
<td>±42</td>
<td>1</td>
<td>3</td>
<td>SIP-7</td>
</tr>
<tr>
<td>DCH010515D</td>
<td>5 ± 10%</td>
<td>±15</td>
<td>±33</td>
<td>1</td>
<td>3</td>
<td>SIP-7</td>
</tr>
</tbody>
</table>

Table 2. Part Numbering Scheme

<table>
<thead>
<tr>
<th>PRODUCT LINE</th>
<th>POWER</th>
<th>INPUT VOLTAGE</th>
<th>OUTPUT VOLTAGE</th>
<th>SINGLE/DUAL</th>
<th>PACKAGE</th>
<th>PIN CONFIG</th>
<th>TRANSPORT MEDIA</th>
</tr>
</thead>
<tbody>
<tr>
<td>DCH</td>
<td>01</td>
<td>05</td>
<td>05</td>
<td>S</td>
<td>N</td>
<td>7</td>
<td>Blank = Tray</td>
</tr>
<tr>
<td>H = 3 kV, unregulated output</td>
<td>01 = 1 W</td>
<td>05 = 5 V</td>
<td>05 = 5 V</td>
<td>S = Single</td>
<td>D = Dual</td>
<td>N = SIP Thru-hole</td>
<td>7 = SIP-7</td>
</tr>
</tbody>
</table>

6 Pin Configuration and Functions

6 Pin Configuration and Functions

Pin Functions

<table>
<thead>
<tr>
<th>PIN NAME</th>
<th>EDJ (SINGLE)</th>
<th>EDJ (DUAL)</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>–V&lt;sub&gt;I&lt;/sub&gt;</td>
<td>2</td>
<td>2</td>
<td>I</td>
<td>Input side common</td>
</tr>
<tr>
<td>+V&lt;sub&gt;I&lt;/sub&gt;</td>
<td>1</td>
<td>1</td>
<td>I</td>
<td>Voltage input</td>
</tr>
<tr>
<td>–V&lt;sub&gt;O&lt;/sub&gt;</td>
<td>5</td>
<td>5</td>
<td>O</td>
<td>–Voltage out</td>
</tr>
<tr>
<td>+V&lt;sub&gt;O&lt;/sub&gt;</td>
<td>7</td>
<td>7</td>
<td>O</td>
<td>+Voltage out</td>
</tr>
<tr>
<td>COM</td>
<td>—</td>
<td>6</td>
<td>—</td>
<td>Output side common</td>
</tr>
</tbody>
</table>
7  Specifications

7.1  Absolute Maximum Ratings
over operating free-air temperature range (unless otherwise noted)\(^{(1)}\)

<table>
<thead>
<tr>
<th></th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input voltage (5-V input models)</td>
<td></td>
<td>7</td>
<td>V</td>
</tr>
<tr>
<td>Storage temperature, (T_{stg})</td>
<td>-55</td>
<td>125</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2  ESD Ratings

<table>
<thead>
<tr>
<th>(V_{(ESD)}) Electrostatic discharge</th>
<th>VALUE</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(^{(1)})</td>
<td>±2000</td>
<td>V</td>
</tr>
<tr>
<td>Charged-device model (CDM), per JEDEC specification JESD22-C101(^{(2)})</td>
<td>±250</td>
<td>V</td>
</tr>
</tbody>
</table>

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3  Recommended Operating Conditions
over operating free-air temperature range (unless otherwise noted)

<table>
<thead>
<tr>
<th>(+V_i) Input voltage</th>
<th>MIN</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>(T_A) Operating ambient temperature</td>
<td>-40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

7.4  Thermal Information

<table>
<thead>
<tr>
<th>THERMAL METRIC(^{(1)})</th>
<th>DCH01 SERIES</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EDJ (SIP-SINGLE)</td>
<td>EDJ (SIP-DUAL)</td>
</tr>
<tr>
<td>(R_{JA}) Junction-to-ambient thermal resistance</td>
<td>66</td>
<td>66</td>
</tr>
<tr>
<td>(\psi_{JT}) Junction-to-top characterization parameter</td>
<td>3</td>
<td>3</td>
</tr>
<tr>
<td>(\psi_{JB}) Junction-to-board characterization parameter</td>
<td>66</td>
<td>66</td>
</tr>
</tbody>
</table>

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
7.5 Electrical Characteristics
At $T_A = 25^\circ C$ and $V_I = 5$ V (unless otherwise noted)

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_I$ Input voltage</td>
<td>All devices nominal</td>
<td>5</td>
<td></td>
<td></td>
<td>V</td>
</tr>
<tr>
<td>$V_{NOM}$ Output voltage</td>
<td>100% load$^{(1)}$</td>
<td>DCH010505S</td>
<td>5.1</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010505D</td>
<td>±5.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512S</td>
<td>12.4</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512D</td>
<td>±12.5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010515S</td>
<td>15.2</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010515D</td>
<td>±15.3</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Load regulation</td>
<td>10% to 100% load$^{(2)}$</td>
<td>DCH010505S</td>
<td>10%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010505D</td>
<td>9%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512S</td>
<td>6%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512D</td>
<td>5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010515S</td>
<td>6%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010515D</td>
<td>5%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output ripple</td>
<td>100% LOAD$^{(1)}$</td>
<td>DCH010505S</td>
<td>35</td>
<td></td>
<td>mVpp</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010505D</td>
<td>20</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512S</td>
<td>18</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512D</td>
<td>19</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010515S</td>
<td>31</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010515D</td>
<td>22</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_O$ Input current</td>
<td>No load; 0% load</td>
<td>DCH010505x</td>
<td>60</td>
<td></td>
<td>mA</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512x</td>
<td>65</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010515x</td>
<td>65</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Efficiency</td>
<td>100% load$^{(1)}$</td>
<td>DCH010505x</td>
<td>72%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512S</td>
<td>74%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512D</td>
<td>75%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010515S</td>
<td>75%</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010515D</td>
<td>76%</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_{ISO}$ Barrier capacitance</td>
<td>DCH010505x &amp; DCH010515x</td>
<td>3</td>
<td></td>
<td></td>
<td>pF</td>
</tr>
<tr>
<td></td>
<td></td>
<td>DCH010512x</td>
<td>4</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output power</td>
<td>100% full load</td>
<td></td>
<td></td>
<td></td>
<td>W</td>
</tr>
<tr>
<td></td>
<td>Over current duration$^{(3)}$</td>
<td></td>
<td>1</td>
<td>sec</td>
<td></td>
</tr>
<tr>
<td>Isolation voltage</td>
<td>$V_I$ at 10% load – $V_O$ at 100% load</td>
<td></td>
<td>−10%</td>
<td>10%</td>
<td></td>
</tr>
<tr>
<td>Line regulation</td>
<td>1% change in $V_I$</td>
<td>3.5</td>
<td></td>
<td></td>
<td>kVDC</td>
</tr>
<tr>
<td>Switching frequency ($f_{SW}$)</td>
<td></td>
<td>70</td>
<td></td>
<td>kHz</td>
<td></td>
</tr>
<tr>
<td>Calculated reliability</td>
<td>Per Telcordia SR-332, 50% stress, $T_A = 40^\circ C$</td>
<td>Single output</td>
<td>18</td>
<td></td>
<td>FITS</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Dual output</td>
<td>22</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

(1) 100% load current = 1 W / $V_{NOM}$ typical.
(2) Load regulation = ($V_O$ at 10% load – $V_O$ at 100% load) / $V_O$ at 100% load.
(3) This converter does not have continuous over-current protection.
7.6 Typical Characteristics

at $T_A = 25^\circ C$ and $V_{IN} = 5$ V (unless otherwise noted)
## Typical Characteristics (continued)

at \( T_A = 25°C \) and \( V_{IN} = 5 \text{ V} \) (unless otherwise noted)

### Efficiency (%)

<table>
<thead>
<tr>
<th>Load Current (mA)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>10</td>
</tr>
<tr>
<td>10</td>
<td>20</td>
</tr>
<tr>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>30</td>
<td>40</td>
</tr>
<tr>
<td>40</td>
<td>50</td>
</tr>
<tr>
<td>50</td>
<td>60</td>
</tr>
<tr>
<td>60</td>
<td>70</td>
</tr>
<tr>
<td>70</td>
<td>80</td>
</tr>
</tbody>
</table>

#### Output 1 Load Current

- 42mA
- 21mA
- 4mA

### Load Voltage (V)

<table>
<thead>
<tr>
<th>Load Current (mA)</th>
<th>Output Voltage (V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>13.2</td>
</tr>
<tr>
<td>10</td>
<td>13.0</td>
</tr>
<tr>
<td>20</td>
<td>12.8</td>
</tr>
<tr>
<td>30</td>
<td>12.6</td>
</tr>
<tr>
<td>40</td>
<td>12.4</td>
</tr>
<tr>
<td>50</td>
<td>12.2</td>
</tr>
</tbody>
</table>

#### Output 1 Load Current

- 42mA
- 21mA
- 4mA

### Ripple Voltage (mV)

<table>
<thead>
<tr>
<th>Load Current (mA)</th>
<th>Ripple Voltage (mV)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>50</td>
</tr>
<tr>
<td>10</td>
<td>40</td>
</tr>
<tr>
<td>20</td>
<td>30</td>
</tr>
<tr>
<td>30</td>
<td>20</td>
</tr>
<tr>
<td>40</td>
<td>10</td>
</tr>
<tr>
<td>50</td>
<td>0</td>
</tr>
</tbody>
</table>

#### Output 1 Load Current

- 42mA
- 21mA
- 4mA

---

**Figure 7.** DCH010512S Efficiency

**Figure 8.** DCH010512D Efficiency

**Figure 9.** DCH010512S Load Regulation

**Figure 10.** DCH010512D Load Regulation

**Figure 11.** DCH010512S Ripple Voltage

**Figure 12.** DCH010512D Ripple Voltage
Typical Characteristics (continued)

at $T_A = 25^\circ C$ and $V_{IN} = 5$ V (unless otherwise noted)

**Figure 13. DCH010515S Efficiency**

**Figure 14. DCH010515D Efficiency**

**Figure 15. DCH010515S Load Regulation**

**Figure 16. DCH010515D Load Regulation**

**Figure 17. DCH010515S Ripple Voltage**

**Figure 18. DCH010515D Ripple Voltage**
Typical Characteristics (continued)

at $T_A = 25^\circ$C and $V_{IN} = 5$ V (unless otherwise noted)

![Figure 19. Safe Operating Area (All DCH0105 Products)](image-url)
8 Detailed Description

8.1 Overview
The DCH01 series of DC/DC converters are 100% production tested at 3.5 kVDC for 1 second. The isolation test voltage represents an operational isolation to transient voltages and must not be relied upon for safety isolation.

The continuous voltage that can be applied across the DCH01 during normal operation must be < 60 VDC (within SELV limits).

8.1.1 Repeated High-Voltage Isolation Testing
Repeated high-voltage isolation testing can degrade the isolation capability of the DCH01.

8.2 Functional Block Diagrams

![Single-Output Block Diagram](image1)

![Dual-Output Block Diagram](image2)

8.3 Feature Description

8.3.1 Isolation
Underwriters Laboratories (UL)™ defines several classes of isolation that are used in modern power supplies.

Safety extra low voltage (SELV) is defined by UL (UL1950 E199929) as a secondary circuit which is so designated and protected that under normal and single fault conditions the voltage between any two accessible parts, or between an accessible part and the equipment earthing terminal for operational isolation does not exceed steady state 42-V peak or 60 V\text{DC} for more than 1 second.

8.3.1.1 Operation or Functional Isolation
Operational or functional isolation is defined by the use of a high-potential (hipot) test only. Typically, this isolation is defined as the use of insulated wire in the construction of the transformer as the primary isolation barrier. The hipot one-second duration test (dielectric voltage, withstand test) is a production test used to verify that the isolation barrier is functioning. Products with operational isolation must never be used as an element in a safety-isolation system.
Feature Description (continued)

8.3.1.2 Basic or Enhanced Isolation

Basic or enhanced isolation is defined by specified creepage and clearance limits between the primary and secondary circuits of the power supply. Basic isolation is the use of an isolation barrier in addition to the insulated wire in the construction of the transformer. Input and output circuits must also be physically separated by specified distances.

8.3.1.3 Continuous Voltage

For a device that has no specific safety agency approvals (operational isolation), the continuous voltage that can be applied across the part in normal operation is less than 42.4 V\textsubscript{RMS} or 60 V\textsubscript{DC}. Ensure that both input and output voltages maintain normal SELV limits. The isolation test voltage represents a measure of immunity to transient voltages.

\begin{shaded}
WARNING
Do not use the device as an element of a safety isolation system when SELV is exceeded.
\end{shaded}

If the device is expected to function correctly with more than 42.4 V\textsubscript{RMS} or 60 V\textsubscript{DC} applied continuously across the isolation barrier, then the circuitry on both sides of the barrier must be regarded as operating at an unsafe voltage. Further isolation or insulation systems must form a barrier between these circuits and any user-accessible circuitry according to safety standard requirements.

8.3.1.4 Isolation Voltage

Hipot test, flash-tested, withstand voltage, proof voltage, dielectric withstand voltage, and isolation test voltage are all terms that relate to the same thing: a test voltage applied for a specified time across a component designed to provide electrical isolation to verify the integrity of that isolation. TI's DCH01 series of dc-dc converters are all 100% production tested at 3.5 kV\textsubscript{DC} for 1 second.

8.3.1.5 Repeated High-Voltage Isolation Testing

Repeated high-voltage isolation testing of a barrier component can degrade the isolation capability, depending on materials, construction, and environment. The DCH01 series of dc-dc converters have toroidal, enameled, wire isolation transformers with no additional insulation between the primary and secondary windings. While a device can be expected to withstand several times the stated test voltage, the isolation capability depends on the wire insulation. Any material, including this enamel (typically polyurethane), is susceptible to eventual chemical degradation when subject to very-high applied voltages. Therefore, strictly limit the number of high-voltage tests and repeated high-voltage isolation testing. However, if it is absolutely required, reduce the voltage by 20% from specified test voltage with a duration limit of 1 second per test.
9 Application and Implementation

NOTE
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI’s customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

9.1.1 Optional Input and Output Filters
DCH01 power modules include internal input and output ceramic capacitors in all their designs. However, some applications require much lower levels of either input reflected or output ripple or noise. This application note describes various filters and design techniques found to be successful in reducing both input and output ripple or noise.

9.1.1.1 Input and Output Capacitors
The easiest way to reduce output ripple and noise is to add one or more ceramic capacitors each with a value of 4.7-µF or greater. Ceramic capacitors must be placed close to the output power terminals. A single 4.7-µF ceramic capacitor reduces the output ripple or noise by 10% to 30%.

Switching regulators draw current from the input line in pulses at their operating frequency. The amount of reflected (input) ripple or noise generated is directly proportional to the equivalent source impedance of the power source including the impedance of any input lines. The addition of a 4.7-µF ceramic capacitor, near the input power pins, reduces reflected conducted ripple or noise by 30% to 50%.

The recommended maximum capacitive load on the output of the DCH01 is 100 µF (non-ceramic).

9.1.1.2 π Filters
If a further reduction in ripple or noise level is required for an application, higher order filters must be used. A π (pi) filter, employing a ferrite bead inductor in series with the input or output terminals of the regulator reduces the ripple or noise by at least 15-20 db (see Figure 22 and Figure 23). Ceramic capacitors are required for the inductor to be effective in reduction of ripple and noise.

These inductors plus ceramic capacitors form an excellent filter because of the rejection at the switching frequency. The placement of this filter is critical. It must be located as close as possible to the input or output pins to be effective. The ferrite bead is small (5.1 mm x 3 mm), easy to use, low cost, and has low dc resistance. Fair-Rite manufactures a surface-mount bead (part number 2773019447) or through hole (part number 2673000701) rated to 5 A. Inductors with a value from 1 µH to 5 µH can be used in place of the ferrite bead inductor.

Figure 22. DCH01 Series π Filter
Application Information (continued)

9.1.2 Start-Up

See Figure 24 for start-up waveforms.

9.1.3 Connecting the DCH01 in Series

It is possible to connect the outputs of multiple DCH01s in series to provide non-standard voltage rails. The outputs of dual output DCH01 versions can also be connected in series to provide 2 × the magnitude of \( V_O \) (as shown in Figure 25). For example, a dual 5-V DCH01 could be connected to provide a 10-V rail.

Figure 23. DCH01 Series \( \pi \) Filter (5 V at 1 W)

Figure 24. Start0up Waveforms

Figure 25. Connecting Dual Outputs in Series
9.1.4 Connecting the DCH01 in Parallel

If the output power from 1 DCH01 is not sufficient, it is possible to parallel the outputs of multiple DCH01s (as shown in Figure 26).

![Diagram showing how to connect multiple DCH01s in parallel.](image-url)
9.2 Typical Application

Figure 27. Typical Application Schematic

9.2.1 Design Requirements
For this design example, use the parameters listed in Table 3 and follow the procedures in the Detailed Design Procedure.

Table 3. Design Example Parameters

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>$+V_I$ (Input voltage)</td>
<td>5 V</td>
</tr>
<tr>
<td>$+V_O$ (Output voltage)</td>
<td>5 V</td>
</tr>
<tr>
<td>$I_{OUT}$ (Output current rating)</td>
<td>200 mA</td>
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</tbody>
</table>

9.2.2 Detailed Design Procedure

9.2.2.1 Input Capacitor
For any DCH01 design, select a 2.2-µF, low-ESR, ceramic input capacitor to ensure a good startup performance.

9.2.2.2 Output Capacitor
For any DCH01 design, select a 4.7-µF, low-ESR, ceramic output capacitor to reduce output ripple.

9.2.3 Application Curves

Figure 28. DCH010505S Efficiency

Figure 29. DCH010505 Start-up Waveforms
10 Power Supply Recommendations

The DCH01 is a switching power supply, and as such can place high peak current demands on the input supply. To avoid the supply falling momentarily during the fast switching pulses, ground and power planes must be used to connect the power to the input of DCH01. If this connection is not possible, then the supplies must be connected in a star formation with the traces made as wide as possible.

11 Layout

11.1 Layout Guidelines

Carefully consider the layout of the PCB in order for the best results to be obtained.

Input and output power and ground planes provide a low-impedance path for the input and output power. For the output, the positive and negative voltage outputs conduct through wide traces to minimize losses.

A good-quality, low-ESR, ceramic capacitor placed as close as practical across the input reduces reflected ripple and ensure a smooth start-up.

The location of the decoupling capacitors in close proximity to their respective pins ensures low losses due to the effects of stray inductance, thus improving the ripple performance. This location is of particular importance to the input decoupling capacitor, because this capacitor supplies the transient current associated with the fast switching waveforms of the power drive circuits.

11.2 Layout Example

![Figure 30. DCH01 Single Output Layout (Component-Side View)](image1)

![Figure 31. DCH01 Single Output Layout (Non-Component-Side View)](image2)
12 Device and Documentation Support

12.1 Related Links
The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

<table>
<thead>
<tr>
<th>PARTS</th>
<th>PRODUCT FOLDER</th>
<th>SAMPLE &amp; BUY</th>
<th>TECHNICAL DOCUMENTS</th>
<th>TOOLS &amp; SOFTWARE</th>
<th>SUPPORT &amp; COMMUNITY</th>
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</tbody>
</table>

12.2 Receiving Notification of Documentation Updates
To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on Alert me to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources
TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks
E2E is a trademark of Texas Instruments.
Underwriters Laboratories (UL) is a trademark of UL LLC.
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12.5 Electrostatic Discharge Caution
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.6 Glossary
SLYZ022 — TI Glossary.
This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.
## PACKAGING INFORMATION

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<th>Orderable Device</th>
<th>Status</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>Package Qty</th>
<th>Eco Plan</th>
<th>Lead finish/ Ball material</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking</th>
<th>Samples</th>
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<td>70</td>
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<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JE709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.
Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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EDJ (R-PDSS-T5) DOUBLE SIDED MODULE

0.770 (19.56) 0.300 (7.62)
0.400 (10.15)
0.085 (2.16)
0.020 (0.51) 0.250 (6.35) 0.025 (0.64)
0.100 (2.54) MAX.
0.300 (7.62) TYP.
0.150 (3.81)
0.050 (1.27)

TOP VIEW

0.830 (21.08) 0.300 (7.62)
0.110 (2.79)
0.100 (2.54) 0.360 (9.14)
0.080 (2.02)

SIDE VIEW

0.050 (1.25) Min. 5 Places
Plated through holes.

PC LAYOUT

NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0.76mm).
D. 3 place decimals are ±0.010 (±0.25mm).
E. Recommended keep out area for user components.
F. Pins are 0.020" (0.51) x 0.025" (0.64).
G. All pins: Material — Copper Alloy
    Finish — Tin (100%) over Nickel plate

4207975-3/C 08/07
EDJ (R-PDSS-T4) DOUBLE SIDED MODULE

**MECHANICAL DATA**

**TOP VIEW**

0.770 (19.56)  
0.400 (10.15)  
0.085 (2.16)  
0.020 (0.51)  
0.100 (2.54)  
0.300 (7.62)  

**SIDE VIEW**

0.300 (7.62) MAX.  
0.250 (6.35) MAX.  
0.025 (0.64) TYP.  
0.050 (1.27)  

**PC LAYOUT**

0.050 (1.25) Min. 4 Places  
Plated through holes.

**NOTES:**

A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0.76mm).
D. 3 place decimals are ±0.010 (±0.25mm).
E. Recommended keep out area for user components.
F. Pins are 0.020” (0.51) x 0.025” (0.64).
G. All pins: Material – Copper Alloy  
Finish – Tin (100%) over Nickel plate
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