



## 216-kHz Digital Audio Interface Transceiver (DIX)

Check for Samples: [DIX9211](#)

### FEATURES

- **Integrated DIX and Signal Routing:**
  - Asynchronous Operation (DIR, DIT)
  - Mux and Routing of PCM Data:
    - I<sup>2</sup>S™, Left-Justified, Right-Justified
  - Multipurpose Input/Output Pins
- **Digital Audio I/F Receiver (DIR):**
  - 24-bit, 216-kHz Capable
  - 50-ps Ultralow Jitter
  - Non-PCM Detection (IEC61937, DTS-CD/LD)
  - 12x S/PDIF Input Ports:
    - 2x Coaxial S/PDIF Inputs
    - 10x Optical S/PDIF Inputs
- **Digital Audio I/F Transmitter (DIT):**
  - 24-Bit, 216-kHz Capable
  - 24-Bit Data Length
  - 48-Bit Channel Status Buffer
  - Synchronous/Asynchronous Operation
- **Routing Function:**
  - Input: 3x PCM, 1x DIR
  - Output: Main Out, Aux Out, DIT
  - Multi-Channel (8-Ch) PCM Routing

### Other Function Features:

- Power Down (Pin and Register Control)
- PCM Port Sampling Frequency Counter
- GPIO and GPO
- OSC for External Crystal (24.576 MHz)
- SPI™, I<sup>2</sup>C™ or Hardware Control Modes
- **Power Supply:**
  - 3.3 V (2.9 V to 3.6 V) for DIX, All Digital
- **Operating Temperature: –40°C to +85°C**
- **Package: 48-Pin LQFP**

### APPLICATIONS

- Home Theater and AVR Equipment
- Television and Soundbars
- Musical Instruments, Recording, and Broadcast
- High-Performance Soundcards

### DESCRIPTION

The DIX9211 is a complete analog and digital front-end for today's multimedia players and recorders.

The DIX9211 integrates an S/PDIF transceiver with up to 12 multiplexed inputs and 3x PCM inputs to allow other audio receivers to be multiplexed along with the analog and S/PDIF signals to a digital signal processor (DSP).



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

| PRODUCT | PACKAGE-LEAD | PACKAGE DESIGNATOR | OPERATING TEMPERATURE RANGE | PACKAGE MARKING | ORDERING NUMBER | TRANSPORT MEDIA, QUANTITY |
|---------|--------------|--------------------|-----------------------------|-----------------|-----------------|---------------------------|
| DIX9211 | LQFP-48      | PT                 | –40°C to +85°C              | DIX9211         | DIX9211PT       | Tray, 250                 |
|         |              |                    |                             |                 | DIX9211PTR      | Tape and Reel, 1000       |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the device product folder on [www.ti.com](http://www.ti.com).

### ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Over operating free-air temperature range (unless otherwise noted).

|                                                              |                                                                                                                                  | DIX9211                                 | UNIT |
|--------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------|------|
| Supply voltage                                               | $V_{CC}, V_{DD}, V_{DDR\bar{X}}$                                                                                                 | –0.3 to +4.0                            | V    |
| Supply voltage differences: $V_{CC}, V_{DD}$                 |                                                                                                                                  | ±0.1                                    | V    |
| Ground voltage differences: AGND, DGND, GND $\bar{R}\bar{X}$ |                                                                                                                                  | ±0.1                                    | V    |
| Digital input voltage                                        | RXIN2, RXIN3, RXIN4/ASCKI0, RXIN5/ABCKI0, RXIN6/ALRCKI0, RXIN7/ADIN0, MC/SCL, MDI/SDA, MDO/ADR, MS/ADR1, $\bar{R}\bar{S}\bar{T}$ | –0.3 to +6.5                            | V    |
|                                                              | MPIO_A0-A3, MPIO_B0-B3, MPIO_C0-C3                                                                                               | –0.3 to +6.5                            | V    |
|                                                              | RXIN0, RXIN1 (For S/PDIF TTL / OPTICAL input)                                                                                    | –0.3 to +6.5                            | V    |
|                                                              | MODE                                                                                                                             | –0.3 to +4.0                            | V    |
| Analog input voltage                                         | RXIN0, RXIN1 (For S/PDIF Coaxial Input Only)                                                                                     | –0.3 to $(V_{DDR\bar{X}} + 0.3) < +4.0$ | V    |
|                                                              | XTI, XTO                                                                                                                         | –0.3 to $(V_{DD} + 0.3) < +4.0$         | V    |
|                                                              | FILT                                                                                                                             | –0.3 to $(V_{CC} + 0.3) < +4.0$         | V    |
| Input current (any pins except supplies)                     |                                                                                                                                  | ±10                                     | mA   |
| Ambient temperature under bias                               |                                                                                                                                  | –40 to +125                             | °C   |
| Storage temperature                                          |                                                                                                                                  | –55 to +150                             | °C   |
| Junction temperature                                         |                                                                                                                                  | +150                                    | °C   |
| Package temperature (reflow, peak)                           |                                                                                                                                  | +260                                    | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

## THERMAL INFORMATION

| THERMAL METRIC <sup>(1)</sup> |                                              | DIX9211    | UNITS |
|-------------------------------|----------------------------------------------|------------|-------|
|                               |                                              | PT PACKAGE |       |
|                               |                                              | 48 PINS    |       |
| $\theta_{JA}$                 | Junction-to-ambient thermal resistance       | 61.0       | °C/W  |
| $\theta_{JCTop}$              | Junction-to-case (top) thermal resistance    | 0.7        |       |
| $\theta_{JB}$                 | Junction-to-board thermal resistance         | 29.6       |       |
| $\psi_{JT}$                   | Junction-to-top characterization parameter   | 18.9       |       |
| $\psi_{JB}$                   | Junction-to-board characterization parameter | 30.0       |       |
| $\theta_{JCbott}$             | Junction-to-case (bottom) thermal resistance | N/A        |       |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

## RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted).

|                                              |                                              | MIN            | NOM    | MAX | UNIT |
|----------------------------------------------|----------------------------------------------|----------------|--------|-----|------|
| DIR analog supply voltage, $V_{CC}$          |                                              | 2.9            | 3.3    | 3.6 | V    |
| ALL digital supply voltage, $V_{DD}$         |                                              | 2.9            | 3.3    | 3.6 | V    |
| Coaxial amplifier supply voltage, $V_{DDRX}$ |                                              | 2.9            | 3.3    | 3.6 | V    |
| Digital input interface level                |                                              | TTL-compatible |        |     |      |
| Digital input/output clock frequency         | DIR, DIT, and Routing sampling frequency     | 7              | 216    |     | kHz  |
|                                              | DIR, DIT, and Routing system clock frequency | 0.896          | 55.296 |     | MHz  |
|                                              | XTI input clock frequency                    | 24.576         |        |     | MHz  |
| Digital output load capacitance              | Except SCKO                                  | 20             |        |     | pF   |
| Digital output load capacitance              | SCKO                                         | 10             |        |     | pF   |
| MODE pin capacitance                         |                                              | 10             |        |     | pF   |
| Operating free-air temperature               |                                              | -40            | +25    | +85 | °C   |

## ELECTRICAL CHARACTERISTICS: GENERAL

All specifications at  $T_A = +25^\circ\text{C}$ , and  $V_{CC} = V_{DD} = V_{DDR\text{X}} = 3.3\text{ V}$ , unless otherwise noted.

| PARAMETER                         |                                                    | TEST CONDITIONS <sup>(1)</sup>                       | DIX9211                                           |                      |                                  | UNIT                 |
|-----------------------------------|----------------------------------------------------|------------------------------------------------------|---------------------------------------------------|----------------------|----------------------------------|----------------------|
|                                   |                                                    |                                                      | MIN                                               | TYP                  | MAX                              |                      |
| DIGITAL INPUT/OUTPUT              |                                                    |                                                      |                                                   |                      |                                  |                      |
| DATA FORMAT                       |                                                    |                                                      |                                                   |                      |                                  |                      |
| Audio data interface format       |                                                    |                                                      | I <sup>2</sup> S, Left-Justified, Right-Justified |                      |                                  |                      |
| Audio data word length            |                                                    |                                                      | 16, 24                                            |                      |                                  | Bits                 |
| Audio data format                 |                                                    |                                                      | MSB first, twos complement                        |                      |                                  |                      |
| f <sub>S</sub>                    | Sampling frequency, DIR                            |                                                      | 7                                                 |                      | 216                              | kHz                  |
|                                   | Sampling frequency, DIT                            |                                                      | 7                                                 |                      | 216                              | kHz                  |
|                                   | Sampling frequency, Routing                        |                                                      | 7                                                 |                      | 216                              | kHz                  |
| INPUT LOGIC                       |                                                    |                                                      |                                                   |                      |                                  |                      |
| V <sub>IH</sub> <sup>(2)(3)</sup> | Input logic level                                  |                                                      | 2.0                                               |                      | 5.5                              | VDC                  |
| V <sub>IL</sub> <sup>(2)(3)</sup> |                                                    |                                                      |                                                   |                      | 0.8                              | VDC                  |
| V <sub>IH</sub> <sup>(4)</sup>    | Input logic level (XTI pin)                        |                                                      | 0.7 V <sub>CC</sub>                               |                      | V <sub>CC</sub>                  | VDC                  |
| V <sub>IL</sub> <sup>(4)</sup>    |                                                    |                                                      |                                                   |                      | 0.3 V <sub>CC</sub>              | VDC                  |
| V <sub>IH</sub> <sup>(5)</sup>    | Input logic level (RXIN0/1 pins)                   |                                                      | 0.7 V <sub>DDR<sub>X</sub></sub>                  |                      | V <sub>DDR<sub>X</sub></sub>     | VDC                  |
| V <sub>IL</sub> <sup>(5)</sup>    |                                                    |                                                      |                                                   |                      | 0.3 V <sub>DDR<sub>X</sub></sub> | VDC                  |
| I <sub>IH</sub> <sup>(2)(4)</sup> | Input logic current                                | V <sub>IN</sub> = V <sub>DD</sub> or V <sub>CC</sub> |                                                   |                      | ±10                              | μA                   |
| I <sub>IL</sub> <sup>(2)(4)</sup> |                                                    | V <sub>IN</sub> = 0 V                                |                                                   |                      |                                  | ±10                  |
| I <sub>IH</sub> <sup>(3)</sup>    | Input logic current ( $\overline{\text{RST}}$ pin) | V <sub>IN</sub> = V <sub>DD</sub>                    |                                                   | 65                   | 100                              | μA                   |
| I <sub>IL</sub> <sup>(3)</sup>    |                                                    | V <sub>IN</sub> = 0 V                                |                                                   |                      |                                  | ±10                  |
| I <sub>IH</sub> <sup>(5)</sup>    | Input logic current (RXIN0/1 pins)                 | V <sub>IN</sub> = V <sub>DDR<sub>X</sub></sub>       |                                                   | 165                  | 300                              | μA                   |
| I <sub>IL</sub> <sup>(5)</sup>    |                                                    | V <sub>IN</sub> = 0 V                                |                                                   |                      | −165                             | −300                 |
| OUTPUT LOGIC                      |                                                    |                                                      |                                                   |                      |                                  |                      |
| V <sub>OH</sub> <sup>(6)</sup>    | Output logic level                                 | I <sub>OUT</sub> = −4 mA                             |                                                   | 2.8                  |                                  | VDC                  |
| V <sub>OL</sub> <sup>(6)</sup>    |                                                    | I <sub>OUT</sub> = 4 mA                              |                                                   |                      |                                  | 0.5                  |
| V <sub>OH</sub> <sup>(7)</sup>    | Output logic level                                 | I <sub>OUT</sub> = −4 mA                             |                                                   | 0.85 V <sub>CC</sub> |                                  | VDC                  |
| V <sub>OL</sub> <sup>(7)</sup>    |                                                    | I <sub>OUT</sub> = 4 mA                              |                                                   |                      |                                  | 0.15 V <sub>CC</sub> |

- (1) PLL lock-up time varies with *ERROR release wait time* setting (Register 23h/ERRWT). Therefore, lock-up time in this table shows the value at ERRWT = 11 as the shortest time setting.
- (2) Pins: MPIO\_A0-A3, MPIO\_B0-B3, MPIO\_C0-C3, RXIN2-RXIN7, MC/SCL, MDI/SDA, MDO/ADR0, MS/ADR1
- (3) Pin:  $\overline{\text{RST}}$
- (4) Pin: XTI
- (5) Pins: RXIN0, RXIN1. Input impedance of RXIN0 and RXIN1 is 20 k $\Omega$  (typical). COAX amplifiers are powered on by Register 34h/RX0DIS and RX1DIS = 0. At power down by Register 34h/RX0DIS and RX1DIS = 1 (default), RXIN0 and RXIN1 are internally tied high.
- (6) Pins: MPIO\_A0-A3, MPIO\_B0-B3, MPIO\_C0-C3, SCKO, BCK, LRCK, DOUT, MPO0-1, ERROR/INT0, NPCM/INT1.
- (7) Pin: XTO.

**ELECTRICAL CHARACTERISTICS: GENERAL (continued)**

All specifications at  $T_A = +25^{\circ}\text{C}$ , and  $V_{CC} = V_{DD} = V_{DDR\bar{X}} = 3.3\text{ V}$ , unless otherwise noted.

| PARAMETER                                   |                       | TEST CONDITIONS <sup>(1)</sup>                                 | DIX9211 |     |     | UNIT |    |
|---------------------------------------------|-----------------------|----------------------------------------------------------------|---------|-----|-----|------|----|
|                                             |                       |                                                                | MIN     | TYP | MAX |      |    |
| POWER-SUPPLY REQUIREMENTS                   |                       |                                                                |         |     |     |      |    |
| V <sub>CC</sub>                             | Voltage range         |                                                                | 2.9     | 3.3 | 3.6 | VDC  |    |
| V <sub>DD</sub>                             |                       |                                                                | 2.9     | 3.3 | 3.6 | VDC  |    |
| V <sub>DDR<sub>X</sub></sub>                |                       |                                                                | 2.9     | 3.3 | 3.6 | VDC  |    |
| I <sub>CC</sub>                             | Supply current        | f <sub>S</sub> = 48 kHz / DIR, f <sub>S</sub> = 48 kHz / DIT   | 4.5     |     |     | mA   |    |
|                                             |                       | f <sub>S</sub> = 192 kHz / DIR, f <sub>S</sub> = 192 kHz / DIT | 7       |     |     | 13   | mA |
|                                             |                       | Full power down, $\overline{\text{RST}}$ = low                 | 150     |     |     | 350  | μA |
| I <sub>DD</sub>                             | Supply current        | f <sub>S</sub> = 48 kHz / DIR, f <sub>S</sub> = 48 kHz / DIT   | 12      |     |     | mA   |    |
|                                             |                       | f <sub>S</sub> = 192 kHz / DIR, f <sub>S</sub> = 192 kHz / DIT | 26      |     |     | 38   | mA |
|                                             |                       | Full power down, $\overline{\text{RST}}$ = low                 | 150     |     |     | 350  | μA |
| I <sub>DDR<sub>X</sub></sub> <sup>(8)</sup> | Supply current        | f <sub>S</sub> = 48 kHz / DIR, f <sub>S</sub> = 48 kHz / DIT   | 3.2     |     |     | mA   |    |
|                                             |                       | f <sub>S</sub> = 192 kHz / DIR, f <sub>S</sub> = 192 kHz / DIT | 3.2     |     |     | 4.8  | mA |
|                                             |                       | Full power down, $\overline{\text{RST}}$ = low                 | 0       |     |     | 30   | μA |
|                                             | Power dissipation     | f <sub>S</sub> = 48 kHz / DIR, f <sub>S</sub> = 48 kHz / DIT   | 75      |     |     | mW   |    |
|                                             |                       | f <sub>S</sub> = 192 kHz / DIR, f <sub>S</sub> = 192 kHz / DIT | 120     |     |     | mW   |    |
|                                             |                       | Full power down, $\overline{\text{RST}}$ = low                 | 1.0     |     |     | mW   |    |
| TEMPERATURE RANGE                           |                       |                                                                |         |     |     |      |    |
|                                             | Operating temperature |                                                                | –40     |     |     | +85  | °C |

(8) Two coaxial amplifiers are powered on by Register 34h/RX1DIS and Register 34h/RX0DIS.

## ELECTRICAL CHARACTERISTICS: Digital Audio I/F Receiver (DIR)

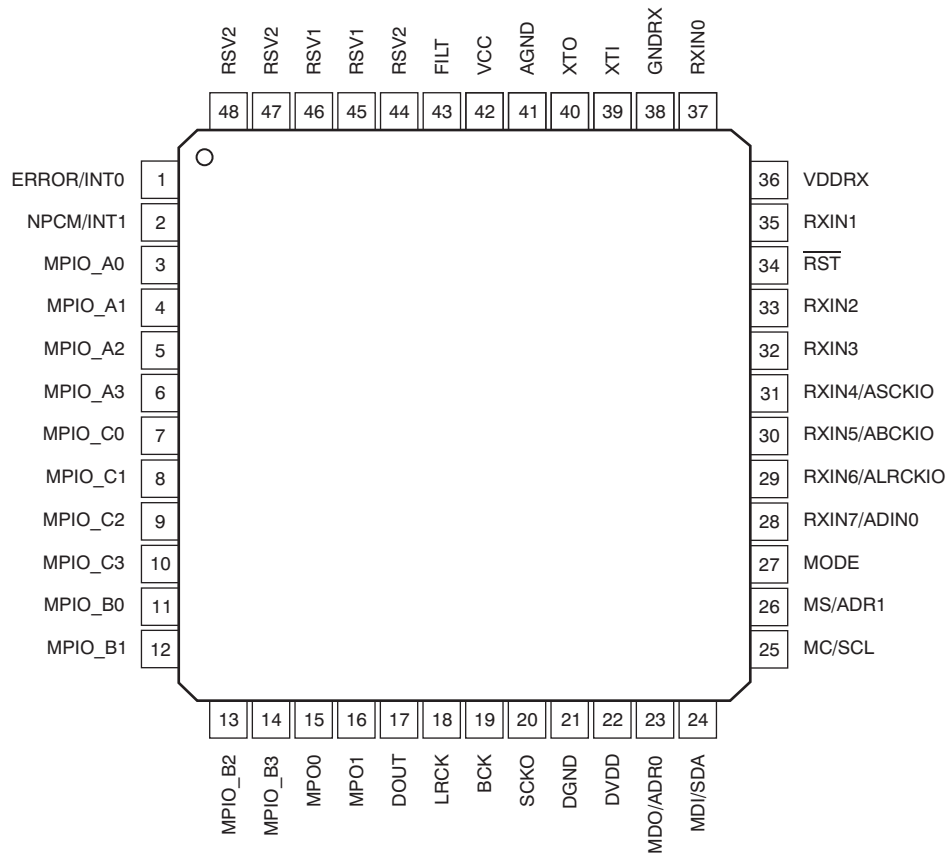
All specifications at  $T_A = +25^\circ\text{C}$ , and  $V_{CC} = V_{DD} = V_{DDR} = 3.3\text{ V}$ , unless otherwise noted.

| PARAMETER                                      | TEST CONDITIONS                                                            | DIX9211            |        |        | UNIT            |
|------------------------------------------------|----------------------------------------------------------------------------|--------------------|--------|--------|-----------------|
|                                                |                                                                            | MIN                | TYP    | MAX    |                 |
| DIR, COAXIAL INPUT AMPLIFIER (RXIN0 and RXIN1) |                                                                            |                    |        |        |                 |
| Input resistance                               |                                                                            |                    | 20     |        | kΩ              |
| Input voltage                                  |                                                                            | 0.2                |        |        | V <sub>PP</sub> |
| Input hysteresis                               |                                                                            |                    | 50     |        | mV              |
| Input sampling frequency                       |                                                                            | 7                  |        | 216    | kHz             |
| DIR, BIPHASE SIGNAL INPUT and PLL              |                                                                            |                    |        |        |                 |
| Input biphase sampling frequency range         | Normal mode                                                                | 28                 |        | 108    | kHz             |
|                                                | Wide mode                                                                  | 7                  |        | 216    | kHz             |
| Input sampling frequency accuracy              | IEC60958-3 (2003-01)                                                       | Level III (±12.5%) |        |        |                 |
| Jitter tolerance                               | IEC60958-3 (2003-01)                                                       | IEC60958-3         |        |        |                 |
| PLL lock up time <sup>(1)</sup>                | From biphase signal detection to error out release (ERROR = L)             |                    |        | 100    | ms              |
| DIR, RECOVERED CLOCK and DATA                  |                                                                            |                    |        |        |                 |
| Serial audio data width                        |                                                                            | 16                 |        | 24     | Bits            |
| System clock frequency                         | 128f <sub>S</sub>                                                          | 0.896              |        | 27.648 | MHz             |
|                                                | 256f <sub>S</sub>                                                          | 1.792              |        | 55.296 | MHz             |
|                                                | 512f <sub>S</sub>                                                          | 3.584              |        | 55.296 | MHz             |
| Bit clock frequency                            | 64f <sub>S</sub>                                                           | 0.448              |        | 13.824 | MHz             |
| LR clock frequency                             | f <sub>S</sub>                                                             | 7                  |        | 216    | kHz             |
| System clock jitter                            | f <sub>S</sub> = 48 kHz, SCKO = 256f <sub>S</sub> , measured period jitter |                    | 50     | 100    | ps, rms         |
| System clock duty cycle                        | 50% reference                                                              | ±5                 |        | ±5     | %               |
| DIT                                            |                                                                            |                    |        |        |                 |
| Output biphase sampling frequency              |                                                                            | 7                  |        | 216    | kHz             |
| Input system clock frequency                   | 128f <sub>S</sub>                                                          | 0.896              |        | 27.648 | MHz             |
|                                                | 256f <sub>S</sub>                                                          | 1.792              |        | 55.296 | MHz             |
|                                                | 512f <sub>S</sub>                                                          | 3.584              |        | 55.296 | MHz             |
| Input bit clock frequency                      | 64f <sub>S</sub>                                                           | 0.448              |        | 13.824 | MHz             |
| Input LR clock frequency                       | f <sub>S</sub>                                                             | 7                  |        | 216    | kHz             |
| OSCILLATOR CIRCUIT, XTI and XMCKO CLOCK        |                                                                            |                    |        |        |                 |
| XTI source clock frequency                     |                                                                            |                    | 24.576 |        | MHz             |
| Frequency accuracy                             |                                                                            | −100               |        | 100    | ppm             |
| XTI input clock duty cycle                     |                                                                            | 45                 |        | 55     | %               |
| XMCKO frequency                                |                                                                            |                    | 24.576 |        | MHz             |
| XMCKO output duty cycle                        | 50% reference                                                              | ±5                 |        | ±5     | %               |
| PCM OUTPUT PORT (SCKO, BCK, LRCK, DOUT)        |                                                                            |                    |        |        |                 |
| System clock frequency                         | 128f <sub>S</sub> / 256f <sub>S</sub> / 512f <sub>S</sub>                  | 0.896              |        | 55.296 | MHz             |
| Bit clock output frequency                     | 64f <sub>S</sub>                                                           | 0.448              |        | 13.824 | MHz             |
| LR clock output frequency                      | f <sub>S</sub>                                                             | 7                  |        | 216    | kHz             |
| ROUTING                                        |                                                                            |                    |        |        |                 |
| System clock frequency                         | 128f <sub>S</sub> / 256f <sub>S</sub> / 512f <sub>S</sub>                  | 0.896              |        | 55.296 | MHz             |
| Bit clock output Frequency                     | 64f <sub>S</sub>                                                           | 0.448              |        | 13.824 | MHz             |
| LR clock output frequency                      | f <sub>S</sub>                                                             | 7                  |        | 216    | kHz             |

(1) PLL lock-up time varies with *ERROR release wait time* setting (Register 23h/ERRWT). Therefore, lock-up time in this table shows the value at ERRWT = 11 as the shortest time setting.

## PIN CONFIGURATIONS

### PT PACKAGE LQFP-48 (TOP VIEW)



## PIN FUNCTIONS

| PIN |            |     |              | DESCRIPTION                                      |
|-----|------------|-----|--------------|--------------------------------------------------|
| NO. | NAME       | I/O | 5-V TOLERANT |                                                  |
| 1   | ERROR/INT0 | O   | No           | DIR Error detection output / Interrupt0 output   |
| 2   | NPCM/INT1  | O   | No           | DIR Non-PCM detection output / Interrupt1 output |
| 3   | MPIO_A0    | I/O | Yes          | Multipurpose I/O, Group A <sup>(1)</sup>         |
| 4   | MPIO_A1    | I/O | Yes          | Multipurpose I/O, Group A <sup>(1)</sup>         |
| 5   | MPIO_A2    | I/O | Yes          | Multipurpose I/O, Group A <sup>(1)</sup>         |
| 6   | MPIO_A3    | I/O | Yes          | Multipurpose I/O, Group A <sup>(1)</sup>         |
| 7   | MPIO_C0    | I/O | Yes          | Multipurpose I/O, Group C <sup>(1)</sup>         |
| 8   | MPIO_C1    | I/O | Yes          | Multipurpose I/O, Group C <sup>(1)</sup>         |
| 9   | MPIO_C2    | I/O | Yes          | Multipurpose I/O, Group C <sup>(1)</sup>         |
| 10  | MPIO_C3    | I/O | Yes          | Multipurpose I/O, Group C <sup>(1)</sup>         |
| 11  | MPIO_B0    | I/O | Yes          | Multipurpose I/O, Group B <sup>(1)</sup>         |
| 12  | MPIO_B1    | I/O | Yes          | Multipurpose I/O, Group B <sup>(1)</sup>         |
| 13  | MPIO_B2    | I/O | Yes          | Multipurpose I/O, Group B <sup>(1)</sup>         |
| 14  | MPIO_B3    | I/O | Yes          | Multipurpose I/O, Group B <sup>(1)</sup>         |
| 15  | MPO0       | O   | No           | Multipurpose output 0                            |

(1) Schmitt trigger input

**PIN FUNCTIONS (continued)**

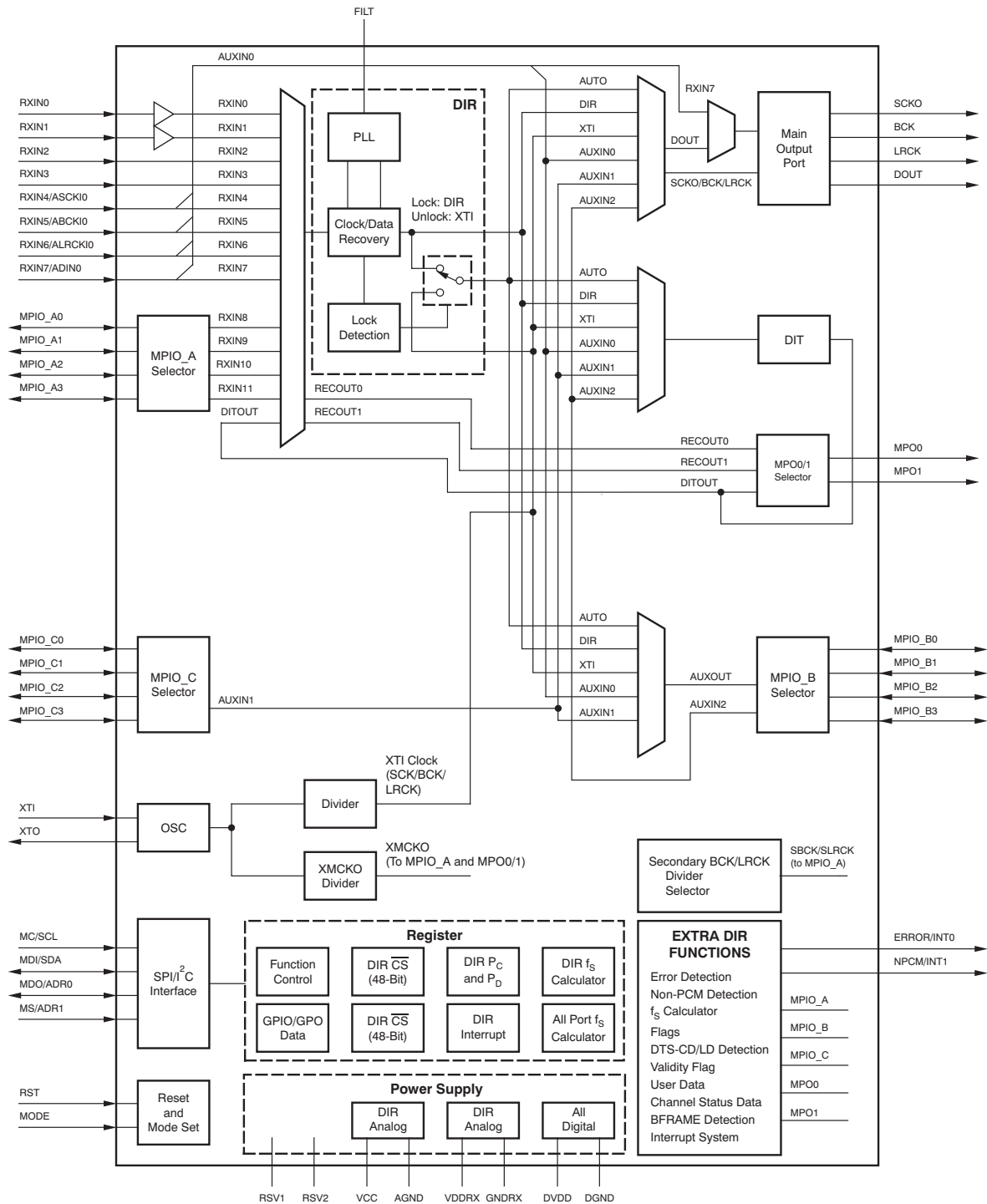
| PIN |                         |     |              | DESCRIPTION                                                                                           |
|-----|-------------------------|-----|--------------|-------------------------------------------------------------------------------------------------------|
| NO. | NAME                    | I/O | 5-V TOLERANT |                                                                                                       |
| 16  | MPO1                    | O   | No           | Multipurpose output 1                                                                                 |
| 17  | DOUT                    | O   | No           | Main output port, serial digital audio data output                                                    |
| 18  | LRCK                    | O   | No           | Main output port, LR clock output                                                                     |
| 19  | BCK                     | O   | No           | Main output port, Bit clock output                                                                    |
| 20  | SCKO                    | O   | No           | Main output port, System clock output                                                                 |
| 21  | DGND                    | –   | –            | Ground, for digital                                                                                   |
| 22  | DVDD                    | –   | –            | Power supply, 3.3 V (typ.), for digital                                                               |
| 23  | MDO/ADRO                | I/O | Yes          | Software control I/F, SPI data output / I <sup>2</sup> C slave address setting <sup>0(2)</sup>        |
| 24  | MDI/SDA                 | I/O | Yes          | Software control I/F, SPI data input / I <sup>2</sup> C data input/output <sup>(2)(3)</sup>           |
| 25  | MC/SCL                  | I   | Yes          | Software control I/F, SPI clock input / I <sup>2</sup> C clock input <sup>(2)</sup>                   |
| 26  | MS/ADR1                 | I   | Yes          | Software control I/F, SPI chip select / I <sup>2</sup> C slave address setting <sup>1(2)</sup>        |
| 27  | MODE                    | I   | No           | Control mode setting, (see the <a href="#">Serial Control Mode</a> section, Control Mode Pin Setting) |
| 28  | RXIN7/ADIN0             | I   | Yes          | Biphase signal, input 7 / AUXIN0, serial audio data input <sup>(2)</sup>                              |
| 29  | RXIN6/ALRCKIO           | I   | Yes          | Biphase signal, input 6 / AUXIN0, LR clock input <sup>(2)</sup>                                       |
| 30  | RXIN5/ABCKIO            | I   | Yes          | Biphase signal, input 5 / AUXIN0, bit clock input <sup>(2)</sup>                                      |
| 31  | RXIN4/ASCKIO            | I   | Yes          | Biphase signal, input 4 / AUXIN0, system clock input <sup>(2)</sup>                                   |
| 32  | RXIN3                   | I   | Yes          | Biphase signal, input 3 <sup>(2)</sup>                                                                |
| 33  | RXIN2                   | I   | Yes          | Biphase signal, input 2 <sup>(2)</sup>                                                                |
| 34  | $\overline{\text{RST}}$ | I   | Yes          | Reset Input, active low <sup>(2)(4)</sup>                                                             |
| 35  | RXIN1                   | I   | Yes          | Biphase signal, input 1, built-in coaxial amplifier                                                   |
| 36  | VDDR <sub>X</sub>       | –   | –            | Power supply, 3.3 V (typ.), for RXIN0 and RXIN1.                                                      |
| 37  | RXIN0                   | I   | Yes          | Biphase signal, input 0, built-in coaxial amplifier                                                   |
| 38  | GNDR <sub>X</sub>       | –   | –            | Ground, for RXIN                                                                                      |
| 39  | XTI                     | I   | No           | Oscillation circuit input for crystal resonator or external XTI clock source input <sup>(5)</sup>     |
| 40  | XTO                     | O   | No           | Oscillation circuit output for crystal resonator                                                      |
| 41  | AGND                    | –   | –            | Ground, for PLL analog                                                                                |
| 42  | VCC                     | –   | –            | Power supply, 3.3 V (typ.), for PLL analog                                                            |
| 43  | FILT                    | O   | No           | External PLL loop filter connection terminal; must connect recommended filter                         |
| 44  | RSV2                    | –   | –            | Reserved; left open                                                                                   |
| 45  | RSV1                    | –   | –            | Reserved; connect to ground                                                                           |
| 46  | RSV1                    | –   | –            | Reserved; connect to ground                                                                           |
| 47  | RSV2                    | –   | –            | Reserved; left open                                                                                   |
| 48  | RSV2                    | –   | –            | Reserved; left open                                                                                   |

(2) Schmitt trigger input

(3) Open-drain configuration in I<sup>2</sup>C mode(4) Onboard pull-down resistor (50 k $\Omega$ , typical)

(5) CMOS Schmitt trigger input

## BLOCK DIAGRAM



## OVERVIEW

### Introduction

The DIX9211 is an analog and digital front-end device for any media player/recorder. It integrates a 216-kHz Digital Audio Transceiver (DIX) and multiple PCM (I<sup>2</sup>S, Left-Justified, Right-Justified) interfaces. Additionally, the device integrates a router that allows any source (DIR or PCM) to be routed to one of three outputs (2x PCM and DIT), thus significantly reducing the number of external components required to route sources to the core DSP.

Each audio interface of the DIX9211 (that is, the DIT and DIR) can operate asynchronously at different sampling rates, allowing an analog source to be sampled at 96 kHz and to be switched over to an S/PDIF source driving encoded data at 48 kHz.

The DIX9211 also features a power down function that can be set via hardware pins and registers, ensuring that the system minimizes power consumption during standby.

### Digital Audio Interface Receiver (DIR)

Up to 12 single-ended S/PDIF input pins are available on the DIX9211 DIR module. Two of the 12 S/PDIF inputs integrate coaxial amplifiers; the other inputs are designed to be directly connected to CMOS sources (up to +5 V), or standard S/PDIF optical modules.

The DIR module outputs the first 48 bits of channel status data from each frame into specific registers that can be read via the control interface. In addition, the DIR can detect non-PCM data (such as compressed multi-channel data) by looking at channel status bits, burst preambles and DTS-CD/LD. When the DIR detects non-PCM audio data, its status can be configured to the NPCM pin (pin 2). Control of pin 2 (NPCM or INT1) is set by register 2Bh.

When the DIR encounters an error (for example, when it loses a lock), an error signal can be configured and sent to the ERROR pin (pin 1). Control of pin 1 (ERROR or INT0) is set by Register 20h. Preamble data P<sub>C</sub> and P<sub>D</sub> (typically used to transmit format information such as Digital Theater Sound, or DTS, or AC-3™ data) can be read from registers Register 3Ah through Register 3Dh. For more information, see the audio data standard IEC61937.

The DIX9211 has two interrupt pins (INT0 and INT1) that are shared with other functions (NPCM and ERROR). The interrupt pins, when configured, can be used for operations such as interrupt transmissions to the DSP (for example, instructing the DSP where the start of the frame is, etc.). Eight different factors can drive the interrupt. For more details, see Register 2Ch and Register 2Dh. The interrupt source can also be stored in a register to be read by a DSP, if required.

When switching from one source to the DIR and vice-versa, additional circuitry in the DIR helps continuity between the crystal clock source and an internal phase-locked loop (PLL). During a clock source switch, a clock transition signal can be output that can then be used by the processor to respond accordingly (such as temporarily muting the output).

An integrated sample rate calculator in the DIR can read and detect both the incoming data rate of the S/PDIF input as well as the sample rate information bits that are within the channel status data.

The DIX9211 has an internal clock divider that changes its system clock (SCK) output rate in order to maintain synchronization between the incoming clock and the receiver (based on the autodetector of the incoming data rate). For example, if the user switches from a 96-kHz source to a 48-kHz source, the divider automatically detects the switch and changes the clock dividing ratio to ensure that the subsequent DSP continues to receive the same system clock.

The DIX9211 also has two output ports for the DIR output. The primary output is available from the Main Port and/or MPIO\_B; the secondary port is available through MPIO\_A. The dividing ratio of BCK and LRCK for the primary output is defined by the DIR. The dividing ratio for the second output (normally taken from MPIO\_A) is defined by Register 32h and Register 33h.

When the PLL is locked, the secondary clock source automatically selects the PLL clock (256f<sub>s</sub>). Otherwise, the XTI clock source is selected. Register 32h should be used for dividing in the lock status (that is, the PLL source). When unlocked, Register 33h should be used (the XTI source).

The DIX9211 has two RECOUT signals that can be routed to the MPO port. The respective sources can be drawn from one of the 12 S/PDIF inputs, or the DIT module.

Channel status, user data, and valid audio data from the S/PDIF stream can be found in various registers or routed to MPIO pins. In addition, the *block start* signal can be routed to an I/O pin, so that any postprocessing DSP can be informed of the start of a frame for decoding data and so forth.

The DIR module in the DIX9211 complies with these digital audio I/F standards:

- S/PDIF
- IEC60958 (formerly IEC958)
- JEITA CPR-1205 (formerly EIAJ CP-1201/340)
- AES3
- EBU Tech 3250 (also known as AES/EBU)

In addition, the DIR Module within the DIX9211 also meets and exceeds jitter tolerance specifications defined by IEC60958-3 for sampling frequencies between 28 kHz and 216 kHz.

### Digital Audio Interface Transmitter (DIT)

The DIT (S/PDIF transmitter) is a relatively simple module. The DIT integrated in the DIX9211 is able to transmit control status and user bits in the data stream, as well as standard 24-bit audio. Channel status, user data, and Audio Valid bits in the stream are configured on incoming MPIO pins.

The DIT complies with the following audio standards:

- S/PDIF
- IEC60958 (formerly IEC958)
- JEITA CPR-1205 (formerly EIAJ CP-1201/340)
- AES3
- EBU Tech 3250 (also known as AES/EBU)

## Auxiliary PCM Audio Input and Output (I/O)

There are up to 3x digital auxiliary (AUX) inputs and one AUX output on the DIX9211. These I/Os are multiplexed and shared with RXIN4 through RXIN7, MPIOB, and MPIOC. Each input and output supports a four-wire digital audio interface that is similar to the I<sup>2</sup>S protocol. Each I/O can support SCK (system clock), BCK (bit clock), LRCK (left/right clock, or word clock) and data transmissions. The audio format supported through the Aux I/O can be configured for I<sup>2</sup>S, 24-bit left-justified (LJ), 24-bit right-justified (RJ), and 16-bit RJ output.

The AUX inputs are designed to be driven in Clock Slave mode. The Aux Output can only operate in Master mode. The system clock can be run from 128f<sub>S</sub>, 256f<sub>S</sub>, and 512f<sub>S</sub>.

## Routing

All 3x AUXIN data and clocks, in addition to data and clocks from the DIR module, are routed to three output ports. The Main Output Port and Aux Output Port (that can be output through MPIO\_B) are both PCM outputs capable of I<sup>2</sup>S, RJ, and LJ. The DIT output is an S/PDIF signal output.

All three outputs have individual multiplexers that can select between the AUXINs or DIR.

## Control Interface

The DIX9211 can be controlled by either SPI or I<sup>2</sup>C (up to a 400-kHz I<sup>2</sup>C bus). However, on startup, the device goes into a default routing mode. Details of this mode are discussed in the [Serial Control Mode](#) section. For certain applications, the default configuration may be suitable, and therefore does not require external programming.

## Multipurpose I/O

The DIX9211 includes 12 MPIO (Multi-Purpose Inputs/Outputs) and two MPO (Multi-Purpose Output) pins. These MPIO/MPO pins can be easily set to different configurations through registers to allow different routing and provide data outputs based on the specific application.

The 12 MPIO pins are divided into three groups (A, B, and C); each group has four pins (MPIO\_Ax, MPIO\_Bx, and MPIO\_Cx).

For example, to access all 12 S/PDIF inputs, the MPIO\_Ax pins can be configured to support S/PDIF RXIN8 and RXIN11. However, if the application requires an additional I<sup>2</sup>S input, then the MPIO\_Ax pins can be configured for an Aux In instead of RXIN8 and RXIN11.

## DIX9211 MODULE DESCRIPTIONS

### Power Supply

The DIX9211 has three power-supply pins and three ground pins. All ground pins (AGND, DGND, and GNDRX) must be connected as closely as possible to the DIX9211. The DIX9211 DVDD and DGND pins are power-supply pins that support all the onboard digital circuitry for the DIX9211. DVDD should be connected to a 3.3-V supply. DVDD drives the internal power-on reset circuit, making it a startup requirement.

VCC and AGND are analog power-supply power pins that support the DIR analog supply rails.

VDDR is a dedicated power supply for the coaxial input amplifiers on pins RXIN0 and RXIN1. It should be connected to a 3.3-V pin. The relative GND pin for this supply is GNDRX. If the coaxial amplifiers are not used (for example, the application only uses optical inputs), then no power supply is required for the VDDR.

Because VCC (3.3 V) is an analog supply (used as part of the power supply for the DIR PLL), care should be taken to ensure minimum noise and ripple are present. 0.1- $\mu$ F ceramic capacitors and 10- $\mu$ F electrolytic capacitors should be used to decouple each supply pin to the respective relative GND.

### Power-Down Function

The DIX9211 has a power-down function that is controlled by the external  $\overline{\text{RST}}$  pin or a power control register.

When the  $\overline{\text{RST}}$  pin is held at GND, the DIX9211 powers down.

When the device is powered down (that is,  $\overline{\text{RST}} = \text{GND}$ ), all register values are cleared and reset to the respective default values. By default, all modules are powered on except for the coaxial amplifier.

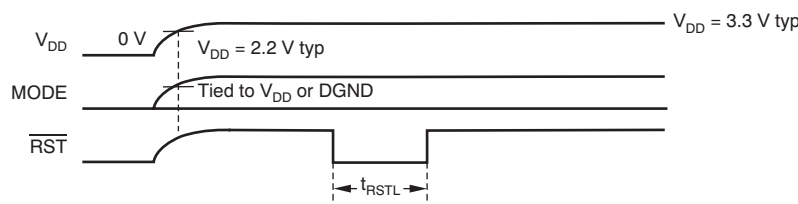
The other option for powering down the device is to use the Power Control Register (Register 40h). The Power Control Register allows selective power down of the DIR, DIT, Coax Amp, and Oscillator circuit without resetting other registers to the respective default modes.

The advantage of using the registers to power down individual modules of the DIX9211 is that the registers retain the respective settings rather than resetting to default.

### System Reset

The DIX9211 has two sources for reset: the internal power-on reset circuit (hereafter called *POR*) and the external reset circuit. Initialization (reset) is done automatically when  $V_{DD}$  exceeds 2.2 V (typ).

When only the onboard POR is to be used, the  $\overline{\text{RST}}$  pin should be connected to  $V_{DD}$  directly. An external pull-up resistor should not be used, because the  $\overline{\text{RST}}$  pin has an internal pull-down resistor (typ 50 k $\Omega$ ). If an external resistor is used, then the reset is not released. The reset sequence is shown in Figure 1.



**Figure 1. Required System Reset Timing**

Table 1 shows the timing requirements to reset the device using the  $\overline{\text{RST}}$  pin.

**Table 1. Timing Requirements for  $\overline{\text{RST}}$  Pin Device Reset**

| SYMBOL            | DESCRIPTION                                                              | MIN | TYP | MAX | UNITS         |
|-------------------|--------------------------------------------------------------------------|-----|-----|-----|---------------|
| $t_{\text{RSTL}}$ | $\overline{\text{RST}}$ pulse width ( $\overline{\text{RST}}$ pin = low) | 1   |     |     | $\mu\text{s}$ |

The condition of each output pins during the device reset is shown in Table 2.

**Table 2. Output Pin Condition During Reset**

| CLASSIFICATION      | PIN NAME                | AT $\overline{\text{RST}} = \text{L}^{(1)}$ |
|---------------------|-------------------------|---------------------------------------------|
| Main Output Port    | SCKO                    | L                                           |
|                     | BCK                     | L                                           |
|                     | LRCK                    | L                                           |
|                     | DOUT                    | L                                           |
| Flag and Status     | ERROR/INT0              | H                                           |
|                     | NPCM/INT1               | L                                           |
| MPIOs and MPOs      | MPIO_A0 through MPIO_A3 | Hi-Z                                        |
|                     | MPIO_B0 through MPIO_B3 | Hi-Z                                        |
|                     | MPIO_C0 through MPIO_C3 | Hi-Z                                        |
|                     | MPO0, MPO1              | L                                           |
| Serial I/F          | MDI/SDA                 | Hi-Z                                        |
|                     | MDO/ADR0                | Hi-Z                                        |
| Oscillation Circuit | XTO                     | Output                                      |
| Coax Input          | RXIN0, RXIN1            | H                                           |

(1) L = low, H = high, Hi-Z = high impedance.

## PCM Audio Interface Format

Each of the modules in the DIX9211 (DIR, DIT, and Aux I/Os) supports these four interface formats:

- 24-bit I<sup>2</sup>S format
- 24-bits Left-Justified format
- 24-bit Right-Justified format
- 16-bit Right-Justified format

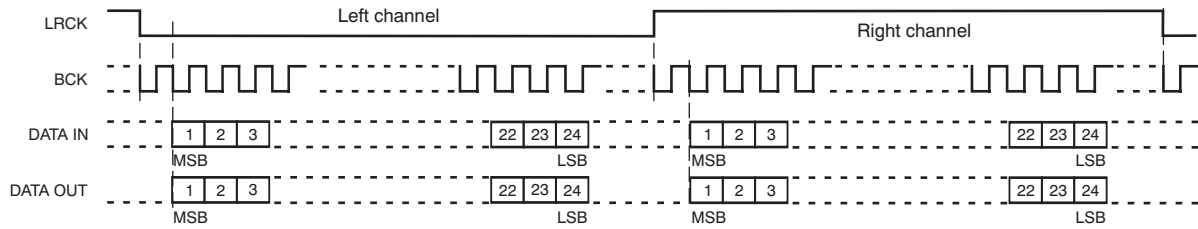
32-bit interfaces are supported for the paths from AUXIN0/1/2 to MainPort/AUXOUT.

All formats are provided twos complement, MSB first. They are selectable through SPI-/I<sup>2</sup>C-accessible registers. The specific control registers are:

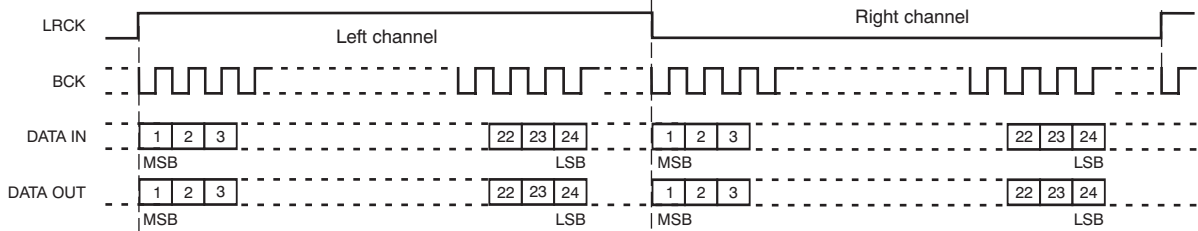
- DIR: RXFMT[2:0]
- DIT: TXFMT[1:0]

Figure 2 illustrates these formats.

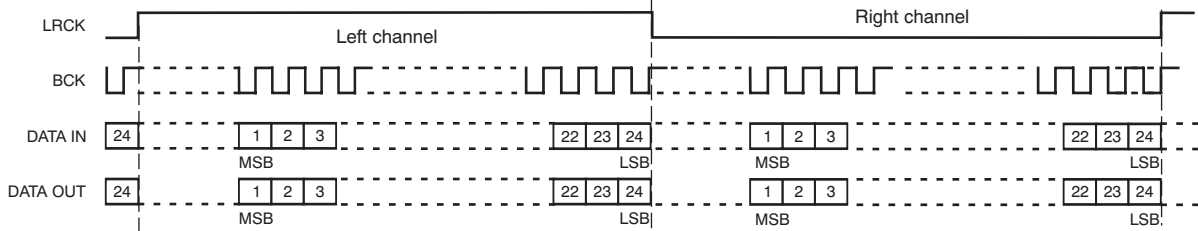
**MSB First, 24-bit I<sup>2</sup>S**



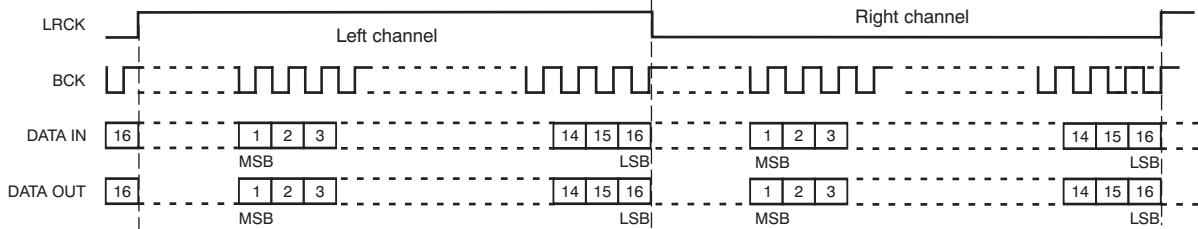
**MSB First, 24-bit Left-Justified**



**MSB First, 24-bit Right-Justified**



**MSB First, 16-bit Right-Justified**



**Figure 2. Audio Data Input/Output Format**

## Digital Audio Interface Receiver (RXIN0 to RXIN11)

### Input Details for Pins RXIN0 Through RXIN11

Up to 12 single-ended S/PDIF input pins are available. Two of the S/PDIF input pins integrate coaxial amplifiers. The other 10 pins are designed to be directly connected to CMOS sources or standard S/PDIF optical modules. Each of the inputs can tolerate 5-V inputs.

The DIR module in the DIX9211 complies with these Digital Audio I/F standards:

- S/PDIF
- IEC60958 (formerly IEC958)
- JEITA CPR-1205 (formerly EIAJ CP-1201/340)
- AES3
- EBU Tech 3250 (also known as AES/EBU)

In addition, the DIR module within the DIX9211 also meets and exceeds jitter tolerance limits as specified by IEC60958-3 for sampling frequencies between 28 kHz and 216 kHz.

Each of the physical connections used for these standards (optical, differential, and single-ended) have different signal levels. Care should be taken to ensure that each of the RXIN pins is not overdriven or underdriven, such as driving a coaxial 0.2-V<sub>PP</sub> signal into a CMOS 3.3-V input.

RXIN0 and RXIN1 integrate coaxial input amplifiers. This architecture means that they can be directly connected to either coaxial input (or RCA/Phono) S/PDIF sources. They can accept a minimum of 0.2V<sub>PP</sub>. They can also be connected to maximum 5-V TTL sources, such as optical receivers. (**NOTE:** Consideration should be made for electrostatic discharge, or ESD, on the input connectors.)

RXIN2 to RXIN11 are 5-V tolerant TTL level inputs. These inputs are typically used as connections to optical receiver modules (known as TOSLINK™ connectors).

RXIN8 through RXIN11 are also part of the MPIO\_A (Multipurpose Input/Output A) group. These I/O pins can either be set as S/PDIF inputs, or reassigned to other functions (see the [MPIO](#) section). To configure MPIO\_A as S/PDIF inputs, set Register MPASEL[1:0] to '00'.

Typically, no additional components are required to connect an optical receiver to any RXIN pin. However, consideration should be given to the output characteristics of the specific receiver modules used, especially if there is a long printed circuit board (PCB) trace between the receiver and the DIX9211 itself.

For differential inputs (such as the AES/EBU standard), differential to single-ended circuitry is required.

### PLL Clock Source (Built-in PLL and VCO) Details

The DIX9211 an has on-chip PLL (including a voltage-controlled oscillator, or VCO) for recovering the clock from the S/PDIF input signal.

The VCO-derived clock is identified as the PLL clock source.

When locked, the onboard PLL generates a system clock that synchronizes with the input biphasic signal. When unlocked, the PLL generates its own free-run clock (from the VCO).

The generated system clocks from the PLL can be set to fixed multiples of the input S/PDIF frequency. Register 30h/PSCK[2:0] can configure the output clock to  $128f_s$ ,  $256f_s$  or  $512f_s$ .

The DIX9211 also has an automatic default output rate that is calculated based on the incoming S/PDIF frequency. This calculation and rate are controlled by Register 30h/PSCKAUTO. In its default mode, the SCK dividing ratio is configured according to these parameters:

- $512f_s$ : 54 kHz and below.
- $256f_s$ : 54 kHz to 108 kHz
- $128f_s$ : 108 kHz and above (or unlocked)

PSCKAUTO takes priority over any settings in PSCK[2:0]. PSCK[2:0] only becomes relevant in the system when the PSCKAUTO Register is set to '0'.

The DIX9211 can decode S/PDIF input signals between sampling frequencies of 7 kHz and 216 kHz for all PSCK[2:0] settings. The relationship between the output clock (SCKO, BCKO, LRCKO) at the PLL source and PSCK[2:0] selection is shown in [Table 3](#).

**Table 3. SCKO, BCKO and LRCKO Frequency Set by PSCK[2:0]**

| OUTPUT CLOCK AT PLL SOURCE |         |       | PSCK[2:0] SETTING |       |       |
|----------------------------|---------|-------|-------------------|-------|-------|
| SCKO                       | BCKO    | LRCKO | PSCK2             | PSCK1 | PSCK0 |
| $128f_s$                   | $64f_s$ | $f_s$ | 0                 | 0     | 0     |
| $256f_s$                   | $64f_s$ | $f_s$ | 0                 | 1     | 0     |
| $512f_s$ <sup>(1)</sup>    | $64f_s$ | $f_s$ | 1                 | 0     | 0     |

(1)  $512f_s$  SCK is only supported at 108 kHz or lower sampling frequency of incoming biphasic signal.

In PLL mode, the output clocks (SCKO, BCKO, LRCKO) are generated from the PLL source clock.

The relationship between the sampling frequencies ( $f_s$ ) of the input S/PDIF signal and the frequency of LRCKO, BCKO, and SCKO are shown in [Table 4](#).

**Table 4. Output Clock Frequency at PLL Lock State**

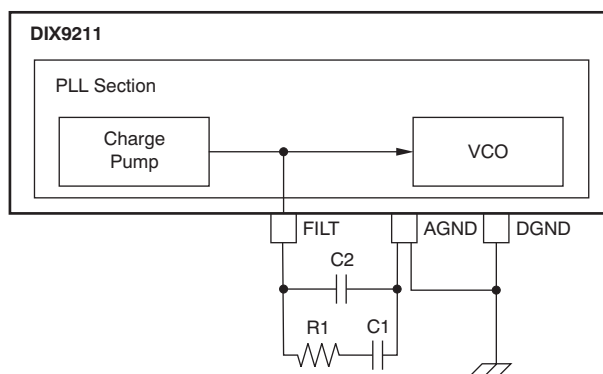
| LRCK       | BCK         | SCK (Depends on PSCK[2:0] Setting) |             |             |
|------------|-------------|------------------------------------|-------------|-------------|
| $f_s$      | $64f_s$     | $128f_s$                           | $256f_s$    | $512f_s$    |
| 8 kHz      | 0.512 MHz   | 1.024 MHz                          | 2.048 MHz   | 4.096 MHz   |
| 11.025 kHz | 0.7056 MHz  | 1.4112 MHz                         | 2.8224 MHz  | 5.6448 MHz  |
| 12 kHz     | 0.768 MHz   | 1.536 MHz                          | 3.072 MHz   | 6.144 MHz   |
| 16 kHz     | 1.024 MHz   | 2.048 MHz                          | 4.096 MHz   | 8.192 MHz   |
| 22.05 kHz  | 1.4112 MHz  | 2.8224 MHz                         | 5.6448 MHz  | 11.2896 MHz |
| 24 kHz     | 1.536 MHz   | 3.072 MHz                          | 6.144 MHz   | 12.288 MHz  |
| 32 kHz     | 2.048 MHz   | 4.096 MHz                          | 8.192 MHz   | 16.384 MHz  |
| 44.1 kHz   | 2.8224 MHz  | 5.6448 MHz                         | 11.2896 MHz | 22.5792 MHz |
| 48 kHz     | 3.072 MHz   | 6.144 MHz                          | 12.288 MHz  | 24.576 MHz  |
| 64 kHz     | 4.096 MHz   | 8.192 MHz                          | 16.384 MHz  | 32.768 MHz  |
| 88.2 kHz   | 5.6448 MHz  | 11.2896 MHz                        | 22.5792 MHz | 45.1584 MHz |
| 96 kHz     | 6.144 MHz   | 12.288 MHz                         | 24.576 MHz  | 49.152 MHz  |
| 128 kHz    | 8.192 MHz   | 16.384 MHz                         | 32.768 MHz  | N/A         |
| 176.4 kHz  | 11.2896 MHz | 22.5792 MHz                        | 45.1584 MHz | N/A         |
| 192 kHz    | 12.288 MHz  | 24.576 MHz                         | 49.152 MHz  | N/A         |

## DIR and PLL Loop Filter Details

The DIX9211 incorporates a PLL for generating clocks synchronized with the input biphase signal (S/PDIF). The onboard PLL requires an external loop filter. The components and configuration shown in [Figure 3](#) and [Table 5](#) are recommended for optimal performance, with these considerations:

- The resistor and capacitors that configure the filter should be located and routed as close as possible to the DIX9211. The external loop filter must be placed on the FILT pins.
- The GND node of the external loop filter must be directly connected with AGND pin of the DIX9211; it must be not combined with other signals.

[Figure 3](#) shows the configuration of the external loop filter and the connection with the DIX9211.



**Figure 3. Loop Filter Connection**

The recommended value of loop filter components is shown in [Table 5](#).

**Table 5. Recommended Value of Loop Filter Components**

| REF. NO.       | RECOMMENDED VALUE | TYPE                        | TOLERANCE |
|----------------|-------------------|-----------------------------|-----------|
| R <sub>1</sub> | 680 Ω             | Metal film or carbon        | ≤ 5%      |
| C <sub>1</sub> | 0.068 μF          | Film or ceramic (CH or C0G) | ≤ 5%      |
| C <sub>2</sub> | 0.0047 μF         | Film or ceramic (CH or C0G) | ≤ 5%      |

## External (XTI) Clocks, Oscillators, and Supporting Circuitry

An external clock source (CMOS or crystal/resonator) is known as the *XTI source*. The XTI source can be either a CMOS logic source, or a crystal resonator (internal circuitry in the DIX9211 can start the crystal resonating). Whichever clock source is used, it must be 24.576 MHz.

The DIX9211 uses the XTI source as a reference clock in order to calculate the sampling frequency of the incoming S/PDIF stream. It is also used as the clock source in XTI clock source mode.

When using a resonator as an XTI source, the following points should be considered:

- The 24.576-MHz resonator should be connected between the XTI and XTO pins
- The resonator should be a fundamental mode type
- A crystal or ceramic resonator can be used as the XTI source
- The values of the load capacitors C<sub>L1</sub> and C<sub>L2</sub> and the current limiting resistor R<sub>d</sub> all depend on the characteristics of the resonator
- No external feedback resistor between the XTI and XTO pins is required, because the resistor is integrated into the device
- No loads other than the resonator should be used on the XTO pin

When using an external oscillation circuit with a CMOS output, the following points should be considered:

- Always supply a 24.576-MHz clock on the XTI pin
- Only 3.3 V is supported on the XTI pin; 5 V is not supported
- XTO should be left floating

Figure 4 illustrates the connections for the XTI and XTO pins for both a resonator connection and an external clock input connection.

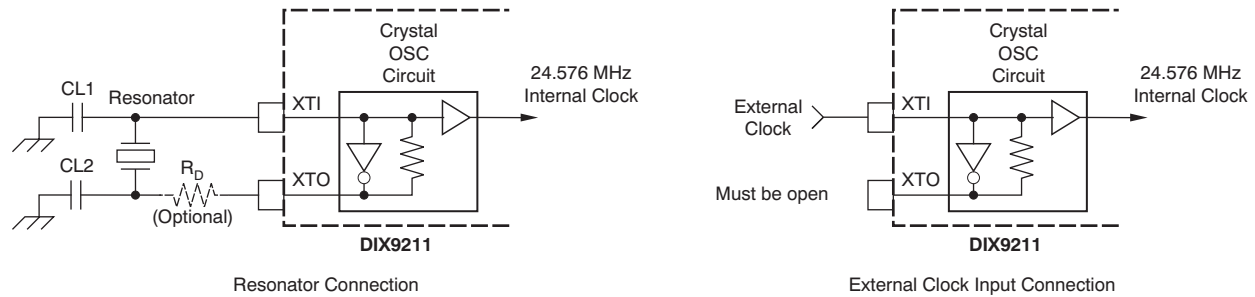


Figure 4. XTI and XTO Connection Diagram

In XTI mode, the output clocks (SCKO, BCKO, and LRCKO) are generated from the XTI source clock.

Register 24h/OSCAUTO controls whether or not the internal oscillator functions while it is not required. When using the DIR as a clock source, the XTI source is not required; thus, the internal oscillator can be switched off. There is a constraint, however, that when the DIR wide mode is being set (for example, in 192-kHz support), the XTI is always used. The sampling frequency calculator also requires the XTI source.

XMCKO (the XTI clock buffered output) provides a buffered (and divided) XTI clock that can be output to MPIO\_A. Register 24h/XMCKEN controls whether the XMCKO should be muted or not, and Register 24h/XMCKDIV controls the division factor.

## DIR Data Description

### Decoded Serial Audio Data Output and Interface Format

The DIX9211 supports the following four data formats for the decoded data:

- 16-bit MSB First, Right-Justified
- 24-bit MSB First, Right-Justified
- 24-bit MSB First, Left-Justified
- 24-bit MSB First, I<sup>2</sup>S

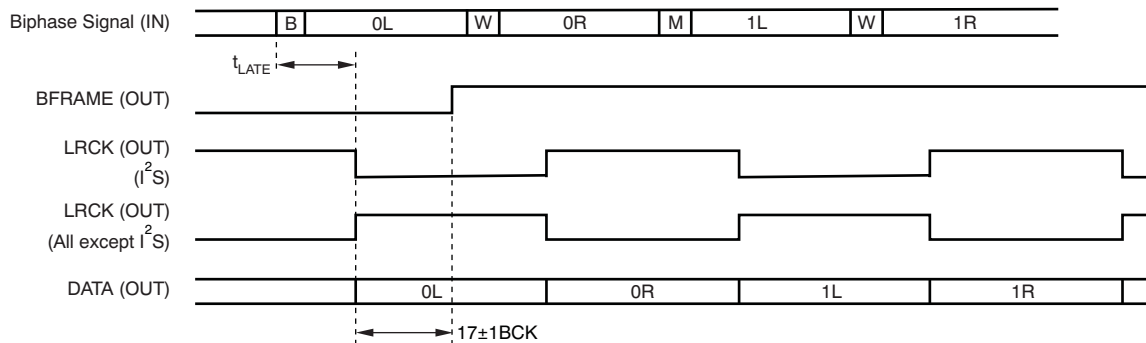
Decoded data are MSB first and twos complement in all formats.

The format of the decoded data is selected by the RXFMT[2:0] register. The possible data formats are shown in Table 6.

Table 6. DIR Serial Audio Data Output Format Set by RXFMT[2:0]

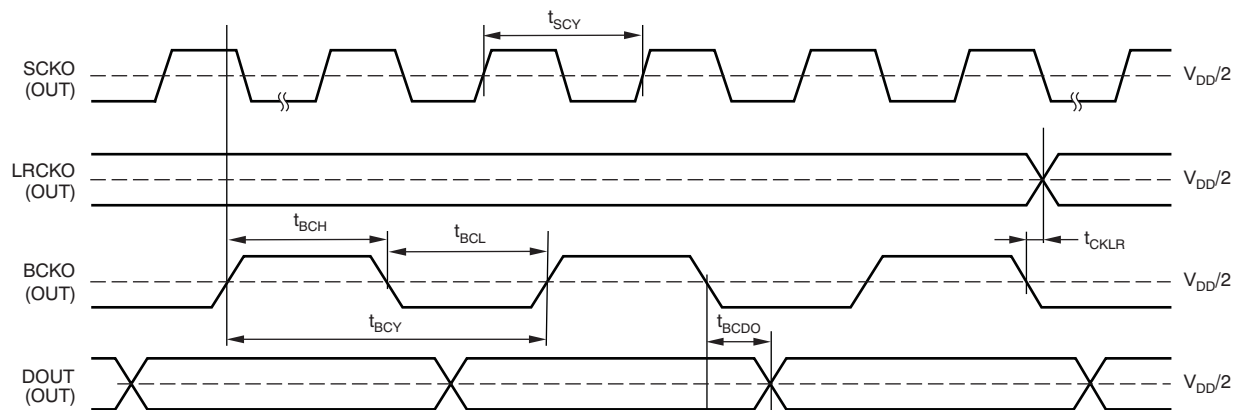
| DIR SERIAL AUDIO DATA OUTPUT FORMAT          | RXFMT[2:0] SETTING |        |        |
|----------------------------------------------|--------------------|--------|--------|
|                                              | RXFMT2             | RXFMT1 | RXFMT0 |
| 24-bit MSB First, Right-Justified            | 0                  | 0      | 0      |
| 16-bit MSB First, Right-Justified            | 0                  | 1      | 1      |
| 24-bit MSB First, I <sup>2</sup> S (Default) | 1                  | 0      | 0      |
| 24-bit MSB First, Left-Justified             | 1                  | 0      | 1      |

Figure 5 shows the latency time between the input biphas signal and LRCKO/DOUT. Figure 6 illustrates the DIR decoded audio data output timing.



| SYMBOL     | DESCRIPTION        | MIN | TYP     | MAX | UNITS |
|------------|--------------------|-----|---------|-----|-------|
| $t_{LATE}$ | LRCKO/DOUT latency |     | $4/f_S$ |     | s     |

**Figure 5. Latency Time Between Input Biphas and LRCKO/DOUT**



| SYMBOL     | DESCRIPTION                                    | MIN | TYP       | MAX | UNITS |
|------------|------------------------------------------------|-----|-----------|-----|-------|
| $t_{SCY}$  | System clock pulse cycle time                  | 18  |           |     | ns    |
| $t_{CKLR}$ | Delay time of BCKO falling edge to LRCKO valid | -10 |           | 10  | ns    |
| $t_{BCY}$  | BCKO pulse cycle time                          |     | $1/64f_S$ |     | s     |
| $t_{BCH}$  | BCKO pulse width high                          | 60  |           |     | ns    |
| $t_{BCL}$  | BCKO pulse width low                           | 60  |           |     | ns    |
| $t_{BCDO}$ | Delay time of BCKO falling edge to DOUT valid  | -10 |           | 10  | ns    |
| $t_R$      | Rising time of all signals                     |     | 5         |     | ns    |
| $t_F$      | Falling time of all signals                    |     | 5         |     | ns    |

NOTE: Load capacitance of LRCKO, BCKO, and DOUT pin is 20 pF. DOUT, LRCKO, and BCKO are synchronized with SCKO.

**Figure 6. DIR Decoded Audio Data Output Timing**

## Channel Status Data, User Data, and Validity Flag

The DIX9211 can output decoded channel status data, user data, and a validity flag synchronized with audio data from the input S/PDIF signal. These signals can be transmitted from any of the three MPIOs (MPIO\_A, MPIO\_B, or MPIO\_C). To assign this function to the MPIOs, see the [MPIO](#) section.

Each type of output data has own dedicated output pin:

- Channel status data (**C**) are output through MPIOs assigned as COUT.
- User data (**U**) are output through MPIOs assigned as UOUT.
- Validity flag (**V**) is output through MPIOs assigned as VOUT
- Data (left and right) are identified as DOUT.

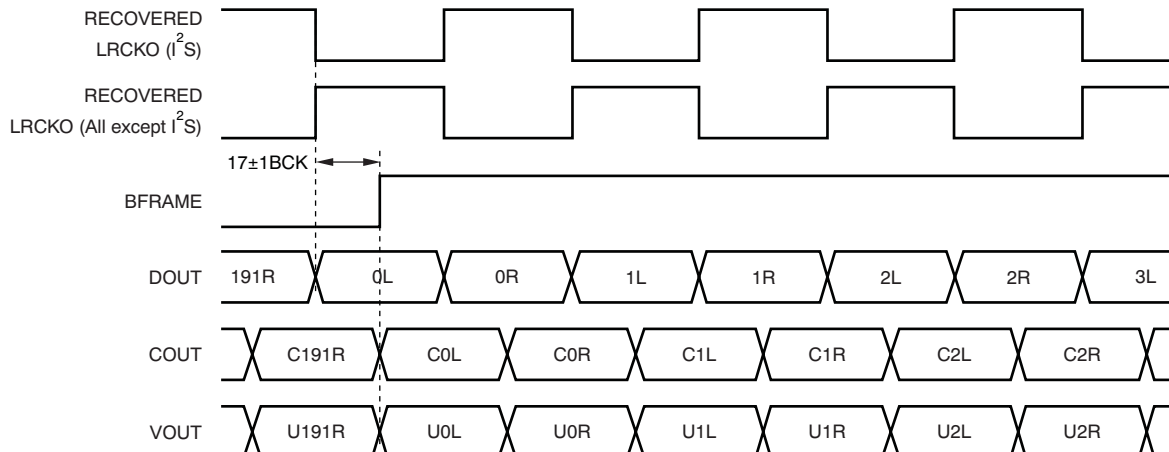
C, U, and V output data are synchronized with the recovered LRCKO (left-right clock output) from the S/PDIF input signal.

The polarity of the recovered LRCKO from the S/PDIF input depends on the Register 2Fh/RXFMT[2:0] setting.

The beginning of each S/PDIF frame (BFRAME) is provided as one of the outputs on the MPIO. It can be used to indicate the start of the frame to the decoding DSP. If the DIR decodes a start-of-frame preamble on the decoded data, then it sets BFRAME high for 8xLRCK periods to signify the start of the frame.

LRCKO can be used as a reference clock for each of the data outputs, BFRAME, DOUT, COUT, UOUT, and VOUT. The relationship between each output is shown in [Figure 7](#).

Numbers 0 to 191 of DOUT, COUT, UOUT, and VOUT in [Figure 7](#) indicate the frame number of the input biphasic signal.



**Figure 7. LRCKO, DOUT, BFRAME, COUT, UOUT, and VOUT Output Timing**

The RXVDLY Register in Register 22h controls when the VOUT pin goes high (either immediately, or at the start of the sample/frame). [Figure 8](#) shows these timing sequences.



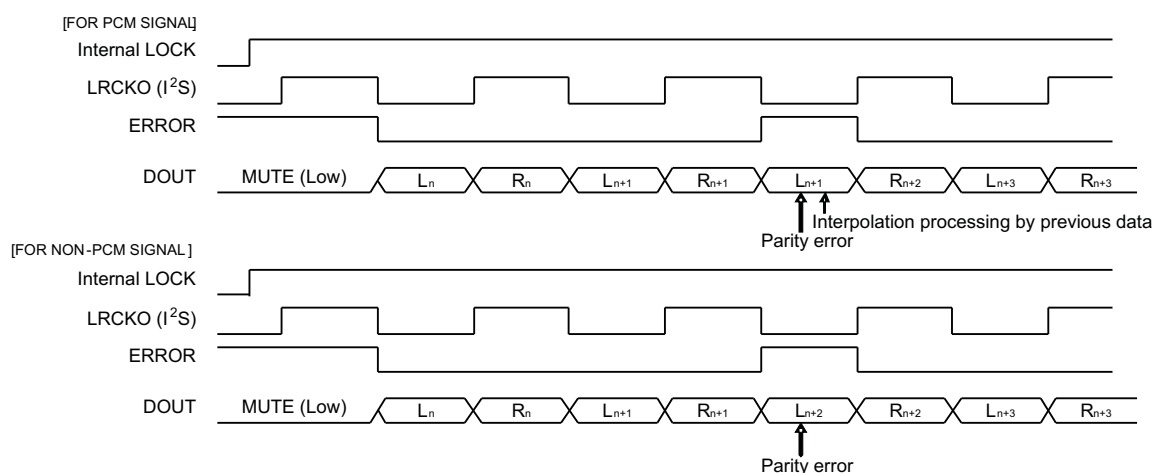
**Figure 8. RXVDLY and VOUT Timing**

## DIR: Parity Error Processing

Error detection and processing for parity errors behave in the following manner:

- For PCM data, when an error is detected (for example, a parity error), then the data from the previous sample are repeated. This sequence is shown in Figure 9, where sample  $L_{n+1}$  is repeated because the incoming data ( $L_{n+2}$ ) had an error.
- For non-PCM data, the data are output as is with no changes. (Non-PCM data implies data which has Channel Status bit 1 = '1'.)

Figure 9 shows the processing for parity error occurrence.



**Figure 9. Processing for Parity Error Occurrence**

The DIX9211 handles parity errors as directed by the 23h/PRTPRO[1:0] registers.

When set to '01', if the error is received eight times sequentially, the DIR output is muted on the next error. Until the mute is enabled, the previously *accurate* sample is repeated. This function is only valid for PCM data.

When set to '10', the device behaves in exactly the same way as it does when set to '01'. However, this function is enabled for both PCM and non-PCM data.

When set to '00', the device ignores parity errors and continues to output whatever data comes into the device.

The setting on '11' is reserved.

## DIR: Errors and Interrupts

The DIX9211 has two pins that are used to inform the system DSP or controller that there is an error, or an interrupt that it should be aware of.

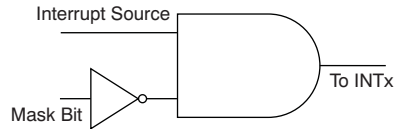
The ERR/INT0 and NPCM/INT1 pins can be configured in these ways:

| HARDWARE PIN | OPTIONS                           |
|--------------|-----------------------------------|
| ERR/INT00    | DIR Error (default), INT0 or Hi-Z |
| NPCM/INT1    | DIR NPCM (default), INT1 or Hi-Z  |

When configured as direct DIR error connections (ERR, NPCM), the system audio processor typically treats them as dedicated interrupt pins to change or control audio processing software. An example would be that the system may mute if an ERR signal is detected. Another example is that if the DSP receives an NPCM interrupt, it begins looking for AC-3 or DTS preambles in the incoming encoded S/PDIF stream.

For more advanced users, the two pins can be set up as interrupt sources. The seven interrupt sources (ERROR, NPCM, DTS-CD/LD, Emphasis, Channel Status Start, Burst Preamble Start,  $f_s$  Calculator Complete) can be masked into Registers INT0 and INT1.

Upon receipt of an interrupt source (such as  $f_s$  Calculator Complete), INT0 or INT1 performs a bitwise evaluation of AND (&) with an inverted mask [Register 2Ah (INT0) and Register 2Bh (INT1)], then perform an eight-way OR of the data. If the output is '1', then INTx is set to '1', which can be used to trigger an interrupt in the host DSP. The host can then poll the INTx register to determine the interrupt source. Figure 10 shows the logic that the device uses to mask the DIR interrupts from the INTx register.

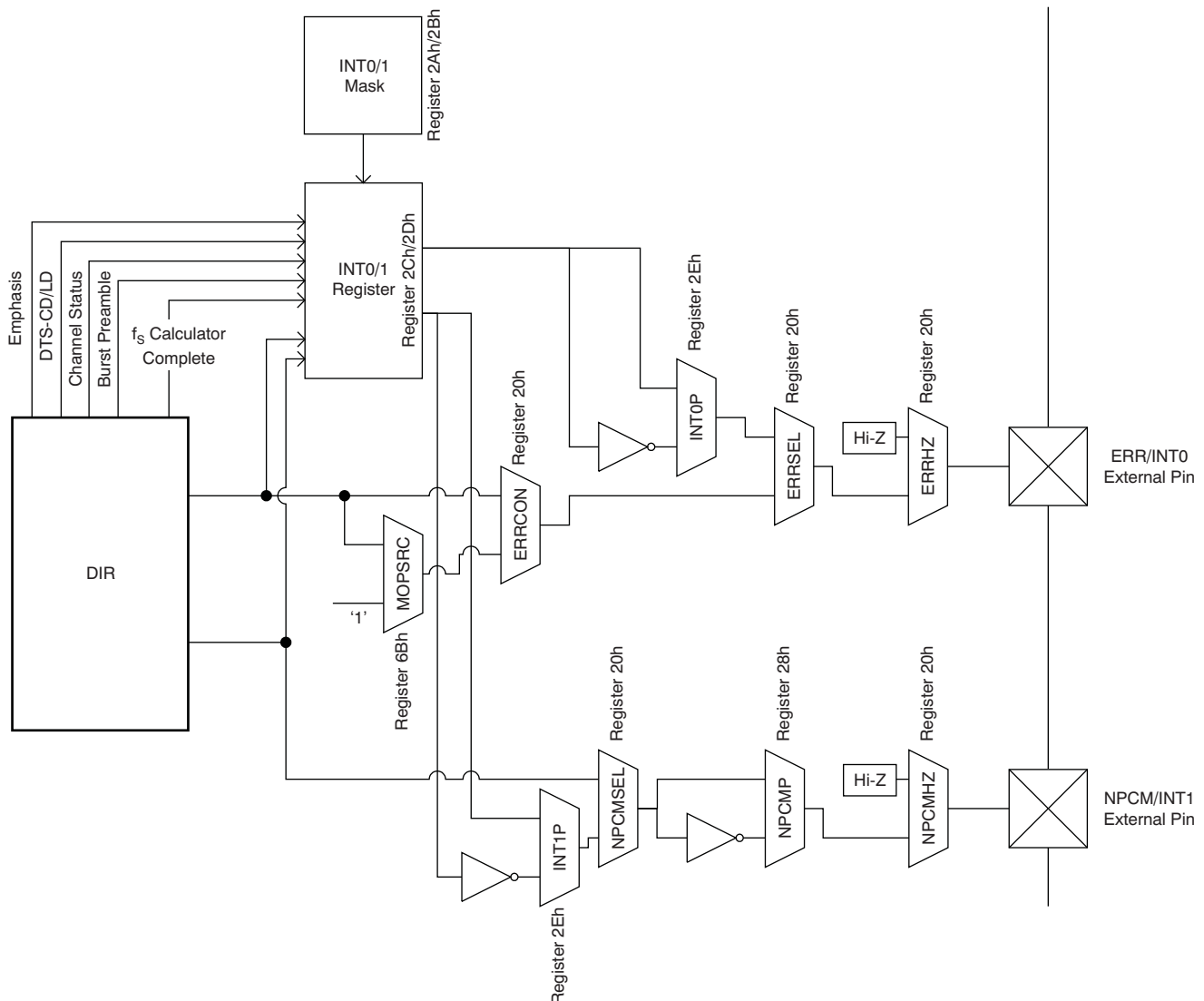


**Figure 10. DIR Interrupt Mask Logic**

Once the register is read, each of the bits in the register (INT0 and INT1) are cleared. If the signal is routed to ERR/INT0 or NPCM/INT1, the output pin is also cleared.

By default, the mask registers are set to mask all inputs; that is, all inputs are rejected, in which case no interrupt can be seen on the output until the mask is changed.

A block diagram for the error output and interrupt output is shown in Figure 11.



**Figure 11. Error Output and Interrupt Output Block Diagram**

There are several allowable error sources from the DIR:

- Change of incoming S/PDIF sample frequency (Register 25h / EFSCHG)
- *Out-of-range* incoming S/PDIF signal (Register 25h / EFSLMT)
- Non-PCM data (Register 25h / ENPCM)
- Data invalid flag is the stream (Validity bit = '1') (Register 25h / EVALID)
- Parity error (Register 25h / EPARITY)
- PLL unlock (default) (Register 25h / EUNLOCK)

The error sources can be selected using Register 25h.

There are also several interrupts within the device that can be masked:

- Error in DIR (this error is selectable from the list above in Register 25h)
- When the device detects non-PCM data
- When the Emphasis flag in the channel status of the incoming data has been set
- When DTS-CD data have been detected by the device
- When the Channel Status (CS) is updated
- When Burst Preamble ( $P_C$ ) is updated
- When the sampling frequency is changed.
- When the analog input crosses the Analog Input Detect level (available only on INT1).

Each interrupt source can be masked by Register 2Ah (INT0) and Register 2Bh (INT1).

#### **DIR: Sampling Frequency Calculator for Incoming S/PDIF Inputs**

The DIX9211 has two integrated sampling frequency calculators. The first calculator is always connected to the output of the DIR. It calculates the actual sampling frequency of the incoming S/PDIF signal. The result can be read from a register, or output through the MPIO pins. Note that this process is not the same as reading the Channel Status value for the sample rate that the transmitting equipment may be sending.

To use this function, a 24.576-MHz clock source must be supplied to the XTI pin. The 24.576-MHz clock is used as a reference clock to calculate the incoming S/PDIF sampling frequency. If the XTI pin is connected to DGND, the function is disabled and the calculation is not performed. If there is an error in the XTI clock frequency, the calculation result and range will be incorrect.

The result is decoded into 4-bit data and stored in Register 39h/SFSOUT[3:0]; the MPIO pins are then assigned to the SFSOUT[3:0] function.

The data in the SFSOUT[3:0] register (and available as a signal for the MPIO section) are the calculated sampling frequency based on the incoming S/PDIF stream, and not what is reported in Channel Status bits 24 to 27. If the PLL becomes unlocked, or attempts to run out of range, SFSOUT[3:0] = '0000' is output, and indicates abnormal operation.

If the XTI source clock is not supplied before the DIX9211 powers up, SFSOUT [3:0] outputs '0000'. If the XTI source clock is stopped, the  $f_s$  calculator holds its most recent calculated result. Once the XTI source clock is restored, the  $f_s$  calculator resumes operation.

Register 39h/SFSST indicates the calculator status. Before reading SFSOUT[3:0], it is recommended that the user verify that the SFSST status is '0'.

The relationship between SFSOUT[3:0] outputs and the range of sampling frequency  $f_s$  is shown in [Table 7](#).

**Table 7. Calculated Biphase Sampling Frequency Output**

| NOMINAL $f_s$ | ACTUAL SAMPLING FREQUENCY RANGE | CALCULATED SAMPLING FREQUENCY OUTPUT <sup>(1)</sup> |         |         |         |
|---------------|---------------------------------|-----------------------------------------------------|---------|---------|---------|
|               |                                 | SFSOUT3                                             | SFSOUT2 | SFSOUT1 | SFSOUT0 |
| Out of range  | Out of range                    | 0                                                   | 0       | 0       | 0       |
| 8 kHz         | 7.84 kHz to 8.16 kHz            | 0                                                   | 0       | 0       | 1       |
| 11.025 kHz    | 10.8045 kHz to 11.2455 kHz      | 0                                                   | 0       | 1       | 0       |
| 12 kHz        | 11.76 kHz to 12.24 kHz          | 0                                                   | 0       | 1       | 1       |
| 16 kHz        | 15.68 kHz to 16.32 kHz          | 0                                                   | 1       | 0       | 0       |
| 22.05 kHz     | 21.609 kHz to 22.491 kHz        | 0                                                   | 1       | 0       | 1       |
| 24 kHz        | 23.52 kHz to 24.48 kHz          | 0                                                   | 1       | 1       | 0       |
| 32 kHz        | 31.36 kHz to 32.64 kHz          | 0                                                   | 1       | 1       | 1       |
| 44.1 kHz      | 43.218 kHz to 44.982 kHz        | 1                                                   | 0       | 0       | 0       |
| 48 kHz        | 47.04 kHz to 48.96 kHz          | 1                                                   | 0       | 0       | 1       |
| 64 kHz        | 62.72 kHz to 65.28 kHz          | 1                                                   | 0       | 1       | 0       |
| 88.2 kHz      | 86.436 kHz to 89.964 kHz        | 1                                                   | 0       | 1       | 1       |
| 96 kHz        | 94.08 kHz to 97.92 kHz          | 1                                                   | 1       | 0       | 0       |
| 128 kHz       | 125.44 kHz to 130.56 kHz        | 1                                                   | 1       | 0       | 1       |
| 176.4 kHz     | 172.872 kHz to 179.928 kHz      | 1                                                   | 1       | 1       | 0       |
| 192 kHz       | 188.16 kHz to 195.84 kHz        | 1                                                   | 1       | 1       | 1       |

(1) The flag SFSOUT[3:0] is output from the register and MPIOs are assigned as SFSOUT[3:0].  
'0' or '1' indicates the register output data. The symbol 'H' or 'L' refers to the MPIO output electrical signal.

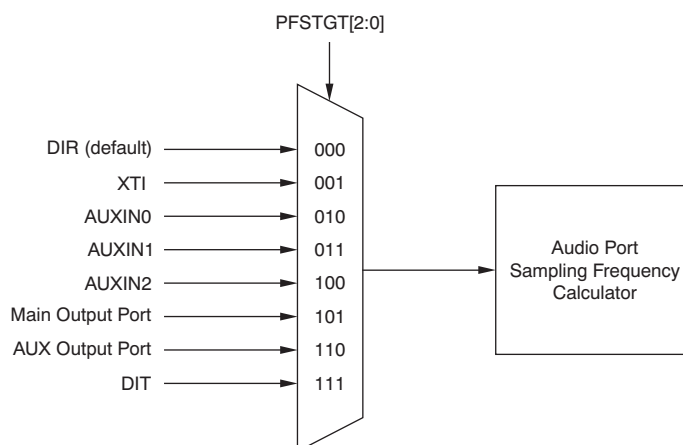
The Biphase Sampling Frequency Calculator is also used for restricting the type of data that can be received.

1. If Register 27h/MSK128 is set to '1', the DIX9211 does not accept 128-kHz sampling frequency data
2. If Register 27h/MSK64 is set to '1', the DIX9211 does not accept 64-kHz sampling frequency data.
3. If Register 27h/NOMLMT is set to '1', the DIX9211 only accepts the nominal audio sampling frequency within  $\pm 2\%$ . The nominal audio sampling frequencies are 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz, and 192 kHz.
4. For Register 27h/HILMT[1:0] and Register 27h/LOLMT[1:0]: These registers are used for setting a higher or lower limit to the acceptable sampling frequency.

Register 21h/RXFSRNG is used for global control of the acceptable sampling frequencies. If normal mode is selected, the range of acceptable sampling frequency is restricted from 28 kHz to 108 kHz. If wide mode is selected, the range is from 7 kHz to 216 kHz.

## DIR: Audio Port Sampling Frequency Calculator

The second sampling frequency calculator can be used to calculate the sampling frequency of DIR, XTI, AUXIN0, AUXIN1, AUXIN2, Main Output Port, AUX Output Port, and DIT Input. Figure 12 illustrates the sampling frequency calculator sources.



**Figure 12. Sampling Frequency Calculator Sources**

The calculated sampling frequency  $f_s$  is decoded to 4-bit data and stored in the PFSOUT[3:0] register. The input source of this counter is selectable from AUXIN0, AUXIN1, AUXIN2, DIR, XTI, Main Output Port, AUX Output Port, and DIT by using the Register 37h/PFSTGT[3:0].

To use this function, a 24.576-MHz clock source must be supplied to the XTI pin. The 24.576-MHz clock is used as a reference clock. If the XTI pin is connected to DGND, the calculation is not performed. If there is an error in the XTI clock frequency, the calculation result and range will be incorrect.

Register 38h/PFSST indicates the calculator status. It is recommended that PFSST is checked (for *complete* status) before reading PFSOUT[3:0].

## OUTPUT REGISTER CONSTRUCTION

The output 8-bit register is subdivided into three sections. The first four bits show the decoded result. The next three bits signify the source; the final bit signifies the calculator status (finished or not).

The lock range of the counter (to the specified  $f_s$  given in [Table 8](#)) are any clock rate within  $\pm 2\%$ . The relation between the nominal  $f_s$  and actual measured  $f_s$  range is shown in [Table 8](#).

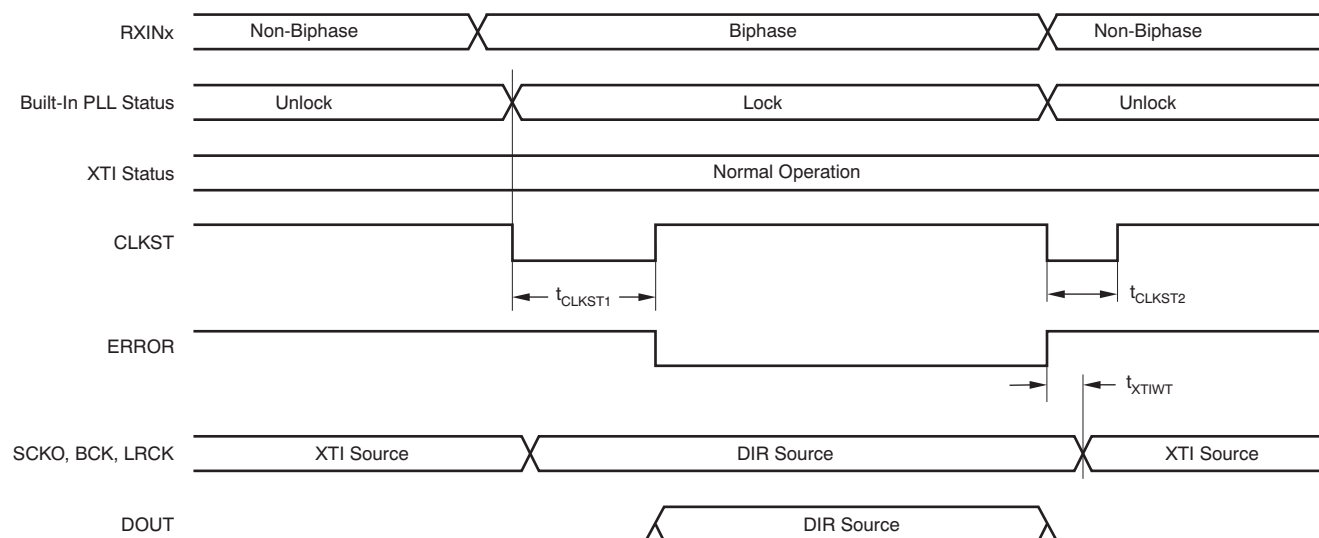
**Table 8. Calculated Port Sampling Frequency Output**

| NOMINAL $f_s$ | ACTUAL SAMPLING<br>FREQUENCY RANGE (MIN) | CALCULATED SAMPLING FREQUENCY OUTPUT |         |         |         |
|---------------|------------------------------------------|--------------------------------------|---------|---------|---------|
|               |                                          | PFSOUT3                              | PFSOUT2 | PFSOUT1 | PFSOUT0 |
| Out of range  | Out of range                             | 0                                    | 0       | 0       | 0       |
| 8 kHz         | 7.84 kHz to 8.16 kHz                     | 0                                    | 0       | 0       | 1       |
| 11.025 kHz    | 10.8045 kHz to 11.2455 kHz               | 0                                    | 0       | 1       | 0       |
| 12 kHz        | 11.76 kHz to 12.24 kHz                   | 0                                    | 0       | 1       | 1       |
| 16 kHz        | 15.68 kHz to 16.32 kHz                   | 0                                    | 1       | 0       | 0       |
| 22.05 kHz     | 21.609 kHz to 22.491 kHz                 | 0                                    | 1       | 0       | 1       |
| 24 kHz        | 23.52 kHz to 24.48 kHz                   | 0                                    | 1       | 1       | 0       |
| 32 kHz        | 31.36 kHz to 32.64 kHz                   | 0                                    | 1       | 1       | 1       |
| 44.1 kHz      | 43.218 kHz to 44.982 kHz                 | 1                                    | 0       | 0       | 0       |
| 48 kHz        | 47.04 kHz to 48.96 kHz                   | 1                                    | 0       | 0       | 1       |
| 64 kHz        | 62.72 kHz to 65.28 kHz                   | 1                                    | 0       | 1       | 0       |
| 88.2 kHz      | 86.436 kHz to 89.964 kHz                 | 1                                    | 0       | 1       | 1       |
| 96 kHz        | 94.08 kHz to 97.92 kHz                   | 1                                    | 1       | 0       | 0       |
| 128 kHz       | 125.44 kHz to 130.56 kHz                 | 1                                    | 1       | 0       | 1       |
| 176.4 kHz     | 172.872 kHz to 179.928 kHz               | 1                                    | 1       | 1       | 0       |
| 192 kHz       | 188.16 kHz to 195.84 kHz                 | 1                                    | 1       | 1       | 1       |

## DIR: Auto Source Selector for Main Output and AUX Output

The AUTO source selector is an automatic system that selects the DIR or XTI output based on specific DIR conditions set by Register 26h. The AUTO source selector is integrated in both the Main Port and the AUX output separately.

The typical behavior for the AUTO source selector is shown in Figure 13. This example is the default register setting for Register 26h. In this case, only Register 26h/AUNLOCK is selected.



**Figure 13. Typical Behavior for AUTO Source Selector**

When the DIR is unlocked, the XTI output is automatically routed to the Main Output Port.

Polarity of the CLKST signal is configured by Register 22h/CLKSTP. The default is active low, which means that clock source either changes from DIR to XTI, or from XTI to DIR.

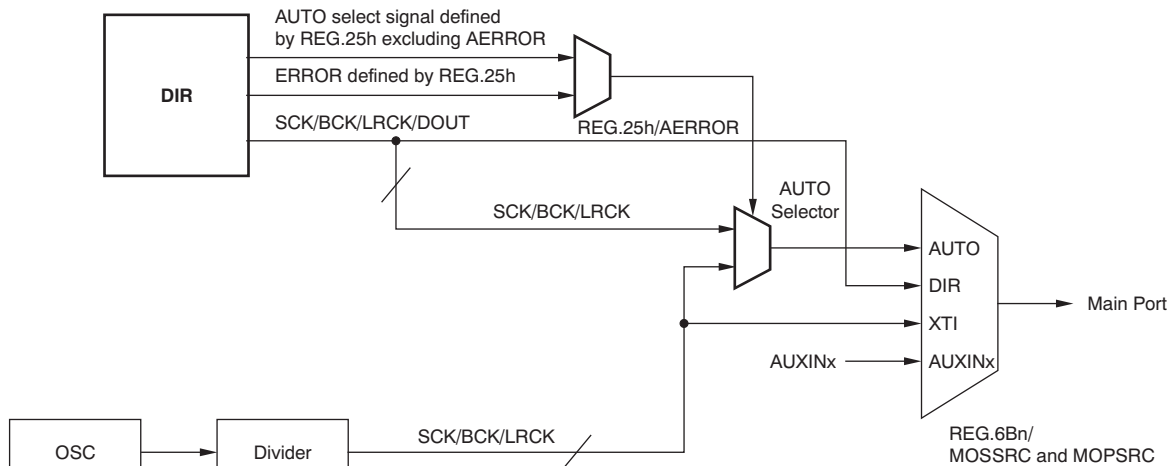
If the DIR is locked, then the DIR output is routed to the Main Output Port automatically after  $t_{CLKST1}$ . During that period, the output port is muted.  $t_{CLKST1}$  can be configured using Register 23h/ERRWT[1:0].  $t_{CLKST2}$  is 50 ms, providing that an XTI clock of 24.576 MHz is applied.

If the DIR loses its lock a subsequent time, the XTI output is routed to the Main Output Port automatically after  $t_{XTIWT}$ . Once again, the output port is muted during this time.  $t_{XTIWT}$  can be configured using Register 23h/XTIWT[1:0].

The auto source selector can be triggered by the following changes in the DIR (Register 26h is used to select which variable to use as the trigger):

- DIR error (discussed earlier in [DIR: Errors and Interrupts](#); configured by Register 25h)
- Out-of-range sampling frequency
- Non-PCM data
- When the Validity flag in the S/PDIF stream is '1'
- When the PLL is unlocked (default)

Figure 14 shows the Clock Tree Diagram for the AUTO source selector.



**Figure 14. Clock Tree Diagram for AUTO Source Selector**

### Non-PCM Data Detection

The DIX9211 can also detect Non-PCM data (AC-3, DTS-CD, etc.) using one of these two methods:

1. Channel Status Bit 1 is '1'.

If Register 28h/CSBIT is set to '1', this function is enabled. Register 39h/SCSBIT1 always indicates Channel Status Bit 1 status even if CSBIT1 is disabled.

2. A Burst Preamble ( $P_A/P_B$ ) is found in the S/PDIF stream.

If Register 28h/PAPB or Register 28h/DTSCD is set to '1', this function is enabled. If DTS-CD detection is active, it uses DTSCD, and can also be set in Register 29h/DTS16, 29h/DTS14, and Register 29h/DTS12[1:0].

If the DIX9211 detects a Burst Preamble when Non-PCM detection is enabled, an error signal and BPSYNC signal are generated. The BPSYNC signal can be monitored through MPIO\_A/MPIO\_B/MPIO\_C. For more details, see the [MPIO](#) section of this document. The error signal can be monitored from either the ERR\_INT0 pin or the NPCM\_INT1 pin.

### $P_C/P_D$ Monitor

The DIX9211 has a  $P_C$  and  $P_D$  buffer for monitoring the latest  $P_C$  or  $P_D$ . Registers 3Ah and 3Bh are assigned for the  $P_C$  buffer; Registers 3Ch and 3Dh are assigned for the  $P_D$  buffer.

The following sequence is an example of reading  $P_C/P_D$  buffers. This example is based on using the INTO function.

1. Set Register 2Ah/MPCRNW0 to '0'.
2. Check that Register 2Ch/OPCRNW0 is '1'.
3. Read the  $P_C$  and  $P_D$  buffers.

## Digital Audio Interface Transmitter

### Overview

The DIX9211 has an onboard Digital Audio Interface Transmitter (DIT) that transmits S/PDIF data from 7 kHz to 216 kHz, up to 24-bit audio data. The first 48 bits of the channel status buffer are programmable. The source for the DIT is selectable from the built-in routing function of the DIX9211 as well as the dedicated inputs assigned to the MPIOs.

### Selection OF DIT Input Source

Selection of the DIT audio and clock sources is done using the Registers 60h/TXSSRC[2:0] and 60h/TXPSRC[2:0]. The system clock source for the DIT is selected using the Register 60h/TXSSRC[2:0]. The PCM audio data source for the DIT (BCK, LRCK, and Data) is selected using the Register 60h/TXPSRC[2:0].

The DIT can also be operated in a standalone mode. In standalone mode, the data source is provided through MPIO\_C. See the [DIT Stand-Alone](#) section for more details.

### DIT Output Biphase

The S/PDIF-encoded signal generated by the DIT module is available through the MPO0 and MPO1 pins. The MPO selection registers (Register 78h/MPOxSEL[3:0]) can be set to '1101' to determine the DIT output through one of these two pins.

In addition to the standard MPOx pins, the DIT output can also be multiplexed to the RECOUT pin, or back into the DIR. An example of where this multiplexing might occur is in a jitter cleaner application. The DIR in the DIX9211 has excellent jitter reduction. Data can be brought in from an auxiliary source, transmitted through the DIT internally, then routed to the DIR. This process, in turn, cleans the clocks and provides a stable, well-clocked PCM source. This feature is especially useful for jittery sources, such as HDMI.

### Audio Data and Clock

The DIT can accept a  $128f_s$ ,  $256f_s$ , or  $512f_s$  system clock. The clock ratio selection is set by using the Register TXSCK[2:0]. A 216-kHz sampling frequency is supported by using the  $128f_s$  or  $256f_s$  system clock ratio. A 108-kHz sampling frequency can be supported up to a  $512f_s$  clock ratio.

$I^2S$ , 24-bit left-justified, 24-bit right-justified, and 16-bit right-justified serial audio interface formats can be used. Only slave mode is supported. [Table 9](#) shows the relationship between typical audio sampling frequencies and the respective BCK and SCK frequencies

**Table 9. Typical Audio Sampling, BCK, and SCK Frequencies**

| LRCK<br>$f_s$ | BCK<br>$64f_s$ | SCK         |             |             |
|---------------|----------------|-------------|-------------|-------------|
|               |                | $128f_s$    | $256f_s$    | $512f_s$    |
| 8 kHz         | 0.512 MHz      | 1.024 MHz   | 2.048 MHz   | 4.096 MHz   |
| 11.025 kHz    | 0.7056 MHz     | 1.4112 MHz  | 2.8224 MHz  | 5.6448 MHz  |
| 12 kHz        | 0.768 MHz      | 1.536 MHz   | 3.072 MHz   | 6.144 MHz   |
| 16 kHz        | 1.024 MHz      | 2.048 MHz   | 4.096 MHz   | 8.192 MHz   |
| 22.05 kHz     | 1.4112 MHz     | 2.8224 MHz  | 5.6448 MHz  | 11.2896 MHz |
| 24 kHz        | 1.536 MHz      | 3.072 MHz   | 6.144 MHz   | 12.288 MHz  |
| 32 kHz        | 2.048 MHz      | 4.096 MHz   | 8.192 MHz   | 16.384 MHz  |
| 44.1 kHz      | 2.8224 MHz     | 5.6448 MHz  | 11.2896 MHz | 22.5792 MHz |
| 48 kHz        | 3.072 MHz      | 6.144 MHz   | 12.288 MHz  | 24.576 MHz  |
| 64 kHz        | 4.096 MHz      | 8.192 MHz   | 16.384 MHz  | 32.768 MHz  |
| 88.2 kHz      | 5.6448 MHz     | 11.2896 MHz | 22.5792 MHz | 45.1584 MHz |
| 96 kHz        | 6.144 MHz      | 12.288 MHz  | 24.576 MHz  | 49.152 MHz  |
| 128 kHz       | 8.192 MHz      | 16.384 MHz  | 32.768 MHz  | N/A         |
| 176.4 kHz     | 11.2896 MHz    | 22.5792 MHz | 45.1584 MHz | N/A         |
| 192 kHz       | 12.288 MHz     | 24.576 MHz  | 49.152 MHz  | N/A         |

### **Data Mute Function**

The DIX9211 has the ability to mute the audio data on its DIT output. This option is set using Register 62h/TXDMUT. During a mute state (TXDMUT = '1'), the biphase stream continues to flow, but all audio data are zeroed.

The channel status data and validity flag are not zeroed. Mute is done at the LRCK edge for both L-ch and R-ch data at the same time.

### **Channel Status Data**

The DIT has the ability to transmit channel status (CS) data for the first 48 bits of the 128-bit stream. These 48 bits cover the standards for both S/PDIF and AES/EBU. These bits are set in Registers TXCS0 through TXCS47. These values are used on both the Left and Right channels of the output stream.

Upon reset, these registers are all '0' by default.

### **User Data**

This DIT does not have the ability to transmit custom user data (known as *U Bits* in the stream).

### **Validity Flag**

Setting the valid flag is possible in the DIT by using Register 62h/TXVFLG. The same value is used for both left and right channels.

### **Standalone Operation**

Standalone operation for the DIT module is provided by supplying external clocks and data (SCK, BCK, LRCK, and Data). In standalone mode, the audio and clock data must be brought into the device through MPIO\_C. To enable standalone mode, set Register 6Fh/MPCSEL[2:0] to '101'. This configuration then bypasses the standard DIT connections through the device and connects them directly to MPIO\_C.

Channel Status and Validity flags continue to be sourced from the same registers as they would during normal DIT operation.

## MPIO Description

### Overview

The DIX9211 offers significant flexibility through its MPIO pins. Depending on the system partitioning of the specific end product, the pins can be reconfigured to offer various I/Os that complement the design.

There are 14 flexible pins: 12 are Input/Output pins, and two pins that are output only.

The 12 multi-purpose I/O (MPIO) pins are grouped into three banks, each with four pins: MPIO\_A, MPIO\_B, and MPIO\_C.

The two multi-purpose outputs (MPO) pins are assigned as MPO0 and MPO1.

### Assignable Signals for MPIO Pins

The DIX9211 has the following signals that can be brought out to MPIOs. Not all MPIOs are equal; be sure to review subsequent sections in this document to see which signals can be brought out to which MPIO. The possible signals are summarized in [Table 10](#).

**Table 10. Allowable MPIO Signals**

| MODULE                 | ALLOWABLE SIGNALS                                                                                 |
|------------------------|---------------------------------------------------------------------------------------------------|
| DIR                    | Extended biphasic input pins for DIR: RXIN8/RXIN9/RXIN10/RXIN11                                   |
|                        | DIR Flags Output: The details of each signal are described in the <a href="#">Flag</a> section.   |
|                        | DIR Interrupt Output: INT0 and INT1                                                               |
|                        | DIR, B frame, serial output of channel status, user data, validity flag                           |
|                        | DIR, decoded result of sampling frequency calculated by built-in $f_s$ counter                    |
| Auxiliary I/O          | AUXIN0, external serial audio data input (SCK/BCK/LRCK/Data)                                      |
|                        | AUXIN1, external serial audio data input (SCK/BCK/LRCK/Data)                                      |
|                        | AUXIN2, external serial audio data input (SCK/BCK/LRCK/Data)                                      |
|                        | AUXOUT, external serial audio data output (SCK/BCK/LRCK/Data)                                     |
| DIT                    | Serial audio data input for DIT Standalone Operation                                              |
| Application-Specific   | AVR Application1: Clock Transition Output, Validity Output, XTI buffered Output, Interrupt Output |
|                        | AVR Application2: Secondary BCK/LRCK Output, XTI buffered Output, Interrupt Output                |
| Digital Logic Specific | GPIO (General Purpose I/O), Logical high or low I/O, selectable I/O direction for each pin        |
|                        | Hi-Z status, selectable for each pin                                                              |

### How to Assign Functions to MPIO

Both MPO0 and MPO1 have a function assignment register. The output of MPO0 can be selected using the MPO0SEL[3:0] register; in the same way, the output of MPO1 can be selected using the MPO1SEL[3:0] register. Selecting the biphasic source can be done using Register 35h/RO0SEL and Register 36h/RO1SEL. Muting the MPO can be done using Registers MPO0MUT and MPO1MUT.

### Selection Of Output Source

The DIX9211 also has a routing function for serial digital audio clocks and data. This function routes between all input sources (DIR, XTI, AUXIN0, AUXIN1, AUXIN2) and Main Out, AUXOUT, and DIT. The selection for Main Out and AUXOUT is set with these registers:

- **Main Out:** Registers 6Bh, MOSSRC[2:0], and MOPSRC[2:0]
- **AUXOUT:** Register 6Ch, AOSSRC[2:0], and AOPSC[2:0]

Muting Main Out and AUXOUT is done using Register 6Ah. Hi-Z control for Main Out is set with Register 6Dh.

## Assignable Signals to MPO Pins

Both MPO pins have the same function. The following signals can be routed to the MPOs:

- DIR flags output (details of signals are described in the [Flag](#) section)
- DIR Interrupt Output: INT0 and INT1
- B frame, serial output of channel status, user data and validity flag of DIR
- GPO (general-purpose output), Hi-Z / Logical high or low
- DIT biphasic Output
- XTI buffered Output
- RECOUT0 or RECOUT1, two independent multiplexers, are provided

To use the limited pins of the DIX9211 economically, the DIR flag outputs and the GPIO are used at same time within the number of MPIO pins assigned to DIR flags or to GPIO functions. *DIR flags* or *GPIO* can be selected for each MPIO zone by using Registers MPASEL[1:0], MPBSEL[2:0], and MPCSEL[2:0]

---

### NOTE

To identify the pins in each MPIO group, the convention \* represents 0 to 3.

---

When DIR flags are required on hardware pins, users should select the desired signals with Registers MPA\*FLG, MPB\*FLG, and MPC\*FLG.

When GPIOs are required, set the I/O direction with GIOA\*DIR, GIOB\*DIR, and GIOC\*DIR registers. When a GPO (general-purpose output) function is required, set the output data with Registers GPOA\*, GPOB\*, and GPOC\*. When a GPI (general-purpose input) function is required, the status of the pins with an assigned GPI function is stored in the GPIA\*, GPIB\*, and GPIC\* registers (these registers are read-only).

## External ADC Mode

To use an external analog-to-digital converter (ADC), the DIX9211 supports *External ADC Mode*. This option enables a connection with an external, 192-kHz capable ADC via the MPIO\_B ports. The external ADC must be a clock slave to the DIX9211. The clock source for the external ADC can be selected using Register 42h/ADCLK.

To use the external ADC mode, Register 6Fh/MPBSEL must be set to '101' (External Slave ADC Input). Then, each MPIO\_B port is assigned for MPIO\_B0 = EASCKO (output), MPIO\_B1 = EABCKO (output), MPIO\_B2 = EALRCKO (output), and MPIO\_B3 = EADIN (input). The MPIO\_B pins should be connected according to this configuration:

- MPIO\_B0 to ADC system clock input
- MPIO\_B1 to ADC bit clock input
- MPIO\_B2 to ADC LR clock input
- MPIO\_B3 to ADC data output

## MPIO and MPO Assignments

The I/O function of the MPIOs and MPOs are assigned by Registers MPASEL[1:0], MPBSEL[2:0], MPCSEL[2:0], MPO0SEL[3:0], and MPO1SEL[3:0]. The available functions are shown in [Table 11](#) through [Table 15](#).

**Table 11. MPIO Group A (Pins: MPIO\_A0 to MPIO\_A3)**

| MPASEL[1:0] | DIRECTION | MPIO GROUP A FUNCTION                                                 |
|-------------|-----------|-----------------------------------------------------------------------|
| 00          | IN        | Biphase input (RXIN8/RXIN9/RXIN10/RXIN11)                             |
| 01          | OUT       | AVR Application 1 (CLKST, VOUT, XMCKO, INT0) (default) <sup>(1)</sup> |
| 10          | OUT       | AVR Application 2 (SBCK, SLRCK, XMCKO, INT0)                          |
| 11          | IN/ OUT   | DIR Flags output or GPIOs                                             |

(1) MPIO\_A0 to MPIO\_A3 are set to Hi-Z by the MPA0HZ to MPA3HZ registers as default.

**Table 12. MPIO Group B (Pins: MPIO\_B0 to MPIO\_B3)**

| MPBSEL[2:0] | DIRECTION | MPIO GROUP B FUNCTION                                         |
|-------------|-----------|---------------------------------------------------------------|
| 000         | IN        | AUXIN2, ASCKI2/ABCKI2/ALRCKI2/ADIN2 (default)                 |
| 001         | OUT       | AUXOUT, ASCKO/ABCKO/ALRCKO/ADOUT                              |
| 010         | OUT       | Sampling frequency calculated result output, SFSOUT[3:0]      |
| 011         | IN/OUT    | DIR Flags Output or GPIO                                      |
| 100         | OUT       | DIR BCU <sub>V<sub>Output</sub></sub> (BFRAME/COUT/UOUT/VOUT) |
| 101         | IN/OUT    | External slave ADC input (EASCKO/EABCKO/EALRCKO/EADIN)        |
| 110         | N/A       | Reserved                                                      |
| 111         | N/A       | Reserved                                                      |

**Table 13. MPIO Group C (Pins: MPIO\_C0 to MPIO\_C3)**

| MPCSEL[2:0] | DIRECTION | MPIO GROUP C FUNCTION                                      |
|-------------|-----------|------------------------------------------------------------|
| 000         | IN        | AUXIN1 (ASCKI1/ABCKI1/ALRCKI1/ADIN1) (default)             |
| 001         | IN/OUT    | Reserved                                                   |
| 010         | OUT       | Sampling frequency calculated result output, SFSOUT[3:0]   |
| 011         | IN/OUT    | DIR Flags output or GPIO                                   |
| 100         | OUT       | DIR BCUV output (BFRAME/COUT/UOUT/VOUT)                    |
| 101         | IN        | DIT Standalone, clock, and data (TXSCK/TXBCK/TXLRCK/TXDIN) |
| 110         | N/A       | Reserved                                                   |
| 111         | N/A       | Reserved                                                   |

**Table 14. MPO0 Pin**

| MPO0SEL[3:0] | DIRECTION | MPO0 FUNCTION                        |
|--------------|-----------|--------------------------------------|
| 0000         | OUT       | Hi-Z                                 |
| 0001         | OUT       | GPO0, Output data = Logic high level |
| 0010         | OUT       | GPO0, Output data = Logic low level  |
| 0011         | OUT       | VOUT                                 |
| 0100         | OUT       | INT0                                 |
| 0101         | OUT       | INT1                                 |
| 0110         | OUT       | CLKST                                |
| 0111         | OUT       | EMPH                                 |
| 1000         | OUT       | BPSYNC                               |
| 1001         | OUT       | DTSCD                                |
| 1010         | OUT       | PARITY                               |
| 1011         | OUT       | LOCK                                 |
| 1100         | OUT       | XMCKO                                |
| 1101         | OUT       | TXOUT (default)                      |
| 1110         | OUT       | RECOUT0                              |
| 1111         | OUT       | RECOUT1                              |

**Table 15. MPO1 Pin**

| MPO1SEL[3:0] | DIRECTION | MPO1 FUNCTION                        |
|--------------|-----------|--------------------------------------|
| 0000         | OUT       | Hi-Z                                 |
| 0001         | OUT       | GPO1, Output data = Logic high level |
| 0010         | OUT       | GPO1, Output data = Logic low level  |
| 0011         | OUT       | VOUT (default)                       |
| 0100         | OUT       | INT0                                 |
| 0101         | OUT       | INT1                                 |
| 0110         | OUT       | CLKST                                |
| 0111         | OUT       | EMPH                                 |
| 1000         | OUT       | BPSYNC                               |
| 1001         | OUT       | DTSCD                                |
| 1010         | OUT       | PARITY                               |
| 1011         | OUT       | LOCK                                 |
| 1100         | OUT       | XMCKO                                |
| 1101         | OUT       | TXOUT                                |
| 1110         | OUT       | RECOUT0                              |
| 1111         | OUT       | RECOUT1                              |

## MPIO Description

### Description for Signal Name Assigned to MPIO

Table 16 through Table 24 list the details of where each of the internal DIX9211 signals can be routed to. For instance, DIR LOCK can be output to any of the MPIO and MPO pins, while SBCK (Secondary Clock Output) can only be brought out through MPIO\_A0.

**Table 16. DIR Flags Output**

| SIGNAL NAME | MPIO GROUP / PIN  | DESCRIPTION                                          |
|-------------|-------------------|------------------------------------------------------|
| CLKST       | All MPIOs, MPO0/1 | Clock transient status signal output                 |
| INT0        | All MPIOs, MPO0/1 | Interrupt system 0, Interrupt event detection output |
| INT1        | All MPIOs, MPO0/1 | Interrupt system 1, Interrupt event detection output |
| EMPH        | All MPIOs, MPO0/1 | Channel status, emphasis detection output            |
| BPSYNC      | All MPIOs, MPO0/1 | Burst preamble sync signal output                    |
| DTSCD       | All MPIOs, MPO0/1 | DTS-CD/LD detection output                           |
| PARITY      | All MPIOs, MPO0/1 | Biphase parity error detection output                |
| LOCK        | All MPIOs, MPO0/1 | PLL lock detection output                            |

**Table 17. DIR B Frame, Channel Status, User Data, Validity Flag Output**

| SIGNAL NAME | MPIO GROUP / PIN  | DESCRIPTION         |
|-------------|-------------------|---------------------|
| BFRAME      | All MPIOs, MPO0/1 | B frame output      |
| COUT        | All MPIOs         | Channel status data |
| UOUT        | All MPIOs         | User data           |
| VOUT        | All MPIOs         | Validity flag       |

**Table 18. DIR Calculated Sampling Frequency Output**

| SIGNAL NAME | MPIO GROUP / PIN | DESCRIPTION                             |
|-------------|------------------|-----------------------------------------|
| SFSOUT0     | All MPIOs        | Calculated $f_s$ , decoded output, bit0 |
| SFSOUT1     | All MPIOs        | Calculated $f_s$ , decoded output, bit1 |
| SFSOUT2     | All MPIOs        | Calculated $f_s$ , decoded output, bit2 |
| SFSOUT3     | All MPIOs        | Calculated $f_s$ , decoded output, bit3 |

**Table 19. Biphase Input**

| SIGNAL NAME | MPIO GROUP / PIN | DESCRIPTION             |
|-------------|------------------|-------------------------|
| RXIN8       | MPIO_A0          | Biphase signal input 8  |
| RXIN9       | MPIO_A1          | Biphase signal input 9  |
| RXIN10      | MPIO_A2          | Biphase signal input 10 |
| RXIN11      | MPIO_A3          | Biphase signal input 11 |

**Table 20. Biphase Output**

| SIGNAL NAME | MPIO GROUP / PIN | DESCRIPTION                             |
|-------------|------------------|-----------------------------------------|
| RECOU0      | MPO0/1           | Independent biphase selector 0, output0 |
| RECOU1      | MPO0/1           | Independent biphase selector 1, output1 |
| TXOUT       | MPO0/1           | Built-in DIT, biphase output            |

**Table 21. AUX Clocks Output**

| SIGNAL NAME | MPIO GROUP / PIN | DESCRIPTION                         |
|-------------|------------------|-------------------------------------|
| SBCK        | MPIO_A0          | Secondary bit clock output          |
| SLRCK       | MPIO_A1          | Secondary LR clock output           |
| XMCKO       | MPIO_A2, MPO0/1  | XTI pin input clock buffered output |

**Table 22. Audio Clock and Data I/O**

| SIGNAL NAME | MPIO GROUP / PIN | DESCRIPTION                                   |
|-------------|------------------|-----------------------------------------------|
| ASCKI1      | MPIO_C0          | AUXIN1, system clock input                    |
| ABCKI1      | MPIO_C1          | AUXIN1, bit clock input                       |
| ALRCKI1     | MPIO_C2          | AUXIN1, LR clock input                        |
| ADIN1       | MPIO_C3          | AUXIN1, data input                            |
| ASCKI2      | MPIO_B0          | AUXIN2, system clock input                    |
| ABCKI2      | MPIO_B1          | AUXIN2, bit clock input                       |
| ALRCKI2     | MPIO_B2          | AUXIN2, LR clock input                        |
| ADIN2       | MPIO_B3          | AUXIN2, data input                            |
| ASCKO       | MPIO_B0          | AUXOUT, system clock output                   |
| ABCKO       | MPIO_B1          | AUXOUT, bit clock output                      |
| ALRCKO      | MPIO_B2          | AUXOUT, LR clock output                       |
| ADOUT       | MPIO_B3          | AUXOUT, data output                           |
| EASCKO      | MPIO_B0          | External Slave ADC Input, system clock output |
| EABCKO      | MPIO_B1          | External Slave ADC Input, bit clock output    |
| EALRCKO     | MPIO_B2          | External Slave ADC Input, LR clock output     |
| EADIN       | MPIO_B3          | External Slave ADC Input, data input          |
| TXSCK       | MPIO_C0          | DIT Standalone, system clock input            |
| TXBCK       | MPIO_C1          | DIT Standalone, bit clock input               |
| TXLRCK      | MPIO_C2          | DIT Standalone, LR clock input                |
| TXDIN       | MPIO_C3          | DIT Standalone, data input                    |

**Table 23. GPIO (General-Purpose Input/Output)**

| SIGNAL NAME | MPIO GROUP / PIN | DESCRIPTION            |
|-------------|------------------|------------------------|
| GPIOA0      | MPIO_A0          | General-purpose input  |
| GPIOA1      | MPIO_A1          | General-purpose input  |
| GPIOA2      | MPIO_A2          | General-purpose input  |
| GPIOA3      | MPIO_A3          | General-purpose input  |
| GPOA0       | MPIO_A0          | General-purpose output |
| GPOA1       | MPIO_A1          | General-purpose output |
| GPOA2       | MPIO_A2          | General-purpose output |
| GPOA3       | MPIO_A3          | General-purpose output |
| GPIOB0      | MPIO_B0          | General-purpose input  |
| GPIOB1      | MPIO_B1          | General-purpose input  |
| GPIOB2      | MPIO_B2          | General-purpose input  |
| GPIOB3      | MPIO_B3          | General-purpose input  |
| GPOB0       | MPIO_B0          | General-purpose output |
| GPOB1       | MPIO_B1          | General-purpose output |
| GPOB2       | MPIO_B2          | General-purpose output |
| GPOB3       | MPIO_B3          | General-purpose output |
| GPIC0       | MPIO_C0          | General-purpose input  |
| GPIC1       | MPIO_C1          | General-purpose input  |
| GPIC2       | MPIO_C2          | General-purpose input  |
| GPIC3       | MPIO_C3          | General-purpose input  |
| GPOC0       | MPIO_C0          | General-purpose output |
| GPOC1       | MPIO_C1          | General-purpose output |
| GPOC2       | MPIO_C2          | General-purpose output |
| GPOC3       | MPIO_C3          | General-purpose output |

**Table 24. GPO (General-Purpose Output)**

| SIGNAL NAME | MPIO GROUP / PIN | DESCRIPTION            |
|-------------|------------------|------------------------|
| GPO0        | MPO0             | General-purpose output |
| GPO1        | MPO1             | General-purpose output |

**MPIO and MPO Assignment: Pin Assignment Details**

Each MPIO group has four pins. [Table 25](#) through [Table 27](#) describe the signals assigned to each group.

**Table 25. MPIO Group A**

| MPASEL[1:0]  | ASSIGNED PIN FUNCTION          |                                |                                |                                |
|--------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
|              | MPIO_A0                        | MPIO_A1                        | MPIO_A2                        | MPIO_A3                        |
| 00           | RXIN8                          | RXIN9                          | RXIN10                         | RXIN11                         |
| 01 (Default) | CLKST                          | VOUT                           | XMCKO                          | INT0                           |
| 10           | SBCK                           | SLRCK                          | XMCKO                          | INT0                           |
| 11           | DIR Flag / GPIO <sup>(1)</sup> | DIR Flag / GPIO <sup>(1)</sup> | DIR Flag / GPIO <sup>(1)</sup> | DIR Flag / GPIO <sup>(1)</sup> |

(1) This function, DIR Flag Output or GPIO, is set for each pin by Registers MPA0FLG, MPA1FLG, MPA2FLG, and MPA3FLG.

**Table 26. MPIO Group B**

| MPBSEL[1:0]   | ASSIGNED PIN FUNCTION          |                                |                                |                                |
|---------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
|               | MPIO_B0                        | MPIO_B1                        | MPIO_B2                        | MPIO_B3                        |
| 000 (Default) | ASCKI2                         | ABCKI2                         | ALRCKI2                        | ADIN2                          |
| 001           | ASCKO                          | ABCKO                          | ALRCKO                         | ADOUT                          |
| 010           | SFSOUT3                        | SFSOUT2                        | SFSOUT1                        | SFSOUT0                        |
| 011           | DIR Flag / GPIO <sup>(1)</sup> | DIR Flag / GPIO <sup>(1)</sup> | DIR Flag / GPIO <sup>(1)</sup> | DIR Flag / GPIO <sup>(1)</sup> |
| 100           | BFRAME                         | COUT                           | UOUT                           | VOUT                           |
| 101           | EASCKO                         | EABCKO                         | EALRCKO                        | EADIN                          |
| 110           | Reserved                       | Reserved                       | Reserved                       | Reserved                       |
| 111           | Test Mode                      | Test Mode                      | Test Mode                      | Test Mode                      |

(1) This function, DIR Flag Output or GPIO, is set for each pin by Registers MPB0FLG, MPB1FLG, MPB2FLG, and MPB3FLG.

**Table 27. MPIO Group C**

| MPCSEL[1:0]   | ASSIGNED PIN FUNCTION          |                                |                                |                                |
|---------------|--------------------------------|--------------------------------|--------------------------------|--------------------------------|
|               | MPIO_C0                        | MPIO_C1                        | MPIO_C2                        | MPIO_C3                        |
| 000 (Default) | ASCKI1                         | ABCKI1                         | ALRCKI1                        | ADIN1                          |
| 001           | Reserved                       | Reserved                       | Reserved                       | Reserved                       |
| 010           | SFSOUT3                        | SFSOUT2                        | SFSOUT1                        | SFSOUT0                        |
| 011           | DIR Flag / GPIO <sup>(1)</sup> | DIR Flag / GPIO <sup>(1)</sup> | DIR Flag / GPIO <sup>(1)</sup> | DIR Flag / GPIO <sup>(1)</sup> |
| 100           | BFRAME                         | COUT                           | UOUT                           | VOUT                           |
| 101           | TXSCK                          | TXBCK                          | TXLRCK                         | TXDIN                          |
| 110           | Reserved                       | Reserved                       | Reserved                       | Reserved                       |
| 111           | Reserved                       | Reserved                       | Reserved                       | Reserved                       |

(1) This function, DIR Flag Output or GPIO, is set for each pin by Registers MPC0FLG, MPC1FLG, MPC2FLG, and MPC3FLG.

## Default Routing Function (After RESET)

The default routing paths are shown in [Figure 15](#) in blue. MPIO\_A0-A3 are selected by CLKST, VOUT, XMCKO, and INT0. Note that by default, MPIO\_A0-A3 pins are *Hi-Z* as set by Registers MPA0HZ, MPA1HZ, MPA2HZ, and MPA3HZ.

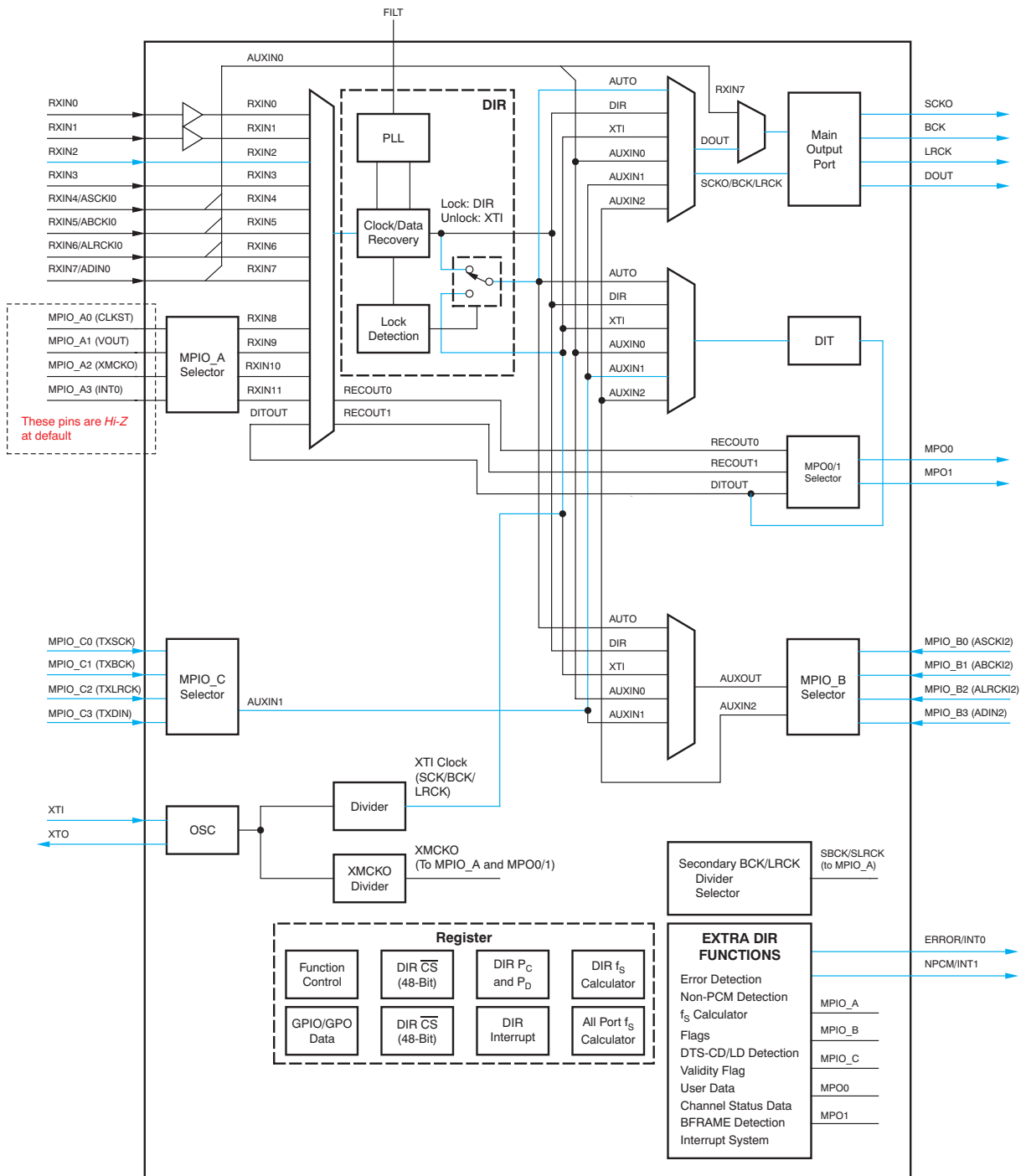


Figure 15. Default Routing Block Diagram

By default, the DIR receives data on RXIN2. When the DIR is unlocked, the XTI has priority, and uses the Main port. When the DIR is locked, data from the MAIN PORT are DIR data.

## Multi-Channel PCM Routing Function

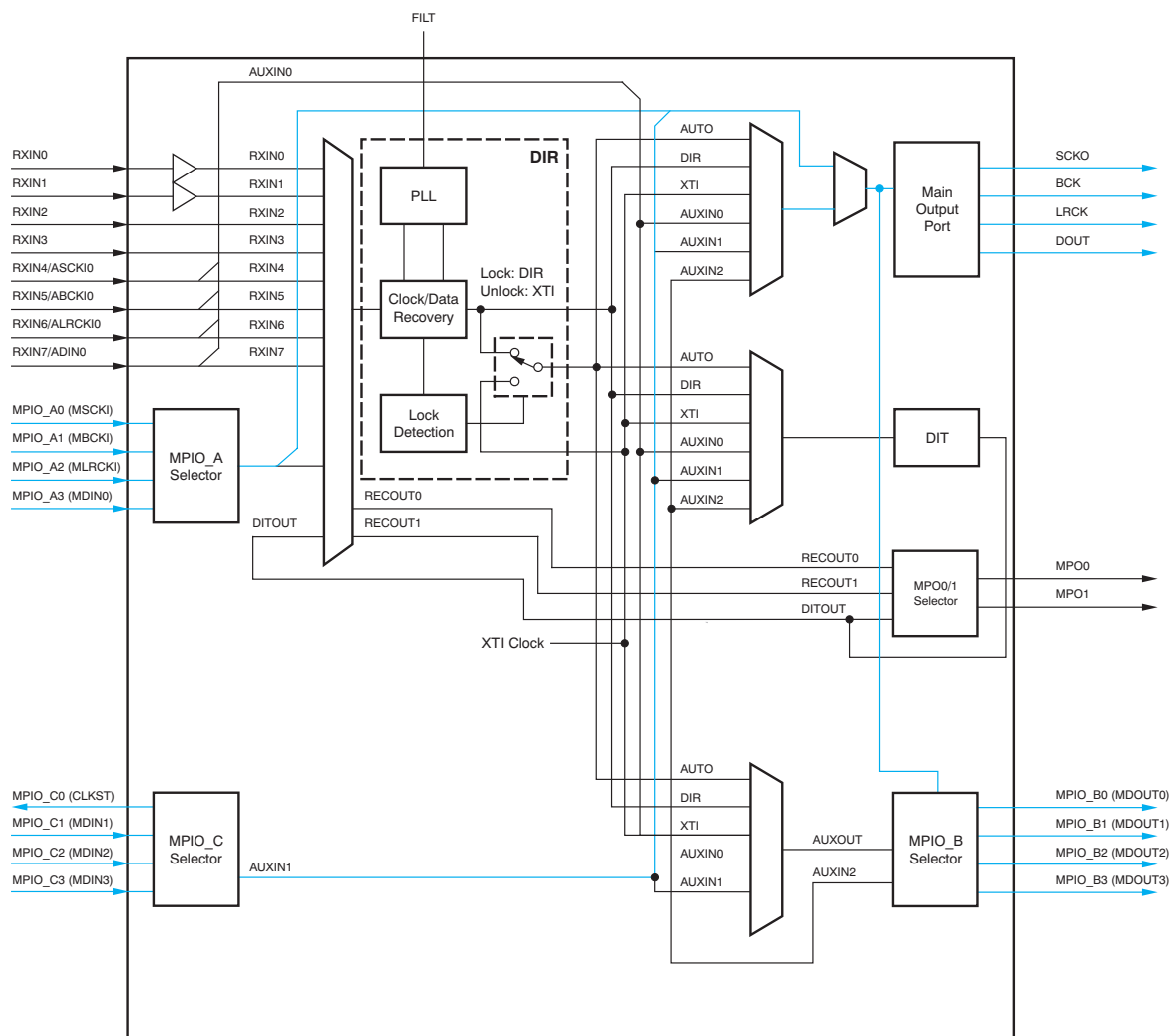
### Overview

The DIX9211 has a multi-channel PCM routing function (maximum of eight channels) that can route multi-channel PCM signals easily. This function is enabled by using all the MPIOs.

MPIO\_A and MPIO\_C are assigned as multi-channel PCM input ports and clock transition outputs (CLKST).

MPIO\_B and the Main audio port are assigned as multi-channel PCM output ports. For some applications, these multi-channel PCM output ports have five data pins. The DOUT pin and the MDOUT pin share the same data.

A detailed block diagram is shown in [Figure 16](#).



Note: Blue lines are default signal path.

**Figure 16. Multi-Channel PCM Routing Block Diagram**

## Initial Setting

To use the multi-channel function, set Register MCHR to '1'. In the multi-channel function, the assigned MPIO function for Registers MPASEL[1:0], MPBSEL[2:0], and MPCSEL[2:0], are invalid; in other words, Register MCHR has greater priority than Registers MPASEL[1:0], MPBSLE[2:0], and MPCSEL[2:0].

### NOTE

In multi-channel PCM mode, Register MCHR (20h) and Register MPAXHz (6Eh) must be set to '0' in order to get the outputs from the main port.

## Output Source Selection

The output source for Multi-Channel PCM Output (the Main output port and MPIO\_B) is selected by a register. [Table 28](#) describes the relationship between the output source and the register (MCHRSRC) setting.

**Table 28. Multi-Channel PCM Output Source and Register Setting**

| MULTI-CHANNEL MODE<br>OUTPUT SOURCE SELECT | MCHRSRC                 |                |
|--------------------------------------------|-------------------------|----------------|
|                                            | '00' or '10'            | '01' or '11'   |
| CLOCK SOURCE                               | MAIN OUT <sup>(1)</sup> | MULTI-CH INPUT |
| DOUT                                       | MAIN OUT <sup>(1)</sup> | MDIN0          |
| MDOUT0                                     | MAIN OUT <sup>(1)</sup> | MDIN0          |
| MDOUT1                                     | Logic low               | MDIN1          |
| MDOUT2                                     | Logic low               | MDIN2          |
| MDOUT3                                     | Logic low               | MDIN3          |

(1) The *Main OUT* data source is discussed in the [DIR](#) section of this data sheet. It can either be the DIR recovered clock and data, or the XTI clock source.

## DSD Input Mode

The DIX9211 can also be used to suppress the jitter of the DSCKI signals, typically generated by an HDMI receiver. DSD signals (DBCKI, DSDRI, DSDLI) are routed to the Main Port as DBCKO, DSDRO, and DSDLO, respectively.

The DIT works with DSCKI for SCK, DBCKI for BCK, internally-created LRCK, DBCKI divided by 64, and '0' data for DIN.

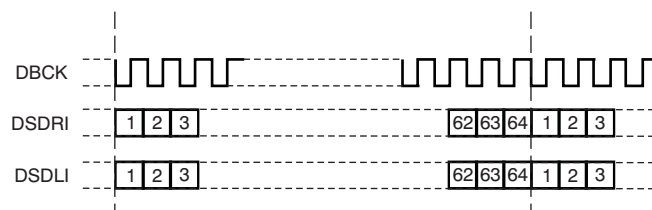
MOLRMTEN (Register 6Ah) can be used to mute/unmute DSDRO from the LRCK port. When MOLRMTEN is set to '1', mute/unmute of DSDRO from LRCK is available by MODMUT = 1/0.

[Table 29](#) summarizes the DSD input mode configuration.

**Table 29. DSD Input Mode Summary**

| SIGNAL NAME | MPIO GROUP / PIN   | DESCRIPTION                                                         |
|-------------|--------------------|---------------------------------------------------------------------|
| DSCKI       | MPIO_C0 or MPIO_B0 | SCK input (256f <sub>S</sub> )                                      |
| DBCKI       | MPIO_C1 or MPIO_B1 | DBCK input for DSD format (64f <sub>S</sub> )                       |
| DSDRI       | MPIO_C2 or MPIO_B2 | R-channel DSD data input for DSD format                             |
| DSDLI       | MPIO_C3 or MPIO_B3 | L-channel DSD data input for DSD format                             |
| DSCKO       | SCKO               | SCK output generated by DIR from DIT output                         |
| DBCKO       | BCK                | DBCK output for DSD format (the same signal as DBCKI)               |
| DSDRO       | LRCK               | R-channel DSD data output for DSD format (the same signal as DSDRI) |
| DSDLO       | DOUT               | L-channel DSD data output for DSD format(the same signal as DSDLI)  |

Figure 17 illustrates the DSD format.



**Figure 17. DSD Format**

### Typical Register Settings

Table 30 and Table 31 show the typical register settings for DSD format.

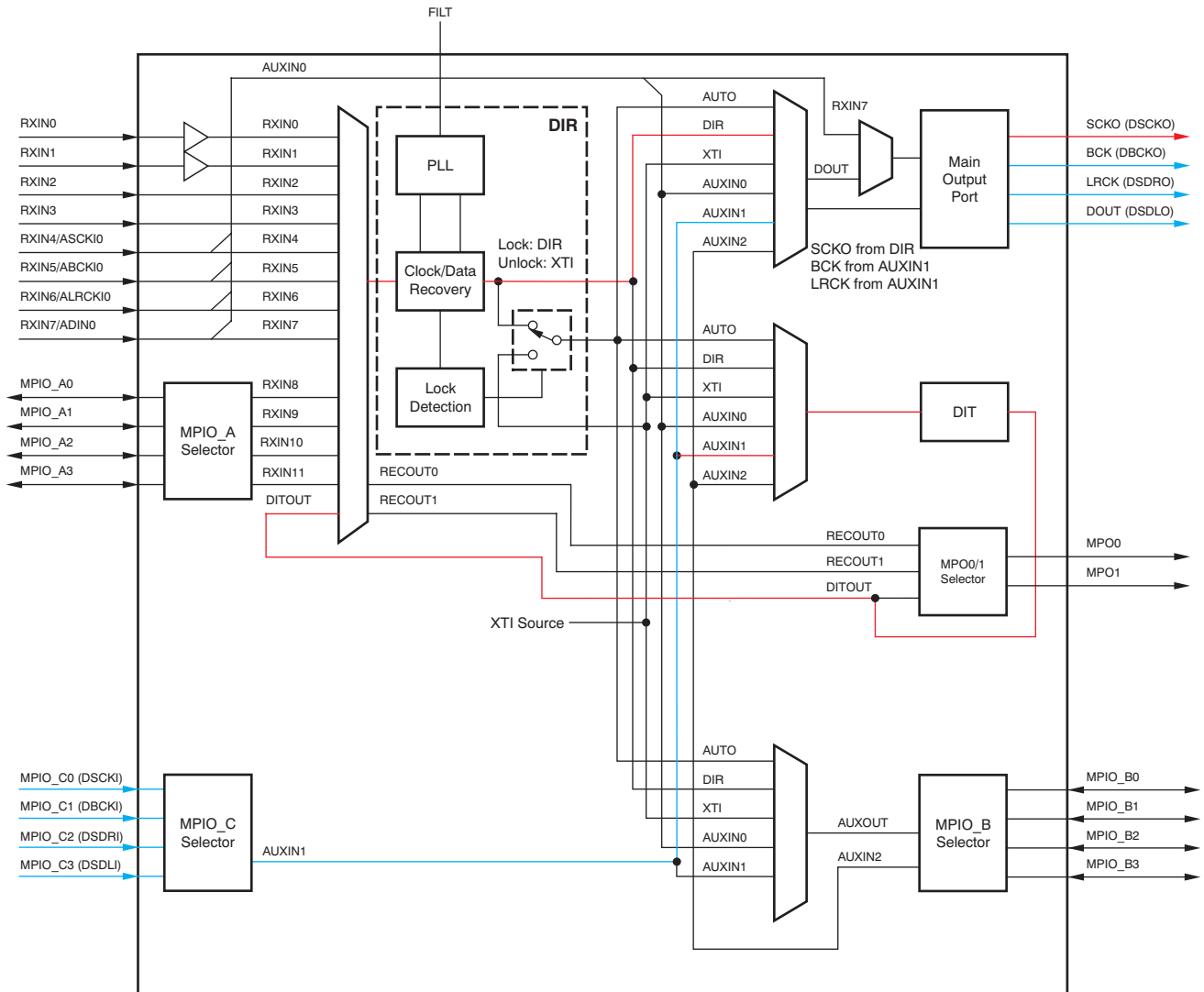
**Table 30. DSD Inputs From MPIO\_Cx Ports**

| REGISTER SETTINGS | DESCRIPTIONS                    |
|-------------------|---------------------------------|
| 34h = CFh         | RXSEL = TXOUT                   |
| 61h = 14h         | TXDSD = Enable                  |
| 6Bh = 14h         | MOSSRC = DIR<br>MOPSRC = AUXIN1 |

**Table 31. DSD Inputs From MPIO\_Bx Ports**

| REGISTER SETTINGS | DESCRIPTIONS                       |
|-------------------|------------------------------------|
| 34h = CFh         | RXSEL = TXOUT                      |
| 60h = 55h         | TXSSRC = AUXIN2<br>TXPSRC = AUXIN2 |
| 61h = 14h         | TXDSD = Enable                     |
| 6Bh = 14h         | MOSSRC = DIR<br>MOPSRC = AUXIN1    |

Figure 18 shows a block diagram of DSD Input Mode (this illustration includes an example of DSD input = MPIO\_Cx pins).



Note: Blue lines are through-paths for DBCKI, DSDRI, and DSDLI. Red lines are DSCKO generation paths.

**Figure 18. DSD Input Mode Block Diagram**

## Serial Control Mode

The DIX9211 supports two types of control interface, which are set using the MODE pin (pin 27), as defined in [Table 32](#).

**Table 32. Mode Control Interface Types**

| MODE         | MODE CONTROL INTERFACE                     |
|--------------|--------------------------------------------|
| Tied to DGND | Two-wire (I <sup>2</sup> C) serial control |
| Tied to VDD  | Four-wire (SPI) serial control             |

The input state of the MODE pin is only sampled during a power-on reset or external reset event. Therefore, any change after device power on or external reset is ignored.

[Table 33](#) shows the pin assignments based on the control interface selected.

**Table 33. Pin Assignments for SPI and I<sup>2</sup>C Control Interfaces**

| PIN | DEFINITION |                       |
|-----|------------|-----------------------|
|     | SPI MODE   | I <sup>2</sup> C MODE |
| 23  | MDO        | ADR0                  |
| 24  | MDI        | SDA                   |
| 25  | MC         | SCL                   |
| 26  | MS         | ADR1                  |

## Four-Wire (SPI) Serial Control

The DIX9211 includes an SPI-compatible serial port, which operates asynchronously to the audio serial interface. The control interface consists of these data sources: MDI/SDA, MS/ADR1, MC/SCL, and MDO/ADR0.

- MDI is the serial data input to program the mode control registers. In other applications, this source may be known as *MOSI*.
- MDO is the serial data output to read back register settings and some flags. In other applications, this source may be known as *MISO*.
- MC is the serial bit clock to shift the data into the control port. In other applications, this clock may be known as *SCK*.
- MS is the select input to enable the mode control port. In other applications, this control may be known as an *active-low Chip Select (CS)*.

## Control Data Word Format

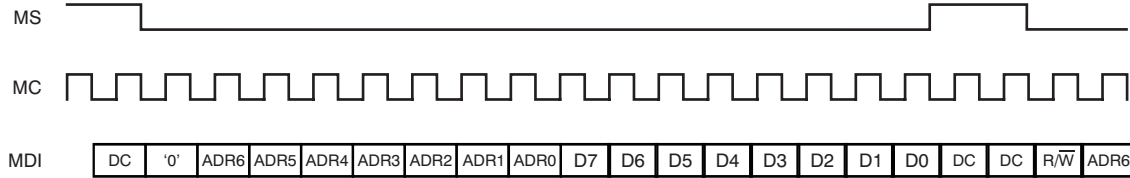
All single write/read operations via the serial control port use 16-bit data words. [Figure 19](#) shows the control data word format. The first bit is for read/write control, where '0' indicates a write operation and '1' shows a read operation. The next seven bits, labeled ADR[6:0], set the register address for the write/read operation. The least significant eight bits, D[7:0] on MDI or MDO, contain the data to be written to (or read from) the register specified by ADR[6:0].



**Figure 19. Control Data Word Format for MDI**

## Register Write Operation

Figure 20 shows the functional timing diagram for a single write operation on the serial control port. MS is held at '1' until a register must be written. To start the register write cycle, MS should be set to '0'. 16 clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI. After the 16th clock cycle has been completed, MS is set to '1' to latch the data into the indexed mode control register.



**Figure 20. Register Write Operation**

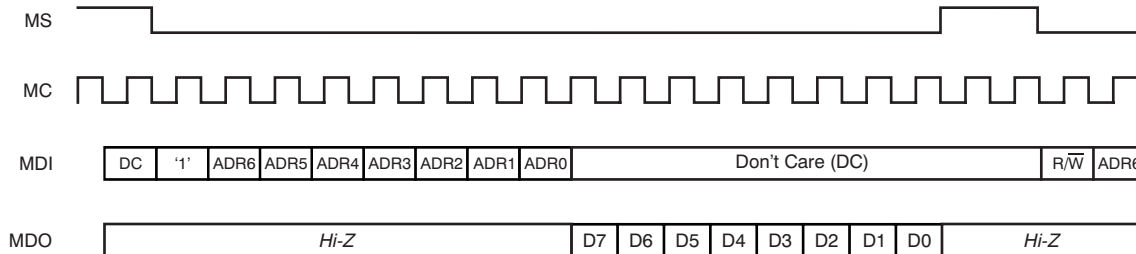
Channel status data are available from the Channel Status registers. To read the first 48 bits of the Channel Status registers accurately, the read should be started  $48f_s$  after the start of the block. However, once MS is pulled to '0', there are no time requirements in which to read the data because the registers are locked.

Both INT0 and INT1 can also be masked to highlight when the Channel Status has been updated. In many cases, Channel Status does not change during playback (of a movie or music). Once the source changes, though, the Channel Status changes. This change causes an interrupt, which can then be used to trigger the DSP to read the Channel Status registers. The interrupt source is called *OCSRNWx* (Output Channel Status Renewal).

The OCSRNWx flag can be held in the INTx register, or masked and brought out to the ERR/INT0 or NPCM/INT1 pin.

## Register Read Operation

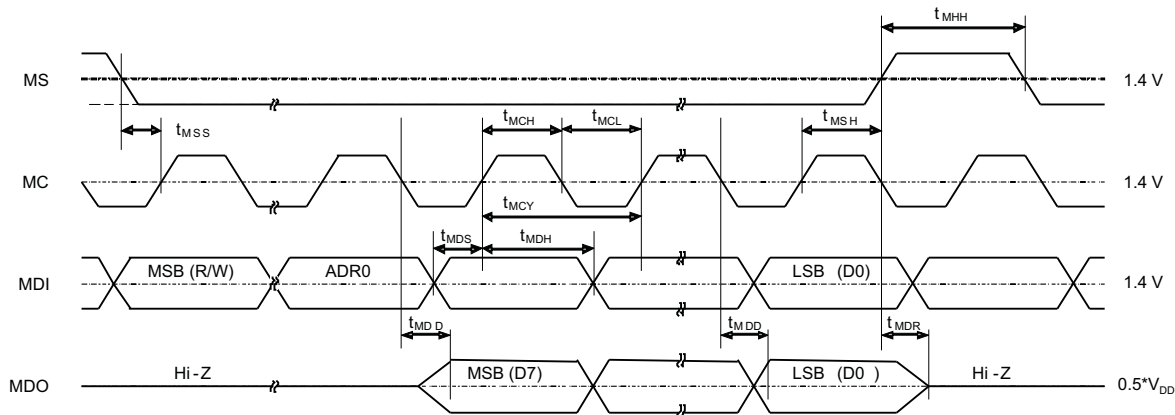
Figure 21 shows the functional timing diagram for single read operations on the SPI serial control port. MS is held high until a register is to be read. To start the register read cycle, MS is set to a *low* state. 16 clocks are then provided on MC, corresponding to the first eight bits of the control data word on MDI, and second eight bits of the read-back data word from MDO. After the 16th clock cycle has been completed, MS is set to *high* for next write or read operation. MDO remains in a *Hi-Z* (or high impedance) state except for a period of eight MC clocks for actual data transfer.



**Figure 21. Register Read Operation**

## Timing Requirements

Figure 22 shows a detailed timing diagram for the four-wire serial control interface. These timing parameters are critical for proper control port operation.



| SYMBOL    | DESCRIPTION                                   | MIN       | MAX | UNITS |
|-----------|-----------------------------------------------|-----------|-----|-------|
| $t_{MCY}$ | MC Pulse cycle time                           | 100       |     | ns    |
| $t_{MCL}$ | MC Low level time                             | 40        |     | ns    |
| $t_{MCH}$ | MC High level time                            | 40        |     | ns    |
| $t_{MHH}$ | MS High level time                            | $t_{MCY}$ |     | ns    |
| $t_{MSS}$ | MS Falling edge to MC rising edge             | 30        |     | ns    |
| $t_{MSH}$ | MS Rising edge from MC rising edge for LSB    | 15        |     | ns    |
| $t_{MDH}$ | MDI Hold time                                 | 15        |     | ns    |
| $t_{MDS}$ | MDI Set-up time                               | 15        |     | ns    |
| $t_{MDD}$ | MDO Enable or delay time from MC falling edge | 0         | 30  | ns    |
| $t_{MDR}$ | MDO Disable time from MS rising edge          | 0         | 30  | ns    |

**Figure 22. Control Interface Timing Requirements**

## Two-Wire (I<sup>2</sup>C) Serial Control

The DIX9211 also supports the I<sup>2</sup>C serial bus and data transmission protocol. It can be configured for fast mode as a slave device. This protocol is explained fully in the [I<sup>2</sup>C specification 2.1](#).

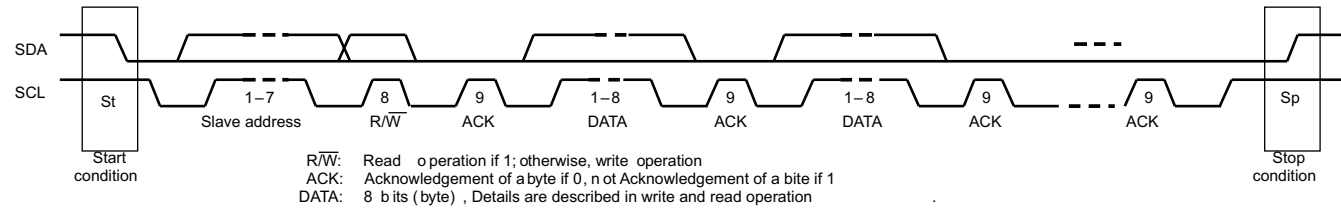
### Slave Address

| MSB |   |   |   |   | LSB  |      |                   |
|-----|---|---|---|---|------|------|-------------------|
| 1   | 0 | 0 | 0 | 0 | ADR1 | ADR0 | R/ $\overline{W}$ |

The DIX9211 has seven bits for its own slave address. The first five bits (MSB) of the slave address are factory-preset to '10000'. The next two bits of the address byte are selectable bits that can be set by MDO/ADR0 and MS/ADR1. A maximum of four DIX9211s can be connected on the same bus at one time. Each DIX9211 responds when it receives its own slave address.

## Packet Protocol

A master device must control the packet protocol, which consists of a start condition, slave address with read/write bit, data if a write procedure is desired, or an acknowledgment if read and stop conditions exist. The DIX9211 supports both slave receiver and transmitter functions. Details of the DATA pulse for both write and read operations are described in [Figure 23](#).



### Figure 23. I<sup>2</sup>C Packet Protocol

## Write Operation

The DIX9211 can only function as an I<sup>2</sup>C slave. A master can write to any DIX9211 registers using either single or multiple accesses. The master sends a DIX9211 slave address with a write bit, a register address, and the data. When undefined registers are accessed, the DIX9211 does not send an acknowledgment. [Figure 24](#) illustrates the write operation. The register address and the write data are 8-bit, MSB-first format.

|             |     |               |                |     |             |     |              |     |              |     |  |     |     |
|-------------|-----|---------------|----------------|-----|-------------|-----|--------------|-----|--------------|-----|--|-----|-----|
| Transmitter | $M$ | $M$           | $\overline{M}$ | $S$ | $M$         | $S$ | $M$          | $S$ | $M$          | $S$ |  | $S$ | $M$ |
| Data Type   | St  | slave address | $\overline{W}$ | ACK | reg address | ACK | write data 1 | ACK | write data 2 | ACK |  | ACK | Sp  |

M: Master Device S: Slave Device St: Start Condition  $\overline{W}$ : Write ACK: Acknowledge Sp: Stop Condition

### Figure 24. Framework for Write Operation

## Read Operation

A master can read the DIX9211 registers. The value of the register address is stored in an indirect index register in advance. The master sends the DIX9211 slave address with a read bit after storing the register address. The DIX9211 then transfers the data to which the index register points. [Figure 25](#) shows the read operation.

|             |     |               |                |     |             |     |     |               |     |     |           |      |     |
|-------------|-----|---------------|----------------|-----|-------------|-----|-----|---------------|-----|-----|-----------|------|-----|
| Transmitter | $M$ | $M$           | $M$            | $S$ | $M$         | $S$ | $M$ | $M$           | $M$ | $S$ | $S$       | $M$  | $M$ |
| Data Type   | St  | slave address | $\overline{W}$ | ACK | reg address | ACK | Sr  | slave address | R   | ACK | read data | NACK | Sp  |

M: Master Device S: Slave Device St: Start Condition Sr: Repeated Start Condition  $\overline{W}$ : Write R: Read

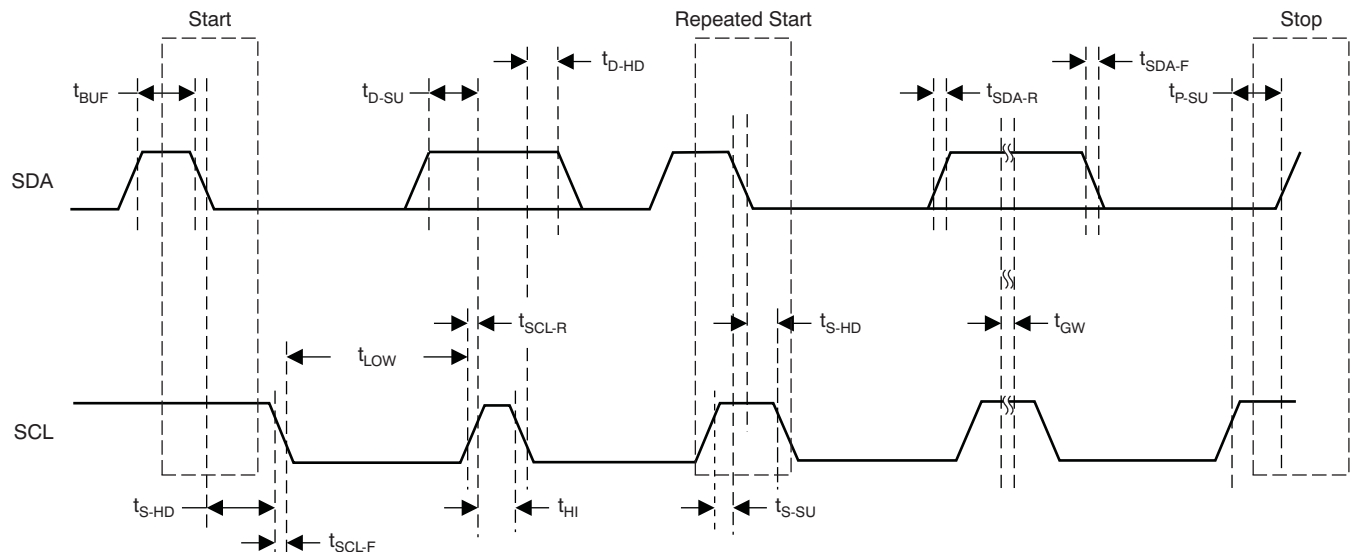
ACK: Acknowledge NACK: Not Acknowledge Sp: Stop Condition

Note: The slave address after the repeated start condition must be the same as the previous slave address.

### Figure 25. Framework for Read Operation

## Timing Diagram

Figure 26 shows the detailed timing diagram for SCL and SDA.



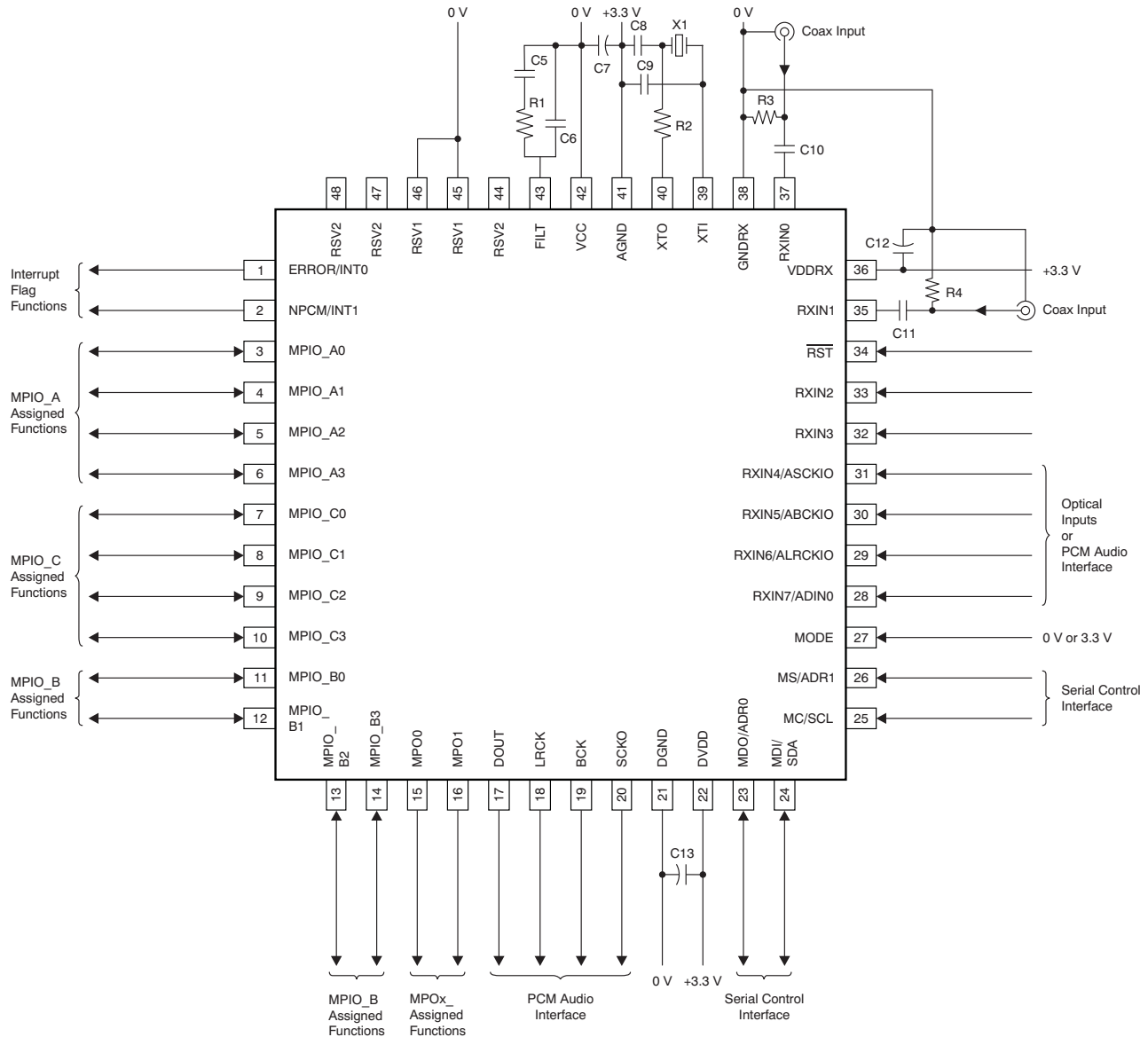
| SYMBOL      | DESCRIPTION                                                                 | STANDARD MODE       |      | FAST MODE            |     | UNITS   |
|-------------|-----------------------------------------------------------------------------|---------------------|------|----------------------|-----|---------|
|             |                                                                             | MIN                 | MAX  | MIN                  | MAX |         |
| $f_{SCL}$   | SCL clock frequency                                                         |                     | 100  |                      | 400 | kHz     |
| $t_{BUF}$   | Bus free time between STOP and START condition                              | 4.7                 |      | 1.3                  |     | $\mu$ s |
| $t_{LOW}$   | Low period of the SCL clock                                                 | 4.7                 |      | 1.3                  |     | $\mu$ s |
| $t_{HI}$    | High period of the SCL clock                                                | 4.0                 |      | 0.6                  |     | $\mu$ s |
| $t_{S-SU}$  | Setup time for START/Repeated START condition                               | 4.7                 |      | 0.6                  |     | $\mu$ s |
| $t_{S-HD}$  | Hold time for START/Repeated START condition                                | 4.0                 |      | 0.6                  |     | $\mu$ s |
| $t_{D-SU}$  | Data setup time                                                             | 250                 |      | 100                  |     | ns      |
| $t_{D-HD}$  | Data hold time                                                              | 0                   | 3450 | 0                    | 900 | ns      |
| $t_{SCL-R}$ | Rise time of SCL signal                                                     |                     | 1000 | $20 + 0.1C_B$        | 300 | ns      |
| $t_{SCL-F}$ | Fall time of SCL signal                                                     |                     | 1000 | $20 + 0.1C_B$        | 300 | ns      |
| $t_{SDA-R}$ | Rise time of SDA signal                                                     |                     | 1000 | $20 + 0.1C_B$        | 300 | ns      |
| $t_{SDA-F}$ | Fall time of SDA signal                                                     |                     | 1000 | $20 + 0.1C_B$        | 300 | ns      |
| $t_{P-SU}$  | Setup time for STOP condition                                               | 4.0                 |      | 0.6                  |     | $\mu$ s |
| $t_{GW}$    | Allowable glitch width                                                      |                     | n/a  |                      | 50  | ns      |
| $C_B$       | Capacitive load for SDA and SCL line                                        |                     | 400  |                      | 100 | pF      |
| $V_{NH}$    | Noise margin at High level for each connected device (including hysteresis) | $0.2 \times V_{DD}$ |      | $0.2 \times V_{DD}$  |     | V       |
| $V_{NL}$    | Noise margin at Low level for each connected device (including hysteresis)  | $0.1 \times V_{DD}$ |      | $0.1 \times V_{DD}$  |     | V       |
| $V_{HYS}$   | Hysteresis of Schmitt-trigger input                                         | n/a                 |      | $0.05 \times V_{DD}$ |     | V       |

Figure 26. Control Interface Timing

## APPLICATION INFORMATION

### TYPICAL CIRCUIT CONNECTION

Figure 27 illustrates a typical circuit connection.



R1: Loop filter resistor, 680  $\Omega$ .

R2: Current-limiting resistor; generally, a 100- $\Omega$  to 500- $\Omega$  resistor is used, but it depends on the crystal resonator.

R3, R4: Coax input termination resistors, 75  $\Omega$ .

C7, C12, C13: 0.1- $\mu$ F ceramic capacitor and 10- $\mu$ F electrolytic capacitor, depending on the power supply.

C5: Loop filter capacitor, 0.068 mF.

C6: Loop filter capacitor, 0.0047 mF.

C8, C9: OSC load capacitor; generally, a 10-pF to 30-pF capacitor is used, but it depends on the crystal resonator and PCB layout.

C10, C11: DC blocking capacitor for coax input, 0.1  $\mu$ F.

X1: Crystal resonator. Use a 24.576-MHz fundamental resonator when the XTI clock source is needed.

**Figure 27. Typical Circuit Connection**

## REGISTER INFORMATION

Table 34. REGISTER MAP

| ADR | REGISTER DESCRIPTION                                                        | R/W | B7      | B6       | B5      | B4       | B3       | B2       | B1      | B0      |
|-----|-----------------------------------------------------------------------------|-----|---------|----------|---------|----------|----------|----------|---------|---------|
| 20h | ERROR Output Condition and Shared Port Settings                             | R/W | RSV     | ERRCON   | MCHR    | RSV      | ERRHZ    | ERRSEL   | NPCMHZ  | NPCMSEL |
| 21h | DIR Initial Settings 1/3                                                    | R/W | RSV     | RSV      | RSV     | RXFSRNG  | RSV      | RSV      | RSV     | RSV     |
| 22h | DIR Initial Settings 2/3                                                    | R/W | RSV     | CLKSTCON | RSV     | CLKSTP   | RSV      | RSV      | RSV     | RXVDLY  |
| 23h | DIR Initial Settings 3/3                                                    | R/W | RSV     | RSV      | XTIWT1  | XTIWT0   | PRTPRO1  | PRTPRO0  | ERRWT1  | ERRWT0  |
| 24h | Oscillation Circuit Control                                                 | R/W | OSCAUTO | RSV      | RSV     | XMCKEN   | XMCKDIV1 | XMCKDIV0 | RSV     | RSV     |
| 25h | ERROR Cause Setting                                                         | R/W | RSV     | RSV      | EFSCHG  | EFSLMT   | ENPCM    | EVALID   | EPARITY | EUNLOCK |
| 26h | AUTO Source Selector Cause Setting                                          | R/W | RSV     | AERROR   | RSV     | AFSLMT   | ANPCM    | AVALID   | RSV     | AUNLOCK |
| 27h | DIR Acceptable $f_s$ Range Setting and Mask                                 | R/W | MSK128  | MSK64    | RSV     | NOMLMT   | HILMT1   | HILMT0   | LOLMT1  | LOLMT0  |
| 28h | Non-PCM Definition Setting                                                  | R/W | RSV     | RSV      | CS1BPLS | NPCMP    | RSV      | DTSCD    | PAPB    | CSBIT1  |
| 29h | DTS CD/LD Detection Setting                                                 | R/W | RSV     | RSV      | RSV     | RSV      | DTS16    | DTS14    | DTSPRD1 | DTSPRD0 |
| 2Ah | INT0 Output Cause Mask Setting                                              | R/W | MERROR0 | MNPCM0   | MEMPHF0 | MDTSCD0  | MCSRNW0  | MPCRNW0  | MFSCHG0 | RSV     |
| 2Bh | INT1 Output Cause Mask Setting                                              | R/W | MERROR1 | MNPCM1   | MEMPHF1 | MDTSCD1  | MCSRNW1  | MPCRNW1  | MFSCHG1 | RSV     |
| 2Ch | INT0 Output Register                                                        | R   | OERROR0 | ONPCM0   | OEMPHF0 | ODTSCD0  | OCSRNW0  | OPCRNW0  | OFSCHG0 | RSV     |
| 2Dh | INT1 Output Register                                                        | R   | OERROR1 | ONPCM1   | OEMPHF1 | ODTSCD1  | OCSRNW1  | OPCRNW1  | OFSCHG1 | OADLVL1 |
| 2Eh | INT0, INT1 Output Polarity Setting                                          | R/W | RSV     | INT1P    | RSV     | RSV      | RSV      | INT0P    | RSV     | RSV     |
| 2Fh | DIR Output Data Format                                                      | R/W | RSV     | RSV      | RSV     | RSV      | RSV      | RXFMT2   | RXFMT1  | RXFMT0  |
| 30h | DIR Recovered System Clock Ratio Setting                                    | R/W | RSV     | RSV      | RSV     | PSCKAUTO | RSV      | PSCK2    | PSCK1   | PSCK0   |
| 31h | XTI Source Clock Frequency Setting                                          | R/W | RSV     | RSV      | XSCCK1  | XSCCK0   | XBCK1    | XBCK0    | XLRCK1  | XLRCK0  |
| 32h | DIR Source, Sec. Bit/LR Clock Frequency Setting                             | R/W | RSV     | PSBCK2   | PSBCK1  | PSBCK0   | RSV      | PSLRCK2  | PSLRCK1 | PSLRCK0 |
| 33h | XTI Source, Sec. Bit/LR Clock Frequency Setting                             | R/W | RSV     | XSBACK2  | XSBACK1 | XSBACK0  | RSV      | XSLRCK2  | XSLRCK1 | XSLRCK0 |
| 34h | DIR Input Biphase Source Select, Coax Amp. Control                          | R/W | RX0DIS  | RX1DIS   | RSV     | RSV      | RXSEL3   | RXSEL2   | RXSEL1  | RXSEL0  |
| 35h | RECOU0 Output Biphase Source Select                                         | R/W | RSV     | RSV      | RSV     | MPO0MUT  | RO0SEL3  | RO0SEL2  | RO0SEL1 | RO0SEL0 |
| 36h | RECOU1 Output Biphase Source Select                                         | R/W | RSV     | RSV      | RSV     | MPO1MUT  | RO1SEL3  | RO1SEL2  | RO1SEL1 | RO1SEL0 |
| 37h | Port $f_s$ Calculator Measurement Target Setting                            | R/W | RSV     | RSV      | RSV     | RSV      | RSV      | PFSTGT2  | PFSTGT1 | PFSTGT0 |
| 38h | Port $f_s$ Calculator Result Output                                         | R   | PFSST   | PFSP02   | PFSP01  | PFSP00   | PFSOUT3  | PFSOUT2  | PFSOUT1 | PFSOUT0 |
| 39h | Incoming Biphase Information and Calculated $f_s$ Output                    | R   | SFSST   | SCSBIT1  | RSV     | RSV      | SFSOUT3  | SFSOUT2  | SFSOUT1 | SFSOUT0 |
| 3Ah | P <sub>C</sub> Buffer Byte0 (Burst Preamble P <sub>C</sub> Output Register) | R   | PC7     | PC6      | PC5     | PC4      | PC3      | PC2      | PC1     | PC0     |
| 3Bh | P <sub>C</sub> Buffer Byte1 (Burst Preamble P <sub>C</sub> Output Register) | R   | PC15    | PC14     | PC13    | PC12     | PC11     | PC10     | PC9     | PC8     |
| 3Ch | P <sub>D</sub> Buffer Byte0 (Burst Preamble P <sub>D</sub> Output Register) | R   | PD7     | PD6      | PD5     | PD4      | PD3      | PD2      | PD1     | PD0     |
| 3Dh | P <sub>D</sub> Buffer Byte1 (Burst Preamble P <sub>D</sub> Output Register) | R   | PD15    | PD14     | PD13    | PD12     | PD11     | PD10     | PD9     | PD8     |
| 40h | System Reset Control                                                        | R/W | MRST    | RSV      | ADDIS   | RXDIS    | RSV      | RSV      | TXDIS   | XODIS   |
| 42h | External ADC Function Control                                               | R/W | RSV     | RSV      | RSV     | ADDTRX7  | RSV      | EADCLK2  | EADCLK1 | EADCLK0 |
| 5Ah | DIR Channel Status Data Buffer 1/6                                          | R   | RXCS7   | RXCS6    | RXCS5   | RXCS4    | RXCS3    | RXCS2    | RXCS1   | RXCS0   |
| 5Bh | DIR Channel Status Data Buffer 2/6                                          | R   | RXCS15  | RXCS14   | RXCS13  | RXCS12   | RXCS11   | RXCS10   | RXCS9   | RXCS8   |
| 5Ch | DIR Channel Status Data Buffer 3/6                                          | R   | RXCS23  | RXCS22   | RXCS21  | RXCS20   | RXCS19   | RXCS18   | RXCS17  | RXCS16  |
| 5Dh | DIR Channel Status Data Buffer 4/6                                          | R   | RXCS31  | RXCS30   | RXCS29  | RXCS28   | EXCS27   | RXCS26   | RXCS25  | RXCS24  |
| 5Eh | DIR Channel Status Data Buffer 5/6                                          | R   | RXCS39  | RXCS38   | RXCS37  | RXCS36   | RXCS35   | RXCS34   | RXCS33  | RXCS32  |
| 5Fh | DIR Channel Status Data Buffer 6/6                                          | R   | RXCS47  | RXCS46   | RXCS45  | RXCS44   | RXCS43   | RXCS42   | RXCS41  | RXCS40  |
| 60h | DIT Function Control 1/3                                                    | R/W | RSV     | TXSSRC2  | TXSSRC1 | TXSSRC0  | RSV      | TXPSRC2  | TXPSRC1 | TXPSRC0 |
| 61h | DIT Function Control 2/3                                                    | R/W | RSV     | TXSCK2   | TXSCK1  | TXSCK0   | RSV      | RSV      | TXFMT1  | TXFMT0  |
| 62h | DIT Function Control 3/3                                                    | R/W | RSV     | RSV      | TXDMUT  | RSV      | TXVFLG   | RSV      | RSV     | RSV     |
| 63h | DIT Channel Status Data Buffer 1/6                                          | R/W | TXCS7   | TXCS6    | TXCS5   | TXCS4    | TXCS3    | TXCS2    | TXCS1   | TXCS0   |
| 64h | DIT Channel Status Data Buffer 2/6                                          | R/W | TXCS15  | TXCS14   | TXCS13  | TXCS12   | TXCS11   | TXCS10   | TXCS9   | TXCS8   |
| 65h | DIT Channel Status Data Buffer 3/6                                          | R/W | TXCS23  | TXCS22   | TXCS21  | TXCS20   | TXCS19   | TXCS18   | TXCS17  | TXCS16  |
| 66h | DIT Channel Status Data Buffer 4/6                                          | R/W | TXCS31  | TXCS30   | TXCS29  | TXCS28   | TXCS27   | TXCS26   | TXCS25  | TXCS24  |
| 67h | DIT Channel Status Data Buffer 5/6                                          | R/W | TXCS39  | TXCS38   | TXCS37  | TXCS36   | TXCS35   | TXCS34   | TXCS33  | TXCS32  |
| 68h | DIT Channel Status Data Buffer 6/6                                          | R/W | TXCS47  | TXCS46   | TXCS45  | TXCS44   | TXCS43   | TXCS42   | TXCS41  | TXCS40  |

**Table 34. REGISTER MAP (continued)**

| ADR | REGISTER DESCRIPTION                          | R/W | B7       | B6       | B5       | B4       | B3       | B2       | B1           | B0       |
|-----|-----------------------------------------------|-----|----------|----------|----------|----------|----------|----------|--------------|----------|
| 6Ah | Main Output and AUXOUT Port Data Mute Control | R/W | AOMUTAS  | MOMUTAS  | RSV      | RSV      | AOLRMTEN | AODMUT   | MOLRMTE<br>N | MODMUT   |
| 6Bh | Main Output Port, Output Source Setting       | R/W | RSV      | MOSSRC2  | MOSSRC1  | MOSSRC0  | RSV      | MOPSRC2  | MOPSRC1      | MOPSRC0  |
| 6Ch | AUX Output Port, Output Source Setting        | R/W | RSV      | AOSSRC2  | AOSSRC1  | AOSSRC0  | RSV      | AOPSRC2  | AOPSRC1      | AOPSRC0  |
| 6Dh | MPIO_B & Main Output Port Hi-Z Control        | R/W | MPB3HZ   | MPB2HZ   | MPB1HZ   | MPB0HZ   | SCKOHZ   | BCKHZ    | LRCKHZ       | DOUTHZ   |
| 6Eh | MPIO_C and MPIO_A Hi-Z Control                | R/W | MPC3HZ   | MPC2HZ   | MPC1HZ   | MPC0HZ   | MPA3HZ   | MPA2HZ   | MPA1HZ       | MPA0HZ   |
| 6Fh | MPIO_A, MPIO_B, MPIO_C Group Function Assign  | R/W | MPASEL1  | MPASEL0  | MPBSEL2  | MPBSEL1  | MPBSEL0  | MPCSEL2  | MPCSEL1      | MPCSEL0  |
| 70h | MPIO_A, Flags/GPIO Assign Setting             | R/W | RSV      | RSV      | MCHSRC1  | MCHSRC0  | MPA3SEL  | MPA2SEL  | MPA1SEL      | MPA0SEL  |
| 71h | MPIO_B, MPIO_C, Flags/GPIO Assign Setting     | R/W | MPB3SEL  | MPB2SEL  | MPB1SEL  | MPB0SEL  | MPC3SEL  | MPC2SEL  | MPC1SEL      | MPC0SEL  |
| 72h | MPIO_A1, MPIO_A0 Output Flag Select           | R/W | MPA1FLG3 | MPA1FLG2 | MPA1FLG1 | MPA1FLG0 | MPA0FLG3 | MPA0FLG2 | MPA0FLG1     | MPA0FLG0 |
| 73h | MPIO_A3, MPIO_A2 Output Flag Select           | R/W | MPA3FLG3 | MPA3FLG2 | MPA3FLG1 | MPA3FLG0 | MPA2FLG3 | MPA2FLG2 | MPA2FLG1     | MPA2FLG0 |
| 74h | MPIO_B1, MPIO_B0 Output Flag Select           | R/W | MPB1FLG3 | MPB1FLG2 | MPB1FLG1 | MPB1FLG0 | MPB0FLG3 | MPB0FLG2 | MPB0FLG1     | MPB0FLG0 |
| 75h | MPIO_B3, MPIO_B2 Output Flag Select           | R/W | MPB3FLG3 | MPB3FLG2 | MPB3FLG1 | MPB3FLG0 | MPB2FLG3 | MPB2FLG2 | MPB2FLG1     | MPB2FLG0 |
| 76h | MPIO_C1, MPIO_C0 Output Flag Select           | R/W | MPC1FLG3 | MPC1FLG2 | MPC1FLG1 | MPC1FLG0 | MPC0FLG3 | MPC0FLG2 | MPC0FLG1     | MPC0FLG0 |
| 77h | MPIO_C3, MPIO_C2 Output Flag Select           | R/W | MPC3FLG3 | MPC3FLG2 | MPC3FLG1 | MPC3FLG0 | MPC2FLG3 | MPC2FLG2 | MPC2FLG1     | MPB2FLG0 |
| 78h | MPO1, MPO0 Function Assign Setting            | R/W | MPO1SEL3 | MPO1SEL2 | MPO1SEL1 | MPO1SEL0 | MPO0SEL3 | MPO0SEL2 | MPO0SEL1     | MPO0SEL0 |
| 79h | GPIO I/O Direction control for MPIO_A, MPIO_B | R/W | GIOB3DIR | GIOB2DIR | GIOB1DIR | GIOB0DIR | GIOA3DIR | GIOA2DIR | GIOA1DIR     | GIOA0DIR |
| 7Ah | GPIO I/O Direction control for MPIO_C         | R/W | RSV      | RSV      | RSV      | RSV      | GIOC3DIR | GIOC2DIR | GIOC1DIR     | GIOC0DIR |
| 7Bh | GPIO Output Data Setting for MPIO_A, MPIO_B   | R/W | GPOB3    | GPOB2    | GPOB1    | GPOB0    | GPOA3    | GPOA2    | GPOA1        | GPOA0    |
| 7Ch | GPIO Output Data Setting for MPIO_C           | R/W | RSV      | RSV      | RSV      | RSV      | GPOC3    | GPOC2    | GPOC1        | GPOC0    |
| 7Dh | GPIO Input Data Register for MPIO_A, MPIO_B   | R   | GPIB3    | GPIB2    | GPIB1    | GPIB0    | GPIA3    | GPIA2    | GPIA1        | GPIA0    |
| 7Eh | GPIO Input Data Register for MPIO_C           | R   | RSV      | RSV      | RSV      | RSV      | GPIC3    | GPIC2    | GPIC1        | GPIC0    |

## REGISTER DESCRIPTIONS

### NOTE

Memo boxes are provided to aid in development. Record your register settings below for future reference.

### Register 20h, ERROR Output Condition and Shared Port Settings (Address: 20h, Write and Read)

| DATA          | B7  | B6     | B5   | B4  | B3    | B2     | B1     | B0      |
|---------------|-----|--------|------|-----|-------|--------|--------|---------|
| Reg Name      | RSV | ERRCON | MCHR | RSV | ERRHZ | ERRSEL | NPCMHZ | NPCMSEL |
| Default Value | 0   | 0      | 0    | 0   | 0     | 0      | 0      | 0       |
| Memo          |     |        |      |     |       |        |        |         |

#### ERRCON: ERROR Output Condition Setting

- 0: ERROR pin output is always DIR status (default)
- 1: ERROR output depends on source control MOPSRC[2:0]
  - DIR/AUTO: Output DIR status
  - Except DIR: ERROR outputs *high* (error status).

#### MCHR: MPIO/Multi-Channel PCM Routing Select

- 0: All MPIOs are controlled by MPASEL[1:0], MPBSEL[1:0], MPCSEL[2:0] (Default)
- 1: All MPIOs are assigned for Multi-Channel PCM Routing I/O.

#### ERRHZ: ERROR/INT0 Port Output Hi-Z Control

- 0: Output (default)
- 1: Hi-Z

#### ERRSEL: ERROR/INT0 Port Output Source Select

- 0: ERROR (default)
- 1: INT0

NOTE: ERRSEL must be '0' when Register 26h/AERROR = 1 or Register 42h/ADFSLMT = 1, or if the signal CLKST is used.

#### NPCMHZ: NPCM/INT1 Port Output Hi-Z Control

- 0: Output (default)
- 1: Hi-Z

#### NPCMSEL: NPCM/INT1 Port Output Source Select

- 0: NPCM (default)
- 1: INT1

### Register 21h, DIR Initial Settings 1/3 (Address: 21h, Write and Read)

| DATA          | B7  | B6  | B5  | B4      | B3  | B2  | B1  | B0  |
|---------------|-----|-----|-----|---------|-----|-----|-----|-----|
| Reg Name      | RSV | RSV | RSV | RXFSRNG | RSV | RSV | RSV | RSV |
| Default Value | 0   | 0   | 0   | 0       | 0   | 0   | 0   | 0   |
| Memo          |     |     |     |         |     |     |     |     |

#### **RXFSRNG: DIR Receivable Incoming Biphase Sampling Frequency Range Setting**

- 0: Wide Mode (7 kHz to 216 kHz) (default)
- 1: Normal Mode (28 kHz to 108 kHz)

### Register 22h, DIR Initial Settings 2/3 (Address: 22h, Write and Read)

| DATA          | B7  | B6       | B5  | B4     | B3  | B2  | B1  | B0     |
|---------------|-----|----------|-----|--------|-----|-----|-----|--------|
| Reg Name      | RSV | CLKSTCON | RSV | CLKSTP | RSV | RSV | RSV | RXVDLY |
| Default Value | 0   | 0        | 0   | 0      | 0   | 0   | 0   | 1      |
| Memo          |     |          |     |        |     |     |     |        |

#### **CLKSTCON: CLKST Output Condition Setting**

- 0: Only PLL Lock status change (default)
- 1: All events where the Main port output clock condition changes, as well as these cases:
  1. MOSSRC/MOPSRC Register is updated to XTI, AUXIN0, AUXIN1, or AUXIN2
  2. DIR and XTI are switched by DIR status when MOSSRC = 000(AUTO) and MOPSRC = 000(AUTO)
  3. Main port sampling frequency changes when PFSTGT = 101(Main output port)

#### NOTES:

- CLKST never outputs when updating MOSSRC and MOPSRC to AUTO or DIR.
- OSCAUTO must be '0' when CLKST is used because CLKST is generated by frequency counting of built-in oscillator circuit.
- To output CLKST, MOSSRC and MOPSRC are set simultaneously.

#### **CLKSTP: CLKST Polarity Setting**

- 0: Active low (default)
- 1: Active high

#### **RXVDLY: VOUT Delay Setting**

- 0: VOUT is active immediately after validity flag is detected
- 1: VOUT is active after synchronization with DOUT data (default)

**Register 23h, DIR Initial Settings 3/3  
(Address: 23h, Write and Read)**

| DATA          | B7  | B6  | B5     | B4     | B3      | B2      | B1     | B0     |
|---------------|-----|-----|--------|--------|---------|---------|--------|--------|
| Reg Name      | RSV | RSV | XTIWT1 | XTIWT0 | PRTPRO1 | PRTPRO0 | ERRWT1 | ERRWT0 |
| Default Value | 0   | 0   | 0      | 0      | 0       | 1       | 0      | 0      |
| Memo          |     |     |        |        |         |         |        |        |

**XTIWT[1:0]: Crystal OSC, Oscillation Start-up Wait Time Setting**

00: 25 ms

01: 50 ms

10: 100 ms

11: 200 ms

XTIWT is counted by the PLL generated clock.

These are the resulting values when the PLL is running with a free-run clock because of no S/PDIF input.

After these delay times, the Main Port source changes from DIR to XTI when DIR is unlocked.

**PRTPRO[1:0]: Process for Parity Error Detection**

00: No process

01: For PCM data only, an 8x continuous parity error is replaced by previous data and muted after ninth parity error at EPARITY = 1 (default)

10: For PCM and non-PCM data, an 8x continuous parity error is replaced by previous data and muted after ninth parity error at EPARITY = 1

11: Reserved (The definition of *Non-PCM* depends on the Non-PCM Definition Setting Register)

Validity flag, user bit, channel status, Non-PCM and DTS-CD detection should be refreshed by waiting more than  $192/f_S$  without any parity error.

**ERRWT[1:0]: ERROR Release Wait Time Setting**

00: ERROR Release after 48 counts of preamble *B* (Default), 192 ms at  $f_S = 48$  kHz

01: ERROR Release after 12 counts of preamble *B*

10: ERROR Release after six counts of preamble *B*

11: ERROR Release after three counts of preamble *B*

These counts are only available when DIR is unlocked or DIR sampling frequency is changed or exceeds limits defined by DIR Acceptable  $f_S$  Range Setting and Mask registers.

CLKST also uses ERRWT to release.

**Register 24h, Oscillation Circuit Control  
(Address: 24h, Write and Read)**

| DATA          | B7      | B6  | B5  | B4     | B3       | B2       | B1  | B0  |
|---------------|---------|-----|-----|--------|----------|----------|-----|-----|
| Reg Name      | OSCAUTO | RSV | RSV | XMCKEN | XMCKDIV1 | XMCKDIV0 | RSV | RSV |
| Default Value | 0       | 0   | 0   | 0      | 0        | 0        | 0   | 0   |
| Memo          |         |     |     |        |          |          |     |     |

**OSCAUTO: Oscillation Circuit Automatic Operation Control**

- 0: Built-in oscillator circuit always operates (default)
- 1: Built-in oscillator circuit is stopped during lock state of DIR but is active when DIR locks and CLKST is active

**NOTES:**

- The XODIS command has more priority than this OSCAUTO register.
- If XODIS is set to power down, the XTI source is not output.

**XMCKENX: MCKO (XTI Clock Buffered Output) Output Enable Control**

- 0: MUTE (Logic low level) (default)
- 1: Output

**XMCKDIV[1:0]: XMCKO (XTI Clock Buffered Output) Output Clock Dividing Ratio**

- 00: XTI/1 (24.576 MHz) (default)
- 01: XTI/2 (12.288 MHz)
- 10: XTI/4 (6.144 MHz)
- 11: XTI/8 (3.072 MHz)

**Register 25h, ERROR Cause Setting  
(Address: 25h, Write and Read)**

| DATA          | B7  | B6  | B5    | B4     | B3    | B2     | B1      | B0      |
|---------------|-----|-----|-------|--------|-------|--------|---------|---------|
| Reg Name      | RSV | RSV | EFCHG | EFSLMT | ENPCM | EVALID | EPARITY | EUNLOCK |
| Default Value | 0   | 0   | 0     | 0      | 0     | 0      | 0       | 1       |
| Memo          |     |     |       |        |       |        |         |         |

The following ERROR Cause Setting registers are independent of the AUTO Source Selector Cause Setting Register (Register 26h).

**EFCHG: DIR Sampling Frequency Change**

- 0: Not selected (default)
- 1: Selected

**EFSLMT: DIR Limiting Acceptable Sampling Frequency**

- 0: Not selected (default)
- 1: Selected

The definition of receivable sampling frequency range depends on the  $f_s$  Limit Setting Register.

**ENPCM: Non-PCM**

- 0: Not selected (default)
- 1: Selected

The definition of *non-PCM* is depend on the Non-PCM Definition Setting Register.

**EVALID: Validity Flag**

- 0: Not selected (default)
- 1: Selected

**EPARITY: Parity Error**

- 0: Not selected (default)
- 1: Selected

**EUNLOCK: PLL Lock Error**

- 0: Not selected
- 1: Selected (default)

This register is used for setting the ERROR output factor.

The required factors of ERROR set to '1' are selected based on OR logic.

**Register 26h, AUTO Source Selector Cause Setting  
(Address: 26h, Write and Read)**

| DATA          | B7  | B6     | B5  | B4     | B3    | B2     | B1  | B0      |
|---------------|-----|--------|-----|--------|-------|--------|-----|---------|
| Reg Name      | RSV | AERROR | RSV | AFSLMT | ANPCM | AVALID | RSV | AUNLOCK |
| Default Value | 0   | 0      | 0   | 0      | 0     | 0      | 0   | 1       |
| Memo          |     |        |     |        |       |        |     |         |

The AUTO source selector is an automatic selector that outputs DIR or XTI output based on the following register settings. The following AUTO Source Selector Cause Setting registers are independent of the ERROR Cause Setting Register (Register 25h).

**AERROR: ERROR**

- 0: Not selected (default)
- 1: Selected

ERROR condition is defined by the ERROR Cause Setting Register (Register 25h).

**AFSLMT: Limiting Acceptable Sampling Frequency**

- 0: Not selected (default)
- 1: Selected

The definition of receivable sampling frequency range depends on the  $f_s$  Limit Setting Register.

**ANPCM: Non-PCM**

- 0: Not selected (default)
- 1: Selected

The definition of Non PCM is depend on the Non-PCM Definition Setting Register.

**AVALID: Validity Flag**

- 0: Not selected (default)
- 1: Selected

**AUNLOCK: PLL Lock Error**

- 0: Not selected
- 1: Selected (default)

**Register 27h, DIR Acceptable  $f_s$  Range Setting and Mask  
(Address: 27h, Write and Read)**

| DATA          | B7     | B6    | B5  | B4     | B3     | B2     | B1     | B0     |
|---------------|--------|-------|-----|--------|--------|--------|--------|--------|
| Reg Name      | MSK128 | MSK64 | RSV | NOMLMT | HILMT1 | HILMT0 | LOLMT1 | LOLMT0 |
| Default Value | 0      | 0     | 0   | 0      | 0      | 0      | 0      | 0      |
| Memo          |        |       |     |        |        |        |        |        |

**MSK128: Mask for  $f_s = 128$  kHz**

0: No mask (default)

1: Mask

DIX9211 does not receive 128-kHz sampling frequency.

This register setting is effective with NOMLMT = '1'.

**MSK64: Mask for  $f_s = 64$  kHz**

0: No mask (default)

1: Mask

DIX9211 does not receive 64-kHz sampling frequency.

This register setting is effective with NOMLMT = '1'.

**NOMLMT: Receive Nominal Audio  $f_s$  within  $\pm 2\%$**

0: No limit (default)

1: Limit

DIX9211 receives the nominal audio sampling frequencies within  $\pm 2\%$ .

The nominal audio sampling frequencies are: 8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz, 24 kHz, 32 kHz, 44.1 kHz, 48 kHz, 64 kHz, 88.2 kHz, 96 kHz, 128 kHz, 176.4 kHz, 192 kHz

**HILMT[1:0]: Acceptable  $f_s$  Higher Limit Setting**

00: No limit (default)

01:  $f_s = 54$  kHz

10:  $f_s = 108$  kHz

11:  $f_s = 216$  kHz

**LOLMT[1:0]: Acceptable  $f_s$  Lower Limit Setting**

00: No limit (default)

01:  $f_s = 7$  kHz

10:  $f_s = 14$  kHz

11:  $f_s = 28$  kHz

This condition of receivable sampling frequency is used as the ERROR and AUTO source selection when EFSLMT or AFSLMT is set to '1'.

**Register 28h, Non-PCM Definition  
(Address: 28h, Write and Read)**

| DATA          | B7  | B6  | B5      | B4    | B3  | B2    | B1   | B0     |
|---------------|-----|-----|---------|-------|-----|-------|------|--------|
| Reg Name      | RSV | RSV | CS1BPLS | NPCMP | RSV | DTSCD | PAPB | CSBIT1 |
| Default Value | 0   | 0   | 0       | 0     | 0   | 0     | 1    | 1      |
| Memo          |     |     |         |       |     |       |      |        |

**CS1BPLS: CSBIT1 Detection Signal Select**

- 0: Hold value (default)
- 1: Pulse

**NPCMP: NPCM Pin Output Polarity**

- 0: Active high (default)
- 1: Active low

**DTSCD: DTS CD/LD Detection**

- 0: Unselected (default)
- 1: Selected

**PAPB: Burst Preamble P<sub>A</sub> and P<sub>B</sub> Detection**

- 0: Unselected
- 1: Selected (default)

**CSBIT1: Channel Status Bit1 = 1 Detection**

- 0: Unselected
- 1: Selected (default)

This register is used to set the definition of non-PCM data. The NPCM pin output and NPCM Register Flag output follow this definition.

There are three types of non-PCM factors to be selected, based on OR logic.

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**NOTE**

The DTSCD Register (Register 29h) must be '1' (that is, selected) in order to output the DTSCD flag from the MPIO, MPO, and INT pins as DIR Flag outputs.

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**Register 29h, DTS-CD/LD Sync Word and Period Detection Setting  
(Address: 29h, Write and Read)**

| DATA          | B7  | B6  | B5  | B4  | B3    | B2    | B1      | B0      |
|---------------|-----|-----|-----|-----|-------|-------|---------|---------|
| Reg Name      | RSV | RSV | RSV | RSV | DTS16 | DTS14 | DTSPRD1 | DTSPRD0 |
| Default Value | 0   | 0   | 0   | 0   | 1     | 1     | 0       | 0       |
| Memo          |     |     |     |     |       |       |         |         |

**DTS16: DTS-CD/LD 16-bit Sync Word Detection**

- 0: Unselected
- 1: Selected (default)

**DTS14: DTS-CD/LD 14-bit Sync Word Detection**

- 0: Unselected
- 1: Selected (default)

**DTSPRD[1:0]: DTS-CD/LD Sync Word Detection Period**

- 00: No period, detect one sync word (default)
- 01: One period
- 10: Two periods
- 11: Four periods

**NOTE**

The DTSCD Register (Register 28h) must be '1' (that is, selected) in order to output the DTSCD flag from the MPIO, MPO, and INT pins as DIR Flag outputs.

**Register 2Ah, INT0 Output Cause Mask Setting  
(Address: 2Ah, Write and Read)**

| DATA          | B7      | B6     | B5      | B4      | B3      | B2      | B1      | B0  |
|---------------|---------|--------|---------|---------|---------|---------|---------|-----|
| Reg Name      | MERROR0 | MNPCM0 | MEMPHF0 | MDTSCD0 | MCSRNW0 | MPCRNW0 | MFSCHG0 | RSV |
| Default Value | 1       | 1      | 1       | 1       | 1       | 1       | 1       | 1   |
| Memo          |         |        |         |         |         |         |         |     |

**MERROR0: ERROR Port Output Status**

0: Not masked

1: Masked (default)

**MNPCM0: NPCM Port Output Status**

0: Not masked

1: Masked (default)

This register setting follows the register setting of non-PCM data identification.

**MEMPHF0: Emphasis Flag in Channel Status**

0: Not masked

1: Masked (default)

**MDTSCD0: DTS-CD/LD Sync Detection**

0: Not masked

1: Masked (default)

This detection condition depends on the register setting for DTS-CD/LD detection conditions.

**MCSRNW0: Channel Status Data of Beginning 48-bit Renewal**

0: Not masked

1: Masked (default)

**MPCRNW0: Burst Preamble P<sub>C</sub> Renewal**

0: Not masked

1: Masked (default)

**MFSCHG0: Renewal Flag of f<sub>S</sub> Calculator Result**

0: Not masked

1: Masked (default)

**Register 2Bh, INT1 Output Cause Mask Setting  
(Address: 2Bh, Write and Read)**

| DATA          | B7      | B6     | B5      | B4      | B3      | B2      | B1      | B0  |
|---------------|---------|--------|---------|---------|---------|---------|---------|-----|
| Reg Name      | MERROR1 | MNPCM1 | MEMPHF1 | MDTSCD1 | MCSRNW1 | MPCRNW1 | MFSCHG1 | RSV |
| Default Value | 1       | 1      | 1       | 1       | 1       | 1       | 1       | 1   |
| Memo          |         |        |         |         |         |         |         |     |

**MERROR1: ERROR Port Output Status**

0: Not masked

1: Masked (default)

**MNPCM1: NPCM Port Output Status**

0: Not masked

1: Masked (default)

This register setting follows the register setting of non-PCM data identification.

**MEMPHF1: Emphasis Flag in Channel Status**

0: Not masked

1: Masked (default)

**MDTSCD1: DTS-CD/LD Sync Detection**

0: Not masked

1: Masked (default)

This detection condition depends on the register setting for DTS-CD/LD detection conditions.

**MCSRNW1: Channel Status Data of Beginning 48-bit Renewal**

0: Not masked

1: Masked (default)

**MPCRNW1: Burst Preamble P<sub>C</sub> Renewal**

0: Not masked

1: Masked (default)

**MFSCHG1: Renewal Flag of f<sub>S</sub> Calculator Result**

0: Not masked

1: Masked (default)

**Register 2Ch, INT0 Output Register  
(Address: 2Ch, Read-Only)**

| DATA          | B7      | B6     | B5      | B4      | B3      | B2      | B1      | B0  |
|---------------|---------|--------|---------|---------|---------|---------|---------|-----|
| Reg Name      | OERROR0 | ONPCM0 | OEMPHF0 | ODTSCD0 | OCSRNW0 | OPCRNW0 | OFSCHG0 | RSV |
| Default Value | N/A     | N/A    | N/A     | N/A     | N/A     | N/A     | N/A     | 0   |
| Memo          |         |        |         |         |         |         |         |     |

**OERROR0: ERROR Port Output Status**

0: No ERROR

1: Detect ERROR

This register setting follows the register setting of the ERROR factor.

**ONPCM0: NPCM Port Output Status**

0: PCM data

1: Non-PCM data

This register setting follows the register setting of non-PCM data identification.

**OEMPHF0: Emphasis Flag in Channel Status**

0: No emphasis

1: Emphasis

**ODTSCD0: DTS-CD/LD Detection**

0: No DTS-CD/LD

1: DTS-CD/LD

This register setting follows the register setting for DTS-CD/LD detection conditions.

**OCSRNW0: Channel Status Data of Beginning 48-bit Renewal**

0: Not detect renewal

1: Detect renewal

**OPCRNW0: Burst Preamble P<sub>C</sub> Renewal**

0: Not detect renewal

1: Detect renewal

**OFSCHG0: Renewal Flag of f<sub>s</sub> Calculator Result**

0: Not detect renewal

1: Detect renewal

When this register is read, the INT0 output is cleared.

**Register 2Dh, INT1 Output Register  
(Address: 2Dh, Read-Only)**

| DATA          | B7      | B6     | B5      | B4      | B3      | B2      | B1      | B0      |
|---------------|---------|--------|---------|---------|---------|---------|---------|---------|
| Reg Name      | OERROR1 | ONPCM1 | OEMPHF1 | ODTSCD1 | OCSRNW1 | OPCRNW1 | OFSCHG1 | OADLVL1 |
| Default Value | N/A     | N/A    | N/A     | N/A     | N/A     | N/A     | N/A     | N/A     |
| Memo          |         |        |         |         |         |         |         |         |

**OERROR1: ERROR Port Output Status**

0: No ERROR

1: Detect ERROR

This register setting follows the register setting of the ERROR factor.

**ONPCM1: NPCM Port Output Status**

0: PCM data

1: Non-PCM data

This register setting follows the register setting of non-PCM data identification.

**OEMPHF1: Emphasis Flag in Channel Status**

0: No emphasis

1: Emphasis

**ODTSCD1: DTS-CD/LD Detection**

0: No DTS-CD/LD

1: DTS-CD/LD

This register setting follows the register setting for DTS-CD/LD detection conditions.

**OCSRNW1: Channel Status Data of Beginning 48-bit Renewal**

0: Not detect renewal

1: Detect renewal

**OPCRNW1: Burst Preamble P<sub>C</sub> Renewal**

0: Not detect renewal

1: Detect renewal

**OFSCHG1: Renewal Flag of f<sub>s</sub> Calculator Result**

0: Not detect renewal

1: Detect renewal

**OADLVL1: ADC Input Level Detection Status**

0: Not detect the defined threshold input level

1: Detect the defined threshold input level

NOTE: The threshold input level is defined by Register 2Eh, ADLVLTH[1:0].

When this register is read, the INT1 output is cleared.

### Register 2Eh, INT0, INT1 Output Polarity Setting (Address: 2Eh, Write and Read)

| DATA          | B7  | B6    | B5  | B4  | B3  | B2    | B1  | B0  |
|---------------|-----|-------|-----|-----|-----|-------|-----|-----|
| Reg Name      | RSV | INT1P | RSV | RSV | RSV | INT0P | RSV | RSV |
| Default Value | 0   | 0     | 0   | 0   | 0   | 0     | 0   | 0   |
| Memo          |     |       |     |     |     |       |     |     |

#### INT1P: INT1 Port, Polarity Setting

- 0: Negative logic (default)
- 1: Positive logic

#### INT0P: INT0 Port, Polarity Setting

- 0: Negative logic (default)
- 1: Positive logic

When the INT0 or INT1 Information Register is read, Register INT0 or INT1 port output is cleared.

### Register 2Fh, DIR Output Data Format (Address: 2Fh, Write and Read)

| DATA          | B7  | B6  | B5  | B4  | B3  | B2     | B1     | B0     |
|---------------|-----|-----|-----|-----|-----|--------|--------|--------|
| Reg Name      | RSV | RSV | RSV | RSV | RSV | RXFMT2 | RXFMT1 | RXFMT0 |
| Default Value | 0   | 0   | 0   | 0   | 0   | 1      | 0      | 0      |
| Memo          |     |     |     |     |     |        |        |        |

#### RXFMT[2:0]: DIR Output Data Format Setting

- 000: 24-bit MSB first, right-justified
- 001: Reserved
- 010: Reserved
- 011: 16-bit MSB first, right-justified
- 100: 24-bit MSB first, I<sup>2</sup>S (default)
- 101: 24-bit MSB first, left-justified
- 110: Reserved
- 111: Reserved

**Register 30h, DIR Recovered System Clock (SCK) Ratio Setting  
(Address: 30h, Write and Read)**

| DATA          | B7  | B6  | B5  | B4       | B3  | B2    | B1    | B0    |
|---------------|-----|-----|-----|----------|-----|-------|-------|-------|
| Reg Name      | RSV | RSV | RSV | PSCKAUTO | RSV | PSCK2 | PSCK1 | PSCK0 |
| Default Value | 0   | 0   | 0   | 0        | 0   | 0     | 1     | 0     |
| Memo          |     |     |     |          |     |       |       |       |

**PSCKAUTO: PLL SCK Dividing Ratio Automatic Control Setting**

0: Disable (default)

1: Enable

This register is used to set the PLL SCK dividing ratio automatic control function.

SCK setting is automatically set depending on the input sampling frequency.

512f<sub>S</sub>: 54 kHz and below

256f<sub>S</sub>: 54 kHz to 108 kHz

128f<sub>S</sub>: 108 kHz and above or unlocked

The register setting of PSCKAUTO is prioritized higher than the PSCK[2:0] register setting.

For instance, if PSCKAUTO = '1', the PSCK[2:0] register setting is ignored.

To use this function, the XTI clock source is required.

**PSCK[2:0]: DIR Recovered Clock Frequency Setting**

000: 128f<sub>S</sub>

001: Reserved

010: 256f<sub>S</sub> (default)

011: Reserved

100: 512f<sub>S</sub>

101: Reserved

110: Reserved

111: Reserved

**Register 31h, XTI Source, Clock (SCK/BCK/LRCK) Frequency Setting  
(Address: 31h, Write and Read)**

| DATA          | B7  | B6  | B5    | B4    | B3    | B2    | B1     | B0     |
|---------------|-----|-----|-------|-------|-------|-------|--------|--------|
| Reg Name      | RSV | RSV | XSCK1 | XSCK0 | XBCK1 | XBCK0 | XLRCK1 | XLRCK0 |
| Default Value | 0   | 0   | 0     | 1     | 1     | 0     | 1      | 0      |
| Memo          |     |     |       |       |       |       |        |        |

**XSCK[1:0]: XTI Clock Source Frequency Setting**

- 00: XTI/1 (24.576 MHz)
- 01: XTI/2 (12.288 MHz) (default)
- 10: XTI/4 (6.144 MHz)
- 11: XTI/8 (3.072 MHz)

**XBCK[1:0]: XTI Clock Source BCK Frequency Setting**

- 00: XTI/2 (12.288 MHz)
- 01: XTI/4 (6.144 MHz)
- 10: XTI/8 (3.072 MHz) (default)
- 11: XTI/16 (1.536 MHz)

**XLRCK[1:0]: XTI Clock Source LRCK Frequency Setting**

- 00: XTI/128 (192 kHz)
- 01: XTI/256 (96 kHz)
- 10: XTI/512 (48 kHz) (default)
- 11: XTI/1024 (24 kHz)

**Register 32h, DIR Source, Secondary Bit/LR Clock (SBCK/SLRCK) Frequency Setting  
(Address: 32h, Write and Read)**

| DATA          | B7  | B6     | B5     | B4     | B3  | B2      | B1      | B0      |
|---------------|-----|--------|--------|--------|-----|---------|---------|---------|
| Reg Name      | RSV | PSBCK2 | PSBCK1 | PSBCK0 | RSV | PSLRCK2 | PSLRCK1 | PSLRCK0 |
| Default Value | 0   | 0      | 1      | 0      | 0   | 0       | 1       | 0       |
| Memo          |     |        |        |        |     |         |         |         |

**PSBCK[2:0]: DIR Clock Source, Secondary BCK (SBCK) Frequency Setting**

- 000:  $16f_S$  (BCK/4)
- 001:  $32f_S$  (BCK/2)
- 010:  $64f_S$  (1x BCK) (default)
- 011:  $128f_S$  (2x BCK)
- 100:  $256f_S$  (4x BCK)
- 101: Reserved
- 110: Reserved
- 111: Reserved

**PSLRCK[2:0]: DIR Clock Source, Secondary LRCK (SLRCK) Frequency Setting**

- 000:  $f_S/4$  (LRCK/4)
- 001:  $f_S/2$  (LRCK/2)
- 010:  $f_S$  (1x LRCK) (default)
- 011:  $2f_S$  (2x LRCK)
- 100:  $4f_S$  (4x LRCK)
- 101: Reserved
- 110: Reserved
- 111: Reserved

**Register 33h, XTI Source, Secondary Bit/LR Clock (SBCK/SLRCK) Frequency Setting  
(Address: 33h, Write and Read)**

| DATA          | B7  | B6     | B5     | B4     | B3  | B2      | B1      | B0      |
|---------------|-----|--------|--------|--------|-----|---------|---------|---------|
| Reg Name      | RSV | XSBCK2 | XSBCK1 | XSBCK0 | RSV | XSLRCK2 | XSLRCK1 | XSLRCK0 |
| Default Value | 0   | 0      | 1      | 0      | 0   | 0       | 1       | 0       |
| Memo          |     |        |        |        |     |         |         |         |

**XSBCK[2:0]: XTI Clock Source, Secondary BCK (SBCK) Frequency Setting**

- 000: XTI/2 (12.288 MHz)
- 001: XTI/4 (6.144 MHz)
- 010: XTI/8 (3.072 MHz) (default)
- 011: XTI/16 (1.536 MHz)
- 100: XTI/32 (0.768 MHz)
- 101: Reserved
- 110: Reserved
- 111: Reserved

**XSLRCK[2:0]: XTI Clock Source, Secondary LRCK (SLRCK) Frequency Setting**

- 000: XTI/128 (192 kHz)
- 001: XTI/256 (96 kHz)
- 010: XTI/512 (48 kHz) (default)
- 011: XTI/1024 (24 kHz)
- 100: XTI/2048 (12 kHz)
- 101: Reserved
- 110: Reserved
- 111: Reserved

**Register 34h, DIR Input Biphase Source Select, Coax Amplifier Control**  
**(Address: 34h, Write and Read)**

| DATA          | B7     | B6     | B5  | B4  | B3     | B2     | B1     | B0     |
|---------------|--------|--------|-----|-----|--------|--------|--------|--------|
| Reg Name      | RX0DIS | RX1DIS | RSV | RSV | RXSEL3 | RXSEL2 | RXSEL1 | RXSEL0 |
| Default Value | 1      | 1      | 0   | 0   | 0      | 0      | 1      | 0      |
| Memo          |        |        |     |     |        |        |        |        |

**RX0DIS: Power Down for RXIN0 Coaxial Amplifier**

- 0: Normal operation
- 1: Power down (default)

**RX1DIS: Power Down for RXIN1 Coaxial Amplifier**

- 0: Normal operation
- 1: Power down (default)

**RXSEL[3:0]: DIR Input Biphase Signal Source Select**

- 0000: RXIN0
- 0001: RXIN1
- 0010: RXIN2 (default)
- 0011: RXIN3
- 0100: RXIN4
- 0101: RXIN5
- 0110: RXIN6
- 0111: RXIN7
- 1000: RXIN8
- 1001: RXIN9
- 1010: RXIN10
- 1011: RXIN11
- 1100: Reserved
- 1101: Reserved
- 1110: Reserved
- 1111: TXOUT (internal DIT output)

**NOTE**

RX0DIS or RX1DIS must be set to '0', even when an S/PDIF, TTL, or OPTICAL input is provided into RXIN0 or RXIN1, without use of the built-in COAX amplifier.

**Register 35h, RECOUT0 Output Biphase Source Settings  
(Address: 35h, Write and Read)**

| DATA          | B7  | B6  | B5  | B4      | B3      | B2      | B1      | B0      |
|---------------|-----|-----|-----|---------|---------|---------|---------|---------|
| Reg Name      | RSV | RSV | RSV | MPO0MUT | RO0SEL3 | RO0SEL2 | RO0SEL1 | RO0SEL0 |
| Default Value | 0   | 0   | 0   | 0       | 0       | 0       | 1       | 0       |
| Memo          |     |     |     |         |         |         |         |         |

**RO0SEL0[3:0]: RECOUT0 Output Biphase Source Select**

- 0000: RXIN0
- 0001: RXIN1
- 0010: RXIN2 (default)
- 0011: RXIN3
- 0100: RXIN4
- 0101: RXIN5
- 0110: RXIN6
- 0111: RXIN7
- 1000: RXIN8
- 1001: RXIN9
- 1010: RXIN10
- 1011: RXIN11
- 1100: Reserved
- 1101: Reserved
- 1110: Reserved
- 1111: TXOUT (internal DIT output)

**MPO0MUT: MPO0 Mute Control**

- 0: Output (default)
- 1: MUTE (Logic low level)

**Register 36h, RECOUT1 Output Biphase Source Settings  
(Address: 36h, Write and Read)**

| DATA          | B7  | B6  | B5  | B4      | B3      | B2      | B1      | B0      |
|---------------|-----|-----|-----|---------|---------|---------|---------|---------|
| Reg Name      | RSV | RSV | RSV | MPO1MUT | RO1SEL3 | RO1SEL2 | RO1SEL1 | RO1SEL0 |
| Default Value | 0   | 0   | 0   | 0       | 0       | 0       | 1       | 0       |
| Memo          |     |     |     |         |         |         |         |         |

**RO1SEL0[3:0]: RECOUT1 Output Biphase Source Select**

0000: RXIN0  
 0001: RXIN1  
 0010: RXIN2 (default)  
 0011: RXIN3  
 0100: RXIN4  
 0101: RXIN5  
 0110: RXIN6  
 0111: RXIN7  
 1000: RXIN8  
 1001: RXIN9  
 1010: RXIN10  
 1011: RXIN11  
 1100: Reserved  
 1101: Reserved  
 1110: Reserved  
 1111: TXOUT (internal DIT output)

**MPO1MUT: MPO1 Mute Control**

0: Output (default)  
 1: MUTE (Logic low level)

**Register 37h, Port Sampling Frequency Calculator Measurement Target Setting  
(Address: 37h, Write and Read)**

| DATA          | B7  | B6  | B5  | B4  | B3  | B2      | B1      | B0      |
|---------------|-----|-----|-----|-----|-----|---------|---------|---------|
| Reg Name      | RSV | RSV | RSV | RSV | RSV | PFSTGT2 | PFSTGT1 | PFSTGT0 |
| Default Value | 0   | 0   | 0   | 0   | 0   | 0       | 0       | 0       |
| Memo          |     |     |     |     |     |         |         |         |

**PFSTGT[2:0]: Port  $f_s$  Calculator, Target Port Setting**

000: DIR (default)  
 001: XT1  
 010: AUXIN0  
 011: AUXIN1  
 100: AUXIN2  
 101: Main output port  
 110: AUX output port  
 111: DIT

### Register 38h, Port Sampling Frequency Calculator Result Output (Address: 38h, Read-Only)

| DATA          | B7    | B6     | B5     | B4     | B3      | B2      | B1      | B0      |
|---------------|-------|--------|--------|--------|---------|---------|---------|---------|
| Reg Name      | PFSST | PFSP02 | PFSP01 | PFSP00 | PFSOUT3 | PFSOUT2 | PFSOUT1 | PFSOUT0 |
| Default Value | N/A   | N/A    | N/A    | N/A    | N/A     | N/A     | N/A     | N/A     |
| Memo          |       |        |        |        |         |         |         |         |

#### PFSST: Port Sampling Frequency Calculate Status

0: Calculated

1: Calculating

#### PFSP0[2:0]: Calculated Port Information

000: DIR

001: XT1

010: AUXIN0

011: AUXIN1

100: AUXIN2

101: Main output port

110: AUX output port

111: DIT

#### PFSOUT[3:0]: Calculated Sampling Frequency

0000: Out of range

0001: 8 kHz

0010: 11.025 kHz

0011: 12 kHz

0100: 16 kHz

0101: 22.05 kHz

0110: 24 kHz

0111: 32 kHz

1000: 44.1 kHz

1001: 48 kHz

1010: 64 kHz

1011: 88.2 kHz

1100: 96 kHz

1101: 128 kHz

1110: 176.4 kHz

1111: 192 kHz

#### NOTE

PFSST, PFSP0, and PFSOUT always output the status when these registers are read.

The other registers do not have clear functions when these are read. To enable these registers, DIR must be powered on. For example, (Register 40h/RXDIS = 0) PFSST indicates *Calculating* and PFSOUT indicates the previous value when no source comes to the port that is selected by Register 37h/PFSTGT.

**Register 39h, Incoming Biphase Information and Sampling Frequency  
(Address: 39h, Read-Only)**

| DATA          | B7    | B6      | B5  | B4  | B3      | B2      | B1      | B0      |
|---------------|-------|---------|-----|-----|---------|---------|---------|---------|
| Reg Name      | SFSST | SCSBIT1 | RSV | RSV | SESOUT3 | SESOUT2 | SESOUT1 | SESOUT0 |
| Default Value | N/A   | N/A     | N/A | N/A | N/A     | N/A     | N/A     | N/A     |
| Memo          |       |         |     |     |         |         |         |         |

**SFSST: Incoming Biphase Signal, Sampling Frequency Calculate Status**

- 0: SFSOUT[3:0] Output is calculated
- 1: In the process of calculating or unlocked

**SCSBIT1: Detected Channel Status Bit1 Flag**

- 0: CS Bit1 = 0 (Audio data)
- 1: CS Bit1 = 1 (Non-audio data)

**SFSOUT[3:0]: Incoming Biphase Signal, Actual Sampling Frequency**

- 0000: Out of range
- 0001: 8 kHz
- 0010: 11.025 kHz
- 0011: 12 kHz
- 0100: 16 kHz
- 0101: 22.05 kHz
- 0110: 24 kHz
- 0111: 32 kHz
- 1000: 44.1 kHz
- 1001: 48 kHz
- 1010: 64 kHz
- 1011: 88.2 kHz
- 1100: 96 kHz
- 1101: 128 kHz
- 1110: 176.4 kHz
- 1111: 192 kHz

**NOTE**

When SFSST becomes '1' (that is, in the process of calculating or unlocked), SFSOUT holds the previous data. SFSST and SFSOUT always output the status when these registers are read. The other registers do not have clear functions when these are read. To enable these registers, DIR must be powered on (Register 40h/RXDIS = 0).

**Register 3Ah–3Bh, P<sub>C</sub> Buffer (Burst Preamble P<sub>C</sub> Output Register)**

| Address: 3Ah, Read-Only |     |     |     |     |     |     |     |     |
|-------------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| DATA                    | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
| Reg Name                | PC7 | PC6 | PC5 | PC4 | PC3 | PC2 | PC1 | PC0 |
| Default Value           | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Memo                    |     |     |     |     |     |     |     |     |

| Address: 3Bh, Read-Only |      |      |      |      |      |      |     |     |
|-------------------------|------|------|------|------|------|------|-----|-----|
| DATA                    | B7   | B6   | B5   | B4   | B3   | B2   | B1  | B0  |
| Reg Name                | PC15 | PC14 | PC13 | PC12 | PC11 | PC10 | PC9 | PC8 |
| Default Value           | N/A  | N/A  | N/A  | N/A  | N/A  | N/A  | N/A | N/A |
| Memo                    |      |      |      |      |      |      |     |     |

PC[4:0]: Burst Preamble P<sub>C</sub>, data type

PC[6:5]: Burst Preamble P<sub>C</sub>, reserved

PC7: Burst Preamble P<sub>C</sub>, Error

PC[12:8]: Burst Preamble P<sub>C</sub>, data type dependent information

PC[15:13]: Burst Preamble P<sub>C</sub>, bit stream no.

Read P<sub>C</sub>/P<sub>D</sub> after ONPCM1/0 goes high by setting MNPCM1 = 1 or MNPCM0 = 1. Polling P<sub>C</sub>/P<sub>D</sub> [15:0] is not allowed.

**Register 3Ch–3Dh, P<sub>D</sub> Buffer (Burst Preamble P<sub>D</sub> Output Register)**

| Address: 3Ch, Read-Only |     |     |     |     |     |     |     |     |
|-------------------------|-----|-----|-----|-----|-----|-----|-----|-----|
| DATA                    | B7  | B6  | B5  | B4  | B3  | B2  | B1  | B0  |
| Reg Name                | PD7 | PD6 | PD5 | PD4 | PD3 | PD2 | PD1 | PD0 |
| Default Value           | N/A | N/A | N/A | N/A | N/A | N/A | N/A | N/A |
| Memo                    |     |     |     |     |     |     |     |     |

| Address: 3Dh, Read-Only |      |      |      |      |      |      |     |     |
|-------------------------|------|------|------|------|------|------|-----|-----|
| DATA                    | B7   | B6   | B5   | B4   | B3   | B2   | B1  | B0  |
| Reg Name                | PD15 | PD14 | PD13 | PD12 | PD11 | PD10 | PD9 | PD8 |
| Default Value           | N/A  | N/A  | N/A  | N/A  | N/A  | N/A  | N/A | N/A |
| Memo                    |      |      |      |      |      |      |     |     |

**PD[15:0]: Burst Preamble P<sub>D</sub>, Length Code (Number of bits)**

PD[15:0] is updated at the time when PC[15:0] is updated. PD[15:0] is never updated when only PC[15:0] is updated. Register 2Ch/OPCRNW0 or Register 2Dh/OPCRNW1 inform the system that PC[15:0] is updated.

**Register 40h, System Reset Control  
(Address: 40h, Write and Read)**

| DATA          | B7   | B6  | B5    | B4    | B3  | B2  | B1    | B0    |
|---------------|------|-----|-------|-------|-----|-----|-------|-------|
| Reg Name      | MRST | RSV | ADDIS | RXDIS | RSV | RSV | TXDIS | XODIS |
| Default Value | 1    | 1   | 0     | 0     | 0   | 0   | 0     | 0     |
| Memo          |      |     |       |       |     |     |       |       |

**MRST: Mode Control Register Reset for All Functions**

- 0: Set default value
- 1: Normal operation (default)

**ADDIS: Power-Saving for Digital Power Supply (DVDD)**

- 0: Normal operation (default)
- 1: Power-saving mode

NOTE : Even in power-saving mode, all functions are active. However, without power-saving mode, DOUT outputs certain data at the power-supply injection.

**RXDIS: Power Down for DIR**

- 0: Normal operation (default)
- 1: Power down

**TXDIS: Power Down for DIT**

- 0: Normal operation (default)
- 1: Power down

**XODIS: Power Down for OSC**

- 0: Normal operation (default)
- 1: Power down

XODIS is superior to OSCAUTO.

**Register 42h, External ADC Function Control  
(Address: 42h, Write and Read)**

| DATA          | B7  | B6  | B5  | B4      | B3  | B2      | B1      | B0      |
|---------------|-----|-----|-----|---------|-----|---------|---------|---------|
| Reg Name      | RSV | RSV | RSV | ADDTRX7 | RSV | EADCLK2 | EADCLK1 | EADCLK0 |
| Default Value | 0   | 0   | 0   | 0       | 0   | 0       | 1       | 0       |
| Memo          |     |     |     |         |     |         |         |         |

**ADDTRX7: ADC Output Data Select to Main Port, DOUT Pin**

0: DOUT = ADC DOUT (default)

1: DOUT = RXIN7 (ADIN0)

This register can select an external ADC data from RXIN7 (ADIN0) to Main Port DOUT pin when an external ADC is used.

When ADFSLMT = 1, ADCLK[2:0] = 001 (ADC clock is DIR output clock) and DIR locks at frequency from 14 kHz to 111 kHz, the ADC is forced into power down.

**EADCLK[2:0]: ADC Clock Source (SCK/BCK/LRCK) Select**

000: AUTO (DIR or XTI)

001: DIR

010: XTI (default)

011: AUXIN0

100: AUXIN1

100: AUXIN2

110: Reserved

111: Reserved

The external ADC clock source must be normally set to XTI source with fixed frequency (the clocks at the XTI source select are generated by the SCK/BCK/LRCK dividers). Its frequency is set by the register of XSCK[1:0], XBCK[1:0], and XLRCK[1:0].).

**Register 5Ah–5Fh, DIR Channel Status Data Buffer  
(Address : 5Ah–5Fh, Read-Only)**

| Address | DATA     |          |          |          |          |          |          |           |
|---------|----------|----------|----------|----------|----------|----------|----------|-----------|
|         | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0        |
| 5Ah     | RXCS7    | RXCS6    | RXCS5    | RXCS4    | RXCS3    | RXCS2    | RXCS1    | RXCS0     |
|         | CS Bit7  | CS Bit6  | CS Bit5  | CS Bit4  | CS Bit3  | CS Bit2  | CS Bit1  | CS Bit0   |
| 5Bh     | RXCS15   | RXCS14   | RXCS13   | RXCS12   | RXCS11   | RXCS10   | RXCS9    | RXCS8     |
|         | CS Bit15 | CS Bit14 | CS Bit13 | CS Bit12 | CS Bit11 | CS Bit10 | CS Bit9  | CS Bit8   |
| 5Ch     | RXCS23   | RXCS22   | RXCS21   | RXCS20   | RXCS19   | RXCS18   | RXCS17   | RXCS16    |
|         | CS Bit23 | CS Bit22 | CS Bit21 | CS Bit20 | CS Bit19 | CS Bit18 | CS Bit17 | CS Bit16  |
| 5Dh     | RXCS31   | RXCS30   | RXCS29   | RXCS28   | RXCS27   | RXCS26   | RXCS25   | RXCS24    |
|         | CS Bit31 | CS Bit30 | CS Bit29 | CS Bit28 | CS Bit27 | CS Bit26 | CS Bit25 | CS Bit24X |
| 5Eh     | RXCS39   | RXCS38   | RXCS37   | RXCS36   | RXCS35   | RXCS34   | RXCS33   | RXCS32    |
|         | CS Bit39 | CS Bit38 | CS Bit37 | CS Bit36 | CS Bit35 | CS Bit34 | CS Bit33 | CS Bit32  |
| 5Fh     | RXCS47   | RXCS46   | RXCS45   | RXCS44   | RXCS43   | RXCS42   | RXCS41   | RXCS40    |
|         | CS Bit47 | CS Bit46 | CS Bit45 | CS Bit44 | CS Bit43 | CS Bit42 | CS Bit41 | CS Bit40  |

RXCS0: Use of channel status block

RXCS1: Linear PCM information

RXCS2: Copyright information

RXCS5 – RXCS3: Additional format information

RXCS7– RXCS6: Channel status mode

RXCS15 – RXCS8: Category code

RXCS19 – RXCS16: Source number

RXCS23 – RXCS20: Channel number

RXCS27 – RXCS24: Sampling frequency

RXCS29 – RXCS28: Clock accuracy

RXCS31 – RXCS30: Not defined

RXCS32: Maximum audio sample word length

RXCS35 – RXCS33: Sample word length

RXCS39 – RXCS36: Original sampling frequency

RXCS47 – RXCS40: Not defined

xx of RXCSxx represents the serial number of the channel status data. L-channel data of the channel status is stored in this register. Its default value is not specified. Therefore, wait until the ERROR/INT0 port goes low and 192 samples pass to read RXCS. RXCS is cleared when DIR unlocks and an L-ch parity error is detected.

**Register 60h, DIT Function Control 1/3  
(Address: 60h, Write and Read)**

| DATA          | B7  | B6      | B5      | B4      | B3  | B2      | B1      | B0      |
|---------------|-----|---------|---------|---------|-----|---------|---------|---------|
| Reg Name      | RSV | TXSSRC2 | TXSSRC1 | TXSSRC0 | RSV | TXPSRC2 | TXPSRC1 | TXPSRC0 |
| Default Value | 0   | 1       | 0       | 0       | 0   | 1       | 0       | 0       |
| Memo          |     |         |         |         |     |         |         |         |

**TXSSRC[2:0]: DIT System Clock Source Select**

- 000: DIR/XTI Automatic (DIR lock = DIR, DIR unlock = XTI)
- 001: DIR
- 010: XTI
- 011: AUXIN0
- 100: AUXIN1 (default)
- 100: AUXIN2
- 110: Reserved
- 111: Reserved

**TXPSRC[2:0]: DIT Bit Clock, LR Clock, Data Source Select**

- 000: DIR/XTI Automatic (DIR lock = DIR, DIR unlock = XTI)
- 001: DIR
- 010: XTI
- 011: AUXIN0
- 100: AUXIN1 (default)
- 100: AUXIN2
- 110: Reserved
- 111: Reserved

**Register 61h, DIT Function Control 2/3  
(Address: 61h, Write and Read)**

| DATA          | B7  | B6     | B5     | B4     | B3  | B2    | B1     | B0     |
|---------------|-----|--------|--------|--------|-----|-------|--------|--------|
| Reg Name      | RSV | TXSCL2 | TXSCK1 | TXSCK0 | RSV | TXDSD | TXFMT1 | TXFMT0 |
| Default Value | 0   | 0      | 0      | 1      | 0   | 0     | 0      | 0      |
| Memo          |     |        |        |        |     |       |        |        |

**TXSCK[2:0]: DIT System Clock Control**

- 000: 128f<sub>S</sub>
- 001: 256f<sub>S</sub> (default)
- 010: 512f<sub>S</sub>
- 011: Reserved
- 100: Controlled by DIR system clock rate
- 100: Controlled by DIR system clock rate
- 110: Controlled by DIR system clock rate
- 111: Controlled by DIR system clock rate

**TXDSD: DIT DSD Input Enable**

- 0: DSD input disable (default)
- 1: DSD input enable

---

**NOTE**

When TXDSD is set to '1', the DIT LR clock is generated by the Bit Clock divided by 64. The DIT source data are forced to all '0's. Provide the DSD source to MPIO\_B0 for the system clock (256f<sub>S</sub>), MPIO\_B1 for the DSD bit clock (64f<sub>S</sub>), MPIO\_B2 for L-ch data, and MPIO\_B3 for R-ch data.

This function is useful when it is desired to suppress system clock jitter by using the path that is DIT to DIR. Jitter of the system clock generated by DIR is also reduced if the jitter is high frequency.

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**TXFMT[1:0]:DIT Audio I/F Format Setting**

- 00: 24-bit I<sup>2</sup>S (default)
- 01: 24-bit left-justified
- 10: 24-bit right-justified
- 11: 16-bit right-justified

### Register 62h, DIT Function Control 3/3 (Address: 62h, Write and Read)

| DATA          | B7  | B6  | B5     | B4  | B3     | B2  | B1  | B0  |
|---------------|-----|-----|--------|-----|--------|-----|-----|-----|
| Reg Name      | RSV | RSV | TXDMUT | RSV | TXVFLG | RSV | RSV | RSV |
| Default Value | 0   | 0   | 0      | 0   | 0      | 0   | 0   | 0   |
| Memo          |     |     |        |     |        |     |     |     |

#### TXDMUT: DIT Output Audio Data Mute Control

- 0: No mute (default)
- 1: Audio data on biphasic signal is Mute (zero data)

#### TXVFLG: DIT Output Validity Flag Control

- 0: V = '0', Valid (default)
- 1: V = '1', Invalid

### Register 63h–68h, DIT Channel Status Data Buffer (Address: 63h–68h, Write and Read)

| Address | DATA     |          |          |          |          |          |          |           |
|---------|----------|----------|----------|----------|----------|----------|----------|-----------|
|         | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0        |
| 63h     | TXCS7    | TXCS6    | TXCS5    | TXCS4    | TXCS3    | TXCS2    | TXCS1    | TXCS0     |
|         | CS Bit7  | CS Bit6  | CS Bit5  | CS Bit4  | CS Bit3  | CS Bit2  | CS Bit1  | CS Bit0   |
| 64h     | TXCS15   | TXCS14   | TXCS13   | TXCS12   | TXCS11   | TXCS10   | TXCS9    | TXCS8     |
|         | CS Bit15 | CS Bit14 | CS Bit13 | CS Bit12 | CS Bit11 | CS Bit10 | CS Bit9  | CS Bit8   |
| 65h     | TXCS23   | TXCS22   | TXCS21   | TXCS20   | TXCS19   | TXCS18   | TXCS17   | TXCS16    |
|         | CS Bit23 | CS Bit22 | CS Bit21 | CS Bit20 | CS Bit19 | CS Bit18 | CS Bit17 | CS Bit16  |
| 66h     | TXCS31   | TXCS30   | TXCS29   | TXCS28   | TXCS27   | TXCS26   | TXCS25   | TXCS24    |
|         | CS Bit31 | CS Bit30 | CS Bit29 | CS Bit28 | CS Bit27 | CS Bit26 | CS Bit25 | CS Bit24X |
| 67h     | TXCS39   | TXCS38   | TXCS37   | TXCS36   | TXCS35   | TXCS34   | TXCS33   | TXCS32    |
|         | CS Bit39 | CS Bit38 | CS Bit37 | CS Bit36 | CS Bit35 | CS Bit34 | CS Bit33 | CS Bit32  |
| 68h     | TXCS47   | TXCS46   | TXCS45   | TXCS44   | TXCS43   | TXCS42   | TXCS41   | TXCS40    |
|         | CS Bit47 | CS Bit46 | CS Bit45 | CS Bit44 | CS Bit43 | CS Bit42 | CS Bit41 | CS Bit40  |

TXCS0: Use of channel status block.

TXCS1: Linear PCM information.

TXCS2: Copyright information.

TXCS5 – TXCS3: Additional format information.

TXCS7 – TXCS6: Channel status mode.

TXCS15 – TXCS8: Category code.

TXCS19 – TXCS16: Source number.

TXCS23 – TXCS20: Channel number.

TXCS27 – TXCS24: Sampling frequency.

TXCS29 – TXCS28: Clock accuracy.

TXCS31 – TXCS30: Not defined.

TXCS32: Maximum audio sample word length.

TXCS35 – TXCS33: Sample word length.

TXCS39 – TXCS36: Original sampling frequency.

TXCS47 – TXCS40: Not defined.

The data in this register are used for both channels (L-ch and R-ch). When these register data are used for the DIT channel status data, a channel status data of bit 48 or later is all '0'. All initial values of this register are all '0'.

**Register 6Ah, Main Output and AUXOUT Port Control  
(Address: 6Ah, Write and Read)**

| DATA          | B7      | B6      | B5  | B4  | B3       | B2     | B1       | B0     |
|---------------|---------|---------|-----|-----|----------|--------|----------|--------|
| Reg Name      | AOMUTAS | MOMUTAS | RSV | RSV | AOLRMTEN | AODMUT | MOLRMTEN | MODMUT |
| Default Value | 0       | 0       | 0   | 0   | 0        | 0      | 0        | 0      |
| Memo          |         |         |     |     |          |        |          |        |

**AOMUTAS: AUX Output Port, Mute Synchronization Select (MPIO\_B2 and MPIO\_B3)**

- 0: AODMUT works with synchronization with LRCK edge. (default)
- 1: AODMUT works without synchronization with LRCK edge

**MOMUTAS: Main Output Port, Mute Synchronization Select (LRCK and DOUT)**

- 0: MODMUT works with synchronization with LRCK edge. (default)
- 1: MODMUT works without synchronization with LRCK edge

**AOLRMTEN: AODMUT Signal Select (MPIO\_B2)**

- 0: Only DOUT (default)
- 1: Both of LRCK and DOUT

**AODMUT: AUX Output Port, Data Mute Control**

- 0: Output (default)
- 1: Mute (the affected signals are selected by Register 6Ah, AOLRMTEN)

**MOLRMTEN : MODMUT signal select**

- 0: Only DOUT (default)
- 1: Both LRCK and DOUT

**MODMUT: Main Output Port, DOUT Mute Control**

- 0: Output (default)
- 1: Mute (the affected signals are selected by Register 6Ah, MOLRMTEN)

Data mutes are done in synchronization with a LRCK edge.

**Register 6Bh, Main Output Port (SCKO/BCK/LRCK/DOUT) Source Setting  
(Address: 6Bh, Write and Read)**

| DATA          | B7  | B6      | B5      | B4      | B3  | B2      | B1      | B0      |
|---------------|-----|---------|---------|---------|-----|---------|---------|---------|
| Reg Name      | RSV | MOSSRC2 | MOSSRC1 | MOSSRC0 | RSV | MOPSRC2 | MOPSRC1 | MOPSRC0 |
| Default Value | 0   | 0       | 0       | 0       | 0   | 0       | 0       | 0       |
| Memo          |     |         |         |         |     |         |         |         |

**MOSSRC[2:0]: Main Output Port, SCK Source Control**

- 000: DIR/XTI Automatic (DIR lock:DIR, DIR unlock:XTI) (default)
- 001: DIR
- 010: XTI
- 011: AUXIN0
- 100: AUXIN1
- 101: AUXIN2
- 110: Reserved
- 111: Reserved

**MOPSRC[2:0]: Main Output Port, BCK/LRCK/DATA Source Control**

- 000: DIR/XTI Automatic (DIR lock:DIR, DIR unlock:XTI) (default)
- 001: DIR
- 010: XTI
- 011: AUXIN0
- 100: AUXIN1
- 101: AUXIN2
- 110: Reserved
- 111: Reserved

This source control register is divided into two parts (MOSSRC and MOPSRC). This architecture allows some additional functionality such as jitter cleaning. To clean the clock jitter of the HDMI receiver output, the HDMI receiver S/PDIF output is connected with the DIX9211 S/PDIF input, and the HDMI receiver I<sup>2</sup>S outputs (BCK/LRCK/DATA) are connected with the DIX9211 PCM input port.

**Register 6Ch, AUX Output Port (AUXSCKO/AUXBCKO/AUXLRCKO/AUXDOUT) Source Setting  
(Address: 6Ch, Write and Read)**

| DATA          | B7  | B6      | B5      | B4      | B3  | B2      | B1      | B0      |
|---------------|-----|---------|---------|---------|-----|---------|---------|---------|
| Reg Name      | RSV | AOSSRC2 | AOSSRC1 | AOSSRC0 | RSV | AOPSRC2 | AOPSRC1 | AOPSRC0 |
| Default Value | 0   | 0       | 0       | 0       | 0   | 0       | 0       | 0       |
| Memo          |     |         |         |         |     |         |         |         |

**AOSSRC[2:0]: AUX Output Port, SCK Source Control**

- 000: DIR/XTI automatic (DIR lock:DIR, DIR unlock:XTI) (default)
- 001: DIR
- 010: XTI
- 011: AUXIN0
- 100: AUXIN1
- 101: Reserved
- 110: Reserved
- 111: Reserved

**AOPSRC[2:0]: AUX Output Port, BCK/LRCK/DATA Source Control**

- 000: DIR/XTI automatic (DIR lock:DIR, DIR unlock:XTI) (default)
- 001: DIR
- 010: XTI
- 011: AUXIN0
- 100: AUXIN1
- 101: Reserved
- 110: Reserved
- 111: Reserved

This source control register is divided into two parts (MOSSRC and MOPSRC). This design allows some additional functionality such as jitter cleaning. To clean the clock jitter of the HDMI receiver output, the HDMI receiver S/PDIF output is connected to the DIX9211 S/PDIF input, and the HDMI receiver I<sup>2</sup>S outputs (BCK/LRCK/DATA) are connected with the DIX9211 PCM input port.

**Register 6Dh, MPIO\_B and Main Output Port Hi-Z Control  
(Address: 6Dh, Write and Read)**

| DATA          | B7     | B6     | B5     | B4     | B3     | B2    | B1     | B0     |
|---------------|--------|--------|--------|--------|--------|-------|--------|--------|
| Reg Name      | MPB3HZ | MPB2HZ | MPB1HZ | MPB0HZ | SCKOHZ | BCKHZ | LRCKHZ | DOUTHZ |
| Default Value | 0      | 0      | 0      | 0      | 0      | 0     | 0      | 0      |
| Memo          |        |        |        |        |        |       |        |        |

**MPB3HZ: MPIO\_B3, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPBSEL. (default)

1: Hi-Z

**MPB2HZ: MPIO\_B2, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPBSEL. (default)

1: Hi-Z

**MPB1HZ: MPIO\_B1, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPBSEL. (default)

1: Hi-Z

**MPB0HZ: MPIO\_B0, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPBSEL. (default)

1: Hi-Z

**SCKOHZ: Main Output Port, SCKO Hi-Z Control**

0: Output (default)

1: Hi-Z

**BCKHZ: Main Output Port, BCKO Hi-Z Control**

0: Output (default)

1: Hi-Z

**LRCKHZ: Main Output Port, LRCKO Hi-Z Control**

0: Output (default)

1: Hi-Z

**DOUTHZ: Main Output Port, DOUT Hi-Z Control**

0: Output (default)

1: Hi-Z

**Register 6Eh, MPIO\_C and MPIO\_A Hi-Z Control  
(Address: 6Eh, Write and Read)**

| DATA          | B7     | B6     | B5     | B4     | B3     | B2     | B1     | B0     |
|---------------|--------|--------|--------|--------|--------|--------|--------|--------|
| Reg Name      | MPC3HZ | MPC2HZ | MPC1HZ | MPC0HZ | MPA3HZ | MPA2HZ | MPA1HZ | MPA0HZ |
| Default Value | 0      | 0      | 0      | 0      | 1      | 1      | 1      | 1      |
| Memo          |        |        |        |        |        |        |        |        |

**MPC3HZ: MPIO\_C3, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPCSEL. (default)

1: Hi-Z

**MPC2HZ: MPIO\_C2, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPCSEL. (default)

1: Hi-Z

**MPC1HZ: MPIO\_C1, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPCSEL. (default)

1: Hi-Z

**MPC0HZ: MPIO\_C0, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPCSEL. (default)

1: Hi-Z

**MPA3HZ: MPIO\_A3, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPASEL.

1: Hi-Z (default)

**MPA2HZ: MPIO\_A2, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPASEL.

1: Hi-Z (default)

**MPA1HZ: MPIO\_A1, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPASEL.

1: Hi-Z (default)

**MPA0HZ: MPIO\_A0, Hi-Z Control**

0: Defined by Group Function Assign register, 6Fh/MPASEL.

1: Hi-Z (default)

**NOTE**

In multi-channel PCM mode, the MCHR and MPAXHz registers (20h) must be set to '0' to get the outputs from the main port.

**Register 6Fh, MPIO\_A, MPIO\_B, MPIO\_C Group Function Assign  
(Address: 6Fh, Write and Read)**

| DATA          | B7      | B6      | B5      | B4      | B3      | B2      | B1      | B0      |
|---------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Reg Name      | MPASEL1 | MPASEL0 | MPBSEL2 | MPBSEL1 | MPBSEL0 | MPCSEL2 | MPCSEL1 | MPCSEL0 |
| Default Value | 0       | 1       | 0       | 0       | 0       | 0       | 0       | 0       |
| Memo          |         |         |         |         |         |         |         |         |

**MPASEL[1:0]: MPIO\_A Group Function Assign Setting**

- 00: Biphase Input Extension (RXIN8 to RXIN11)
- 01: CLKST Output, VOUT Output, XMCKO Output, INTO Output (default)
- 10: Secondary BCK/LRCK Output, XMCKO Output, INTO Output
- 11: DIR Flags Output or GPIO (Selected by MPA3SEL, MPA2SEL, MPA1SEL, MPA0SEL)

**MPBSEL[2:0]: MPIO\_B Group Function Assign Setting**

- 000: AUXIN2 (default)
- 001: AUXOUT
- 010: Sampling Frequency Calculated Result: FSOUT[3:0]
- 011: DIR Flags Output or GPIO (Selected by MPB3SEL, MPB2SEL, MPB1SEL, MPB0SEL)
- 100: DIR BCUV OUT, BFRAME/VOUT/UOUT/COU
- 101: External Slave ADC Input (Clocks: Out, Data: In, EASCKO/EABCKO/EALRCKO/EADIN)
- 110: Reserved
- 111: Test Mode

**MPCSEL[2:0]: MPIO\_C Group Function Assign Setting**

- 000: AUXIN1 (default)
- 001: Reserved
- 010: Sampling Frequency Calculated Result: FSOUT[3:0]
- 011: DIR Flags Output or GPIO (Selected by MPC3SEL, MPC2SEL, MPC1SEL, MPC0SEL)
- 100: DIR BCUV OUT, BFRAME/VOUT/UOUT/COU
- 101: DIT Standalone Operation, Clock, and Data I/O, TXSCK/TXBCK/TXLRCK/TXDIN
- 110: Reserved
- 111: Reserved

**Register 70h, MPIO\_A Flags or GPIO Assign Setting  
(Address: 70h, Write and Read)**

| DATA          | B7  | B6  | B5       | B4       | B3      | B2      | B1      | B0      |
|---------------|-----|-----|----------|----------|---------|---------|---------|---------|
| Reg Name      | RSV | RSV | MCHRSRC1 | MCHRSRC0 | MPA3SEL | MPA2SEL | MPA1SEL | MPA0SEL |
| Default Value | 0   | 0   | 0        | 0        | 0       | 0       | 0       | 0       |
| Memo          |     |     |          |          |         |         |         |         |

**MCHRSRC: AUX Output Port, SCK Source Control**

- 00: See [Table 28](#), Multi-Channel PCM Routing (default)
- 01: See [Table 28](#), Multi-Channel PCM Routing
- 10: See [Table 28](#), Multi-Channel PCM Routing
- 11: See [Table 28](#), Multi-Channel PCM Routing

**MPA3SEL: MPIO\_A3 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPA3FLG[3:0] (default)
- 1: GPIO, set by GIOA3DIR/GPOA3/GPIA3

**MPA2SEL: MPIO\_A2 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPA2FLG[3:0] (default)
- 1: GPIO, set by GIOA2DIR/GPOA2/GPIA2

**MPA1SEL: MPIO\_A1 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPA1FLG[3:0] (default)
- 1: GPIO, set by GIOA1DIR/GPOA1/GPIA1

**MPA0SEL: MPIO\_A0 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPA0FLG[3:0] (default)
- 1: GPIO, set by GIOA0DIR/GPOA0/GPIA0

**Register 71h, MPIO\_B, MPIO\_C Flags or GPIO Assign Setting  
(Address: 71h, Write and Read)**

| DATA          | B7      | B6      | B5      | B4      | B3      | B2      | B1      | B0      |
|---------------|---------|---------|---------|---------|---------|---------|---------|---------|
| Reg Name      | MPB3SEL | MPB2SEL | MPB1SEL | MPB0SEL | MPC3SEL | MPC2SEL | MPC1SEL | MPC0SEL |
| Default Value | 0       | 0       | 0       | 0       | 0       | 0       | 0       | 0       |
| Memo          |         |         |         |         |         |         |         |         |

**MPB3SEL: MPIO\_B3 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPB3FLG[3:0] (default)
- 1: GPIO, set by GIOB3DIR/GPOB3/GPIB3

**MPB2SEL: MPIO\_B2 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPB2FLG[3:0] (default)
- 1: GPIO, set by GIOB2DIR/GPOB2/GPIB2

**MPB1SEL: MPIO\_B1 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPB1FLG[3:0] (default)
- 1: GPIO, set by GIOB1DIR/GPOB1/GPIB1

**MPB0SEL: MPIO\_B0 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPB0FLG[3:0] (default)
- 1: GPIO, set by GIOB0DIR/GPOB0/GPIB0

**MPC3SEL: MPIO\_C3 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPC3FLG[3:0] (default)
- 1: GPIO, set by GIOC3DIR/GPOC3/GPIC3

**MPC2SEL: MPIO\_C2 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPC2FLG[3:0] (default)
- 1: GPIO, set by GIOC2DIR/GPOC2/GPIC2

**MPC1SEL: MPIO\_C1 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPC1FLG[3:0] (default)
- 1: GPIO, set by GIOC1DIR/GPOC1/GPIC1

**MPC0SEL: MPIO\_C0 Pin Function, DIR Flags or GPIO Select**

- 0: DIR Flags, set by MPC0FLG[3:0] (default)
- 1: GPIO, set by GIOC0DIR/GPOC0/GPIC0

**Register 72h, MPIO\_A1, MPIO\_A0 Output Flag Select  
(Address: 72h, Write and Read)**

| DATA          | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0       |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Reg Name      | MPA1FLG3 | MPA1FLG2 | MPA1FLG1 | MPA1FLG0 | MPA0FLG3 | MPA0FLG2 | MPA0FLG1 | MPA0FLG0 |
| Default Value | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |
| Memo          |          |          |          |          |          |          |          |          |

**MPA1FLG[3:0]: MPIO\_A1 Pin, Flag Select**

0000: CLKST (default)  
 0001: EMPH  
 0010: BPSYNC  
 0011: DTSCD  
 0100: PARITY  
 0101: LOCK  
 0110: VOUT  
 0111: UOUT  
 1000: COUT  
 1001: BFRAME  
 1010: FSOUT0  
 1011: FSOUT1  
 1100: FSOUT2  
 1101: FSOUT3  
 1110: INT0  
 1111: INT1

**MPA0FLG[3:0]: MPIO\_A0 Pin, Flag Select**

0000: CLKST (default)  
 0001: EMPH  
 0010: BPSYNC  
 0011: DTSCD  
 0100: PARITY  
 0101: LOCK  
 0110: VOUT  
 0111: UOUT  
 1000: COUT  
 1001: BFRAME  
 1010: FSOUT0  
 1011: FSOUT1  
 1100: FSOUT2  
 1101: FSOUT3  
 1110: INT0  
 1111: INT1

These register settings are effective only at MPASEL[1:0] = '11', MPA3SEL = '0', and MPA2SEL = '0'.

**Register 73h, MPIO\_A3, MPIO\_A0 Output Flag Select  
(Address: 73h, Write and Read)**

| DATA          | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0       |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Reg Name      | MPA3FLG3 | MPA3FLG2 | MPA3FLG1 | MPA3FLG0 | MPA2FLG3 | MPA2FLG2 | MPA2FLG1 | MPA2FLG0 |
| Default Value | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |
| Memo          |          |          |          |          |          |          |          |          |

**MPA3FLG[3:0]: MPIO\_A3 Pin, Flag Select**

0000: CLKST (default)  
0001: EMPH  
0010: BPSYNC  
0011: DTSCD  
0100: PARITY  
0101: LOCK  
0110: VOUT  
0111: UOUT  
1000: COUT  
1001: BFRAME  
1010: FSOUT0  
1011: FSOUT1  
1100: FSOUT2  
1101: FSOUT3  
1110: INT0  
1111: INT1

**MPA2FLG[3:0]: MPIO\_A2 Pin, Flag Select**

0000: CLKST (default)  
0001: EMPH  
0010: BPSYNC  
0011: DTSCD  
0100: PARITY  
0101: LOCK  
0110: VOUT  
0111: UOUT  
1000: COUT  
1001: BFRAME  
1010: FSOUT0  
1011: FSOUT1  
1100: FSOUT2  
1101: FSOUT3  
1110: INT0  
1111: INT1

These register settings are effective only at MPASEL[1:0] = '11', MPA3SEL = '0', and MPA2SEL = '0'.

**Register 74h, MPIO\_B1, MPIO\_B0 Output Flag Select  
(Address: 74h, Write and Read)**

| DATA          | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0       |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Reg Name      | MPB1FLG3 | MPB1FLG2 | MPB1FLG1 | MPB1FLG0 | MPB0FLG3 | MPB0FLG2 | MPB0FLG1 | MPB0FLG0 |
| Default Value | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |
| Memo          |          |          |          |          |          |          |          |          |

**MPB1FLG[3:0]: MPIO\_B1 Pin, Flag Select**

0000: CLKST (default)  
 0001: EMPH  
 0010: BPSYNC  
 0011: DTSCD  
 0100: PARITY  
 0101: LOCK  
 0110: VOUT  
 0111: UOUT  
 1000: COUT  
 1001: BFRAME  
 1010: FSOUT0  
 1011: FSOUT1  
 1100: FSOUT2  
 1101: FSOUT3  
 1110: INT0  
 1111: INT1

**MPB0FLG[3:0]: MPIO\_B0 Pin, Flag Select**

0000: CLKST (default)  
 0001: EMPH  
 0010: BPSYNC  
 0011: DTSCD  
 0100: PARITY  
 0101: LOCK  
 0110: VOUT  
 0111: UOUT  
 1000: COUT  
 1001: BFRAME  
 1010: FSOUT0  
 1011: FSOUT1  
 1100: FSOUT2  
 1101: FSOUT3  
 1110: INT0  
 1111: INT1

These register settings are effective only at MPBSEL[2:0] = '011', MPB1SEL = '0', and MPB0SEL = '0'.

**Register 75h, MPIO\_B3, MPIO\_B2 Output Flag Select  
(Address: 75h, Write and Read)**

| DATA          | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0       |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Reg Name      | MPB3FLG3 | MPB3FLG2 | MPB3FLG1 | MPB3FLG0 | MPB2FLG3 | MPB2FLG2 | MPB2FLG1 | MPB2FLG0 |
| Default Value | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |
| Memo          |          |          |          |          |          |          |          |          |

**MPB3FLG[3:0]: MPIO\_B3 Pin, Flag Select**

0000: CLKST (default)  
0001: EMPH  
0010: BPSYNC  
0011: DTSCD  
0100: PARITY  
0101: LOCK  
0110: VOUT  
0111: UOUT  
1000: COUT  
1001: BFRAME  
1010: FSOUT0  
1011: FSOUT1  
1100: FSOUT2  
1101: FSOUT3  
1110: INT0  
1111: INT1

**MPB2FLG[3:0]: MPIO\_B2 Pin, Flag Select**

0000: CLKST (default)  
0001: EMPH  
0010: BPSYNC  
0011: DTSCD  
0100: PARITY  
0101: LOCK  
0110: VOUT  
0111: UOUT  
1000: COUT  
1001: BFRAME  
1010: FSOUT0  
1011: FSOUT1  
1100: FSOUT2  
1101: FSOUT3  
1110: INT0  
1111: INT1

These register settings are effective only at MPBSEL[2:0] = '011', MPB3SEL = '0', and MPB2SEL = '0'.

**Register 76h, MPIO\_C1, MPIO\_C0 Output Flag Select  
(Address: 76h, Write and Read)**

| DATA          | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0       |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Reg Name      | MPC1FLG3 | MPC1FLG2 | MPC1FLG1 | MPC1FLG0 | MPC0FLG3 | MPC0FLG2 | MPC0FLG1 | MPC0FLG0 |
| Default Value | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |
| Memo          |          |          |          |          |          |          |          |          |

**MPC1FLG[3:0]: MPIO\_C1 Pin, Flag Select**

0000: CLKST (default)  
 0001: EMPH  
 0010: BPSYNC  
 0011: DTSCD  
 0100: PARITY  
 0101: LOCK  
 0110: VOUT  
 0111: UOUT  
 1000: COUT  
 1001: BFRAME  
 1010: FSOUT0  
 1011: FSOUT1  
 1100: FSOUT2  
 1101: FSOUT3  
 1110: INT0  
 1111: INT1

**MPC0FLG[3:0]: MPIO\_C0 Pin, Flag Select**

0000: CLKST (default)  
 0001: EMPH  
 0010: BPSYNC  
 0011: DTSCD  
 0100: PARITY  
 0101: LOCK  
 0110: VOUT  
 0111: UOUT  
 1000: COUT  
 1001: BFRAME  
 1010: FSOUT0  
 1011: FSOUT1  
 1100: FSOUT2  
 1101: FSOUT3  
 1110: INT0  
 1111: INT1

These register settings are effective only at MPCSEL[2:0] = '011', MPC1SEL = '0', and MPC0SEL = '0'.

**Register 77h, MPIO\_C3, MPIO\_C2 Output Flag Select  
(Address: 77h, Write and Read)**

| DATA          | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0       |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Reg Name      | MPC3FLG3 | MPC3FLG2 | MPC3FLG1 | MPC3FLG0 | MPC2FLG3 | MPC2FLG2 | MPC2FLG1 | MPC2FLG0 |
| Default Value | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |
| Memo          |          |          |          |          |          |          |          |          |

**MPC3FLG[3:0]: MPIO\_C3 Pin, Flag Select**

0000: CLKST (default)  
0001: EMPH  
0010: BPSYNC  
0011: DTSCD  
0100: PARITY  
0101: LOCK  
0110: VOUT  
0111: UOUT  
1000: COUT  
1001: BFRAME  
1010: FSOUT0  
1011: FSOUT1  
1100: FSOUT2  
1101: FSOUT3  
1110: INT0  
1111: INT1

**MPC2FLG[3:0]: MPIO\_C2 Pin, Flag Select**

0000: CLKST (default)  
0001: EMPH  
0010: BPSYNC  
0011: DTSCD  
0100: PARITY  
0101: LOCK  
0110: VOUT  
0111: UOUT  
1000: COUT  
1001: BFRAME  
1010: FSOUT0  
1011: FSOUT1  
1100: FSOUT2  
1101: FSOUT3  
1110: INT0  
1111: INT1

These register settings are effective only at MPCSEL[2:0] = '011', MPC3SEL = '0', and MPC2SEL = '0'.

**Register 78h, MPO1, MPO0 Function Assign Setting  
(Address: 78h, Write and Read)**

| DATA          | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0       |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Reg Name      | MPO1SEL3 | MPO1SEL2 | MPO1SEL1 | MPO1SEL0 | MPO0SEL3 | MPO0SEL2 | MPO0SEL1 | MPO0SEL0 |
| Default Value | 0        | 0        | 1        | 1        | 1        | 1        | 0        | 1        |
| Memo          |          |          |          |          |          |          |          |          |

**MPO1SEL[3:0]: MPO1 Pin, Output Control**

0000: Hi-Z  
 0001: GPO, Output data = High level  
 0010: GPO, Output data = Low level  
 0011: VOUT (default)  
 0100: INT0  
 0101: INT1  
 0110: CLKST  
 0111: EMPH  
 1000: BPSYNC  
 1001: DTSCD  
 1010: PARITY  
 1011: LOCK  
 1100: XMCKO  
 1101: TXOUT  
 1110: RECOUT0  
 1111: RECOUT1

**MPO0SEL[3:0]: MPO0 Pin, Output Control**

0000: Hi-Z  
 0001: GPO, Output data = High level  
 0010: GPO, Output data = Low level  
 0011: VOUT  
 0100: INT0  
 0101: INT1  
 0110: CLKST  
 0111: EMPH  
 1000: BPSYNC  
 1001: DTSCD  
 1010: PARITY  
 1011: LOCK  
 1100: XMCKO  
 1101: TXOUT (default)  
 1110: RECOUT0  
 1111: RECOUT1

**Register 79h, GPIO I/O Direction Control for MPIO\_A, MPIO\_B  
(Address: 79h, Write and Read)**

| DATA          | B7       | B6       | B5       | B4       | B3       | B2       | B1       | B0       |
|---------------|----------|----------|----------|----------|----------|----------|----------|----------|
| Reg Name      | GIOB3DIR | GIOB2DIR | GIOB1DIR | GIOB0DIR | GIOA3DIR | GIOA2DIR | GIOA1DIR | GIOA0DIR |
| Default Value | 0        | 0        | 0        | 0        | 0        | 0        | 0        | 0        |
| Memo          |          |          |          |          |          |          |          |          |

**GIOB3DIR: MPIO\_B3 Pin, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOB2DIR: MPIO\_B2 Pin, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOB1DIR: MPIO\_B1 Pin, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOB0DIR: MPIO\_B0 Pin, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOA3DIR: MPIO\_A3 Pin Function, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOA2DIR: MPIO\_A2 Pin Function, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOA1DIR: MPIO\_A1 Pin Function, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOA0DIR: MPIO\_A0 Pin Function, GPIO I/O Direction Control**

0: Input (default)

1: Output

These registers are effective only at MPIO\_A and MPIO\_B assigned as GPIO. I/O direction setting is available by pin.

**Register 7Ah, GPIO I/O Direction Control for MPIO\_C  
(Address: 7Ah, Write and Read)**

| DATA          | B7  | B6  | B5  | B4  | B3       | B2       | B1       | B0       |
|---------------|-----|-----|-----|-----|----------|----------|----------|----------|
| Reg Name      | RSV | RSV | RSV | RSV | GIOC3DIR | GIOC2DIR | GIOC1DIR | GIOC0DIR |
| Default Value | 0   | 0   | 0   | 0   | 0        | 0        | 0        | 0        |
| Memo          |     |     |     |     |          |          |          |          |

**GIOC3DIR: MPIO\_C3 Pin, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOC2DIR: MPIO\_C2 Pin, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOC1DIR: MPIO\_C1 Pin, GPIO I/O Direction Control**

0: Input (default)

1: Output

**GIOC0DIR: MPIO\_C0 Pin, GPIO I/O Direction Control**

0: Input (default)

1: Output

These registers are effective only at MPIO\_C assigned as GPIO. I/O direction setting is available by pin.

**Register 7Bh, GPIO Output Data Setting for MPIO\_A, MPIO\_B  
(Address: 7Bh, Write and Read)**

| DATA          | B7    | B6    | B5    | B4    | B3    | B2    | B1    | B0    |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Reg Name      | GPOB3 | GPOB2 | GPOB1 | GPOB0 | GPOA3 | GPOA2 | GPOA1 | GPOA0 |
| Default Value | 0     | 0     | 0     | 0     | 0     | 0     | 0     | 0     |
| Memo          |       |       |       |       |       |       |       |       |

**GPOB3: MPIO\_B3 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOB2: MPIO\_B2 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOB1: MPIO\_B1 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOB0: MPIO\_B0 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOA3: MPIO\_A3 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOA2: MPIO\_A2 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOA1: MPIO\_A1 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOA0: MPIO\_A0 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

These registers are effective only as GPIOs are assigned to output.

**Register 7Ch, GPIO Output Data Setting for MPIO\_C  
(Address: 7Ch, Write and Read)**

| DATA          | B7  | B6  | B5  | B4  | B3    | B2    | B1    | B0    |
|---------------|-----|-----|-----|-----|-------|-------|-------|-------|
| Reg Name      | RSV | RSV | RSV | RSV | GPOC3 | GPOC2 | GPOC1 | GPOC0 |
| Default Value | 0   | 0   | 0   | 0   | 0     | 0     | 0     | 0     |
| Memo          |     |     |     |     |       |       |       |       |

**GPOC3: MPIO\_C3 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOC2: MPIO\_C2 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOC1: MPIO\_C1 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

**GPOC0: MPIO\_C0 Pin, GPIO Output Data Setting**

- 0: Output low level (default)
- 1: Output high level

These registers are effective only as GPIOs are assigned to output.

**Register 7Dh, GPIO Input Data Register for MPIO\_A, MPIO\_B  
(Address: 7Dh, Read-Only)**

| DATA          | B7    | B6    | B5    | B4    | B3    | B2    | B1    | B0    |
|---------------|-------|-------|-------|-------|-------|-------|-------|-------|
| Reg Name      | GPIB3 | GPIB2 | GPIB1 | GPIB0 | GPIA3 | GPIA2 | GPIA1 | GPIA0 |
| Default Value | N/A   | N/A   | N/A   | N/A   | N/A   | N/A   | N/A   | N/A   |
| Memo          |       |       |       |       |       |       |       |       |

**GPIB3: MPIO\_B3 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIB2: MPIO\_B2 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIB1: MPIO\_B1 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIB0: MPIO\_B0 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIA3: MPIO\_A3 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIA2: MPIO\_A2 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIA1: MPIO\_A1 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIA0: MPIO\_A0 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**Register 7Eh, GPIO Input Data Register for MPIO\_C  
(Address: 7Eh, Read-Only)**

| DATA          | B7  | B6  | B5  | B4  | B3    | B2    | B1    | B0    |
|---------------|-----|-----|-----|-----|-------|-------|-------|-------|
| Reg Name      | RSV | RSV | RSV | RSV | GPIC3 | GPIC2 | GPIC1 | GPIC0 |
| Default Value | N/A | N/A | N/A | N/A | N/A   | N/A   | N/A   | N/A   |
| Memo          |     |     |     |     |       |       |       |       |

**GPIC3: MPIO\_C3 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIC2: MPIO\_C2 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIC1: MPIO\_C1 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

**GPIC0: MPIO\_C0 Pin, GPIO Input Data**

0: Detect low level

1: Detect high level

## PACKAGING INFORMATION

| Orderable part number      | Status<br>(1) | Material type<br>(2) | Package   Pins | Package qty   Carrier  | RoHS<br>(3) | Lead finish/<br>Ball material<br>(4) | MSL rating/<br>Peak reflow<br>(5) | Op temp (°C) | Part marking<br>(6) |
|----------------------------|---------------|----------------------|----------------|------------------------|-------------|--------------------------------------|-----------------------------------|--------------|---------------------|
| <a href="#">DIX9211PT</a>  | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (5+1) | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | DIX9211             |
| DIX9211PT.B                | Active        | Production           | LQFP (PT)   48 | 250   JEDEC TRAY (5+1) | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | DIX9211             |
| <a href="#">DIX9211PTR</a> | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | DIX9211             |
| DIX9211PTR.B               | Active        | Production           | LQFP (PT)   48 | 1000   LARGE T&R       | Yes         | NIPDAU                               | Level-1-260C-UNLIM                | -40 to 85    | DIX9211             |

<sup>(1)</sup> **Status:** For more details on status, see our [product life cycle](#).

<sup>(2)</sup> **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

<sup>(3)</sup> **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

<sup>(4)</sup> **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

<sup>(5)</sup> **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

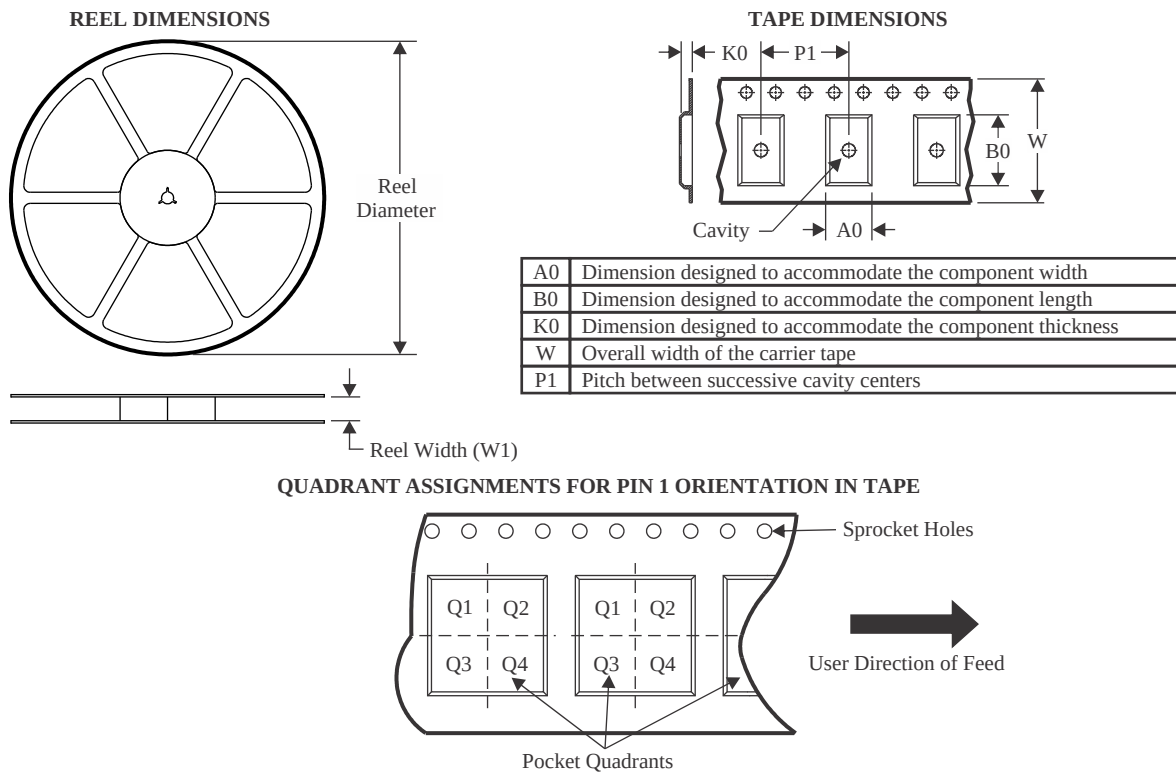
<sup>(6)</sup> **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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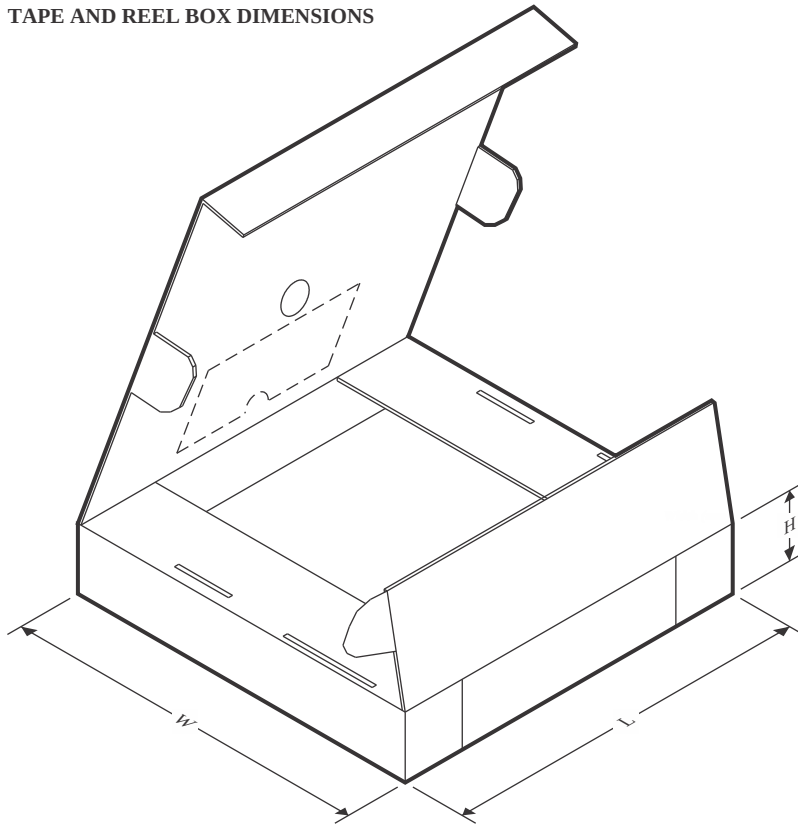
## TAPE AND REEL INFORMATION



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| DIX9211PTR | LQFP         | PT              | 48   | 1000 | 330.0              | 16.4               | 9.6     | 9.6     | 1.9     | 12.0    | 16.0   | Q2            |

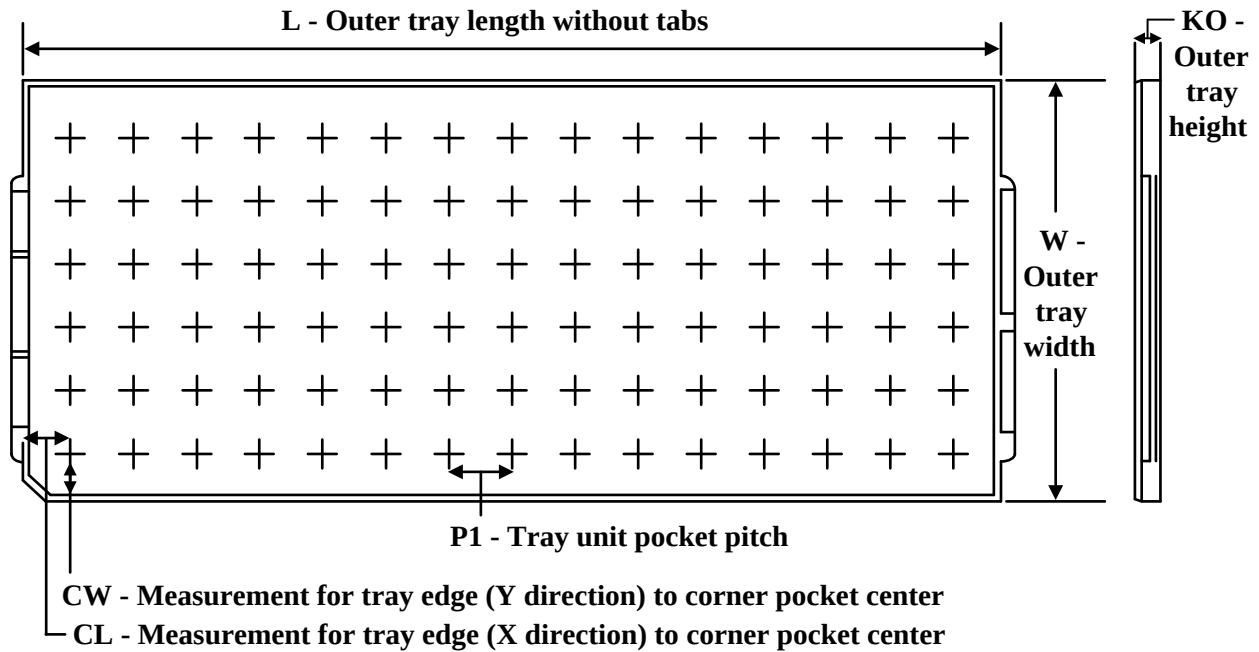
## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device     | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|------------|--------------|-----------------|------|------|-------------|------------|-------------|
| DIX9211PTR | LQFP         | PT              | 48   | 1000 | 350.0       | 350.0      | 43.0        |

## TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

\*All dimensions are nominal

| Device      | Package Name | Package Type | Pins | SPQ | Unit array matrix | Max temperature (°C) | L (mm) | W (mm) | K0 (μm) | P1 (mm) | CL (mm) | CW (mm) |
|-------------|--------------|--------------|------|-----|-------------------|----------------------|--------|--------|---------|---------|---------|---------|
| DIX9211PT   | PT           | LQFP         | 48   | 250 | 10 x 25           | 150                  | 315    | 135.9  | 7620    | 12.2    | 11.1    | 11.25   |
| DIX9211PT.B | PT           | LQFP         | 48   | 250 | 10 x 25           | 150                  | 315    | 135.9  | 7620    | 12.2    | 11.1    | 11.25   |

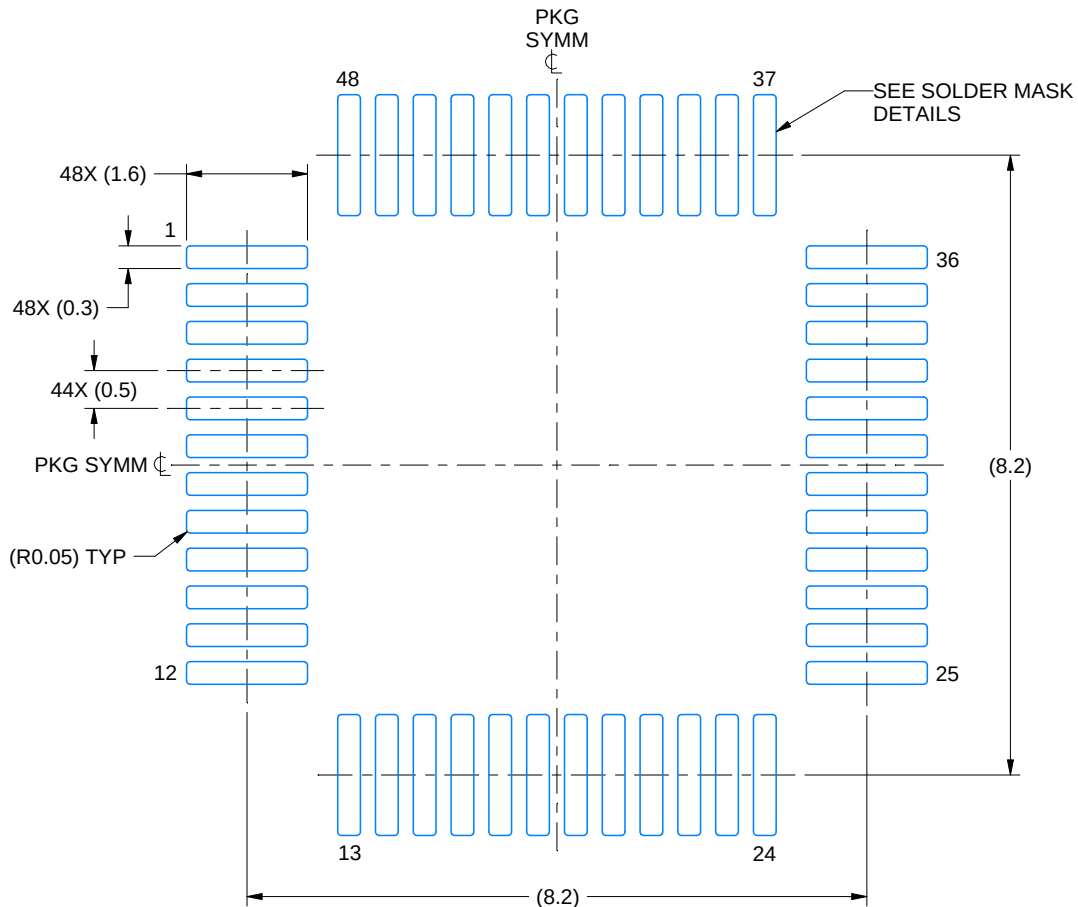


# EXAMPLE BOARD LAYOUT

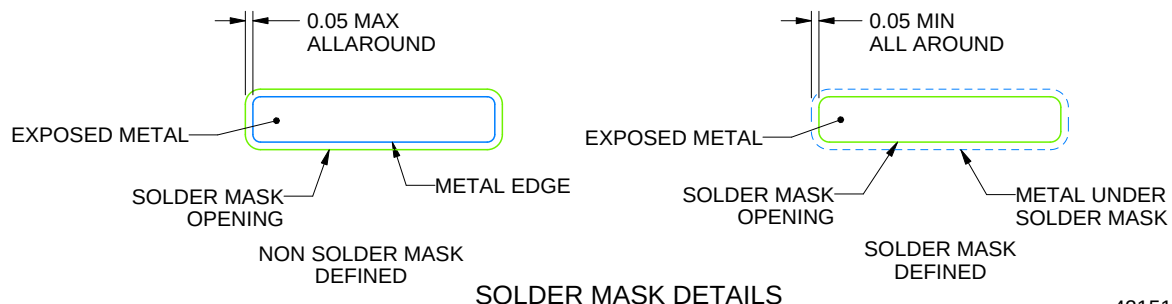
PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE 10.000



SOLDER MASK DETAILS

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NOTES: (continued)

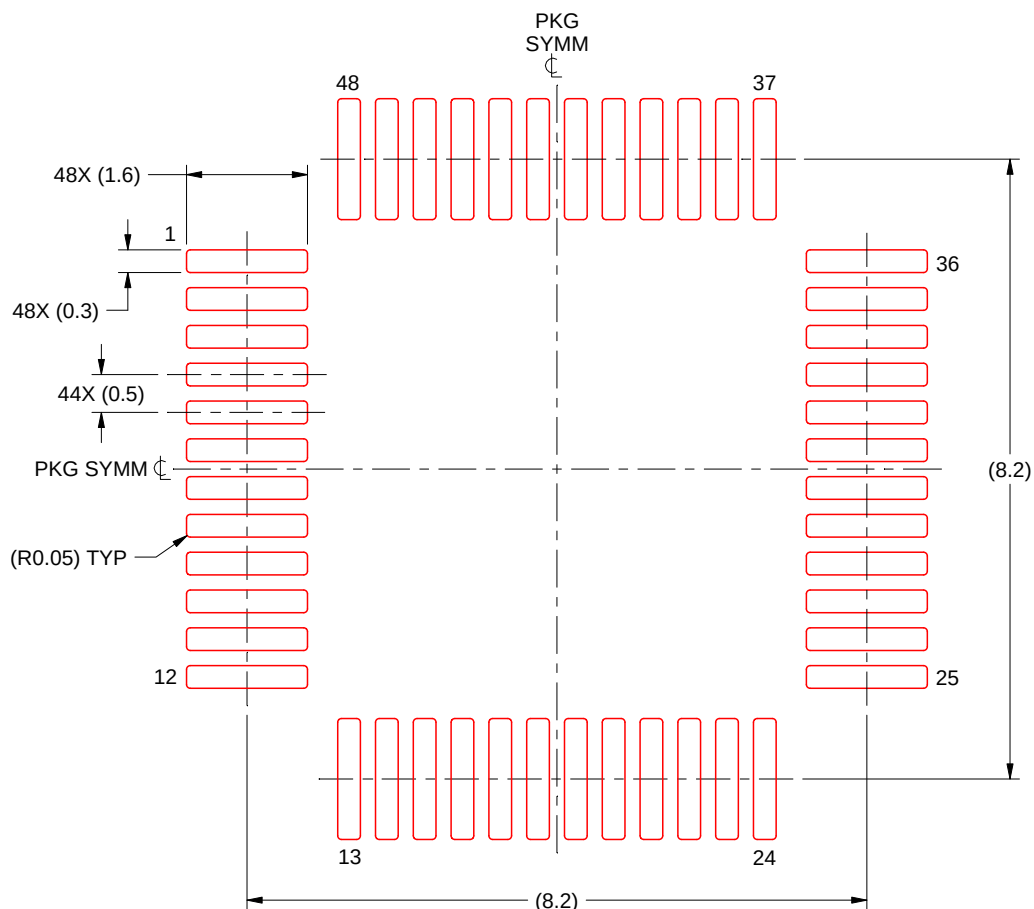
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PT0048A

LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK



SOLDER PASTE EXAMPLE  
BASED ON 0.1 mm THICK STENCIL  
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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