

DLP472TP 0.47 4K UHD Digital Micromirror Device

1 Features

- 0.47-inch diagonal micromirror array
 - 4K UHD (3840 × 2160) display resolution
 - 5.4µm micromirror pitch
 - ±17° micromirror tilt (relative to the flat surface)
 - Bottom illumination
- SubLVDS input data bus
- Supports 4K UHD at 60Hz
- Supports 1080p up to 240Hz
- LED operation supported by the DLPC8445 display controller and the DLPA3085 power management IC (PMIC) and LED driver

2 Applications

- [Mobile smart TV](#)
- [Mobile projector](#)
- [Digital signage](#)

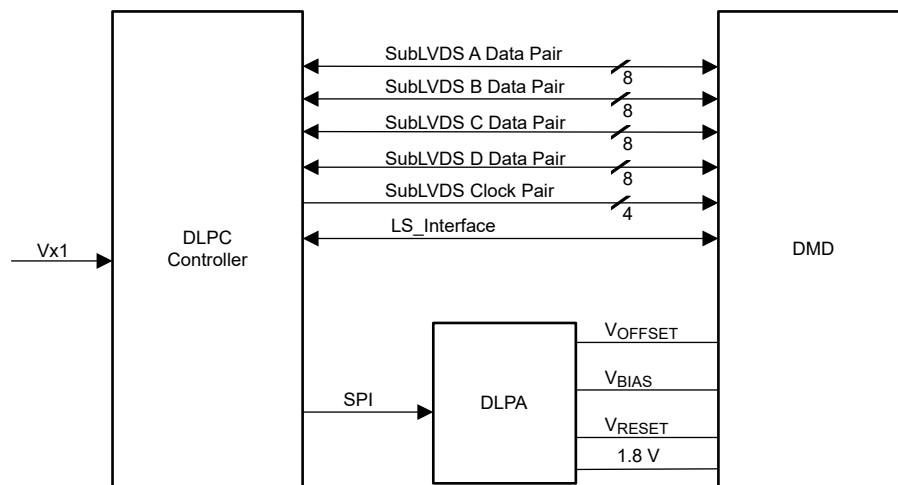
3 Description

The DLP472TP digital micromirror device (DMD) is a digitally controlled micro-electro-mechanical system (MEMS) spatial light modulator (SLM) that enables bright 4K UHD display systems. The TI DLP® products 0.47" 4K UHD chipset comprises the DLP472TP DMD, the DLPC8445 display controller, and the DLPA3085 PMIC and LED driver. The compact physical size of the chipset provides a complete system solution that enables small form factor 4K UHD displays.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	PACKAGE SIZE
DLP472TP	FQY (166)	24.50mm × 11.00mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

ADVANCE INFORMATION

4 Device and Documentation Support

4.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

4.2 Device Support

4.2.1 Device Nomenclature

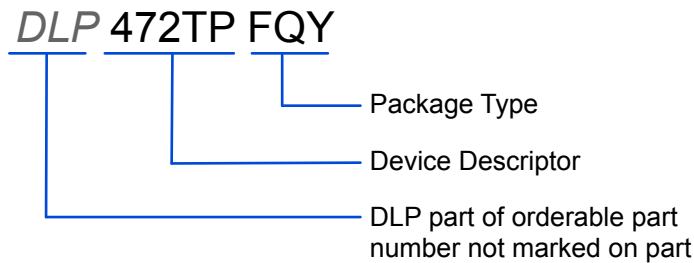


Figure 4-1. Part Number Description

4.2.2 Device Markings

The device marking includes both human-readable information and a 2-dimensional matrix code. The human-readable information is described in Figure 4-2 and includes the legible character string GHJJJK 472TPFQY. GHJJJK is the lot trace code and 472TPFQY is the device marking.

Example: GHJJJK DLP472TPFQY

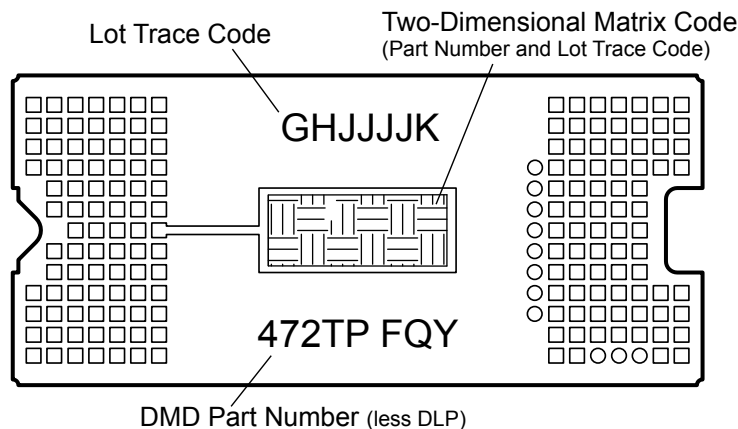


Figure 4-2. DMD Marking Locations

4.3 Documentation Support

4.3.1 Related Documentation

The following documents contain additional information related to the chipset components used with the DMD.

- [DLPC8445 High Resolution Controller Data Sheet](#)
- [DLPA3085 PMIC and High-Current LED Driver IC Data Sheet](#)

4.4 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

4.5 Trademarks

DLP® is a registered trademark of Texas Instruments.
All trademarks are the property of their respective owners.

4.6 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

4.7 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
May 2024	*	Initial Release

6 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XDLP472TPFQY	ACTIVE	CLGA	FQY	174	80	RoHS & Green	NI/AU	N / A for Pkg Type	0 to 70		Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

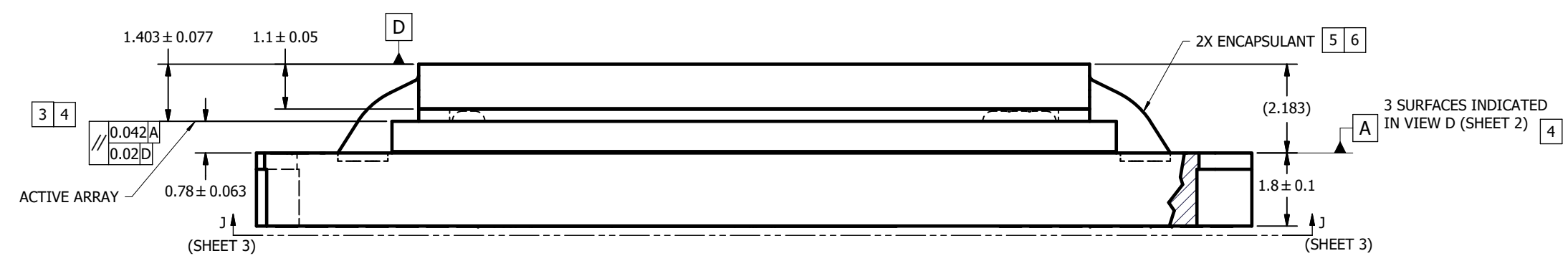
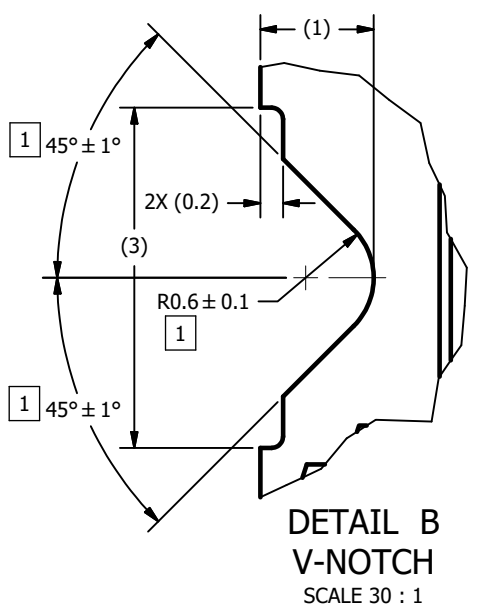
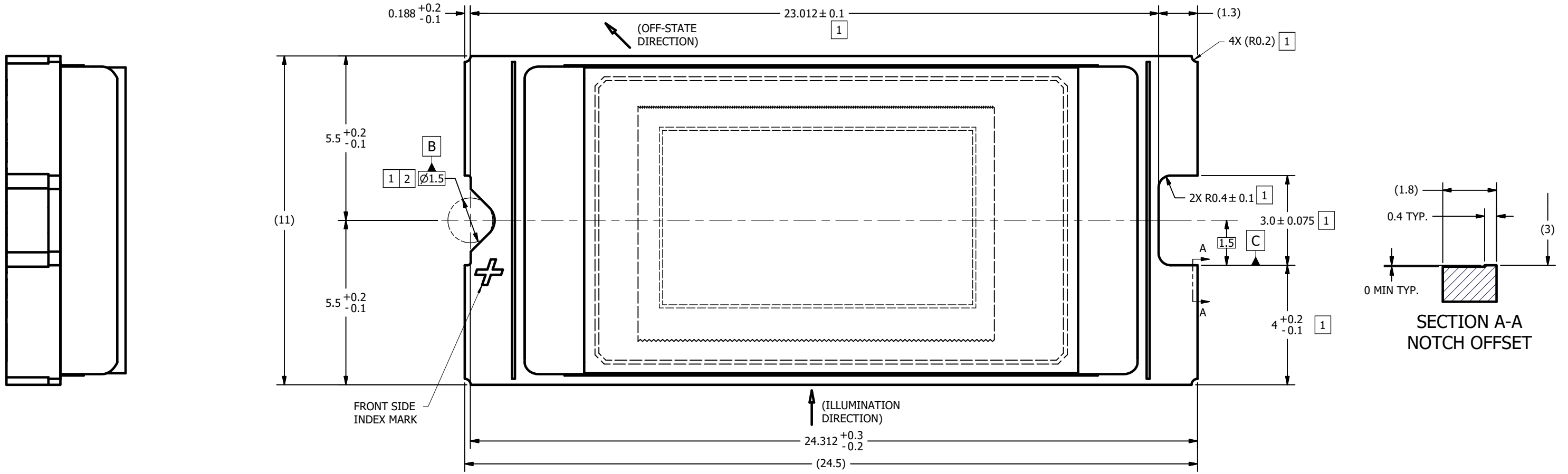
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

© COPYRIGHT 2022 TEXAS INSTRUMENTS
UN-PUBLISHED. ALL RIGHTS RESERVED.

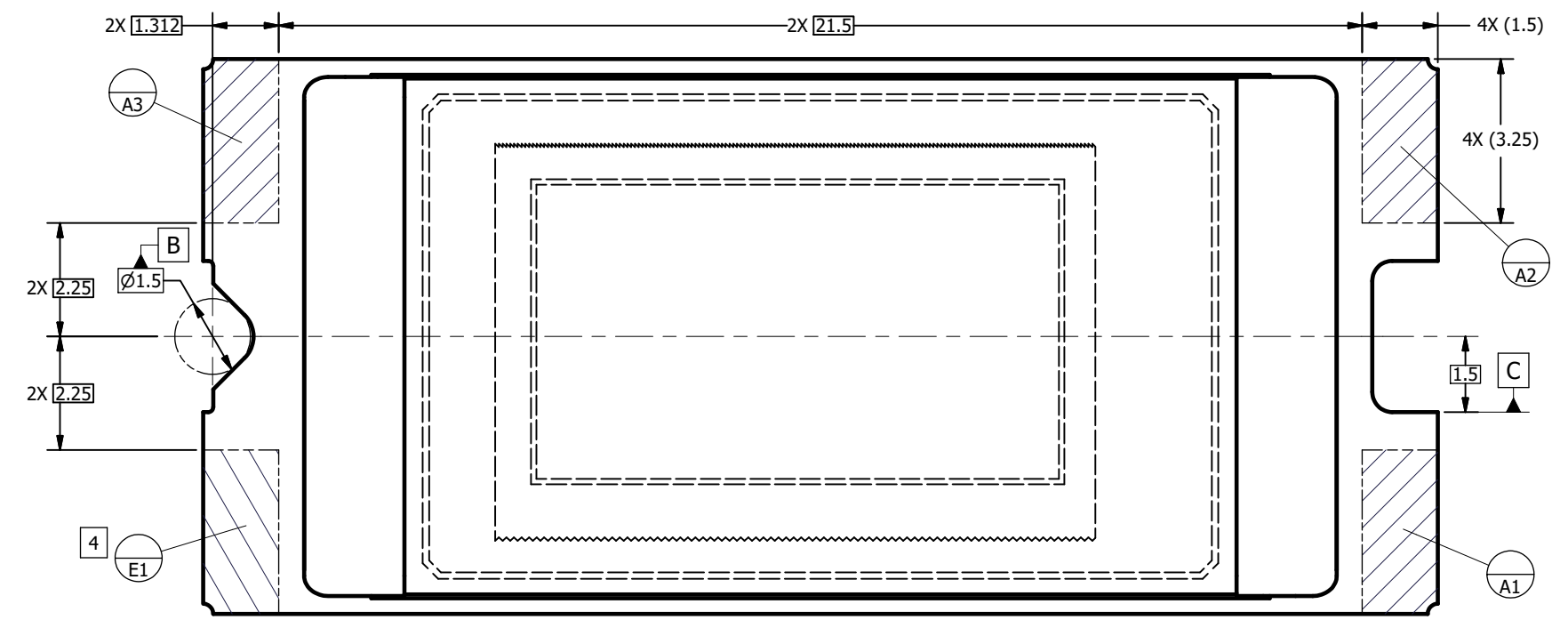
REVISIONS		DATE	BY
REV	DESCRIPTION		
A	ECO 2202674: INITIAL RELEASE	12/22/22	HG

NOTES UNLESS OTHERWISE SPECIFIED:

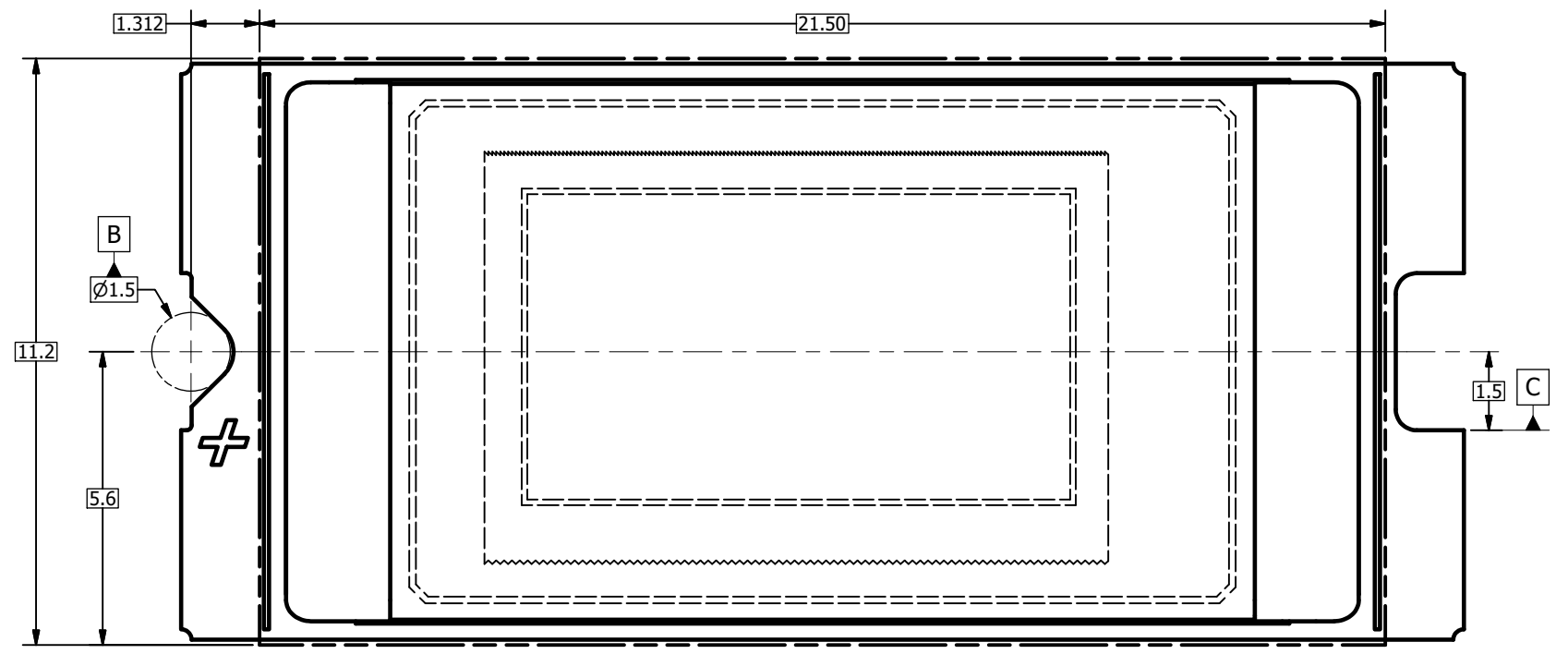
- 1 NOTCH DIMENSIONS ARE DEFINED BY UPPERMOST LAYERS OF CERAMIC, AS SHOWN IN SECTION A-A.
- 2 SEE DETAIL B FOR "V-NOTCH" DIMENSIONS.
- 3 DIE PARALLELISM TOLERANCE APPLIES TO DMD ACTIVE ARRAY ONLY.
- 4 WHILE ONLY THE THREE DATUM A TARGET AREAS A1, A2, AND A3 ARE USED FOR MEASUREMENT, ALL 4 CORNERS SHOULD BE CONTACTED, INCLUDING E1, TO SUPPORT MECHANICAL LOADS.
- 5 ENCAPSULANT TO BE CONTAINED WITHIN DIMENSIONS SHOWN IN VIEW D (SHEET 2). NO ENCAPSULANT IS ALLOWED ON TOP OF THE WINDOW.
- 6 ENCAPSULANT NOT TO EXCEED THE HEIGHT OF THE WINDOW.
- 7 ROTATION ANGLE OF DMD ACTIVE ARRAY IS A REFINEMENT OF THE LOCATION TOLERANCE AND HAS A MAXIMUM ALLOWED VALUE OF 0.6 DEGREES.
- 8 BOUNDARY MIRRORS SURROUNDING THE DMD ACTIVE ARRAY.



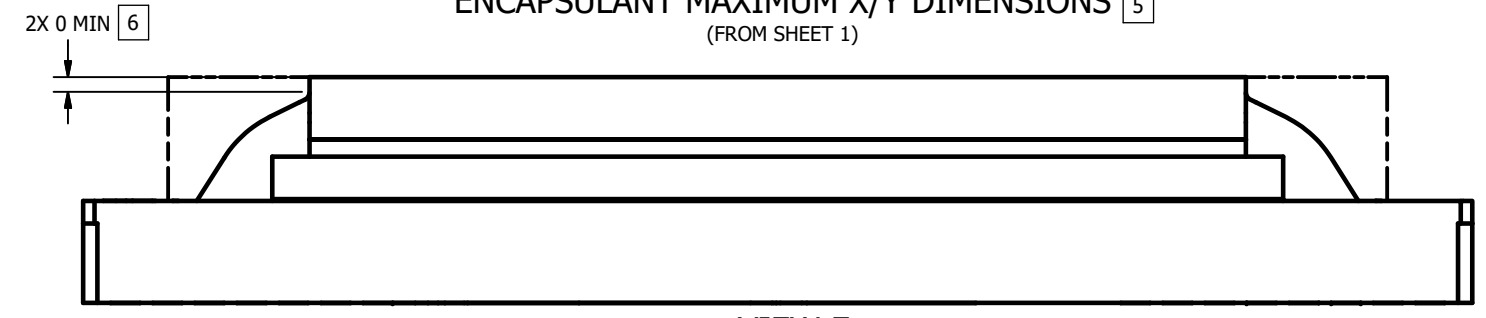
UNLESS OTHERWISE SPECIFIED		DRAWN H. GAGLIARDI DATE 12/22/2023		 TEXAS INSTRUMENTS Dallas, Texas	
● DIMENSIONS ARE IN MILLIMETERS ● TOLERANCES: ANGLES ± 1° 2 PLACE DECIMALS ± 0.25 1 PLACE DECIMALS ± 0.50 ● DIMENSIONAL LIMITS APPLY BEFORE PROCEEDING ● INTERPRET DIMENSIONS IN ACCORDANCE WITH ASME Y14.5M-1994 ● REMOVE ALL BURRS AND SHARP EDGES ● PARENTHETICAL INFORMATION FOR REFERENCE ONLY		ENGINEER H. GAGLIARDI 12/22/2022 QA/CE P. KONRAD 12/27/2022 CM B. HASKETT 12/22/2022			
THIRD ANGLE PROJECTION NEXT ASSY 0314DA USED ON APPLICATION		APPROVED J. MCKINLEY 12/22/2022 M. GARCIA 1/3/2023		SIZE D DWG NO. 2518523 REV A SCALE 15:1 SHEET 1 OF 3	



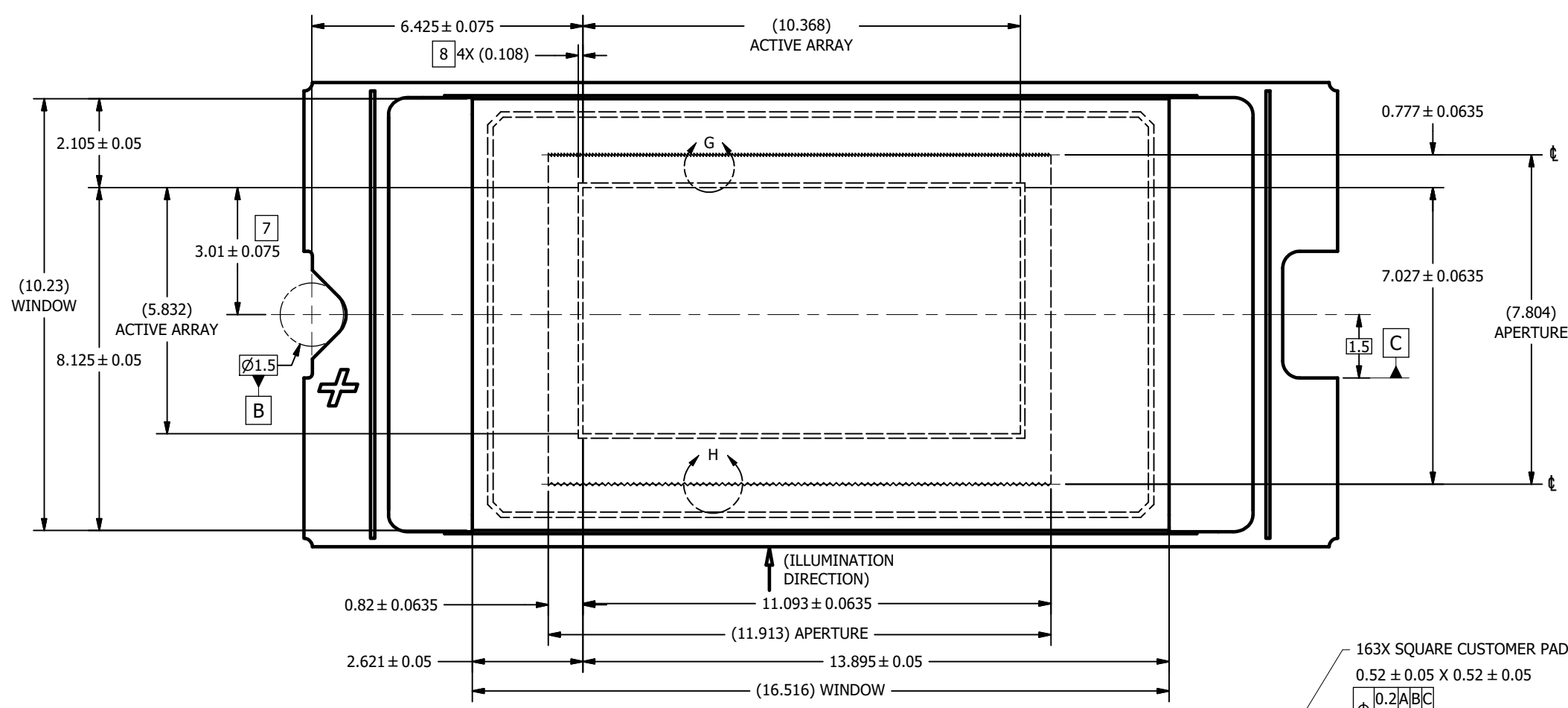
VIEW C
DATUMS A AND E
 (SUBSTRATE METALLIZATION OMITTED FOR CLARITY)
 (FROM SHEET 1)



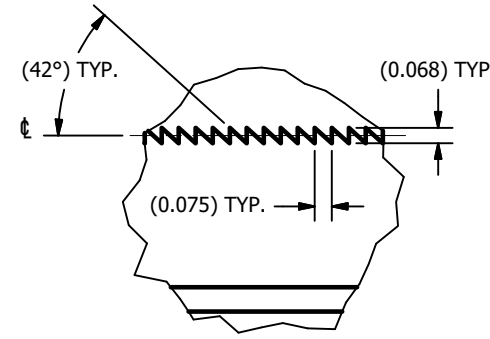
VIEW D
ENCAPSULANT MAXIMUM X/Y DIMENSIONS 5
 (FROM SHEET 1)



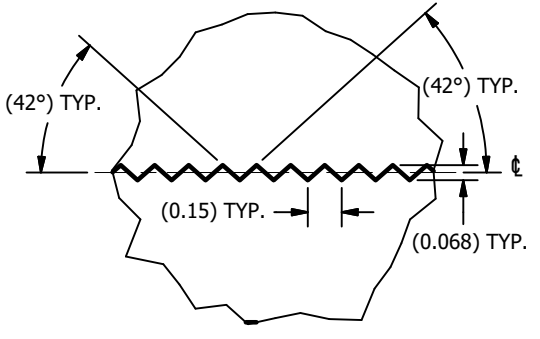
VIEW E
ENCAPSULANT MAXIMUM HEIGHT



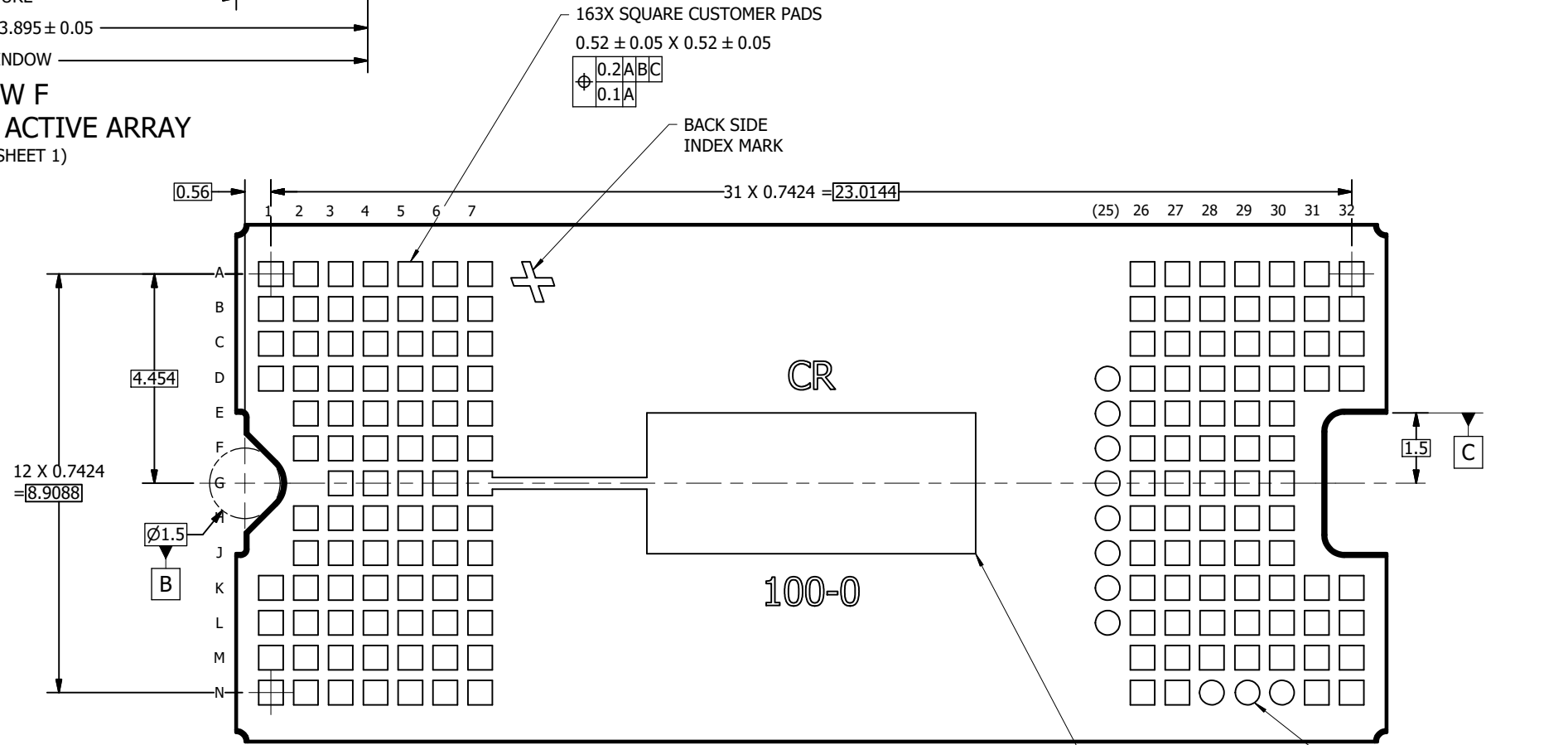
VIEW F
WINDOW AND ACTIVE ARRAY
(FROM SHEET 1)



DETAIL G
APERTURE TOP EDGE
SCALE 60 : 1



DETAIL H
APERTURE BOTTOM EDGE
SCALE 60 : 1



VIEW J-J
BACK SIDE METALLIZATION
(FROM SHEET 1)

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2024, Texas Instruments Incorporated