

DLPC23xS-Q1 Automotive Digital Micromirror Device Controller

1 Features

- Qualified for automotive applications
- AEC-Q100 qualified with the following results:
 - Device temperature grade 2: –40°C to +105°C ambient operating temperature
 - Device HBM ESD classification level 2
 - Device CDM ESD classification level C4B
- [Functional Safety Quality-Managed](#)
 - Documentation available to aid ISO 26262 functional safety system design up to ASIL-B
- DMD display controller supporting:
 - DLP553xS-Q1 and DLP462xS-Q1 automotive interior display chipsets
- Video processing
 - Scales input image to match DMD resolution
 - Bezel adjustment up ±50% vertical image position and ±10% horizontal reducing the need for mechanical alignment (HUD)
 - Support for pixel doubling or quadrupling to allow low resolution video input
 - Gamma correction
- Embedded processor with error correction (ECC)
 - On-chip diagnostic and self-test capability
 - System diagnostics including temperature monitoring, device interface monitoring, and photodiode monitoring
 - Integrated management of smooth dimming
 - Configurable GPIO
- No external RAM required, internal SRAM for image processing
- 600MHz SubLVDS DMD interface for low power and emission
- Spread spectrum clocking for reduced EMI
- Video input interface
 - Single OpenLDI (FPD-Link I) port up to 110MHz
 - 24-bit RGB parallel interface up to 110MHz
- Configurable host control interface
 - Serial peripheral interface (SPI) 10MHz
 - I²C (400kHz)
 - Host IRQ signal to provide real-time feedback for critical system errors
- Interface to TPS99000S-Q1 system management and illumination controller

2 Applications

- [Wide field of view and augmented reality head-up display \(HUD\)](#)
- Digital cluster, navigation, and infotainment windshield displays

3 Description

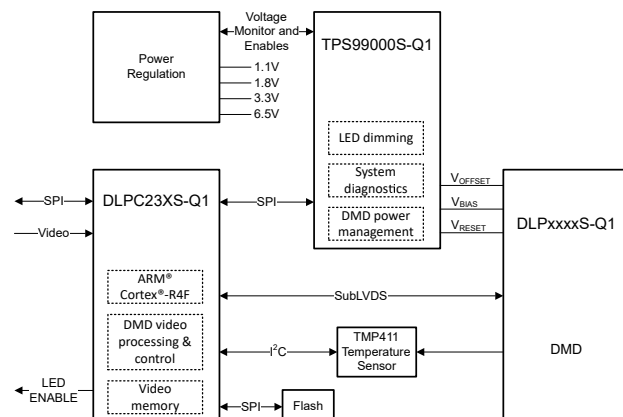
The DLPC23xS-Q1 digital micromirror device (DMD) Controller for automotive applications is used in chipsets for interior and exterior display applications with a functional safety requirement (such as augmented reality HUDs and windshield clusters). The [DLP5530S-Q1](#) chipset includes a 0.55" DMD and the [DLP4620S-Q1](#) chipset includes a 0.46" DMD. Both chipsets also include the TPS99000S-Q1 System Management and Illumination controller. The DLPC23xS-Q1 integrates an embedded processor with error code correction (SECDED ECC), enabling host control and real-time feedback, on-chip diagnostics, and system monitoring functions. On-chip SRAM is included to remove the need for external DRAM. Combined with the TPS99000S-Q1, the DLPC23xS-Q1 supports high dynamic range dimming of over 5000:1 for HUD applications. SubLVDS 600MHz DMD interface allows high DMD refresh rates to generate seamless and brilliant digital images, while simultaneously reducing radiated emissions.

To aid in the design and manufacture of automotive qualified projectors based on DLP technology, there are a number of established [optical module manufacturers and design houses](#) that can be leveraged to support your design.

Device Information

| PART NUMBER | PACKAGE ⁽¹⁾ | BODY SIZE (NOM) |
|-------------|------------------------|-------------------|
| DLPC230S-Q1 | ZDQ (BGA, 324) | 23.00mm × 23.00mm |
| DLPC231S-Q1 | ZEK (nFBGA, 324) | 15.00mm × 15.00mm |

(1) For more information, see the *Mechanical, Packaging, and Orderable* addendum.



DLP5530S-Q1 or DLP4620S-Q1 TI DLP® Chipset System Block Diagram



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4 Pin Configuration and Functions

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 | 18 | 19 | 20 | 21 | 22 | |
|----|----------------|------------------|------------------|------------------|------------------|---------------|------------------|------------------|------------------|------------------|-----------------|---------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|------------------|-------------|-------------|-------------|
| A | GND18A_LVDS | DMD_HS1_WDATA0_N | DMD_HS1_WDATA1_N | DMD_HS1_WDATA2_N | DMD_HS1_WDATA3_N | DMD_HS1_CLK_N | DMD_HS1_WDATA4_N | DMD_HS1_WDATA5_N | DMD_HS1_WDATA6_N | DMD_HS1_WDATA7_N | DMD_LSO_WDATA_N | DMD_LSO_CLK_N | DMD_HSO_WDATA7_N | DMD_HSO_WDATA6_N | DMD_HSO_WDATA5_N | DMD_HSO_WDATA4_N | DMD_HSO_WDATA3_N | DMD_HSO_WDATA2_N | DMD_HSO_WDATA1_N | DMD_HSO_WDATA0_N | GND18A_LVDS | | |
| B | VCC18A_LVDS | DMD_HS1_WDATA0_P | DMD_HS1_WDATA1_P | DMD_HS1_WDATA2_P | DMD_HS1_WDATA3_P | DMD_HS1_CLK_P | DMD_HS1_WDATA4_P | DMD_HS1_WDATA5_P | DMD_HS1_WDATA6_P | DMD_HS1_WDATA7_P | DMD_LSO_WDATA_P | DMD_LSO_CLK_P | DMD_HSO_WDATA7_P | DMD_HSO_WDATA6_P | DMD_HSO_WDATA5_P | DMD_HSO_WDATA4_P | DMD_HSO_WDATA3_P | DMD_HSO_WDATA2_P | DMD_HSO_WDATA1_P | DMD_HSO_WDATA0_P | VCC18A_LVDS | | |
| C | VCC18A_LVDS | GND18A_LVDS | GND18A_LVDS | GND18A_LVDS | GND18A_LVDS | GND18A_LVDS | GND18A_LVDS | DMD_LSO_RDATA | DMD_LSO_RDATA | DMD_LSO_WDATA | DMD_LSO_CLK | GND11AD_PLLD | GND11AD_PLLM | GNDIOLA_COSC | VCC3IO_COSC | VCC3IO_COSC | GND18A_LVDS | GND18A_LVDS | GND18A_LVDS | GND18A_LVDS | GND18A_LVDS | VCC18A_LVDS | VCC18A_LVDS |
| D | PMIC_SPI_DOUT | VCC18A_LVDS | VCC18A_LVDS | VCC18A_LVDS | VCC18A_LVDS | RPI_1 | VCC18A_LVDS | GND18A_LVDS | RPI_LS | VCC18IO | DMD_DE_N_ARSTZ | VCC11AD_PLLD | VCC11AD_PLLM | PLL_REFCLK_O | PLL_REFCLK_I | OSC_BYPASS | RPI_0 | VCC18A_LVDS | VCC18A_LVDS | VCC18A_LVDS | VCC18A_LVDS | VCC18A_LVDS | GPIO_31 |
| E | PMIC_SPI_CLK | PMIC_SPI_CSZ_0 | PMIC_PA_RKZ | VCC11A_DDI_1 | | | | | | | | | | | | | | VCC11A_DDI_0 | VCC18A_LVDS | GPIO_30 | GPIO_29 | | |
| F | PMIC_SPI_DIN | PMIC_LED_SEL_0 | RESETZ | VCC11A_DDI_1 | | | | | | | | | | | | | | VCC11A_DDI_0 | GPIO_28 | GPIO_27 | GPIO_26 | | |
| G | PMIC_LED_SEL_1 | PMIC_LED_SEL_2 | PMIC_INT_Z | VCC | | | | | | | | | | | | | | VCC3IO_2 | JTAGTDO_3 | JTAGTMS_1 | JTAGTCK | | |
| H | PMIC_LED_SEL_3 | PMIC_AD_3_CLK | HWTEST_EN | VCC3IO_MVGP | | | | | | | | | | | | | | VCC | JTAGTDO_2 | VSYN | HSYN | | |
| J | PMIC_AD_3_MISO | PMIC_AD_3_MISO | GPIO_00 | VCC3IO | | | | GND | GND | VCC | GND | GND | GND | | | | | VCC | JTAGTDO_1 | PDATA_2_3 | PDATA_2_2 | | |
| K | GPIO_01 | GPIO_02 | GPIO_03 | VCC3IO | | | | GND | GND | GND | GND | GND | GND | | | | | VCC3IO_1_NTF | JTAGTDI | PDATA_2_1 | PDATA_2_0 | | |
| L | GPIO_04 | GPIO_05 | GPIO_06 | VCC | | | | GND | GND | GND | GND | GND | GND | | | | | VCC3IO_1_NTF | JTAGTRST | PDATA_1_9 | PDATA_1_8 | | |
| M | GPIO_07 | GPIO_08 | GPIO_09 | VCC3IO | | | | GND | GND | GND | GND | GND | GND | | | | | VCC3IO_1_NTF | JTAGTMS_3 | PDATA_1_7 | PDATA_1_6 | | |
| N | GPIO_10 | GPIO_11 | GPIO_12 | VCC3IO | | | | GND | GND | GND | GND | GND | GND | | | | | VCC | JTAGTMS_2 | PDATA_1_4 | PDATA_1_5 | | |
| P | GPIO_13 | GPIO_14 | GPIO_15 | VCC3IO | | | | GND | GND | GND | GND | GND | GND | | | | | VCC | HOST_IIC_SDA | DATEN | PDATA_1_3 | | |
| R | GPIO_16 | GPIO_17 | GPIO_18 | HOST_IF_SEL | | | | | | | | | | | | | | VCC3IO_1_NTF | HOST_IIC_SCL | PDATA_1_1 | PCLK | | |
| T | GPIO_19 | GPIO_20 | GPIO_21 | VCC | | | | | | | | | | | | | | VCC3IO_1_NTF | HOST_IRQ | PDATA_9 | PDATA_1_2 | | |
| U | GPIO_22 | GPIO_23 | GPIO_24 | VCC | | | | | | | | | | | | | | VCC | HOST_SPI_DOUT | PDATA_7 | PDATA_1_0 | | |
| V | HOST_SPI_MODE | FLSH_SPI_DIO_0 | GPIO_25 | VCC3IO_FLSH | | | | | | | | | | | | | | VCC | HOST_SPI_DIN | PDATA_5 | PDATA_8 | | |
| W | FLSH_SPI_CLK | FLSH_SPI_DIO_1 | FLSH_SPI_DIO_3 | VCC3IO | VCC3IO | VCC | EFUSE_VDDQ | VCC | VCC33A_LVDS | VCC | VCC11A_LVDS | VCC11A_LVDS | VCC33A_LVDS | GND33A_LVDS | VCC33A_LVDS | VCC | VCC11A_LVDS | VCC11A_LVDS | VCC33A_LVDS | HOST_SPI_CSZ | PDATA_3 | PDATA_6 | |
| Y | FLSH_SPI_CSZ | FLSH_SPI_DIO_2 | GND | TSTPT_0 | TSTPT_2 | TSTPT_4 | TSTPT_6 | EFUSE_PROG_R33 | VCC33A_LVDS | GND11A_LVDS | GND11A_LVDS | GND11A_LVDS | VCC33A_LVDS | GND33A_LVDS | VCC33A_LVDS | GND11A_LVDS | GND11A_LVDS | GND11A_LVDS | VCC33A_LVDS | HOST_SPI_CLK | PDATA_2 | PDATA_4 | |
| AA | GND | GND | RTTPUB_ENZ | TSTPT_1 | TSTPT_3 | TSTPT_5 | TSTPT_7 | GND33A_LVDS | L1_DATA0_N | L1_DATA1_N | L1_CLK_N | L1_DATA2_N | L1_DATA3_N | GND33A_LVDS | L2_DATA0_N | L2_DATA1_N | L2_CLK_N | L2_DATA2_N | L2_DATA3_N | GND33A_LVDS | PDATA_0 | PDATA_1 | |
| AB | GND | GND | CRCZ_CH_KSM_SEL | MSTR_SCL | MSTR_SDA | ETM_TRA_CECLK | ETM_TRA_CECLK | GND33A_LVDS | L1_DATA0_P | L1_DATA1_P | L1_CLK_P | L1_DATA2_P | L1_DATA3_P | GND33A_LVDS | L2_DATA0_P | L2_DATA1_P | L2_CLK_P | L2_DATA2_P | L2_DATA3_P | GND33A_LVDS | GND33A_LVDS | GND | |

Note that there is one VCC power ball located in the thermal ball array.

Figure 4-1. DLPC230 ZDQ Package 324-Pin BGA Top View

| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | |
|----|-------------------|-------------------|-------------------|-------------------|----------------|----------------|-----------------|-------------|-------------|----------|---------------|---------------|-------------|----------------|----------------|----------------|---------------|-----------------|----|
| 18 | GND18A_LVDS | VCC18A_LVDS | DMD_HS0_WDAT_A1_N | DMD_HS0_WDAT_A0_N | GPIO_28 | JTAGTD02 | JTAGTM_S3 | HSYNC | VSYNC | PDATA_17 | PDATA_14 | PCLK | PDATA_9 | PDATA_8 | PDATA_6 | PDATA_4 | PDATA_2 | GND | 18 |
| 17 | DMD_HS0_WDAT_A2_N | DMD_HS0_WDAT_A2_P | DMD_HS0_WDAT_A1_P | DMD_HS0_WDAT_A0_P | GPIO_29 | JTAGTD03 | JTAGTDI | JTAGTCK | PDATA_21 | PDATA_18 | PDATA_15 | DATEN | PDATA_12 | PDATA_7 | PDATA_5 | PDATA_3 | PDATA_1 | PDATA_0 | 17 |
| 16 | DMD_HS0_WDAT_A3_N | DMD_HS0_WDAT_A3_P | GND18A_LVDS | VCC18A_LVDS | GPIO_30 | GPIO_26 | JTAGTRS_TZ | JTAGTM_S1 | PDATA_22 | PDATA_19 | PDATA_16 | PDATA_13 | PDATA_11 | PDATA_10 | HOST_SP_I_DIN | HOST_SP_I_CSZ | HOST_SP_I_CLK | VCC33A_LVDS | 16 |
| 15 | DMD_HS0_CLK_N | DMD_HS0_CLK_P | VCC18A_LVDS | RPI_0 | GPIO_31 | GPIO_27 | JTAGTD01 | JTAGTM_S2 | PDATA_23 | PDATA_20 | HOST_II_C_SDA | HOST_II_C_SCL | HOST_IR_Q | HOST_SP_I_DOUT | VCC33A_LVDS | GND33A_LVDS | GND33A_LVDS | GND33A_LVDS | 15 |
| 14 | DMD_HS0_WDAT_A4_N | DMD_HS0_WDAT_A4_P | GND18A_LVDS | VCC18A_LVDS | GND18A_LVDS | VCC3IO_2 | VCC3IO_2 | VCC3IO_INTF | VCC3IO_INTF | GND | VCC3IO_INTF | VCC3IO_INTF | GND | VCC11A_LVDS | GND33A_LVDS | VCC33A_LVDS | L2_DATA_3_N | L2_DATA_3_P | 14 |
| 13 | DMD_HS0_WDAT_A5_N | DMD_HS0_WDAT_A5_P | OSC_BYPASS | PLL_REF_CLK_O | VCC18A_LVDS | VCC11A_DDI_0 | VCC11A_DDI_0 | VCCK | GND | VCCK | GND | VCCK | GND | VCC11A_LVDS | VCC33A_LVDS | GND33A_LVDS | L2_DATA_2_N | L2_DATA_2_P | 13 |
| 12 | DMD_HS0_WDAT_A6_N | DMD_HS0_WDAT_A6_P | GNDIOL_A_COSC | PLL_REF_CLK_I | GND18A_LVDS | VCC18A_LVDS | GND | GND | GND | GND | GND | GND | GND | VCC11A_LVDS | GND33A_LVDS | VCC33A_LVDS | L2_CLK_N | L2_CLK_P | 12 |
| 11 | DMD_HS0_WDAT_A7_N | DMD_HS0_WDAT_A7_P | GND11A_D_PLLM | VCC11A_D_PLLM | VCC3IO_COSC | VCCK | GND | GND | GND | GND | GND | GND | VCCK | VCC11A_LVDS | VCC33A_LVDS | GND33A_LVDS | L2_DATA_1_N | L2_DATA_1_P | 11 |
| 10 | DMD_LS0_CLK_N | DMD_LS0_CLK_P | VCC11A_D_PLLD | GND11A_D_PLLD | GND18A_LVDS | VCC18A_LVDS | GND | GND | GND | GND | GND | GND | VCC11A_LVDS | EFUSE_P_OR33 | ETM_TR_ACECLK | VCC33A_LVDS | L2_DATA_0_N | L2_DATA_0_P | 10 |
| 9 | DMD_LS0_WDAT_A_N | DMD_LS0_WDAT_A_P | DMD_LS0_CLK | DMD_DE_N_ARSTZ | VCC18IO | VCCK | GND | GND | GND | GND | GND | GND | VCCK | EFUSE_V_DDQ | ETM_TR_ACECTL | GND33A_LVDS | GND33A_LVDS | GND33A_LVDS | 9 |
| 8 | DMD_HS1_WDAT_A7_N | DMD_HS1_WDAT_A7_P | DMD_LS1_RDAT_A | DMD_LS0_WDAT_A | GND18A_LVDS | VCC18A_LVDS | GND | GND | GND | GND | GND | GND | VCCK | VCC3IO | TSTPT_5 | VCC33A_LVDS | L1_DATA_3_N | L1_DATA_3_P | 8 |
| 7 | DMD_HS1_WDAT_A6_N | DMD_HS1_WDAT_A6_P | DMD_LS0_RDAT_A | RPI_LS | VCC11A_DDI_1 | VCC18A_LVDS | GND | GND | GND | GND | GND | GND | VCC3IO | TSTPT_7 | TSTPT_3 | MSTR_S_DA | L1_DATA_2_N | L1_DATA_2_P | 7 |
| 6 | DMD_HS1_WDAT_A5_N | DMD_HS1_WDAT_A5_P | VCC18A_LVDS | GND18A_LVDS | VCC11A_DDI_1 | GND18A_LVDS | VCCK | GND | VCCK | VCC3IO | VCCK | VCC3IO | VCCK | TSTPT_6 | MSTR_S_CL | GND33A_LVDS | L1_CLK_N | L1_CLK_P | 6 |
| 5 | DMD_HS1_WDAT_A4_N | DMD_HS1_WDAT_A4_P | GND18A_LVDS | VCC18A_LVDS | PMIC_SP_I_DOUT | PMIC_SP_I_CLK | VCC3IO_MVGP | VCC3IO_MVGP | HWTEST_EN | GPIO_12 | VCC3IO | GPIO_24 | VCC3IO_FLSH | VCC3IO_FLSH | TSTPT_2 | GND33A_LVDS | L1_DATA_1_N | L1_DATA_1_P | 5 |
| 4 | DMD_HS1_CLK_N | DMD_HS1_CLK_P | VCC18A_LVDS | RPI_1 | PMIC_PA_RKZ | PMIC_LE_DSEL_0 | PMIC_SP_I_CSZ_0 | GPIO_00 | GPIO_07 | GPIO_11 | GPIO_16 | GPIO_20 | GPIO_23 | TSTPT_4 | TSTPT_1 | VCC33A_LVDS | L1_DATA_0_N | L1_DATA_0_P | 4 |
| 3 | DMD_HS1_WDAT_A3_N | DMD_HS1_WDAT_A3_P | GND18A_LVDS | VCC18A_LVDS | PMIC_SP_I_DIN | RESETZ | PMIC_A_D3_MISO | GPIO_04 | GPIO_06 | GPIO_10 | GPIO_15 | GPIO_19 | GPIO_22 | GPIO_25 | TSTPT_0 | VCC33A_LVDS | GND33A_LVDS | GND33A_LVDS | 3 |
| 2 | DMD_HS1_WDAT_A2_N | DMD_HS1_WDAT_A2_P | DMD_HS1_WDAT_A1_P | DMD_HS1_WDAT_A0_P | PMIC_IN_TZ | PMIC_LE_DSEL_2 | PMIC_A_D3_MISO | GPIO_05 | GPIO_03 | GPIO_09 | GPIO_14 | GPIO_18 | GPIO_21 | HOST_SP_I_MODE | FLSH_SPI_DIO_1 | FLSH_SPI_DIO_3 | RTTPUB_ENZ | CRCZ_CH_KSM_SEL | 2 |
| 1 | GND18A_LVDS | VCC18A_LVDS | DMD_HS1_WDAT_A1_N | DMD_HS1_WDAT_A0_N | PMIC_LE_DSEL_1 | PMIC_LE_DSEL_3 | PMIC_A_D3_CLK | GPIO_02 | GPIO_01 | GPIO_08 | GPIO_13 | GPIO_17 | HOST_IF_SEL | FLSH_SPI_DIO_0 | FLSH_SPI_DIO_2 | FLSH_SPI_CSZ | FLSH_SPI_CLK | GND | 1 |
| | A | B | C | D | E | F | G | H | J | K | L | M | N | P | R | T | U | V | |

**Figure 4-2. DLPC231 ZEK Package
324-Pin BGA
Top View**

Table 4-1. Pin Functions—Board Level Test, Debug, and Initialization

| NAME | PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------------|--------|--------|--------------------|---|
| | ZDQ324 | ZEK324 | | |
| RESETZ | F3 | F3 | I ₇ | Active low power-on reset for the DLPC23xS-Q1. A low-to-high transition starts self-configuration and initialization of the ASIC. ('0' = Reset, '1' = Normal Operation) All ASIC power and input clocks must be stable before this reset is deasserted high. The signals listed below must be forced low by external pulldown, and will then be driven low as the power supplies stabilize with RESETZ asserted. <i>PMIC_LEDSEL_0, PMIC_LEDSEL_1, PMIC_LEDSEL_2, PMIC_LEDSEL_3, DMD_DEN_ARSTZ, PMIC_AD3_CLK, and PMIC_AD3_MOSI</i> All other bidirectional and output signals will be tristated while reset is asserted. External pullups or pulldowns must be added where necessary to protect external devices that can typically be driven by the ASIC to prevent device malfunction. This pin includes hysteresis. Specific timing requirements for this signal are shown in Section 5.12 . |
| PMIC_PARKZ | E3 | E4 | I ₇ | DMD Park Control ('0' = Park, '1' = Un-Park) The TI TPS99000S-Q1 device is used to control this signal. As part of this function, it monitors power to the DLPC23xS-Q1 watching for an imminent power loss condition, upon which it will drive the PMIC_PARKZ signal accordingly. The specific timing requirements for this signal are shown in Section 5.12 . |
| HOST_IF_SEL | R4 | N1 | B _{13,14} | Selects which input interface port will be used for Host Command and Control. The port that is not selected as the Host Command and Control port will be available as a Diagnostic Processor monitoring port. ('0' = Host SPI, '1' = Host I ² C) This pin includes a weak internal pulldown. If a pullup is used to obtain a '1' value, the pullup value must be ≤ 8kΩ. Tristated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5μs after RESETZ is deasserted. It can be driven as an output for TI debug use after sampling. |
| HOST_SPI_MODE | V1 | P2 | B _{13,14} | Selects the SPI mode (clock phase and polarity) that will be used with the HOST SPI interface. This value is applicable regardless of whether the Host SPI interface is used for Host Command and Control, or for the Diagnostic Processor monitoring port. ('0' = SPI Mode 0 or 3, '1' = SPI Mode 1 or 2) This pin includes a weak internal pulldown. If a pullup is used to obtain a '1' value, the pullup value must be ≤ 8kΩ. Tristated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5μs after RESETZ is deasserted. It can be driven as an output for TI debug use after sampling. |
| RTTPUB_ENZ | AA3 | U2 | B _{13,14} | TI internal use. Must be left unconnected. Includes a weak pulldown |
| CRCZ_CHKSUM_SEL | AB3 | V2 | B _{13,14} | Selects whether the Host will use 8-bit CRC or checksum on the Host Command and Control interface. This value is only applicable for the Host Command and Control interface. The value for the Diagnostic Processor monitoring port will be specified in Flash. ('0' = 8-bit CRC, '1' = 8-bit checksum) This pin includes a weak internal pulldown. If a pullup is used to obtain a '1' value, the pullup value must be ≤ 8kΩ. Tristated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5μs after RESETZ is deasserted. It can be driven as an output for TI debug use after sampling. |
| ETM_TRACECLK | AB6 | R10 | O ₁₃ | TI internal use. Must be left unconnected (clock for Trace Debug) |
| ETM_TRACECTL | AB7 | R9 | O ₁₃ | TI internal use. Must be left unconnected (control for Trace Debug) |

Table 4-1. Pin Functions—Board Level Test, Debug, and Initialization (continued)

| NAME | PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------|--------|--------|--------------------|---|
| | ZDQ324 | ZEK324 | | |
| TSTPT_0 | Y4 | R3 | B _{13,14} | Test pin 0 / STAY-IN-BOOT: Selects whether the system must stay in the Boot Application, or proceed with the normal load of the Main Application. (‘0’ = Load Main Application, ‘1’ = Stay in Boot Application) This pin includes a weak internal pulldown. If a pullup is being used to obtain a ‘1’ value, the pullup value must be ≤ 8kΩ. Tristated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5μs after RESETZ is deasserted. It can be driven as an output for debug use after sampling as described in Section 7.3.11 . |
| TSTPT_1 | AA4 | R4 | B _{13,14} | Test pin 1: This pin must be externally pulled down, left open or unconnected. Includes a weak pulldown. It can be driven as an output for debug use as described in Section 7.3.11 . |
| TSTPT_2 | Y5 | R5 | B _{13,14} | Test pin 2: This pin must be externally pulled down, left open or unconnected. Includes a weak pulldown. It can be driven as an output for debug use as described in Section 7.3.11 . |
| TSTPT_3 | AA5 | R7 | B _{13,14} | Test pin 3: This pin must be externally pulled down, left open or unconnected. Includes a weak pulldown. It can be driven as an output for debug use as described in Section 7.3.11 . |
| TSTPT_4 | Y6 | P4 | B _{13,14} | Test pin 4: This pin must be externally pulled down, left open or unconnected. Includes a weak pulldown. It can be driven as an output for debug use as described in Section 7.3.11 . |
| TSTPT_5 | AA6 | R8 | B _{13,14} | Test pin 5 / Spread Spectrum Disable: Selects whether spread spectrum flash settings are used or whether spread spectrum clocking will be disabled. (‘0’ = Spread Spectrum Disabled, ‘1’ = Use flash Spread Spectrum settings) This pin includes a weak internal pulldown. If a pullup is being used to obtain a ‘1’ value, the pullup value must be ≤ 8kΩ. This signal is tristated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5μs after RESETZ is deasserted. It can be driven as an output for debug use after sampling as described in Section 7.3.11 . |
| TSTPT_6 | Y7 | P6 | B _{13,14} | Test pin 6: An external pullup resistor must be used (≤ 8kΩ because pin includes a weak pulldown). This signal is tristated while RESETZ is asserted low, and is sampled as a host directive approximately 1.5μs after RESETZ is deasserted. It can be driven as an output for debug use after sampling as described in Section 7.3.11 . |
| TSTPT_7 | AA7 | P7 | B _{13,14} | Test pin 7: This pin must be externally pulled down, left open or unconnected. Includes a weak pulldown. It can be driven as an output for debug use as described in Section 7.3.11 . |
| HWTEST_EN | H3 | J5 | I ₁₄ | Manufacturing test enable signal. This signal must be connected directly to ground on the PCB. Includes a weak internal pulldown and hysteresis |
| JTAGTCK | G22 | H17 | I ₁₁ | JTAG Serial Data Clock Includes a weak internal pullup |

Table 4-1. Pin Functions—Board Level Test, Debug, and Initialization (continued)

| NAME | PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|-----------|--------|--------|--------------------|---|
| | ZDQ324 | ZEK324 | | |
| JTAGTMS1 | G21 | H16 | I ₁₁ | JTAG Test Mode Select Includes a weak internal pullup |
| JTAGTRSTZ | L20 | G16 | I ₁₁ | JTAG Reset Includes a weak internal pullup and Hysteresis. For normal operation, this pin must be pulled to ground through an external 8kΩ or less resistor. Failure to pull this pin low during normal operation will cause start-up and initialization problems. For JTAG Boundary Scan, this pin must be pulled-up or left disconnected. |
| JTAGTDI | K20 | G17 | I ₁₁ | JTAG Serial Data In Includes a weak internal pullup |
| JTAGTDO1 | J20 | G15 | B _{10,11} | JTAG Serial Data Out Includes a weak internal pullup |
| JTAGTDO2 | H20 | F18 | B _{10,11} | This pin must be left open or unconnected. Includes a weak internal pullup |
| JTAGTDO3 | G20 | F17 | B _{10,11} | This pin must be left open or unconnected. Includes a weak internal pullup |
| JTAGTMS2 | N20 | H15 | I ₁₁ | This pin must be left open or unconnected. Includes a weak internal pullup. See Section 7.3.11 for important debug access considerations. |
| JTAGTMS3 | M20 | G18 | I ₁₁ | This pin must be left open or unconnected. Includes a weak internal pullup. See Section 7.3.11 for important debug access considerations. |

(1) See [Table 4-10](#) for more information on I/O definitions.

Table 4-2. Pin Functions—Parallel Port Input Data and Control

| NAME | PIN ⁽¹⁾ | | I/O ⁽²⁾ | DESCRIPTION PARALLEL RGB MODE |
|----------|--------------------|--------|--------------------|----------------------------------|
| | ZDQ324 | ZEK324 | | |
| PCLK | R22 | M18 | I ₁₁ | Pixel clock |
| VSYNC | H21 | J18 | I ₁₁ | Vsync ⁽³⁾ |
| HSYNC | H22 | H18 | I ₁₁ | Hsync ⁽³⁾ |
| DATEN | P21 | M17 | I ₁₁ | Data Valid |
| | | | | (TYPICAL RGB 888) |
| PDATA_0 | AA21 | V17 | I ₁₁ | Blue (bit weight 1) |
| PDATA_1 | AA22 | U17 | | Blue (bit weight 2) |
| PDATA_2 | Y21 | U18 | | Blue (bit weight 4) |
| PDATA_3 | W21 | T17 | | Blue (bit weight 8) |
| PDATA_4 | Y22 | T18 | | Blue (bit weight 16) |
| PDATA_5 | V21 | R17 | | Blue (bit weight 32) |
| PDATA_6 | W22 | R18 | | Blue (bit weight 64) |
| PDATA_7 | U21 | P17 | | Blue (bit weight 128) |
| | | | | (TYPICAL RGB 888) |
| PDATA_8 | V22 | P18 | I ₁₁ | Green (bit weight 1) |
| PDATA_9 | T21 | N18 | | Green (bit weight 2) |
| PDATA_10 | U22 | P16 | | Green (bit weight 4) |
| PDATA_11 | R21 | N16 | | Green (bit weight 8) |
| PDATA_12 | T22 | N17 | | Green (bit weight 16) |
| PDATA_13 | P22 | M16 | | Green (bit weight 32) |
| PDATA_14 | N21 | L18 | | Green (bit weight 64) |
| PDATA_15 | N22 | L17 | | Green (bit weight 128) |
| | | | | (TYPICAL RGB 888) |

Table 4-2. Pin Functions—Parallel Port Input Data and Control (continued)

| PIN ⁽¹⁾ | | | I/O ⁽²⁾ | DESCRIPTION PARALLEL RGB MODE |
|--------------------|--------|--------|--------------------|----------------------------------|
| NAME | ZDQ324 | ZEK324 | | |
| PDATA_16 | M22 | L16 | I ₁₁ | Red (bit weight 1) |
| PDATA_17 | M21 | K18 | | Red (bit weight 2) |
| PDATA_18 | L22 | K17 | | Red (bit weight 4) |
| PDATA_19 | L21 | K16 | | Red (bit weight 8) |
| PDATA_20 | K22 | K15 | | Red (bit weight 16) |
| PDATA_21 | K21 | J17 | | Red (bit weight 32) |
| PDATA_22 | J22 | J16 | | Red (bit weight 64) |
| PDATA_23 | J21 | J15 | | Red (bit weight 128) |

- (1) Unused inputs must be grounded or pulled down to ground through an external resistor ($\leq 10k\Omega$).
(2) See [Table 4-10](#) for more information on I/O definitions.
(3) VSYNC and HSYNC polarity are software programmable.

Table 4-3. Pin Functions—OpenLDI Ports Input Data and Control

| PIN ^{(1) (2)} | | | I/O ⁽³⁾ | DESCRIPTION |
|--|--|--|--------------------|--|
| NAME | ZDQ324 | ZEK325 | | |
| L1_CLK_P L1_CLK_N | AB11 AA11 | V6 U6 | I ₁₈ | OpenLDI (FPD Link I) Port 1 Clock Lane |
| L1_DATA0_P L1_DATA0_N L1_DATA1_P L1_DATA1_N L1_DATA2_P L1_DATA2_N L1_DATA3_P L1_DATA3_N | AB9 AA9 AB10 AA10 AB12 AA12 AB13 AA13 | V4 U4 V5 U5 V7 U7 V8 U8 | I ₁₈ | OpenLDI (FPD Link I) Port 1 Data Lanes: Intraport data lane swapping can be done on a product configuration basis to support board considerations. |
| L2_CLK_P L2_CLK_N | AB17 AA17 | V12 U12 | I ₁₈ | OpenLDI (FPD Link I) Port 2 Clock Lane |
| L2_DATA0_P L2_DATA0_N L2_DATA1_P L2_DATA1_N L2_DATA2_P L2_DATA2_N L2_DATA3_P L2_DATA3_N | AB15 AA15 AB16 AA16 AB18 AA18 AB19 AA19 | V10 U10 V11 U11 V13 U13 V14 U14 | I ₁₈ | OpenLDI (FPD Link I) Port 2 Data Lanes: Intraport data lane swapping can be done on a product configuration basis to support board considerations. |

- (1) The system only supports the operational use of one port. As two ports are available, the host can select which port they wish to be active (to optimize board routing as an example).
(2) The inputs for any unused ports must be left unconnected, and will be powered down by the system.
(3) See [Table 4-10](#) for more information on I/O definitions.

Table 4-4. Pin Functions—DMD Reset and Bias Control Interfaces

| PIN ^{(1) (2)} | | | I/O ⁽³⁾ | DESCRIPTION |
|------------------------|--------|--------|--------------------|---|
| NAME | ZDQ324 | ZEK324 | | |
| DMD_DEN_ARSTZ | D11 | D9 | O ₁ | DMD driver enable signal ('1' = Enabled, '0' = Reset) This signal will be driven low after the DMD is parked and before power is removed from the DMD. If the 1.8V power to the DLPC23xS-Q1 is independent of the 1.8V power to the DMD, then an external pulldown resistor ($\leq 2.2k\Omega$) must be used to hold the signal low in the event DLPC23xS-Q1 power is inactive while DMD power is applied. |
| DMD_LS0_CLK | C11 | C9 | O ₂ | TI internal use. Must be left unconnected |
| DMD_LS0_WDATA | C10 | D8 | O ₂ | TI internal use. Must be left unconnected |
| DMD_LS0_RDATA | C9 | C7 | I ₃ | DMD, low-speed single-ended serial read data |
| DMD_LS1_RDATA | C8 | C8 | I ₃ | DMD, low-speed single-ended serial read data (Training data response for second port of DMD) |

Table 4-4. Pin Functions—DMD Reset and Bias Control Interfaces (continued)

| PIN ^{(1) (2)} | | | I/O ⁽³⁾ | DESCRIPTION |
|------------------------------------|------------|------------|--------------------|---|
| NAME | ZDQ324 | ZEK324 | | |
| DMD_LS0_CLK_P DMD_LS0_CLK_N | B12 A12 | B10 A10 | O ₄ | DMD low-speed differential interface clock |
| DMD_LS0_WDATA_P DMD_LS0_WDATA_N | B11 A11 | B9 A9 | O ₄ | DMD low-speed differential interface write data |

- (1) The low-speed write control interface to the DMD is differential.
(2) All control interface reads will make use of the single-ended low-speed signals. The read data will be clocked by the write clock.
(3) See [Table 4-10](#) for more information on I/O definitions.

Table 4-5. Pin Functions—DMD SubLVDS Interfaces

| PIN | | | I/O ⁽¹⁾ | DESCRIPTION |
|--|--|--|--------------------|--|
| NAME | ZDQ324 | ZEK324 | | |
| DMD_HS0_CLK_P DMD_HS0_CLK_N | B17 A17 | B15 A15 | O ₄ | DMD high-speed interface, Port 0 Clock Lane. |
| DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N | B21 A21 B20 A20 B19 A19 B18 A18 B16 A16 B15 A15 B14 A14 B13 A13 B14 A14 B13 A13 | D17 D18 C17 C18 B17 A17 B16 A16 B14 A14 B13 A13 B12 A12 B11 A11 | O ₄ | DMD high-speed interface, Port 0 Data Lanes: The true numbering and application of the DMD_HS_DATA pins are software configuration dependent as discussed in Section 7.3.3 . |
| DMD_HS1_CLK_P DMD_HS1_CLK_N | B6 A6 | B4 A4 | O ₄ | DMD high-speed interface, Port 1 Clock Lane |
| DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N | B2 A2 B3 A3 B4 A4 B5 A5 B7 A7 B8 A8 B9 A9 B10 A10 | D2 D1 C2 C1 B2 A2 B3 A3 B5 A5 B6 A6 B7 A7 B8 A8 | O ₄ | DMD high-speed interface, Port 1 Data Lanes: The true numbering and application of the DMD_HS_DATA pins are software configuration dependent as discussed in Section 7.3.3 . |

- (1) See [Table 4-10](#) for more information on I/O definitions.

Table 4-6. Pin Functions—Peripheral Interfaces

| NAME | PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|--------------------------|--------|--------|--------------------|---|
| | ZDQ324 | ZEK324 | | |
| HOST_IRQ ⁽²⁾ | T20 | N15 | O ₁₀ | Host interrupt (output active HIGH) This signal is used to indicate that the DLPC23xS-Q1 has detected a serious error for which the ASIC has initiated an Emergency Shutdown. This is discussed further in Section 6.1 . The DLPC23xS-Q1 tristates this output during reset. An external pulldown ($\leq 10\text{k}\Omega$) is required to drive this signal to its inactive state. |
| HOST_IIC_SCL | R20 | M15 | B ₁₂ | I ² C Port, Host Command and Control to ASIC, SCL (bidirectional, open-drain): An external pullup is required. |
| HOST_IIC_SDA | P20 | L15 | B ₁₂ | I ² C Port, Host Command and Control to ASIC, SDA (bidirectional, open-drain): An external pullup is required. |
| HOST_SPI_CLK | Y20 | U16 | I ₁₁ | SPI Port, Host Command and Control to ASIC, clock |
| HOST_SPI_CSZ | W20 | T16 | I ₁₁ | SPI Port, Host Command and Control to ASIC, chip select (active low input) An external pullup resistor ($\leq 2.2\text{k}\Omega$) is required to avoid a floating chip select input to the ASIC. |
| HOST_SPI_DIN | V20 | R16 | I ₁₁ | SPI Port, Host Command and Control to ASIC, receive data in |
| HOST_SPI_DOUT | U20 | P15 | O ₁₀ | SPI Port, Host Command and Control to ASIC, transmit data out |
| FLSH_SPI_CSZ | Y1 | T1 | O ₈ | SPI Port, Control Interface to Flash device, chip select (active low output) An external pullup resistor ($\leq 10\text{k}\Omega$) is required to avoid a floating chip select input to the Flash. |
| FLSH_SPI_CLK | W1 | U1 | O ₈ | SPI Port, Control Interface to Flash device, clock |
| FLSH_SPI_DIO_0 | V2 | P1 | B _{8,9} | SPI Port, Control Interface to Flash device, transmit and receive data An external pullup resistor ($\leq 10\text{k}\Omega$) is required. |
| FLSH_SPI_DIO_1 | W2 | R2 | B _{8,9} | SPI Port, Control Interface to Flash device, transmit and receive data An external pullup resistor ($\leq 10\text{k}\Omega$) is required. |
| FLSH_SPI_DIO_2 | Y2 | R1 | B _{8,9} | SPI Port, Control Interface to Flash device, transmit and receive data An external pullup resistor ($\leq 3.3\text{k}\Omega$) is required. |
| FLSH_SPI_DIO_3 | W3 | T2 | B _{8,9} | SPI Port, Control Interface to Flash device, transmit and receive data An external pullup resistor ($\leq 3.3\text{k}\Omega$) is required. |
| PMIC_INTZ ⁽²⁾ | G3 | E2 | I ₇ | TPS99000S-Q1 interrupt (input with hysteresis) The ASIC provides a weak internal pullup. |
| PMIC_SPI_CLK | E1 | F5 | O ₆ | SPI Port, General Control Interface to TPS99000S-Q1, clock |
| PMIC_SPI_CSZ0 | E2 | G4 | O ₆ | SPI Port, General Control Interface to TPS99000S-Q1, chip select 0 (active low output) An external pullup resistor ($\leq 10\text{k}\Omega$) must be used to avoid floating chip select inputs to the external SPI device during ASIC reset assertion. |
| PMIC_SPI_DIN | F1 | E3 | I ₇ | SPI Port, General Control Interface to TPS99000S-Q1, receive data in |
| PMIC_SPI_DOUT | D1 | E5 | O ₆ | SPI Port, General Control Interface to TPS99000S-Q1, transmit data out |
| PMIC_AD3_CLK | H2 | G1 | O ₂₀ | Sequencer Clock / TPS99000S-Q1 primary system clock An external pulldown resistor ($\leq 10\text{k}\Omega$) must be used to avoid uncontrolled behavior during ASIC reset assertion. |
| PMIC_AD3_MISO | J2 | G2 | I ₁₄ | Measurement control interface to TPS99000S-Q1, receive data in |
| PMIC_AD3_MOSI | J1 | G3 | O ₂₀ | Measurement control interface to TPS99000S-Q1, transmit data out An external pulldown resistor ($\leq 10\text{k}\Omega$) must be used to avoid uncontrolled behavior during ASIC reset assertion. |
| PMIC_LEDSEL_0 | F2 | F4 | O ₆ | LED Control Interface to TPS99000S-Q1 An external pulldown resistor ($\leq 10\text{k}\Omega$) must be used to avoid uncontrolled illumination during ASIC reset assertion. |
| PMIC_LEDSEL_1 | G1 | E1 | O ₆ | LED Control Interface to TPS99000S-Q1 An external pulldown resistor ($\leq 10\text{k}\Omega$) must be used to avoid uncontrolled illumination during ASIC reset assertion. |

Table 4-6. Pin Functions—Peripheral Interfaces (continued)

| PIN | | | I/O ⁽¹⁾ | DESCRIPTION |
|---------------|--------|--------|--------------------|--|
| NAME | ZDQ324 | ZEK324 | | |
| PMIC_LEDSEL_2 | G2 | F2 | O ₆ | LED Control Interface to TPS99000S-Q1 An external pulldown resistor ($\leq 10k\Omega$) must be used to avoid uncontrolled illumination during ASIC reset assertion. |
| PMIC_LEDSEL_3 | H1 | F1 | O ₆ | LED Control Interface to TPS99000S-Q1 An external pulldown resistor ($\leq 10k\Omega$) must be used to avoid uncontrolled illumination during ASIC reset assertion. |
| MSTR_SDA | AB5 | T7 | B ₁₅ | I ² C Port, SDA. (bidirectional, open-drain) An external pullup is required. Typical use of the Master I ² C port is communication with temperature sensing devices and an optional EEPROM. The Master I ² C I/Os are powered by VCC3IO (3.3V only). |
| MSTR_SCL | AB4 | R6 | B ₁₅ | I ² C Port, SCL. (bidirectional, open-drain) An external pullup is required. Typical use of the Master I ² C port is communication with temperature sensing devices and an optional EEPROM. The Master I ² C I/Os are powered by VCC3IO (3.3V only). |

- (1) See [Table 4-10](#) for more information on I/O definitions.
(2) For more information about usage, see [Section 6.1](#).

Table 4-7. Pin Functions—GPIO Peripheral Interface

| PIN ^{(1) (3)} | | | I/O ⁽²⁾ | DESCRIPTION |
|------------------------|--------|--------|--------------------|------------------------|
| NAME | ZDQ324 | ZEK324 | | |
| GPIO_31 | D22 | E15 | B _{20,14} | General purpose I/O 31 |
| GPIO_30 | E21 | E16 | B _{20,14} | General purpose I/O 30 |
| GPIO_29 | E22 | E17 | B _{20,14} | General purpose I/O 29 |
| GPIO_28 | F20 | E18 | B _{20,14} | General purpose I/O 28 |
| GPIO_27 | F21 | F15 | B _{20,14} | General purpose I/O 27 |
| GPIO_26 | F22 | F16 | B _{20,14} | General purpose I/O 26 |
| GPIO_25 | V3 | P3 | B _{20,14} | General purpose I/O 25 |
| GPIO_24 | U3 | M5 | B _{20,14} | General purpose I/O 24 |
| GPIO_23 | U2 | N4 | B _{20,14} | General purpose I/O 23 |
| GPIO_22 | U1 | N3 | B _{20,14} | General purpose I/O 22 |
| GPIO_21 | T3 | N2 | B _{20,14} | General purpose I/O 21 |
| GPIO_20 | T2 | M4 | B _{20,14} | General purpose I/O 20 |
| GPIO_19 | T1 | M3 | B _{20,14} | General purpose I/O 19 |
| GPIO_18 | R3 | M2 | B _{20,14} | General purpose I/O 18 |
| GPIO_17 | R2 | M1 | B _{20,14} | General purpose I/O 17 |
| GPIO_16 | R1 | L4 | B _{20,14} | General purpose I/O 16 |
| GPIO_15 | P3 | L3 | B _{20,14} | General purpose I/O 15 |
| GPIO_14 | P2 | L2 | B _{20,14} | General purpose I/O 14 |
| GPIO_13 | P1 | L1 | B _{20,14} | General purpose I/O 13 |
| GPIO_12 | N3 | K5 | B _{20,14} | General purpose I/O 12 |
| GPIO_11 | N2 | K4 | B _{20,14} | General purpose I/O 11 |
| GPIO_10 | N1 | K3 | B _{20,14} | General purpose I/O 10 |
| GPIO_09 | M3 | K2 | B _{20,14} | General purpose I/O 09 |

Table 4-7. Pin Functions—GPIO Peripheral Interface (continued)

| PIN ^{(1) (3)} | | | I/O ⁽²⁾ | DESCRIPTION |
|------------------------|--------|--------|--------------------|------------------------|
| NAME | ZDQ324 | ZEK324 | | |
| GPIO_08 | M2 | K1 | B _{20,14} | General purpose I/O 08 |
| GPIO_07 | M1 | J4 | B _{20,14} | General purpose I/O 07 |
| GPIO_06 | L3 | J3 | B _{20,14} | General purpose I/O 06 |
| GPIO_05 | L2 | H2 | B _{20,14} | General purpose I/O 05 |
| GPIO_04 | L1 | H3 | B _{20,14} | General purpose I/O 04 |
| GPIO_03 | K3 | J2 | B _{20,14} | General purpose I/O 03 |
| GPIO_02 | K2 | H1 | B _{20,14} | General purpose I/O 02 |
| GPIO_01 | K1 | J1 | B _{20,14} | General purpose I/O 01 |
| GPIO_00 | J3 | H4 | B _{20,14} | General purpose I/O 00 |

- (1) Some GPIO signals are reserved for specific purposes. These signals vary per product configuration. These product allocations are discussed further in [Section 7.3.7](#). All GPIO that are available for Host use must be configured as an input, a standard output, or an open-drain output. This is set in the flash configuration or by command using the Host command interface. The reset default for all GPIO is as an input signal. An external pullup ($\leq 10k\Omega$) is required for each signal configured as open-drain.
- (2) See [Table 4-10](#) for more information on I/O definitions.
- (3) All GPIO include hysteresis.

Table 4-8. Pin Functions—Clock and PLL Support

| PIN | | | I/O ⁽¹⁾ | DESCRIPTION |
|--------------|--------|--------|--------------------|--|
| NAME | ZDQ324 | ZEK324 | | |
| PLL_REFCLK_I | D15 | D12 | I ₁₇ | Reference clock crystal input. If an external oscillator is used in place of a crystal, this pin must be left unconnected (floating with no added capacitive load). |
| PLL_REFCLK_O | D14 | D13 | B _{16,17} | Reference clock crystal return. If an external oscillator is used in place of a crystal, this pin must be used for the oscillator input. |
| OSC_BYPASS | D16 | C13 | I ₁₉ | Selects whether an external crystal or external oscillator will be used to drive the internal PLL. (‘0’ = Crystal, ‘1’ = Oscillator) This pin includes a weak internal pulldown. If a pullup is used to obtain a ‘1’ value, the pullup value must be $\leq 8k\Omega$. |

- (1) See [Table 4-10](#) for more information on I/O definitions.

Table 4-9. Pin Functions—Power and Ground

| NAME | PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|--------------|---|---|--------------------|---|
| | ZDQ324 | ZEK324 | | |
| VCC18A_LVDS | B1, B22, C1, C22, D2, D3, D4, D5, D7, D18, D19, D20, D21, E20 | B1, B18, C4, C6, C15, D3, D5, D14, D16, E13, F7, F8, F10, F12 | PWR | 1.8V Power for the differential High-Speed and Low-Speed DMD Interfaces |
| GND18A_LVDS | A1, A22, C2, C3, C4, C5, C6, C7, C16, C17, C18, C19, C20, C21, D8 | A1, A18, C3, C5, C14, C16, D6, E8, E10, E12, E14, F6 | RTN | 1.8V GND for the differential High-Speed and Low-Speed DMD Interfaces |
| VCC18IO | D10 | E9 | PWR | 1.8V Power for 1.8V IO |
| VCC3IO_MVGP | H4 | G5, H5 | PWR | 3.3V Power for TPS99000S-Q1 Interfaces |
| VCC3IO_FLSH | V4 | N5, P5 | PWR | 3.3V Power for the Serial Flash Interface |
| VCC3IO_INTF | K19, L19, M19, R19, T19 | H14, L14, J14, M14 | PWR | 3.3V Power for the Parallel Data, JTAG, and Host Command Interfaces |
| VCC3IO_COSC | C15 | E11 | PWR | 3.3V I/O Power for the Crystal Oscillator |
| GNDIOLA_COSC | C14 | C12 | RTN | 3.3V I/O GND for the Crystal Oscillator |

Table 4-9. Pin Functions—Power and Ground (continued)

| NAME | PIN | | I/O ⁽¹⁾ | DESCRIPTION |
|--------------|---|---|--------------------|---|
| | ZDQ324 | ZEK324 | | |
| VCC3IO | J4, K4, M4, N4, P4, W4, W5, G19 | F14, G14, K6, L5, M6, N7, P8 | PWR | 3.3V I/O Power for all "other" I/O (such as GPIO, TSTPT, PMIC_AD3) |
| VCC33A_LVDS | W9, W13, W15, W19, Y9, Y13, Y15, Y19 | T3, T4, T8, T10, R11, T12, R13, T14, R15, V16 | PWR | 3.3V I/O Power for the OpenLDI Interface |
| GND33A_LVDS | W14, Y14, AA8, AA14, AA20, AB8, AB14, AB20, AB21 | R12, R14, T5, T6, T9, T11, T13, T15, U3, U9, U15, V3, V9, V15 | RTN | 3.3V I/O GND for the OpenLDI Interface |
| VCC11AD_PLLM | D13 | D11 | PWR | 1.1V Analog/Digital Power for MCG (Master Clock Generator) PLL |
| GND11AD_PLLM | C13 | C11 | RTN | 1.1V Analog/Digital GND for MCG (Master Clock Generator) PLL |
| VCC11AD_PLLD | D12 | C10 | PWR | 1.1V Analog/Digital Power for DCG (DMD Clock Generator) PLL |
| GND11AD_PLLD | C12 | D10 | RTN | 1.1V Analog/Digital GND for DCG (DMD Clock Generator) PLL |
| VCC11A_DDI_0 | E19, F19 | F13, G13 | PWR | 1.1V Filtered Core Power - External Filter Group A (HS DMD Interface 0) |
| VCC11A_DDI_1 | E4, F4 | E6, E7 | PWR | 1.1V Filtered Core Power - External Filter Group B (HS DMD Interface 1) |
| VCC11A_LVDS | W11, W12, W17, W18 | N10, P11, P12, P13, P14 | PWR | 1.1V Filtered Core Power - External Filter Group C (OpenLDI Interface) |
| VCCK | G4, H19, (J11), J19, L4, N19, P19, T4, U4, U19, V19, W6, W8, W10, W16 | F9, F11, G6, H13, K13, L6, J6, M13, N6, N8, N9, N11 | PWR | 1.1V Core Power (Ball numbers in parenthesis are also used as thermal ball and are located within the package center region) |
| GND | (J9, J10, J12, J13, J14, K9, K10, K11, K12, K13, K14, L9, L10, L11, L12, L13, L14, M9, M10, M11, M12, M13, M14, N9, N10, N11, N12, N13, N14, P9, P10, P11, P12, P13, P14), Y3, AA1, AA2, AB1, AB2, AB22, Y10, Y11, Y12, Y16, Y17, Y18 | (G7, G8, G9, G10, G11, G12, H7, H8, H9, H10, H11, H12, J7, J8, J9, J10, J11, J12, K7, K8, K9, K10, K11, K12, L7, L8, L9, L10, L11, L12, M7, M8, M9, M10, M11, M12), H6, J13, K14, L13, N12, N13, N14, V1, V18 | RTN | 1.1V Core GND (Ball numbers in parenthesis are also used as thermal ball and are located within the package center region) |
| EFUSE_VDDQ | W7 | P9 | | Manufacturing use only. Must be tied to ground |
| EFUSE_POR33 | Y8 | P10 | | Manufacturing use only. Must be tied to ground |
| RPI_0 | D17 | D15 | I ₅ | Bandgap Reference for SubLVDS drivers (Supports DMD_HS0_xxxx). Requires a resistor (1% Tolerance) to GND18A_LVDS - Value specified in Table 8-4 . |
| RPI_1 | D6 | D4 | I ₅ | Bandgap Reference for SubLVDS drivers (Supports DMD_HS1_xxxx). Requires a resistor (1% Tolerance) to GND18A_LVDS - Value specified in Table 8-4 . |
| RPI_LS | D9 | D7 | I ₅ | Bandgap References for SubLVDS drivers (Supports DMD_LS0_xxxx differential bus signals). Requires a resistor (1% Tolerance) to GND18A_LVDS - Value specified in Table 8-4 . |

(1) See [Table 4-10](#) for more information on I/O definitions.

Table 4-10. I/O Type Subscript Definition

| I/O ⁽¹⁾ | | SUPPLY REFERENCE | ESD STRUCTURE |
|--------------------|--|------------------|----------------------------------|
| SUBSCRIPT | DESCRIPTION | | |
| 1 | 1.8V LVCMOS Input | VCC18IO | ESD diode to GND and supply rail |
| 2 | 1.8V LVCMOS Output | VCC18IO | ESD diode to GND and supply rail |
| 3 | 1.8V LVCMOS Input | VCC18IO | ESD diode to GND and supply rail |
| 4 | 1.8V SubLVDS Output | VCC18A_LVDS | ESD diode to GND and supply rail |
| 5 | 1.8V SubLVDS Input | VCC18A_LVDS | ESD diode to GND and supply rail |
| 6 | 3.3V LVCMOS Output | VCC3IO_MVGP | ESD diode to GND and supply rail |
| 7 | 3.3V LVCMOS Input | VCC3IO_MVGP | ESD diode to GND and supply rail |
| 8 | 3.3V LVCMOS Output | VCC3IO_FLSH | ESD diode to GND and supply rail |
| 9 | 3.3V LVCMOS Input | VCC3IO_FLSH | ESD diode to GND and supply rail |
| 10 | 3.3V LVCMOS Output | VCC3IO_INTF | ESD diode to GND and supply rail |
| 11 | 3.3V LVCMOS Input | VCC3IO_INTF | ESD diode to GND and supply rail |
| 12 | 3.3V I ² C I/O | VCC3IO_INTF | ESD diode to GND and supply rail |
| 13 | 3.3V LVCMOS Output | VCC3IO | ESD diode to GND and supply rail |
| 14 | 3.3V LVCMOS Input | VCC3IO | ESD diode to GND and supply rail |
| 15 | 3.3V I ² C I/O with 3mA drive | VCC3IO | ESD diode to GND and supply rail |
| 16 | 3.3V LVCMOS Output | VCC3IO_OSC | ESD diode to GND and supply rail |
| 17 | 3.3V LVCMOS Input | VCC3IO_OSC | ESD diode to GND and supply rail |
| 18 | 3.3V LVDS Input | VCC33A_LVDS | ESD diode to GND and supply rail |
| 19 | 3.3V LVCMOS Input | VCC3IO_OSC | ESD diode to GND and supply rail |
| 20 | 3.3V LVCMOS Output | VCC3IO | ESD diode to GND and supply rail |
| TYPE | | | |
| I | Input | | N/A |
| O | Output | | |
| B | Bidirectional | | |
| PWR | Power | | |
| RTN | Ground return | | |

(1) External inputs (OLDI, Parallel RGB, GPIO, and so on) must not be driven until power supplies are valid.

Table 4-11. Internal Pullup and Pulldown Characteristics

| INTERNAL PULLUP AND PULLDOWN RESISTOR CHARACTERISTICS ^{(1) (2)} | VCCIO | MIN | MAX | UNIT |
|--|-------|-----|-----|------|
| Weak pullup resistance | 3.3V | 40 | 190 | kΩ |
| Weak pulldown resistance | 3.3V | 30 | 190 | kΩ |

(1) The resistance is dependent on the supply voltage level applied to the I/O.

(2) An external 8kΩ or less pullup or pulldown (if needed) will work for any voltage condition to correctly override any associated internal pullups or pulldowns.

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted)⁽¹⁾

| | | MIN | MAX | UNIT |
|-------------------------------------|--------------------------------|------|--------------------|------|
| SUPPLY VOLTAGE⁽²⁾ | | | | |
| V _(VCC) (Core) | | -0.5 | 1.5 | V |
| V _(VCC11A_DDIx) (Core) | | -0.5 | 1.5 | V |
| V _(VCC11A_LVDS) (Core) | | -0.5 | 1.5 | V |
| V _(VCC11AD_PLLM) (Core) | | -0.5 | 1.5 | V |
| V _(VCC11AD_PLLD) (Core) | | -0.5 | 1.5 | V |
| V _(VCC18A_LVDS) | | -0.5 | 2.5 | V |
| V _(VCC18IO) | | -0.5 | 2.5 | V |
| V _(VCC3IO_MVGP) | | -0.5 | 4.6 | V |
| V _(VCC3IO_INF) | | -0.5 | 4.6 | V |
| V _(VCC3IO_FLSH) | | -0.5 | 4.6 | V |
| V _(VCC3IO_OSC) | | -0.5 | 4.6 | V |
| V _(VCC3IO) | | -0.5 | 4.6 | V |
| V _(VCC33A_LVDS) | | -0.5 | 4.6 | V |
| GENERAL | | | | |
| T _J | Operating junction temperature | -40 | 125 | °C |
| T _C | Operating case temperature | -40 | 124 ⁽³⁾ | °C |
| I _{lat} | Latch-up | -100 | 100 | mA |
| T _{stg} | Storage temperature range | -40 | 150 | °C |

- (1) Stresses beyond those listed under [Section 5.1](#) may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under [Section 5.3](#). Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND.
- (3) Value calculated using package parameters defined in [Section 5.4](#).

5.2 ESD Ratings

| | | VALUE ZDQ PACKAGE | VALUE ZEK PACKAGE | UNIT | |
|--------------------|-------------------------|---|---|------|------|
| V _(ESD) | Electrostatic discharge | Human-body model (HBM), per AEC Q100-002 ⁽¹⁾ | | V | |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins (except corner pins) | | ±500 |
| | | | Corner pins only (ZDQ: A1, A22, AB0, and AB22) (ZEK: A1, A18, V1, V18) | | ±750 |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | NOM | MAX | UNIT |
|-----------------------------|---|---------------------------------|-------|-----|-------|------|
| V _(VCCK) | Core power 1.1V (main 1.1V) | ±5% tolerance | 1.045 | 1.1 | 1.155 | V |
| V _(VCC11A_DDL_0) | Core power 1.1V (External Filter Group A - HS DMD Interface 0) | ±8.18% tolerance ⁽¹⁾ | 1.01 | 1.1 | 1.19 | V |
| V _(VCC11A_DDL_1) | Core power 1.1V (External Filter Group B - HS DMD Interface 1) | ±8.18% tolerance ⁽¹⁾ | 1.01 | 1.1 | 1.19 | V |
| V _(VCC11A_LVDS) | Core power 1.1V (External Filter Group C - OpenLDI Interface) | ±8.18% tolerance ⁽¹⁾ | 1.01 | 1.1 | 1.19 | V |
| V _(VCC11AD_PLLM) | MCG PLL 1.1V power (Analog/Digital) | ±8.18% tolerance ⁽¹⁾ | 1.01 | 1.1 | 1.19 | V |
| V _(VCC11AD_PLLD) | DCG PLL 1.1V power (Analog/Digital) | ±8.18% tolerance ⁽¹⁾ | 1.01 | 1.1 | 1.19 | V |
| V _(VCC18IO) | 1.8V I/O power (Supports DMD Single-Ended LS interface I/O) | ±8.3% tolerance | 1.65 | 1.8 | 1.95 | V |
| V _(VCC18A_LVDS) | 1.8V I/O power (Supports High-Speed and Low-Speed differential DMD interfaces) | ±8.3% tolerance | 1.65 | 1.8 | 1.95 | V |
| V _(VCC3IO_MVGP) | 3/3V I/O power (Supports TPS9900S-Q1: SPI, interrupt, park, RESETZ, and LEDSEL interfaces) | ±8.5% tolerance | 3.02 | 3.3 | 3.58 | V |
| V _(VCC3IO_FLSH) | 3/3V I/O power (Supports serial flash interface) | ±8.5% tolerance | 3.02 | 3.3 | 3.58 | V |
| V _(VCC3IO_INTF) | 3.3V I/O power (Supports: host command (SPI and I ² C), parallel data interface, HOST_IRQ, and JTAG) | ±8.5% tolerance | 3.02 | 3.3 | 3.58 | V |
| V _(VCC3IO_OSC) | 3.3V I/O power (Supports Oscillator) | ±8.5% tolerance | 3.02 | 3.3 | 3.58 | V |
| V _(VCC33A_LVDS) | 3.3V I/O power (Supports OpenLDI interface) | ±8.5% tolerance | 3.02 | 3.3 | 3.58 | V |
| V _(VCC3IO) | 3.3V I/O power (Supports all remaining I/O including: GPIO, PMIC_AD3, TSTPT, ETM_TRACE, et cetera) | ±8.5% tolerance | 3.02 | 3.3 | 3.58 | V |
| T _J | Operating junction temperature | | –40 | | 125 | °C |
| T _C | Operating case temperature | | –40 | | 124 | °C |
| T _A | Operating ambient temperature ⁽²⁾ | | –40 | | 105 | °C |

(1) These I/O supply ranges are wider to facilitate additional external filtering.

(2) Operating ambient temperature is dependent on system thermal design. Operating case temperature may not exceed its specified range across ambient temperature conditions.

5.4 Thermal Information

| THERMAL METRIC ⁽¹⁾ | | ZDQ (BGA) | ZEK (nfBGA) | UNIT |
|--------------------------------|--|-----------|-------------|------|
| | | 324 PINS | 324 PINS | |
| Ψ _{JT} ⁽²⁾ | Temperature variance from junction to package top center temperature, per unit power dissipation | 0.77 | 0.2 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

(2) $(0.94W) \times (0.2^{\circ}C/W) \approx 0.19^{\circ}C$ temperature difference.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP ⁽¹⁾ | MAX ⁽²⁾ | UNIT |
|---|--|---|-----|--------------------|--------------------|------|
| TOTAL | | | | | | |
| $I_{(VCC11)}$ | 1.1V total current | | | 201 | 467.1 | mA |
| $I_{(VCC18)}$ | 1.8V total current | | | 71 | 151.6 | mA |
| $I_{(VCC33)}$ | 3.3V total current | | | 28.1 | 30.1 | mA |
| ESTIMATED CURRENT PER SUPPLY⁽³⁾ | | | | | | |
| $I_{(VCCK)}$ | 1.1V Core current | | | 131.5 | 390.7 | mA |
| $I_{(VCC11A_DDI_0)}$ | 1.1V Core current (Filtered) | At 600MHz data rate | | 15.8 | 17.4 | mA |
| $I_{(VCC11A_DDI_1)}$ | 1.1V Core current (Filtered) | At 600MHz data rate | | 15.8 | 17.4 | mA |
| $I_{(VCC11A_LVDS)}$ | 1.1V Core current (Filtered) | OpenLDI Interface, single port, 5 lanes active | | 22.5 | 24.8 | mA |
| $I_{(VCC11AD_PLL)}$ | 1.1V Core current (MCG PLL) | | | 7.7 | 8.4 | mA |
| $I_{(VCC11AD_PLLD)}$ | 1.1V Core current (DCG PLL) | | | 7.7 | 8.4 | mA |
| $I_{(VCC18A_LVDS)}$ | 1.8V I/O current (Both 8-bit ports - DMD HS differential Interface) | At 600MHz data rate | | 63.3 | 131.5 | mA |
| $I_{(VCC18A_LVDS)}$ | 1.8V I/O current (DMD LS differential Interface) | At 120MHz data rate | | 5.2 | 10.7 | mA |
| $I_{(VCC18IO)}$ | 1.8V I/O current (DMD LS single-ended interfaces, DMD reset) | | | 2.5 | 9.4 | mA |
| $I_{(VCC3IO_MVGP)}$ | 3.3V I/O current (TPS99000S-Q1 SPI, TPS99000S-Q1 Reset, PMIC_PARKZ, RESETZ) | | | 1.7 | 1.8 | mA |
| $I_{(VCC3IO_INTF)}$ | 3.3V I/O current (Host SPI, Host I ² C, Host IRQ, JTAG, Parallel Port) | | | 1.7 | 1.8 | mA |
| $I_{(VCC3IO_FLSH)}$ | 3.3V I/O current (Serial Flash SPI interface) | | | 5.5 | 5.9 | mA |
| $I_{(VCC3IO_OSC)}$ | 3.3V I/O current (Crystal/Oscillator) | With 3k Ω external series resistor (R _S) | | 0.975 | 1.3 | mA |
| $I_{(VCC3IO)}$ | 3.3V I/O current (GPIO, PMIC_AD3, Mstr I ² C, TSTPT, ETM, and so forth) | | | 12.6 | 13.5 | mA |
| $I_{(VCC33A_LVDS)}$ | 3.3V I/O current (OpenLDI Interface - each port - 5 lanes active) | | | 6.3 | 6.8 | mA |

- (1) Typical-case power measured with PVT condition = nominal process, typical voltage, typical temperature (25°C case temperature). Input source 1152 × 576 24-bit 60Hz OpenLDI with RGBW ramp image.
- (2) Worst-case power PVT condition = corner process, high voltage, high temperature (105°C case temperature). Input source 1358 × 566 24-bit. 60Hz OpenLDI with pseudo-random noise image.
- (3) Estimated current per supply was not directly measured. These values are based on an approximate expected current consumption percentage of the total measured current drawn by each voltage rail.

5.6 Electrical Characteristics for Fixed Voltage I/O

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|------------------------------------|--|-----------------------------|-----|----------------|------|
| V _{IH} | High-level input threshold voltage | 1.8V LVCMOS (I/O type 3) | | | 0.7 × VCC18IO | V |
| | | 3.3V LVCMOS (I/O type 7) | | | 2.0 | |
| | | 3.3V LVCMOS (I/O type 9) | | | 2.0 | |
| | | 3.3V LVCMOS (I/O type 11) | | | 2.0 | |
| | | 3.3V I ² C buffer (I/O type 12) | | | 0.7 × VCC_INTF | |
| | | 3.3V LVCMOS (I/O type 14) | | | 2.0 | |
| | | 3.3V LVCMOS (I/O type 16,17) | | | 0.7 × VCC3IO | |
| | | 3.3V LVCMOS (I/O type 19) | | | 2.0 | |
| | | 3.3V I ² C buffer (I/O type 15) | | | 0.7 × VCC3IO | |
| V _{IL} | Low-level input threshold voltage | 1.8V LVCMOS (I/O type 3) | | | 0.3 × VCC18IO | V |
| | | 3.3V LVCMOS (I/O type 7) | | | 0.8 | |
| | | 3.3V LVCMOS (I/O type 9) | | | 0.8 | |
| | | 3.3V LVCMOS (I/O type 11) | | | 0.8 | |
| | | 3.3V I ² C buffer (I/O type 12) | | | 0.3 × VCC_INTF | |
| | | 3.3V LVCMOS (I/O type 14) | | | 0.8 | |
| | | 3.3V LVCMOS (I/O type 16,17) | | | 0.3 × VCC3IO | |
| | | 3.3V LVCMOS (I/O type 19) | | | 0.8 | |
| | | 3.3V I ² C buffer (I/O type 15) | | | 0.3 × VCC3IO | |
| V _{OH} | High-level output voltage | 1.8V LVCMOS (I/O type 1,2) | I _{OH} = Max rated | | 0.75 × VCC18IO | V |
| | | 3.3V LVCMOS (I/O type 6) | I _{OH} = Max rated | | 2.4 | |
| | | 3.3V LVCMOS (I/O type 8) | I _{OH} = Max rated | | 2.4 | |
| | | 3.3V LVCMOS (I/O type 10) | I _{OH} = Max rated | | 2.4 | |
| | | 3.3V I ² C buffer (I/O type 12) | I _{OH} = Max rated | | N/A | |
| | | 3.3V LVCMOS (I/O type 13) | I _{OH} = Max rated | | 2.4 | |
| | | 3.3V I ² C buffer (I/O type 15) | I _{OH} = Max rated | | N/A | |
| | | 3.3V LVCMOS (I/O type 20) | I _{OH} = Max rated | | 2.4 | |
| V _{OL} | Low-level output voltage | 1.8V LVCMOS (I/O type 1,2) | I _{OL} = Max rated | | 0.4 | V |
| | | 3.3V LVCMOS (I/O type 6) | I _{OL} = Max rated | | 0.4 | |
| | | 3.3V LVCMOS (I/O type 8) | I _{OL} = Max rated | | 0.4 | |
| | | 3.3V LVCMOS (I/O type 10) | I _{OL} = Max rated | | 0.4 | |
| | | 3.3V I ² C buffer (I/O type 12) | I _{OL} = Max rated | | 0.4 | |
| | | 3.3V LVCMOS (I/O type 13) | I _{OL} = Max rated | | 0.4 | |
| | | 3.3V I ² C buffer (I/O type 15) | I _{OL} = Max rated | | 0.4 | |
| | | 3.3V LVCMOS (I/O type 20) | I _{OL} = Max rated | | 0.4 | |
| I _{OH} | High-level output current | 1.8V LVCMOS (I/O type 1) | | | 6 | mA |
| | | 1.8V LVCMOS (I/O type 2) | | | 7.2 | |
| | | 3.3V LVCMOS (I/O type 6) | | | 6 | |
| | | 3.3V LVCMOS (I/O type 8) | | | 6 | |
| | | 3.3V LVCMOS (I/O type 10) | | | 6 | |
| | | 3.3V I ² C buffer (I/O type 12) | | | N/A | |
| | | 3.3V LVCMOS (I/O type 13) | | | 8 | |
| | | 3.3V I ² C buffer (I/O type 15) | | | N/A | |
| | | 3.3V LVCMOS (I/O type 20) | | | 6 | |

5.6 Electrical Characteristics for Fixed Voltage I/O (continued)

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------|--------------------------------|--|-----|------|-----|------|
| I _{OL} | Low-level output current | 1.8V LVCMOS (I/O type 1) | | 6 | | mA |
| | | 1.8V LVCMOS (I/O type 2) | | 7.2 | | |
| | | 3.3V LVCMOS (I/O type 6) | | 6 | | |
| | | 3.3V LVCMOS (I/O type 8) | | 6 | | |
| | | 3.3V LVCMOS (I/O type 10) | | 6 | | |
| | | 3.3V I ² C buffer (I/O type 12) | | 3 | | |
| | | 3.3V LVCMOS (I/O type 13) | | 8 | | |
| | | 3.3V I ² C buffer (I/O type 15) | | 3 | | |
| | | 3.3V LVCMOS (I/O type 20) | | 6 | | |
| I _{OZ} | High-impedance leakage current | 1.8V LVCMOS (I/O type 1,2) | | ±1.0 | ±10 | µA |
| | | 3.3V LVCMOS (I/O type 6) | | ±1.0 | ±10 | |
| | | 3.3V LVCMOS (I/O type 8) | | ±1.0 | ±10 | |
| | | 3.3V LVCMOS (I/O type 10) | | ±1.0 | ±10 | |
| | | 3.3V I ² C buffer (I/O type 12) | | | ±10 | |
| | | 3.3V LVCMOS (I/O type 13) | | ±1.0 | ±10 | |
| | | 3.3V LVCMOS (I/O type 16) | | ±1.0 | | |
| | | 3.3V I ² C buffer (I/O type 15) | | | ±10 | |
| | | 3.3V LVCMOS (I/O type 20) | | ±1.0 | ±10 | |

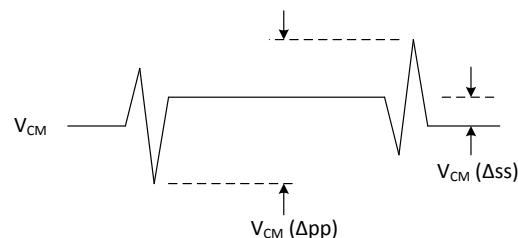
(1) The number inside each parenthesis for the I/O refers to the type defined in Table 4-10.

5.7 DMD High-Speed SubLVDS Electrical Characteristics

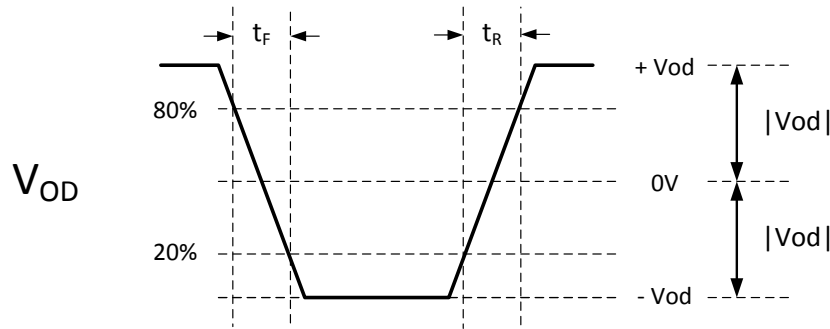
over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|--------------------------------------|---|-----------------------------|-------|------|-------|------|
| V _{CM} | Steady-state common mode voltage | 1.8V SubLVDS (I/O type 4,5) | 0.8 | 0.9 | 1.0 | V |
| V _{CM} (Δpp) ⁽¹⁾ | V _{CM} change peak-to-peak (during switching) | 1.8V SubLVDS (I/O type 4,5) | | | 75 | mV |
| V _{CM} (Δss) ⁽¹⁾ | V _{CM} change steady state | 1.8V SubLVDS (I/O type 4,5) | -10 | | 10 | mV |
| V _{OD} ⁽²⁾ | Differential output voltage magnitude. R _{BGR} = 75kΩ. | 1.8V SubLVDS (I/O type 4,5) | 155 | 200 | 250 | mV |
| V _{OD} (Δ) ⁽³⁾ | V _{OD} change (between logic states) | 1.8V SubLVDS (I/O type 4,5) | -10 | | 10 | mV |
| V _{OH} | Single-ended output voltage high | 1.8V SubLVDS (I/O type 4,5) | 0.88 | 1.00 | 1.125 | V |
| V _{OL} | Single-ended output voltage low | 1.8V SubLVDS (I/O type 4,5) | 0.675 | 0.80 | 0.925 | V |
| t _R ⁽²⁾ | Differential output rise time | 1.8V SubLVDS (I/O type 4,5) | | | 250 | ps |
| t _F ⁽²⁾ | Differential output fall time | 1.8V SubLVDS (I/O type 4,5) | | | 250 | ps |
| f _{MAX} | Max switching rate | 1.8V SubLVDS (I/O type 4,5) | | | 1200 | Mbps |
| DCout | Output duty cycle | 1.8V SubLVDS (I/O type 4,5) | 45% | 50% | 55% | |
| T _{Xterm} ⁽¹⁾ | Internal differential termination | 1.8V SubLVDS (I/O type 4,5) | 80 | 100 | 120 | Ω |

(1) Definition of V_{CM} changes:



- (2) Note that V_{OD} is the differential voltage swing measured across a 100Ω termination resistance connected directly between the transmitter differential pins. $|V_{OD}|$ is the magnitude of the peak to peak voltage swing across the P and N output pins. Because V_{CM} cancels out when measured differentially, V_{OD} voltage swings relative to 0. Rise and fall times are defined for the differential V_{OD} signal as follows:



Differential Output Signal

(Note: V_{CM} is removed when signals are viewed differentially)

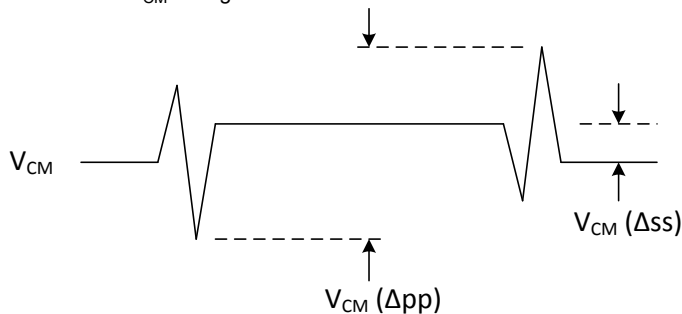
- (3) When TX data input = '1', differential output voltage V_{OD1} is defined. When TX data input = '0', differential output voltage V_{OD0} is defined. As such, the steady state magnitude of the difference is: $|V_{OD}| (\Delta) = ||V_{OD1}| - |V_{OD0}||$.

5.8 DMD Low-Speed SubLVDS Electrical Characteristics

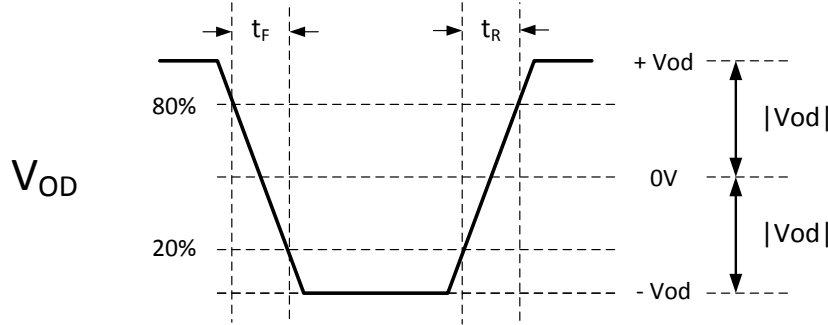
over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | MIN | NOM | MAX | UNIT | |
|------------------------------|--|-----------------------------|-------|------|-------|----------|
| V_{CM} | Steady-state common mode voltage | 1.8V SubLVDS (I/O type 4,5) | 0.8 | 0.9 | 1.0 | V |
| $V_{CM} (\Delta_{pp})^{(1)}$ | V_{CM} change peak-to-peak (during switching) | 1.8V SubLVDS (I/O type 4,5) | | | 75 | mV |
| $V_{CM} (\Delta_{ss})^{(1)}$ | V_{CM} change steady state | 1.8V SubLVDS (I/O type 4,5) | -10 | | 10 | mV |
| $ V_{OD} ^{(2)}$ | Differential output voltage magnitude. $R_{BGR} = 75k\Omega$. | 1.8V SubLVDS (I/O type 4,5) | 155 | 200 | 250 | mV |
| $V_{OD} (\Delta)^{(3)}$ | V_{OD} change (between logic states) | 1.8V SubLVDS (I/O type 4,5) | -10 | | 10 | mV |
| V_{OH} | Single-ended output voltage high | 1.8V SubLVDS (I/O type 4,5) | 0.88 | 1.00 | 1.125 | V |
| V_{OL} | Single-ended output voltage low | 1.8V SubLVDS (I/O type 4,5) | 0.675 | 0.80 | 0.925 | V |
| $t_R^{(2)}$ | Differential output rise time | 1.8V SubLVDS (I/O type 4,5) | | | 250 | ps |
| $t_F^{(2)}$ | Differential output fall time | 1.8V SubLVDS (I/O type 4,5) | | | 250 | ps |
| t_{MAX} | Max switching rate | 1.8V SubLVDS (I/O type 4,5) | | | 240 | Mbps |
| DCout | Output duty cycle | 1.8V SubLVDS (I/O type 4,5) | 45% | 50% | 55% | |
| TX_{term} | Internal differential termination | 1.8V SubLVDS (I/O type 4,5) | 80 | 100 | 120 | Ω |

- (1) Definition of V_{CM} changes:



- (2) Note that V_{OD} is the differential voltage swing measured across a 100Ω termination resistance connected directly between the transmitter differential pins. $|V_{OD}|$ is the magnitude of the peak to peak voltage swing across the P and N output pins. Because V_{CM} cancels out when measured differentially, V_{OD} voltage swings relative to 0. Rise and fall times are defined for the differential V_{OD} signal as follows:



Differential Output Signal

(Note: V_{CM} is removed when signals are viewed differentially)

- (3) When TX data input = '1', differential output voltage V_{OD1} is defined. When TX data input = '0', differential output voltage V_{OD0} is defined. As such, the steady state magnitude of the difference is: $|V_{OD}| (\Delta) = ||V_{OD1}| - |V_{OD0}||$.

5.9 OpenLDI LVDS Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | | MIN | NOM | MAX | UNIT |
|-------------|-----------------------------------|-------------------------|------|-----|-----|----------|
| V_{CM} | Steady-state common mode voltage | 3.3V LVDS (I/O type 18) | 0.35 | 1.2 | 1.6 | V |
| $ V_{ID} $ | Differential input voltage | 3.3V LVDS (I/O type 18) | 100 | | 700 | mV |
| R_{Xterm} | Internal differential termination | 3.3V LVDS (I/O type 18) | 90 | 111 | 132 | Ω |

5.10 Power Dissipation Characteristics

| PARAMETER | | VALUE | UNIT |
|-----------|-------------------------|-------|------|
| P_{MAX} | Package - Maximum Power | 0.94 | W |

5.11 System Oscillators Timing Requirements

| | | | MIN | NOM | MAX | UNIT |
|-------------|--|--------------------------------------|--------------|--------|--------|------|
| f_{clock} | Clock frequency, MOSC ⁽¹⁾ | | 15.997 | 16.000 | 16.003 | MHz |
| t_c | Cycle time, MOSC ⁽¹⁾ | | 62.488 | 62.500 | 62.512 | ns |
| $t_{w(H)}$ | Pulse duration ⁽²⁾ , MOSC, high | 50% to 50% reference points (signal) | 40% of t_c | | | |
| $t_{w(L)}$ | Pulse duration ⁽²⁾ , MOSC, low | 50% to 50% reference points (signal) | 40% of t_c | | | |
| t_t | Transition time ⁽²⁾ , MOSC, $t_t = t_f / t_r$ | 20% to 80% reference points (signal) | 0.2 | | 2 | ns |
| t_{jp} | Long term periodic jitter ⁽²⁾ , MOSC (that is the deviation in period from ideal period due solely to high frequency jitter) | | | | 100 | ps |

- (1) The MOSC input cannot support spread spectrum clock spreading.
- (2) Applies only when driven through an external digital oscillator. This is a 1 sigma RMS value.

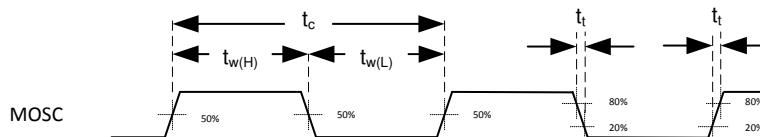


Figure 5-1. System Oscillators

Table 5-1. Crystal / Oscillator Electrical Characteristics

| PARAMETER | NOMINAL | UNIT |
|---------------------------------|---------|------|
| PLL_REFCLK_I TO GND capacitance | 3.5 | pF |

Table 5-1. Crystal / Oscillator Electrical Characteristics (continued)

| PARAMETER | NOMINAL | UNIT |
|---------------------------------|---------|------|
| PLL_REFCLK_O TO GND capacitance | 3.45 | pF |

5.12 Power Supply and Reset Timing Requirements

| | | | MIN | MAX | UNIT |
|--|---|--|-----|-----|---------|
| TPS99000S-Q1 REQUIREMENTS⁽¹⁾ | | | | | |
| t_{ramp} | Power supply ramp time ⁽²⁾ | Power supply ramp to minimum recommended operating voltage | 0.5 | 10 | ms |
| t_{ps_aln} | 1.1V Power Supply Alignment ⁽³⁾ | Leading edge for application or removal of power. Each 1.1V power supply to the DLPC23xS-Q1 must be applied simultaneously within this time. | | 10 | μ s |
| t_{rst} | RESETZ low to Power Supply disable ⁽⁴⁾ | Leading edge for removal of power | 1.0 | | μ s |
| $t_{w(L1)}$ | Pulse duration, active low, RESETZ ⁽⁴⁾ | 95% power to 50% RESETZ reference point At initial application of power | 5.0 | | ms |
| $t_{w(L2)}$ | Pulse duration, active low, RESETZ | 50% to 50% reference points (RESETZ) Subsequent resets after initial application of power | 1.0 | | μ s |
| t_t | Transition time, RESETZ, $t_t = t_f$ and t_r | 20% to 80% reference points (signal) | | 6 | μ s |

- (1) The TPS99000S-Q1 controls power supply timing for the DLPC23xS-Q1. Refer to the [TPS99000S-Q1 System Management and Illumination Controller Data Sheet DLPS202](#) for additional system power timing requirements.
- (2) Power supplies do not need to ramp simultaneously, but each supply must reach its minimum voltage within the maximum ramp time specified.
- (3) The DLPC23xS-Q1 does not require specific sequencing or alignment of 1.8V and 3.3V supplies. However, the TPS99000S-Q1 enforces sequencing of the 1.1V, 1.8V, and 3.3V voltage rails. The following describes DLPC23xS-Q1 behavior when the voltage rails are not brought up simultaneously:
 - VCKK (1.1V core) Power = On, I/O Power = Off, RESETZ = '0': While this condition exists, additional leakage current can be drawn, and all outputs are unknown (likely to be a weak "low").
 - VCKK (1.1V core) Power = Off, I/O Power = On, RESETZ = '0': While this condition exists all outputs are tristated.

Neither of these two conditions will impact normal DLPC23xS-Q1 reliability.

- (4) RESETZ must be held low if any supply (Core or I/O) is less than its minimum specified on value. For more information on RESETZ, see [Section 4](#).

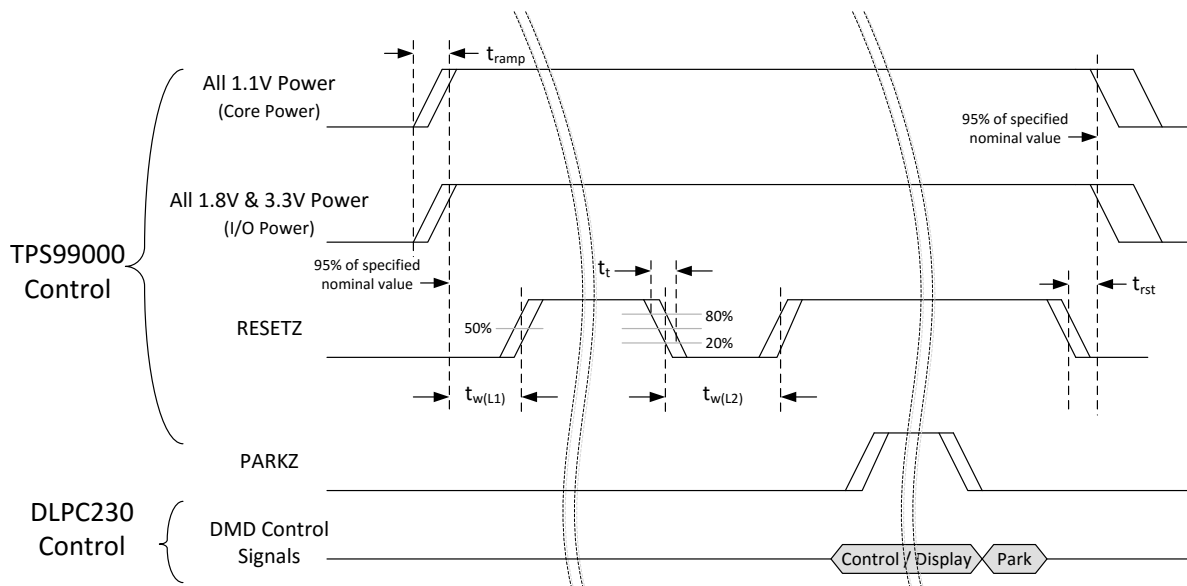


Figure 5-2. Power Supply and RESETZ Timing

5.13 Parallel Interface General Timing Requirements

| | | MIN | MAX | UNIT | |
|-----------------|---|-----------------------------|-------------------------|--------------------|-----|
| f_{clock} | Clock frequency, PCLK | 12.0 | 110.0 | MHz | |
| t_{p_clkper} | Clock period, PCLK | 50% reference points | 9.091 | 83.33 | ns |
| t_{p_wh} | Pulse duration low, PCLK | 50% reference points | 2.286 | | ns |
| t_{p_wl} | Pulse duration high, PCLK | 50% reference points | 2.286 | | ns |
| t_{p_su} | Setup time – HSYNC, DATEN, PDATA(23:0) valid before the active edge of PCLK | 50% reference points | 0.8 | | ns |
| t_{p_h} | Hold time – HSYNC, DATEN, PDATA(23:0) valid after the active edge of PCLK | 50% reference points | 0.8 | | ns |
| t_{t_clk} | Transition time – PCLK | 20% to 80% reference points | 6 | | ns |
| t_t | Transition time – all other signals on this port | 20% to 80% reference points | 6 | | ns |
| f_{spread} | Supported Spread Spectrum range | Percent of f_{clock} rate | -1% | +1% ⁽¹⁾ | |
| f_{mod} | Supported Spread Spectrum Modulation Frequency ^{(1) (2)} | 25 | 65 ⁽³⁾ | | kHz |
| t_{p_clkjit} | Clock jitter, PCLK | | $t_{p_clkper} - 5.414$ | | ps |

- (1) This value is limited by the maximum clock frequency for f_{clock} (that is, if $f_{clock} = \text{max clock freq}$, then $f_{spread} \text{ max} = 0\%$).
- (2) Modulation Waveforms supported: Sine and Triangle.
- (3) Spread spectrum modulation tested at a maximum of 35 kHz. Simulated up to 65 kHz.

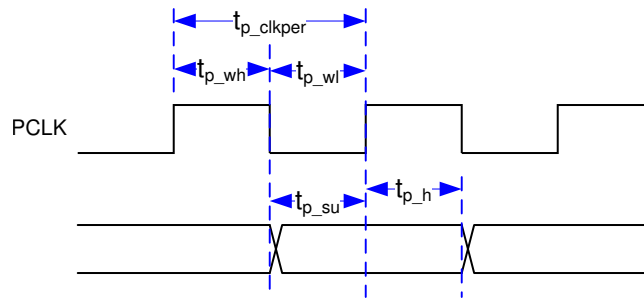


Figure 5-3. Parallel Interface General Timing

5.14 OpenLDI Interface General Timing Requirements

The DLPC23xS-Q1 ASIC input interface supports a subset of the industry standard OpenLDI (FPD-Link I) interface (Open LVDS Display Interface Specification v0.95 - May 13, 1999). Specifically, from the standard, the ASIC supports the 24-bit, Single Pixel Format, using the Unbalanced Operating Mode and Pixel Mapping.

| | | MIN | NOM | MAX | UNIT | |
|-------------------|---|------------------------------|---------------------|----------------------------|--------------------|----|
| f_{clock} | Clock frequency, L1_CLK_P/N, L2_CLK_P/N | 20.0 | | 110 | MHz | |
| t_p | Clock period, PCLK | 50% reference points | 9.091 | 50 | ns | |
| t_{skew} | Skew Margin (between clock and data) | $f_{clock} = 85 \text{ MHz}$ | -400 ⁽⁵⁾ | 0 | 400 ⁽⁵⁾ | ps |
| t_{skew_ports} | Clock to clock skew margin between ports on same ASIC, and between ports on different ASICs | | | 1 | clocks | |
| t_{ip0} | Input data position 1 | $(t_p / 7) - t_{skew}$ | $(t_p / 7)$ | $(t_p / 7) + t_{skew}$ | ps | |
| t_{ip6} | Input data position 2 | $2 * (t_p / 7) - t_{skew}$ | $2 * (t_p / 7)$ | $2 * (t_p / 7) + t_{skew}$ | ps | |
| t_{ip5} | Input data position 3 | $3 * (t_p / 7) - t_{skew}$ | $3 * (t_p / 7)$ | $3 * (t_p / 7) + t_{skew}$ | ps | |
| t_{ip4} | Input data position 4 | $4 * (t_p / 7) - t_{skew}$ | $4 * (t_p / 7)$ | $4 * (t_p / 7) + t_{skew}$ | ps | |
| t_{ip3} | Input data position 5 | $5 * (t_p / 7) - t_{skew}$ | $5 * (t_p / 7)$ | $5 * (t_p / 7) + t_{skew}$ | ps | |
| t_{ip2} | Input data position 6 | $6 * (t_p / 7) - t_{skew}$ | $6 * (t_p / 7)$ | $6 * (t_p / 7) + t_{skew}$ | ps | |

5.14 OpenLDI Interface General Timing Requirements (continued)

The DLPC23xS-Q1 ASIC input interface supports a subset of the industry standard OpenLDI (FPD-Link I) interface (Open LVDS Display Interface Specification v0.95 - May 13, 1999). Specifically, from the standard, the ASIC supports the 24-bit, Single Pixel Format, using the Unbalanced Operating Mode and Pixel Mapping.

| | | MIN | NOM | MAX | UNIT |
|---------------------|---|------------------------------------|-----|--------------------|--------------------|
| t_{jitter} | Input Jitter Tolerance (cycle to cycle, peak to peak) | | | 100 | ps |
| f_{spread} | Supported Spread Spectrum range | percent of f_{clock} rate | | -1% ⁽¹⁾ | +1% ⁽²⁾ |
| f_{mod} | Supported Spread Spectrum Modulation Frequency ^{(3) (4)} | 25 | | 65 | kHz |

- (1) This value is limited by the minimum clock frequency for f_{clock} (that is, if $f_{\text{clock}} = \text{min clock freq}$, then $f_{\text{spread max}} = 0\%$).
- (2) This value is limited by the maximum clock frequency for f_{clock} (that is, if $f_{\text{clock}} = \text{max clock freq}$, then $f_{\text{spread max}} = 0\%$).
- (3) Modulation Waveforms supported: Sine and Triangle.
- (4) Spread spectrum on OpenLDI interfaces was simulated, but not tested.
- (5) t_{skew} for other f_{clock} values can be estimated by $\pm t_{\text{skew}} = -7.143 * f_{\text{clock}} + 1007.1 - (t_{\text{jitter}} - 100)$

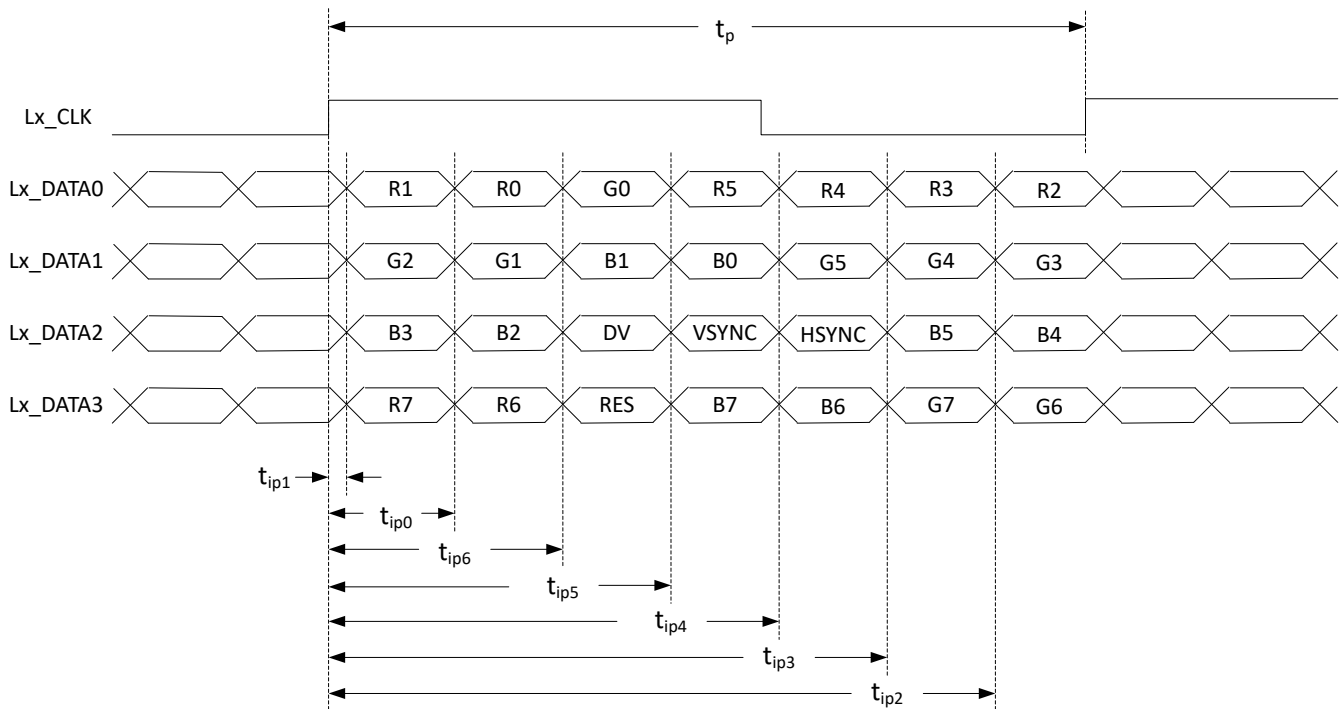


Figure 5-4. OpenLDI Interface Timing

5.15 Parallel/OpenLDI Interface Frame Timing Requirements

See⁽¹⁾

| | | | MIN | MAX | UNIT |
|--------------|---|--|-----|------|--------|
| VSYNC | Vertical Sync Rate (for the specified active source resolution) | Section 6.2.1 for supported resolutions. | 58 | 61 | Hz |
| t_{p_vsw} | Pulse duration – VSYNC high | 50% reference points | 1 | | lines |
| t_{p_vbp} | Vertical back porch (VBP) – time from the leading edge of VSYNC to the leading edge HSYNC for the first active line (includes t_{p_vsw}). | 50% reference points | 2 | | lines |
| t_{p_vfp} | Vertical front porch (VFP) – time from the leading edge of the HSYNC following the last active line in a frame to the leading edge of VSYNC | 50% reference points | 1 | | lines |
| t_{p_tvb} | Total vertical blanking – time from the leading edge of HSYNC following the last active line of one frame to the leading edge of HSYNC for the first active line in the next frame. (This is equal to the sum of VBP (t_{p_vbp}) + VFP (t_{p_vfp})) | 50% reference points | 14 | | lines |
| t_{p_hsw} | Pulse duration – HSYNC high | 50% reference points | 8 | | PCLKs |
| t_{p_hbp} | Horizontal back porch – time from rising edge of HSYNC to rising edge of DATEN (includes t_{p_hsw}) | 50% reference points | 9 | | PCLKs |
| t_{p_hfp} | Horizontal front porch – time from falling edge of DATEN to rising edge of HSYNC | 50% reference points | 8 | | PCLKs |
| t_{p_thb} | Total horizontal blanking | 50% reference points | 64 | | PCLKs |
| TPPL | Total Pixels Per Line | | | 8191 | Pixels |

(1) While these requirements are not specific to the OpenLDI interface, they are appropriate for any source that drives an OpenLDI transmitter connected to the ASIC OpenLDI interface.

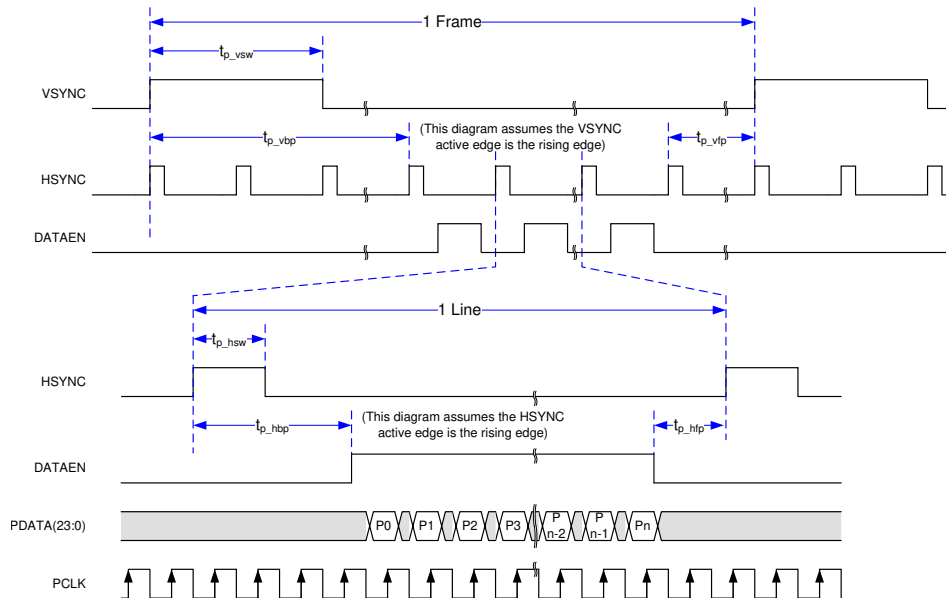


Figure 5-5. Source Frame Timing

5.16 Host/Diagnostic Port SPI Interface Timing Requirements

The DLPC23xS-Q1 ASIC Host/Diagnostic SPI port interface timing requirements are shown below.⁽¹⁾

| | | MIN | MAX | UNIT |
|--------------------|---|-----------------------------|-------|------|
| f_{clock} | Clock frequency, HOST_SPI_CLK (50% reference points) | | 10.00 | MHz |
| $t_{\text{p_wh}}$ | Pulse duration low, HOST_SPI_CLK (50% reference points) | 45.0 | | ns |
| $t_{\text{p_wl}}$ | Pulse duration high, HOST_SPI_CLK (50% reference points) | 45.0 | | ns |
| t_t | Transition time – all input signals | 20% to 80% reference points | 6 | ns |
| $t_{\text{p_su}}$ | Setup time – HOST_SPI_DIN valid before HOST_SPI_CLK capture edge (50% reference points) | 10.0 | | ns |
| $t_{\text{p_h}}$ | Hold time – HOST_SPI_DIN valid after HOST_SPI_CLK capture edge | 50% reference points | 18.0 | ns |
| t_{out} | Clock-to-Data out - HOST_SPI_DOUT from HOST_SPI_CLK launch edge (50% reference points) | 0.0 | 35.0 | ns |

- (1) The DLPC23xS-Q1 Host/Diagnostic Port SPI interface supports SPI Modes 0, 1, 2, and 3 (that is, both clock polarities and both clock phases). The HOST_SPI_MODE input must be set to match the SPI mode being used.

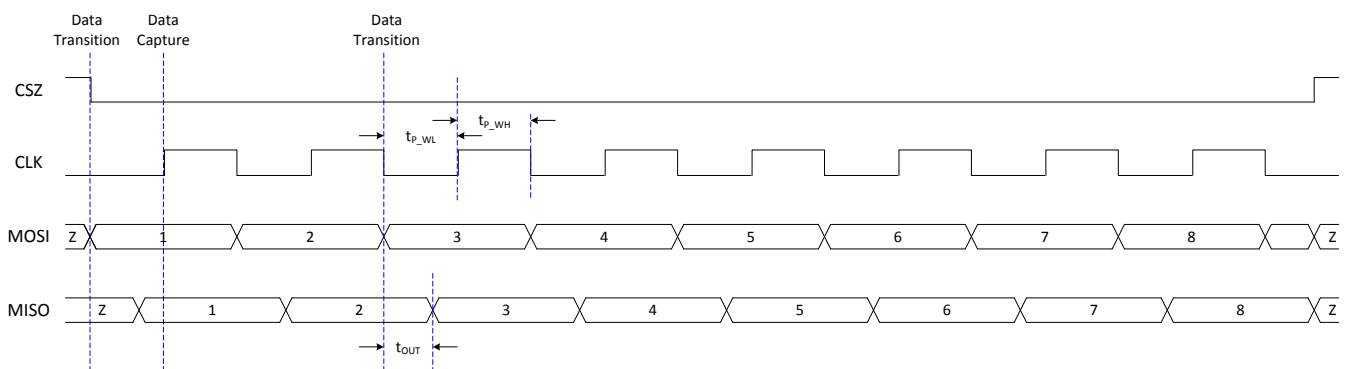


Figure 5-6. Host/Diagnostic Port SPI Interface Timing (Example: SPI Mode 0 (Clock Polarity = 0, Clock Phase = 0))

5.17 Host/Diagnostic Port I²C Interface Timing Requirements

The DLPC23xS-Q1 ASIC Host/Diagnostic I²C port interface timing requirements are shown below.^{(1) (2)}

| | | MIN | MAX | UNIT |
|--------------------|---|---------------|-----|------|
| f_{clock} | Clock frequency, HOST_I ² C_SCL (50% reference points) | Fast-Mode | 400 | kHz |
| | | Standard Mode | 100 | |
| C_L | Capacitive Load (for each bus line) | | 200 | pF |

- (1) Meets all I²C timing per the I²C Bus Specification (except for capacitive loading as specified above). For reference see version 2.1 of the Phillips/NXP specification.
 (2) The maximum clock frequency does not account for rise time, nor added capacitance of PCB or external components which can adversely impact this value.

5.18 Flash Interface Timing Requirements

The DLPC23xS-Q1 ASIC flash memory interface consists of a SPI serial interface. See [Section 7.3.4](#).

| (1) | | | MIN | MAX | UNIT |
|------------------------|---|-----------------------------|-------|----------------------|------|
| f_{clock} | Clock frequency, FLSH_SPI_CLK | When VCC3IO_FLSH = 3.3VDC | 9.998 | 50.01 ⁽²⁾ | MHz |
| $t_{\text{p_clkper}}$ | Clock period, FLSH_SPI_CLK (50% reference points) | When VCC3IO_FLSH = 3.3VDC | 20.0 | 100 | ns |
| $t_{\text{p_wh}}$ | Pulse duration low, FLSH_SPI_CLK (50% reference points) | When VCC3IO_FLSH = 3.3VDC | 9 | | ns |
| $t_{\text{p_wl}}$ | Pulse duration high, FLSH_SPI_CLK (50% reference points) | When VCC3IO_FLSH = 3.3VDC | 9 | | ns |
| t_{t} | Transition time – all input signals | 20% to 80% reference points | | 6 | ns |
| $t_{\text{p_su}}$ | Setup time – FLSH_SPI_DIO[3:0] valid before FLSH_SPI_CLK falling edge (50% reference points) | When VCC3IO_FLSH = 3.3VDC | 7.0 | | ns |
| $t_{\text{p_h}}$ | Hold time – FLSH_SPI_DIO[3:0] valid after FLSH_SPI_CLK falling edge | 50% reference points | 0.0 | | ns |
| $t_{\text{p_clqv}}$ | FLSH_SPI_DIO[3:0] output delay valid time (with respect to falling edge of FLSH_SPI_CLK or falling edge of FLSH_SPI_CSZ) (50% reference points) | When VCC3IO_FLSH = 3.3VDC | -3.0 | 3.0 | ns |

- (1) The DLPC23xS-Q1 communicates with flash devices using a slight variant of SPI Transfer Mode 0 (that is, clock polarity = 0, clock phase = 0). Instead of capturing MISO data on the clock edge opposite from that used to transmit MOSI data, the DLPC23xS-Q1 captures MISO data on the same clock edge used to transmit the next MOSI data. As such, the DLPC23xS-Q1 Flash SPI interface requires that MISO data from the flash device remain active until the end of the full clock cycle to allow the last data bit to be captured. This is shown in [Figure 5-8](#).
- (2) The actual maximum clock rate driven from the DLPC23xS-Q1 can be slightly less than this value.

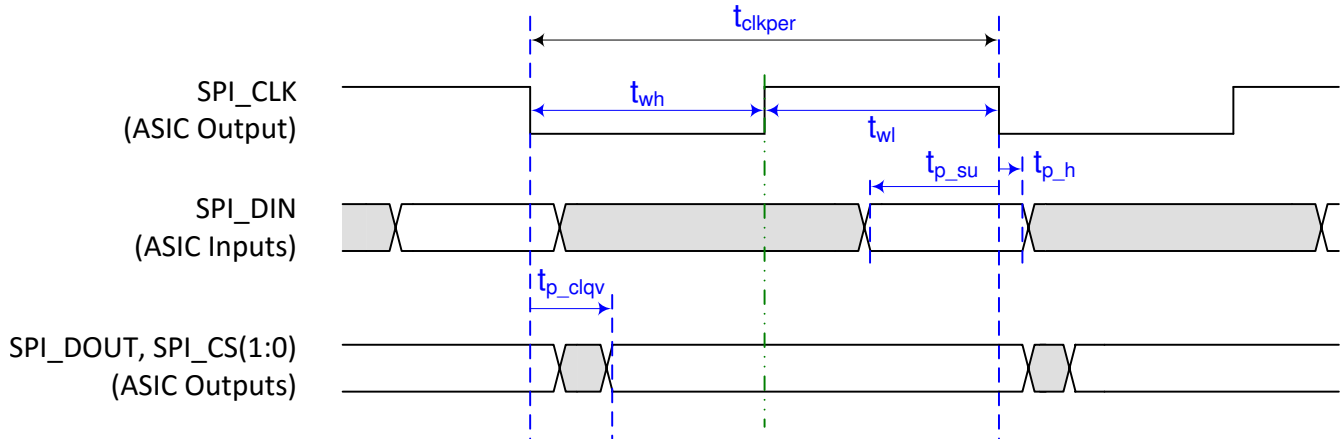


Figure 5-7. Flash Interface Timing

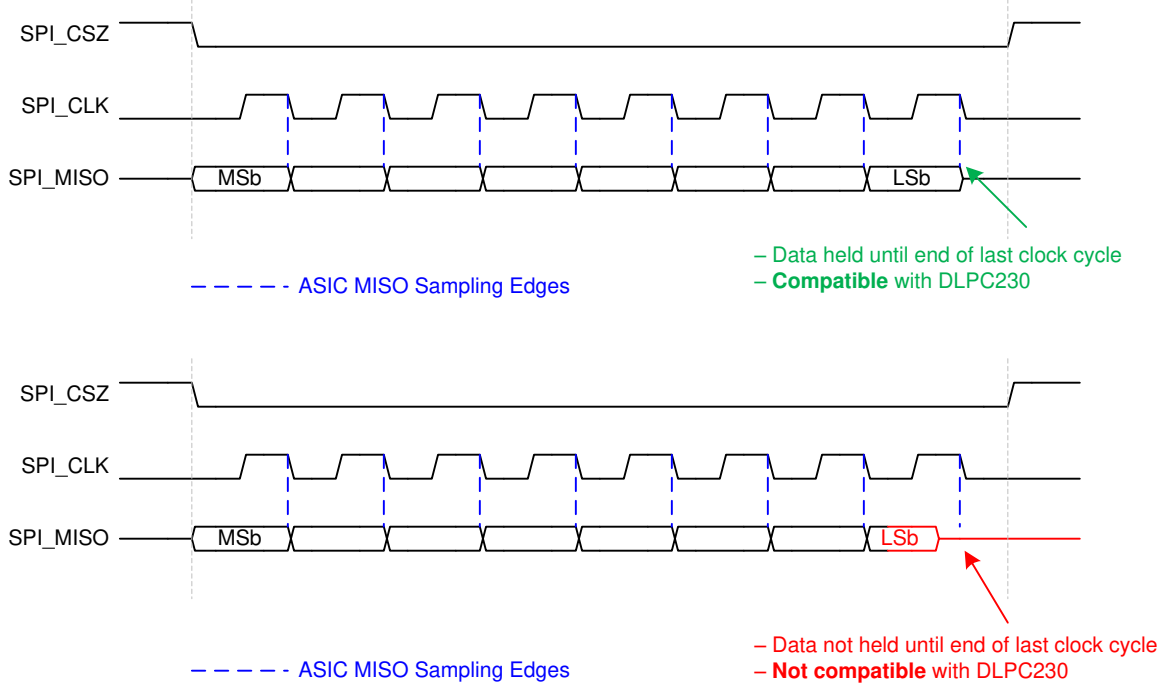


Figure 5-8. Flash Interface Data Capture Requirements

5.19 TPS99000S-Q1 SPI Interface Timing Requirements

The DLPC23xS-Q1 ASIC to TPS99000S-Q1 interface consists of a SPI serial interface.

| (1) | | MIN | MAX | UNIT |
|------------------------|--|-----------------------------|--------|------|
| f_{clock} | Clock frequency, PMIC_SPI_CLK | 9.998 | 30.006 | MHz |
| $t_{\text{p_clkper}}$ | Clock period, PMIC_SPI_CLK (50% reference points) | 33.3 | 100 | ns |
| $t_{\text{p_wh}}$ | Pulse duration high, PMIC_SPI_CLK (50% reference points) | 11.5 | | ns |
| $t_{\text{p_wl}}$ | Pulse duration low, PMIC_SPI_CLK (50% reference points) | 11.5 | | ns |
| t_t | Transition time – all input signals | 20% to 80% reference points | | 6 |
| $t_{\text{p_su}}$ | Setup time – PMIC_SPI_DIN valid before PMIC_SPI_CLK falling edge (50% reference points) | 7.0 | | ns |
| $t_{\text{p_h}}$ | Hold time – PMIC_SPI_DIN valid after PMIC_SPI_CLK falling edge | 50% reference points | | 0.0 |
| $t_{\text{p_clqv}}$ | PMIC_SPI_DOUT output delay (valid) time (with respect to falling edge of PMIC_SPI_CLK or falling edge of PMIC_SPI_CSZ0) (50% reference points) | -3.0 | 3.0 | ns |

- (1) The DLPC23xS-Q1 communicates with the TPS99000S-Q1 using a slight variant of SPI Transfer Mode 0 (that is, clock polarity = 0, clock phase = 0). Instead of capturing MISO data on the clock edge opposite from that used to transmit MOSI data, the DLPC23xS-Q1 captures MISO data on the same clock edge used to transmit the next MOSI data. As such, the DLPC23xS-Q1 SPI interface to the TPS99000S-Q1 requires that MISO data from the TPS99000S-Q1 remain active until the end of the full clock cycle to allow the last data bit to be captured. This is shown in Figure 5-12.

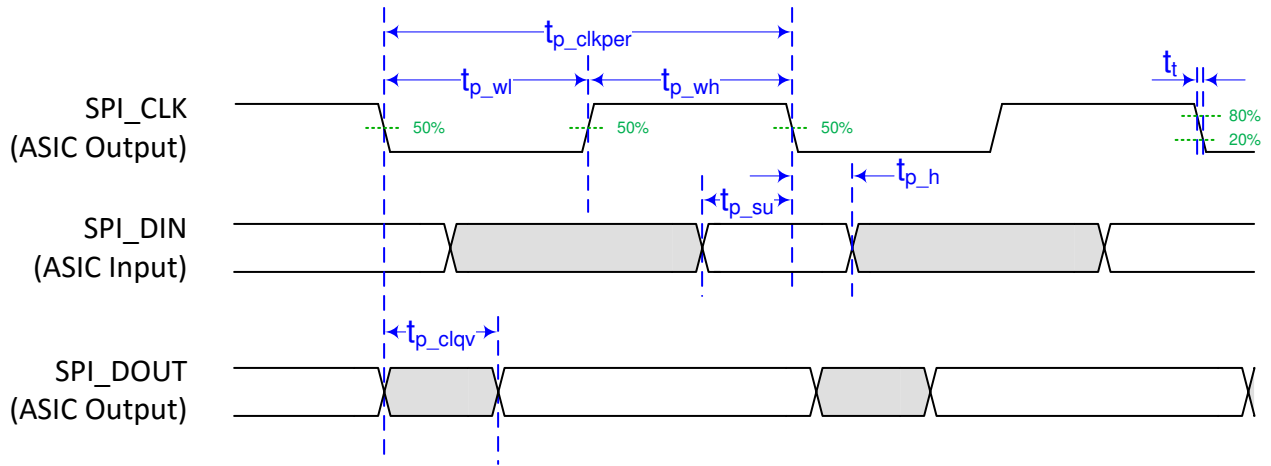


Figure 5-9. TPS99000S-Q1 Interface Timing

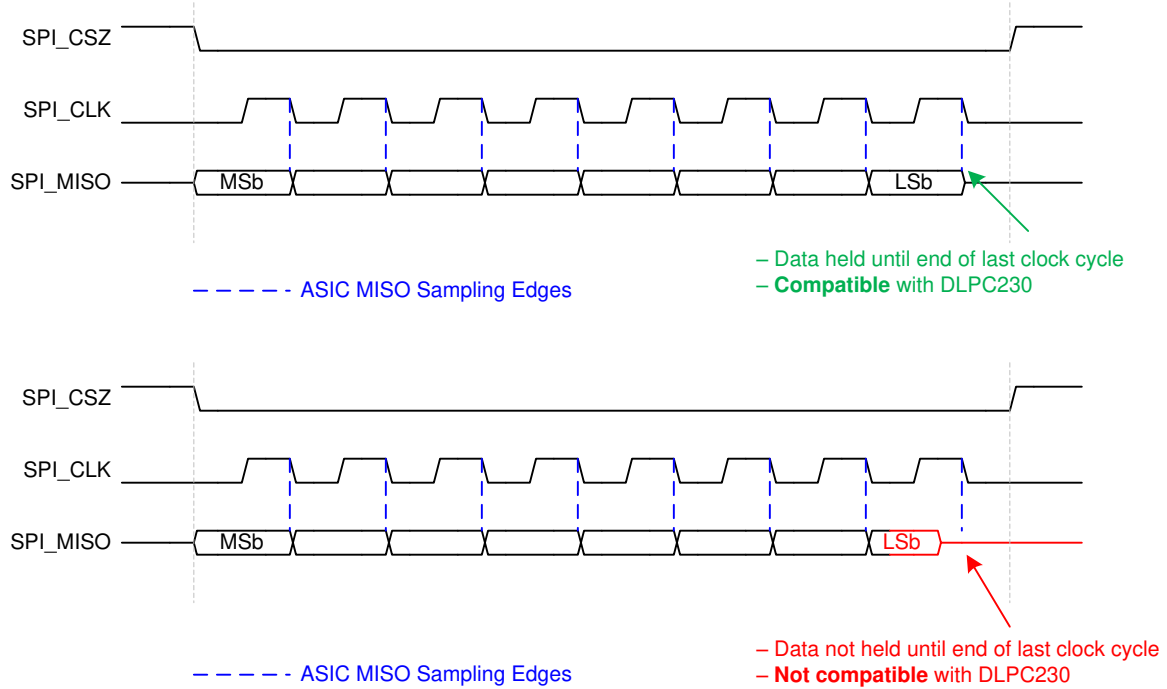


Figure 5-10. TPS99000S-Q1 Interface Data Capture Requirements

5.20 TPS99000S-Q1 AD3 Interface Timing Requirements

The DLPC23xS-Q1 ASIC to TPS99000S-Q1 AD3 interface is used to retrieve ADC measurements from the TPS99000S-Q1. The interface is similar to SPI and includes a clock, MOSI, and MISO signal.

| (1) (2) (3) | | MIN | MAX | UNIT |
|------------------------|--|-----------------------------|--------|------|
| f_{clock} | Clock frequency, PMIC_AD3_CLK | 29.326 | 30.006 | MHz |
| $t_{\text{p_clkper}}$ | Clock period, PMIC_AD3_CLK (50% reference points) | 33.327 | 34.100 | ns |
| $t_{\text{p_wh}}$ | Pulse duration high, PMIC_AD3_CLK (50% reference points) (Referenced to $t_{\text{p_clkper}}$) | 40% | | |
| $t_{\text{p_wl}}$ | Pulse duration low, PMIC_AD3_CLK (50% reference points) (Referenced to $t_{\text{p_clkper}}$) | 40% | | |
| t_{t} | Transition time – all input signals | 20% to 80% reference points | | 6 ns |
| $t_{\text{p_su}}$ | Setup time – PMIC_AD3_MISO valid before PMIC_AD3_CLK rising edge (50% reference points) | 14.5 | | ns |
| $t_{\text{p_h}}$ | Hold time – PMIC_AD3_MISO valid after PMIC_AD3_CLK rising edge (50% reference points) | 0 | | ns |
| $t_{\text{p_clqv}}$ | PMIC_AD3_MOSI output delay (valid) time (with respect to falling edge of PMIC_SPI_CLK) (50% reference points) | -2.0 | 2.0 | ns |

- (1) PMIC_AD3_MOSI ((DLPC23xS-Q1) Output / (TPS99000S-Q1) Input) is transmitted on the falling edge of PMIC_AD3_CLK.
- (2) PMIC_AD3_MISO ((DLPC23xS-Q1) Input / (TPS99000S-Q1) Output) is captured on the rising edge of PMIC_AD3_CLK.
- (3) PMIC_AD3_CLK is used as the primary TPS99000S-Q1 system clock in addition to supporting the AD3 interface.

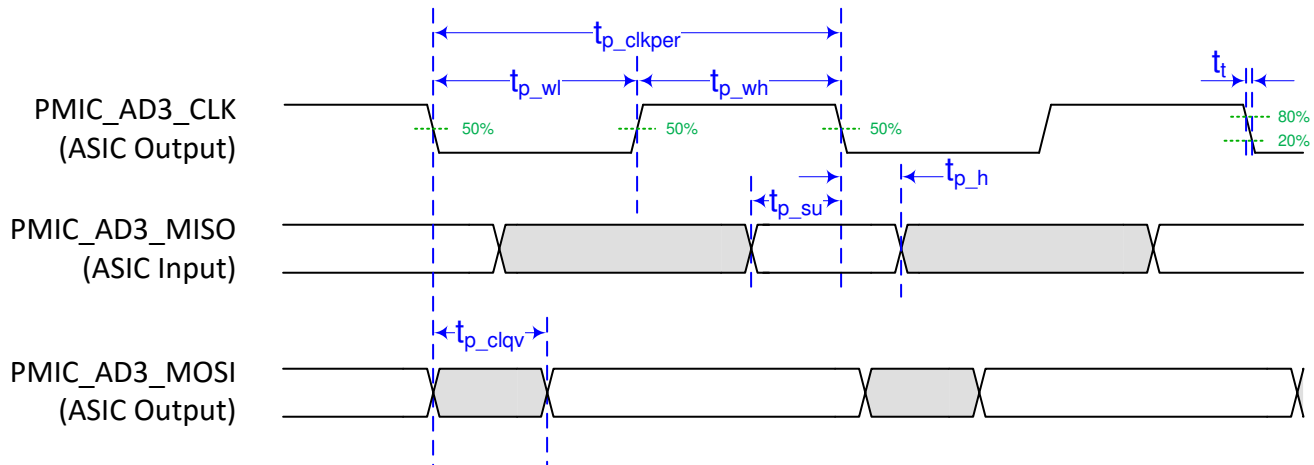


Figure 5-11. TPS99000S-Q1 AD3 Interface Timing

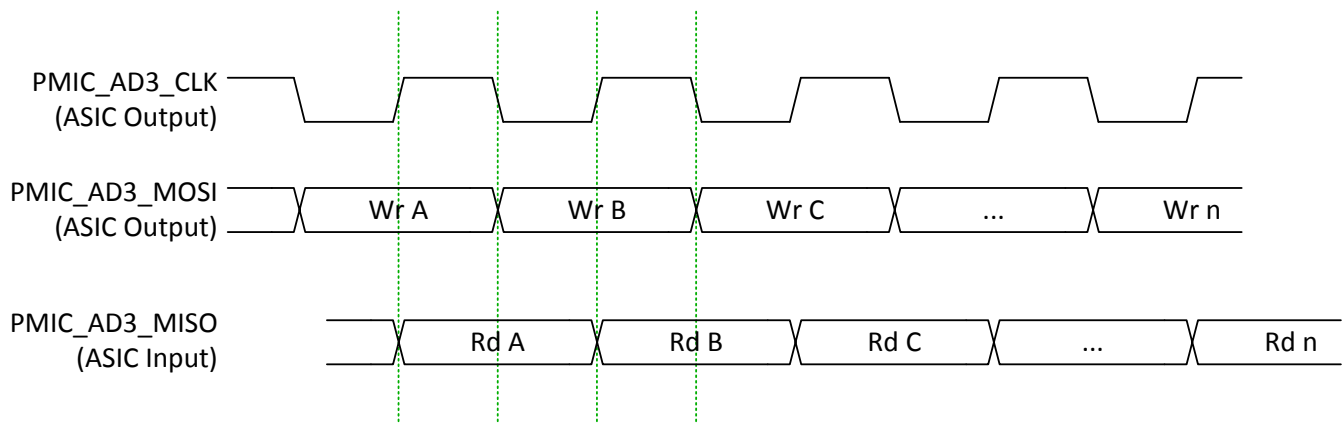


Figure 5-12. TPS99000S-Q1 AD3 Data Capture and Transition

5.21 DLPC23xS-Q1 I²C Port Interface Timing Requirements

The DLPC23xS-Q1 Controller (for example, DLPC23xS-Q1 to TMP411A) I²C port interface timing requirements are shown below.

| | | (1) (2) | MIN | MAX | UNIT |
|--------------------|---|---------------|-----|-----|------|
| f _{clock} | Clock frequency, MSTR_SCL (50% reference points) | Fast-Mode | | 400 | kHz |
| | | Standard Mode | | 100 | |
| C _L | Capacitive Load (for each bus line) | | | 200 | pF |

- (1) Meets all I²C timing per the I²C Bus Specification (except for Capacitive Loading as specified above).
 (2) The maximum clock frequency does not account for rise time, nor added capacitance of PCB or external components, which can adversely impact this value.

5.22 Chipset Component Usage Specification

TI DLP[®] chipsets include a DMD and one or more controllers. Reliable function and operation of TI DMDs requires that they be used in conjunction with all of the other components in the applicable chipset, including those components that contain or implement TI DMD control technology, such as the DLPC23xS-Q1. TI DMD control technology is the TI technology and devices for operating or controlling a DLP[®] products DMD.

6 Parameter Measurement Information

6.1 HOST_IRQ Usage Model

In the DLPC23xS-Q1, the Host_IRQ signal is used to serve as an indication that a serious system error has occurred for which the ASIC has executed an emergency shutdown. The specific errors that precipitated the shutdown can be retrieved through the Host Command and Control interface. The actions that are taken by the ASIC for an emergency shutdown are:

- LEDs are disabled.
- The DMD is parked and powered-down.
- The ASIC operational mode is transitioned to Standby.
- The precipitating errors are captured for later review.
- The Host_IRQ signal is set to a high state.

To recover from an emergency shutdown, the system will require a full power cycle (deassertion of PROJ_ON). The host must obtain the error history from the ASIC prior to this full reset, as the reset will remove all error history from the system.

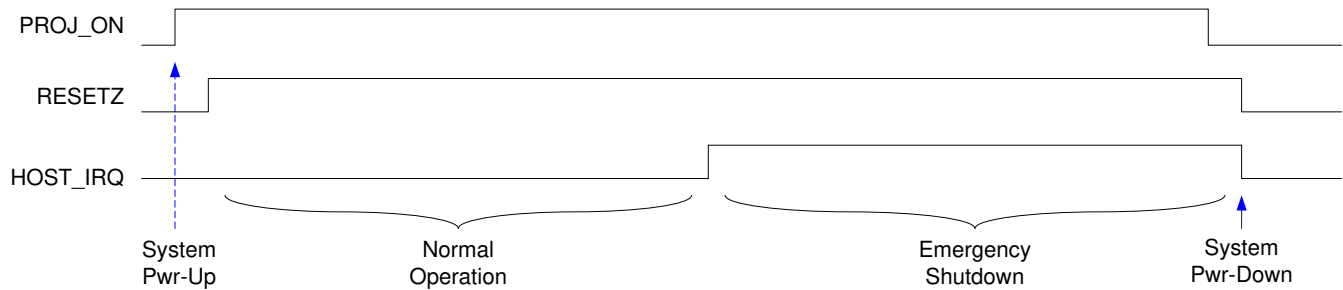


Figure 6-1. Host IRQ Timing

6.2 Input Source

The video input source can be configured to accommodate various desired input resolutions. Image processing such as scaling and line replication can be applied to achieve the necessary display resolution. The desired input resolution can depend on product configuration.

For information on how the input image is displayed, refer to the [DLPC230-Q1, DLPC230S-Q1 Programmer's Guide for Display Applications](#), or [DLPC230-Q1 Programmer's Guide for Light Control Applications](#).

6.2.1 Supported Input Sources

The supported sources with typical timings are shown in [Table 6-1](#). These typical timing examples do not minimize blanking or pixel clock rate. Refer to [Section 5.15](#) for minimum timing specifications.

Table 6-1. Typical Timing for Supported Source Resolutions

| HORIZONTAL RESOLUTION | VERTICAL RESOLUTION | HORIZONTAL BLANKING | | | | VERTICAL BLANKING | | | | VERTICAL RATE (Hz) | PIXEL CLOCK (MHz) |
|-----------------------|---------------------|----------------------|---------------------|---------------------------|----------------------------|----------------------|--------------|--------------------|---------------------|--------------------|-------------------|
| | | TOTAL ⁽¹⁾ | SYNC (PIXEL CLOCKS) | BACK PORCH (PIXEL CLOCKS) | FRONT PORCH (PIXEL CLOCKS) | TOTAL ⁽¹⁾ | SYNC (LINES) | BACK PORCH (LINES) | FRONT PORCH (LINES) | | |
| 576 | 288 | 322 | 8 | 154 | 160 | 181 | 8 | 83 | 90 | 60 | 25.270 |
| 1152 | 576 | 80 | 8 | 32 | 40 | 25 | 8 | 14 | 3 | 60 | 44.426 |
| 1152 | 1152 | 80 | 8 | 32 | 40 | 33 | 8 | 6 | 19 | 60 | 87.595 |
| 480 | 240 | 420 | 32 | 80 | 308 | 230 | 10 | 6 | 214 | 60 | 25.35 |
| 960 | 480 | 240 | 96 | 120 | 24 | 20 | 10 | 7 | 3 | 60 | 36.000 |
| 960 | 960 | 160 | 8 | 80 | 48 | 28 | 10 | 15 | 3 | 60 | 66.250 |
| 1358 | 566 | 92 | 8 | 32 | 52 | 44 | 10 | 31 | 3 | 60 | 53.050 |

Table 6-1. Typical Timing for Supported Source Resolutions (continued)

| HORIZONTAL RESOLUTION | VERTICAL RESOLUTION | HORIZONTAL BLANKING | | | | VERTICAL BLANKING | | | | VERTICAL RATE (Hz) | PIXEL CLOCK (MHz) |
|-----------------------|---------------------|----------------------|---------------------|---------------------------|----------------------------|----------------------|--------------|--------------------|---------------------|--------------------|-------------------|
| | | TOTAL ⁽¹⁾ | SYNC (PIXEL CLOCKS) | BACK PORCH (PIXEL CLOCKS) | FRONT PORCH (PIXEL CLOCKS) | TOTAL ⁽¹⁾ | SYNC (LINES) | BACK PORCH (LINES) | FRONT PORCH (LINES) | | |
| 1220 | 610 | 156 | 8 | 80 | 44 | 19 | 10 | 6 | 3 | 60 | 51.900 |

- (1) Sync clocks/lines are counted as a part of total blanking in these examples (Total Blanking = sync + back porch + front porch). Note that the specifications in [Section 5.15](#) include sync width as part of back porch (Total Blanking = back porch + front porch).

6.2.2 Parallel Interface Supported Data Transfer Formats

- 24-bit RGB888 on a 24 data wire interface

6.2.2.1 OpenLDI Interface Supported Data Transfer Formats

- 1X 24-bit RGB888 on a 5-lane differential interface

Section 6.2.2.1.1 shows the required OpenLDI bus mapping for the supported data transfer formats.

6.2.2.1.1 OpenLDI Interface Bit Mapping Modes

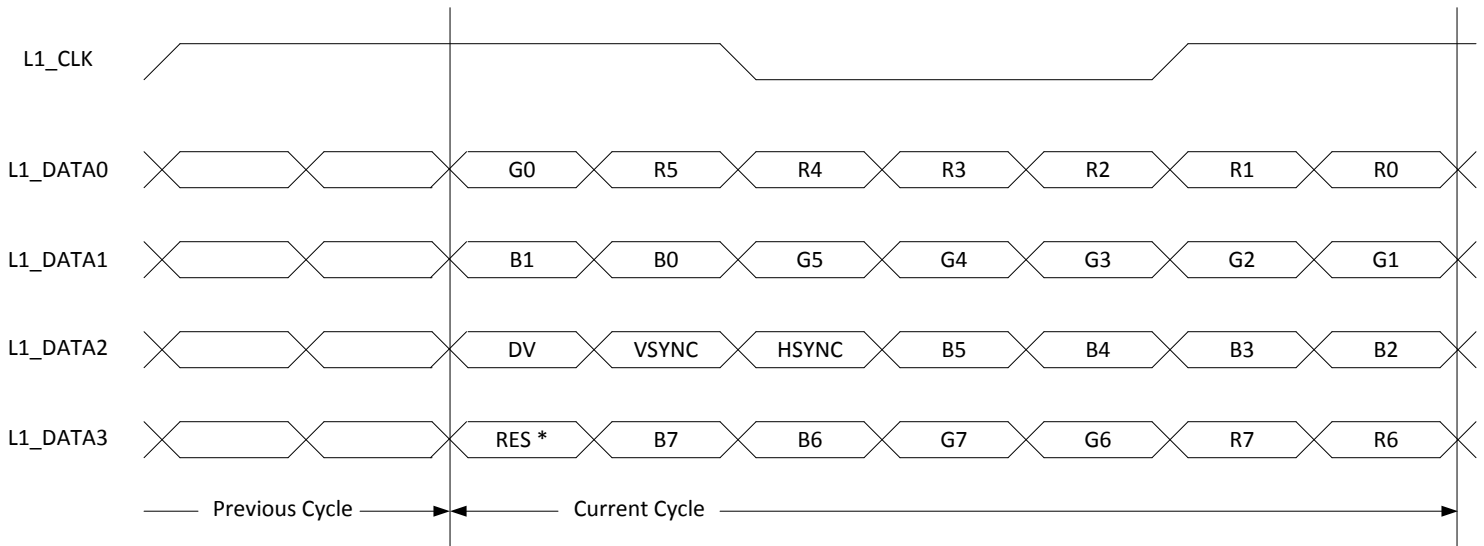


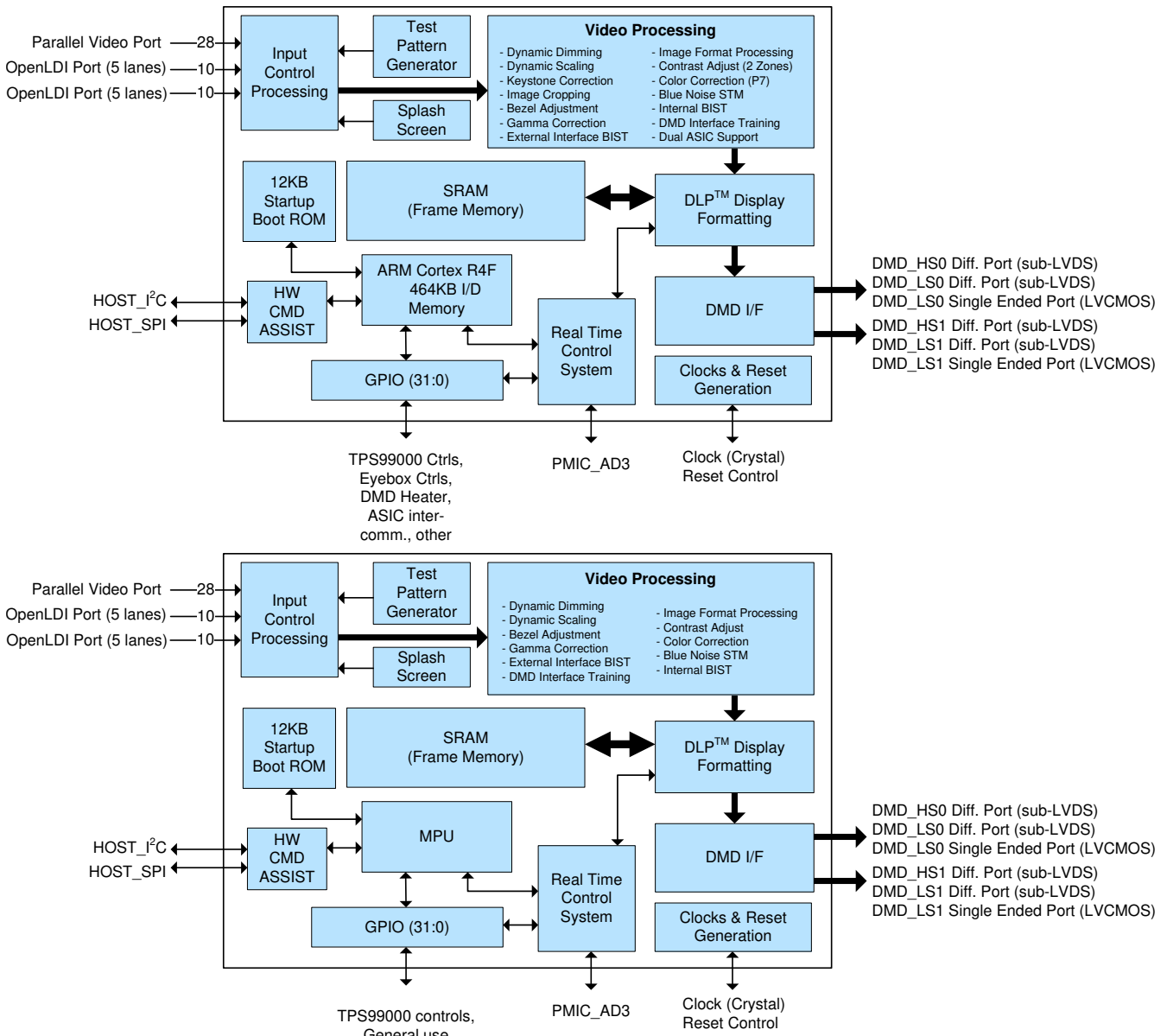
Figure 6-2. OpenLDI 24-bit Single Port

7 Detailed Description

7.1 Overview

The automotive DLP® Products chipset consists of three components – the DMD (DLP5530S-Q1 or DLP462xS-Q1), the DLPC23xS-Q1, and the TPS99000S-Q1. The DLPC23xS-Q1 is the display controller for the DMD - it formats incoming video and controls the timing of the DMD. It also controls TPS99000S-Q1 light source signal timing to coordinate with DMD timing to synchronize light output with DMD mirror movement. The DLPC23xS-Q1 is designed for automotive applications with a wide operating temperature range and diagnostic features to identify and correct specific system-level failures. The DLPC23xS-Q1 provides interfaces such as OpenLDI (video) and SubLVDS (DMD interface) to minimize power consumption and EMI. Applications include head-up display (HUD) and adaptive high beam and smart headlight.

7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 Parallel Interface

The parallel interface complies with standard graphics interface protocol, which includes a vertical sync signal (VSYNC), horizontal sync signal (HSYNC), data valid signal (DATEN), a 24-bit data bus (PDATA_x), and a pixel clock (PCLK). [Figure 5-5](#) shows the relationship of these signals.

Note

VSYNC must remain active at all times. If VSYNC is lost, the DMD must be transitioned to a safe state. When the system detects a VSYNC loss, it will switch to a test pattern or splash image as specified in flash by the Host.

The parallel interface supports intra-interface bit multiplexing (specified in flash) that can help with board layout as needed. The intra-interface bit multiplexing allows the mapping of any PDATA_x input to any internal data bus bit. When utilizing this feature, each unique input pin can only be mapped to one unique destination bit. The typical mapping is shown in [Figure 7-1](#). An example of an alternate mapping is shown in [Figure 7-2](#).

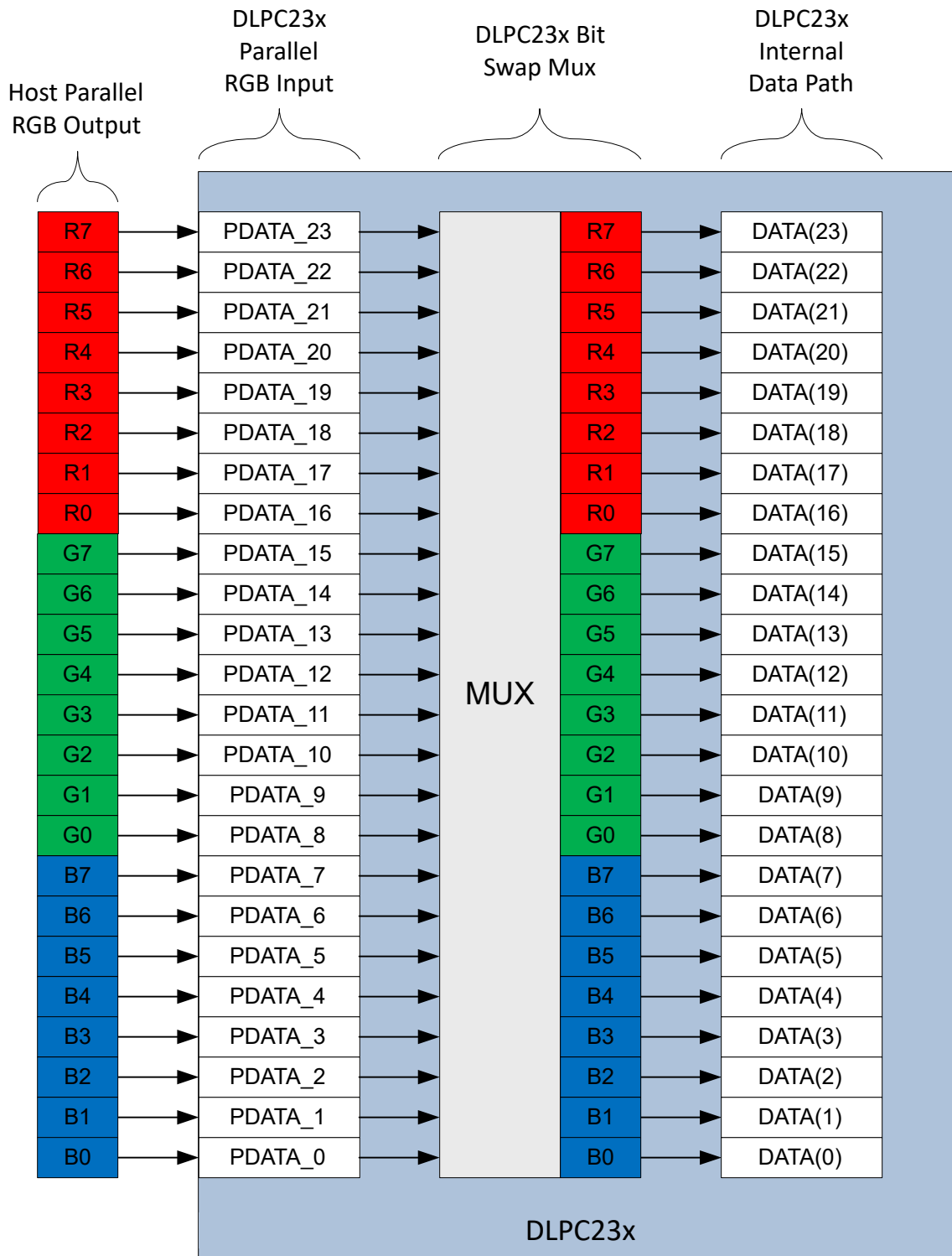


Figure 7-1. Example of Typical Parallel Port Bit Mapping

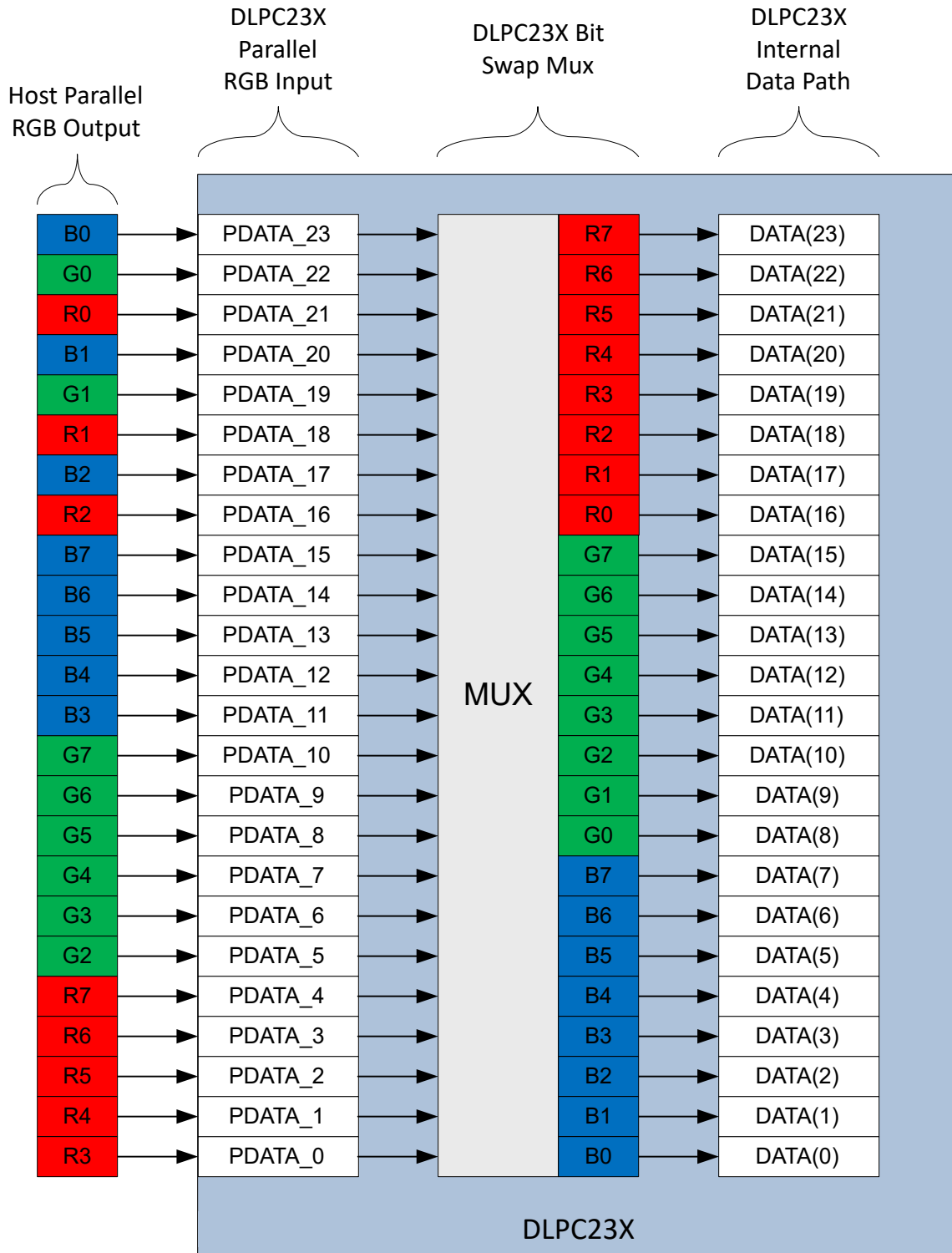


Figure 7-2. Example of Alternate Parallel Port Bit Mapping

7.3.2 OpenLDI Interface

Each DLPC23xS-Q1 OpenLDI interface port supports intra-port lane multiplexing (specified in flash) that can help with board layout as needed. The intra-port multiplexing allows the mapping of any Lx_DATA lane pair to any internal data lane pair. When utilizing this feature, each unique lane pair can only be mapped to one unique

destination lane pair. The typical lane mapping is shown in [Figure 7-3](#). An example of an alternate lane mapping is shown in [Figure 7-4](#).

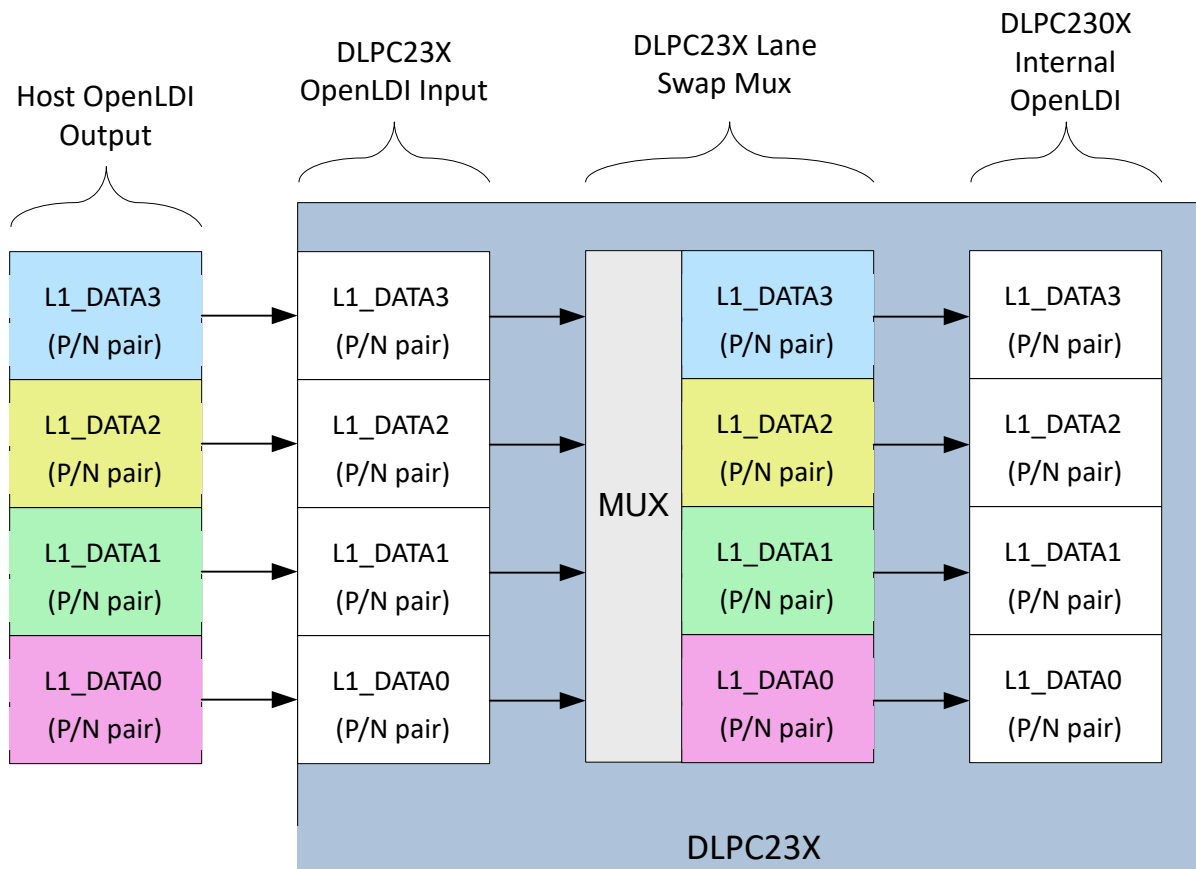


Figure 7-3. Example of Typical OpenLDI Port Lane Mapping

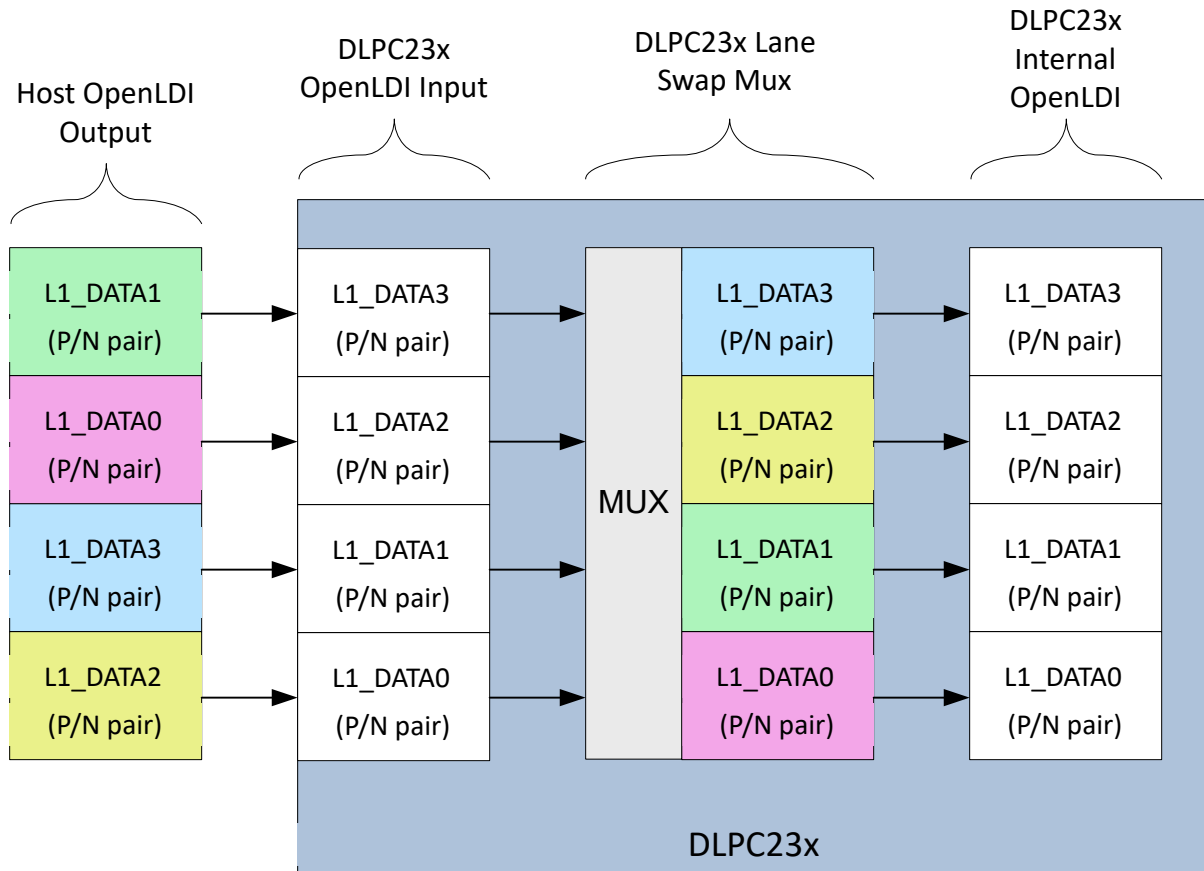


Figure 7-4. Example of Alternate OpenLDI Port Lane Mapping

7.3.3 DMD (SubLVDS) Interface

The DLPC23xS-Q1 ASIC DMD interface supports two high-speed SubLVDS output-only interfaces for data transmission, a single low-speed SubLVDS output-only interface for command write transactions, as well as a low-speed single-ended input interface used for command read transactions. The DLPC23xS-Q1 supports a limited number of DMD interface swap configurations (specified in Flash) that can help board layout by remapping specific combinations of DMD interface lines to other DMD interface lines as needed. [Table 7-1](#) shows some of the options available.

Table 7-1. ASIC to 8-Lane DMD Pin Mapping Options

| DLPC23xS-Q1 ASIC PIN ROUTING OPTIONS TO DMD PINS | | | | |
|--|------------------------------|------------------------------|---|--------------------|
| BASILINE | FULL FLIP HS0/HS1 180 | SWAP HS0 PORT WITH HS1 PORT | SWAP HS0 PORT WITH HS1 PORT AND FULL FLIP 180 | DMD PINS |
| HS0_WDATA0_P HS0_WDATA0_N | HS0_WDATA7_P HS0_WDATA7_N | HS1_WDATA0_P HS1_WDATA0_N | HS1_WDATA7_P HS1_WDATA7_N | D_AP(0) D_AN(0) |
| HS0_WDATA1_P HS0_WDATA1_N | HS0_WDATA6_P HS0_WDATA6_N | HS1_WDATA1_P HS1_WDATA1_N | HS1_WDATA6_P HS1_WDATA6_N | D_AP(1) D_AN(1) |
| HS0_WDATA2_P HS0_WDATA2_N | HS0_WDATA5_P HS0_WDATA5_N | HS1_WDATA2_P HS1_WDATA2_N | HS1_WDATA5_P HS1_WDATA5_N | D_AP(2) D_AN(2) |
| HS0_WDATA3_P HS0_WDATA3_N | HS0_WDATA4_P HS0_WDATA4_N | HS1_WDATA3_P HS1_WDATA3_N | HS1_WDATA4_P HS1_WDATA4_N | D_AP(3) D_AN(3) |
| HS0_WDATA4_P HS0_WDATA4_N | HS0_WDATA3_P HS0_WDATA3_N | HS1_WDATA4_P HS1_WDATA4_N | HS1_WDATA3_P HS1_WDATA3_N | D_AP(4) D_AN(4) |
| HS0_WDATA5_P HS0_WDATA5_N | HS0_WDATA2_P HS0_WDATA2_N | HS1_WDATA5_P HS1_WDATA5_N | HS1_WDATA2_P HS1_WDATA2_N | D_AP(5) D_AN(5) |
| HS0_WDATA6_P HS0_WDATA6_N | HS0_WDATA1_P HS0_WDATA1_N | HS1_WDATA6_P HS1_WDATA6_N | HS1_WDATA1_P HS1_WDATA1_N | D_AP(6) D_AN(6) |
| HS0_WDATA7_P HS0_WDATA7_N | HS0_WDATA0_P HS0_WDATA0_N | HS1_WDATA7_P HS1_WDATA7_N | HS1_WDATA0_P HS1_WDATA0_N | D_AP(7) D_AN(7) |
| HS1_WDATA0_P HS1_WDATA0_N | HS1_WDATA7_P HS1_WDATA7_N | HS0_WDATA0_P HS0_WDATA0_N | HS0_WDATA7_P HS0_WDATA7_N | D_BP(0) D_BN(0) |
| HS1_WDATA1_P HS1_WDATA1_N | HS1_WDATA6_P HS1_WDATA6_N | HS0_WDATA1_P HS0_WDATA1_N | HS0_WDATA6_P HS0_WDATA6_N | D_BP(1) D_BN(1) |
| HS1_WDATA2_P HS1_WDATA2_N | HS1_WDATA5_P HS1_WDATA5_N | HS0_WDATA2_P HS0_WDATA2_N | HS0_WDATA5_P HS0_WDATA5_N | D_BP(2) D_BN(2) |
| HS1_WDATA3_P HS1_WDATA3_N | HS1_WDATA4_P HS1_WDATA4_N | HS0_WDATA3_P HS0_WDATA3_N | HS0_WDATA4_P HS0_WDATA4_N | D_BP(3) D_BN(3) |
| HS1_WDATA4_P HS1_WDATA4_N | HS1_WDATA3_P HS1_WDATA3_N | HS0_WDATA4_P HS0_WDATA4_N | HS0_WDATA3_P HS0_WDATA3_N | D_BP(4) D_BN(4) |
| HS1_WDATA5_P HS1_WDATA5_N | HS1_WDATA2_P HS1_WDATA2_N | HS0_WDATA5_P HS0_WDATA5_N | HS0_WDATA2_P HS0_WDATA2_N | D_BP(5) D_BN(5) |
| HS1_WDATA6_P HS1_WDATA6_N | HS1_WDATA1_P HS1_WDATA1_N | HS0_WDATA6_P HS0_WDATA6_N | HS0_WDATA1_P HS0_WDATA1_N | D_BP(6) D_BN(6) |
| HS1_WDATA7_P HS1_WDATA7_N | HS1_WDATA0_P HS1_WDATA0_N | HS0_WDATA7_P HS0_WDATA7_N | HS0_WDATA0_P HS0_WDATA0_N | D_BP(7) D_BN(7) |

7.3.4 Serial Flash Interface

The DLPC23xS-Q1 uses an external SPI serial flash memory device for configuration and operational data. The minimum supported size is 16 Mb. Larger devices can be required based on operation data and splash image size. The maximum supported size is 128 Mb. It must be noted that the system will support 256 Mb and 512 Mb devices, however, only the first 128 Mb of space are used.

The external serial flash device is supported on a single SPI interface and mostly complies with industry standard SPI flash protocol (See [Figure 5-8](#)). The Host will specify the maximum supported flash interface

frequency (which can be based on device limits, system limits, and/or other factors) and the system will program the closest obtainable value less than or equal to this specified maximum.

The DLPC23xS-Q1 ASIC flash must be connected to the designated SPI flash interface (FLSH_SPI_XXX) to enable support for system initialization, configuration, and operation.

The DLPC23xS-Q1 must support any flash device that is compatible with the modes of operation, features, and performance as defined in this section.

Table 7-2. SPI Flash Required Features or Modes of Operation

| FEATURE | DLPC23xS-Q1 REQUIREMENT | COMMENTS |
|---|--|----------------------------|
| SPI interface width | Single Wire, Two Wire, Four Wire | |
| SPI protocol | SPI mode 0 | |
| Fast READ addressing | Auto-incrementing | |
| Programming mode | Page mode | |
| Page size | 256 Bytes | |
| Sector (or Subsector) size | 4 KB | Required erase granularity |
| Block structure | Uniform sector / Subsector | |
| Block protection bits | 0 = Disabled (with Default = 0 = Disabled) | |
| Status register bit(0) | Write in progress (WIP) {also called flash busy} | |
| Status register bit(1) | Write enable latch (WEN) | |
| Status register bits(6:2) | A value of 0 disables programming protection | |
| Status register bit(7) | Status register write protect (SRWP) | |
| Status register bits(15:8) (expanded status register), or Secondary Status register | The DLPC23xS-Q1 supports multi-byte status registers, as well as separate, additional status registers, but only for specific devices/register addresses. The supported registers and addresses are specified in Table 7-3 . | |

CAUTION

The selected SPI flash device must block repeated status writes from being written to internal register. The boot application writes to the flash device status register once per 256 bytes during programming. Most flash devices discard status register writes when the status content does not change. Some flash parts, such as the Micron N25Q128A13ESFA0F, do not block status writes when the status data is repeated. This causes the status register to exceed its maximum write limit after several programming cycles, making them incompatible with the DLPC23xS-Q1. Note that the main application does not write to the status register.

For each write operation, the DLPC23xS-Q1 boot application executes the following:

1. Write enable command
2. Write status command (to unprotect memory)
3. Read status command to poll the successful execution of the write status (repeated as needed)
4. Write enable command
5. Program or erase command
6. Read status command (repeated as needed) to poll the successful execution of the program or erase operation
7. Write disable command (during programming; this is not performed after erase command.)

For each write operation, the DLPC230S-Q1 main application executes the following:

1. Write enable command
2. Program or erase command
3. Read status command (repeated as needed) to poll the successful execution of the program or erase operation

4. Write disable command (during programming; this is not performed after erase command)

The specific instruction op-code and timing compatibility requirements are listed in [Table 7-3](#) and [Flash Interface Timing Requirements](#). Note that DLPC230S-Q1 does not read the flash's full electronic signature ID and thus cannot automatically adapt protocol and clock rates based on the ID.

Table 7-3. SPI Flash Instruction Op-Code and Access Profile Compatibility Requirements

| SPI FLASH COMMAND | FIRST BYTE (OP-CODE) | SECOND BYTE | THIRD BYTE | FOURTH BYTE | FIFTH BYTE | SIXTH BYTE | NO. OF DUMMY CLOCKS | COMMENTS |
|------------------------------|----------------------|-------------|------------|-------------|------------------------|------------------------|---------------------|------------------------------------|
| Fast READ (1/1) | 0x0B | ADDRS(0) | ADDRS(1) | ADDRS(2) | dummy | DATA(0) ⁽¹⁾ | 8 | See Table 7-4 . |
| Dual READ (1/2) | 0x3B | ADDRS(0) | ADDRS(1) | ADDRS(2) | dummy | DATA(0) ⁽¹⁾ | 8 | See Table 7-4 . |
| 2X READ (2/2) | 0xBB | ADDRS(0) | ADDRS(1) | ADDRS(2) | dummy | DATA(0) ⁽¹⁾ | 4 | See Table 7-4 . |
| Quad READ (1/4) | 0x6B | ADDRS(0) | ADDRS(1) | ADDRS(2) | dummy | DATA(0) ⁽¹⁾ | 8 | See Table 7-4 . |
| 4X READ (4/4) | 0xEB | ADDRS(0) | ADDRS(1) | ADDRS(2) | dummy | DATA(0) ⁽¹⁾ | 6 | See Table 7-4 . |
| Read status | 0x05 | n/a | n/a | STATUS(0) | STATUS(1) | | 0 | Status(1) - Winbond only |
| Write status | 0x01 | STATUS(0) | STATUS(1) | | | | 0 | Status(1) - Winbond only |
| Read Volatile Conf Reg | 0x85 | Data(0) | | | | | 0 | Micron Only |
| Write Volatile Conf Reg | 0x81 | Data(0) | | | | | 0 | Micron Only |
| Write Enable | 0x06 | | | | | | 0 | |
| Write Disable | 0x04 | | | | | | 0 | |
| Page program | 0x02 | ADDRS(0) | ADDRS(1) | ADDRS(2) | DATA(0) ⁽¹⁾ | | 0 | |
| Sector/Subsector Erase (4KB) | 0x20 | ADDRS(0) | ADDRS(1) | ADDRS(2) | | | 0 | |
| Full Chip Erase | 0xC7 | | | | | | 0 | |
| Software Reset Enable | 0x66 | | | | | | | |
| Software Reset | 0x99 | | | | | | | |
| Read Id | 0x9F | Data(0) | Data(1) | Data(2) | | | | System only reads 1st three bytes. |

(1) Only the first data byte is shown, data continues.

More detailed information on the various read operations supported are shown in [Table 7-4](#).

Table 7-4. SPI Flash Supported Read Operation Details

| READ TYPE ⁽²⁾ | NUMBER OF LINES FOR OP-CODE ⁽¹⁾ | NUMBER OF LINES FOR ADDRESS | NUMBER OF LINES FOR DUMMY BYTES | NUMBER OF LINES FOR RETURN DATA |
|--------------------------|--|-----------------------------|---------------------------------|---------------------------------|
| Fast Read (1/1) | 1 | 1 | 1 | 1 |
| Dual Read (1/2) | 1 | 1 | 1 | 2 |
| 2X Read (2/2) | 1 | 2 | 2 | 2 |
| Quad Read (1/4) | 1 | 1 | 1 | 4 |
| 4X Read (4/4) | 1 | 4 | 4 | 4 |

(1) System does not support Read op-codes being spread across more than one data line.

(2) Flash vendors have diverged in naming and controlling their various read capabilities. As such, the Host needs to be very careful to fully understand what is and what is not supported by the DLPC23xS-Q1. In general, for the supported devices, the DLPC23xS-Q1 only supports "Extended SPI" or "SPI Mode" (as defined in the various Flash Data Sheets). It does not support "Dual SPI Mode", "Quad SPI Mode", "QPI", "QPI Mode", "Dual QPI", "Quad QPI", "DTR", or "DDR". If uncertain, most devices will support "Fast Reads" in a manner that is consistent with the DLPC23xS-Q1.

Table 7-5. DLPC23xS-Q1 Compatible SPI Flash Device Options

| DENSITY (M-BITS) ⁽²⁾ ⁽³⁾ | VENDOR | PART NUMBER | PACKAGE SIZE |
|--|-----------------------|-----------------------|--------------|
| 3.3V Compatible Devices | | | |
| 128 | Micron ⁽¹⁾ | MT25QL128ABA8ESF-OAAT | SO16 |
| 128 | Macronix | MX25L12835FMR-10G | SO16 |
| 128 | Macronix | MX25L12845GMR-10G | SO16 |
| 128 | Macronix | MX25L12839FXDQ-10G | BGA25 |

- (1) Care must be used when considering Numonyx versions of Micron serial flash devices as they typically do not have the 4KB sector size needed to be DLPC23xS-Q1 compatible.
- (2) For any devices not listed on this table, special care must be taken to insure that the requirements shown in [Table 7-2](#) and [Table 7-3](#) are met.
- (3) The boot application writes to the flash device status register once per 256 bytes during programming. Most flash devices discard status register writes when the status content does not change. Some flash parts, such as Micron N25Q128A13ESFA0F, do not block status writes when the status data is repeated. This causes the status register to exceed its maximum write limit after several programming cycles, making them incompatible with the DLPC23xS-Q1. Note that the main application does not write to the status register.

While the DLPC23xS-Q1 supports a variety of clock rates and read operation types, it does have a minimum flash read bandwidth requirement which is shown in [Table 7-6](#). This minimum read bandwidth can be met in any number of different ways, with the variables being clock rate and read type. The Host is required to select a flash device which can meet this minimum read bandwidth using the DLPC23xS-Q1 supported interface capabilities. It must be noted that the Host will specify to the system (through flash parameter) the maximum supported clock rate as well as the supported read types for their selected flash device, with which the DLPC23xS-Q1 SW will automatically select an appropriate combination to maximize this bandwidth (which must at least meet the minimum bandwidth requirement assuming a solution exists per the specified parameters).

Table 7-6. SPI Flash Interface Bandwidth Requirements

| PARAMETER | MIN | MAX | UNIT |
|--|-------|-----|------|
| FLSH_RD _{BW} Flash Read Interface Bandwidth | 47.00 | | Mbps |

7.3.5 Serial Flash Programming

The serial flash can be programmed through the DLPC23xS-Q1 using Host commands through the SPI or I²C command and control interface.

7.3.6 Host Command and Diagnostic Processor Interfaces

The DLPC23xS-Q1 provides an interface port for Host commands, as well as an interface port for a *diagnostic processor*. There are two external communication ports dedicated for this use: one SPI interface and one I²C interface. The host specifies (through the ASIC input pin) which port is used for which purpose (for example, Host Command Interface → SPI, therefore "diagnostic processor" → I²C — or they can be reversed).

[Section 5.16](#) shows the timing requirements for the SPI interface. [Section 5.17](#) shows the timing requirements for the I²C interface. The I²C target address pair is 36h/37h.

7.3.7 GPIO Supported Functionality

The DLPC23xS-Q1 provides 32 general purpose I/O that are available to support a variety of functions for a number of different product configurations. In general, most of these I/O will only support one specific function based on a specific product configuration, although that function can be different for a different product configuration. There are also a few of these I/O that have been reserved for use by the Host for whatever function they can require. In addition, most of these I/O can also be made available for TI test and debug use. Definitions for the HUD and Headlight product configurations are shown in [Table 7-7](#) and [Table 7-8](#).

Table 7-7. GPIO Supported Functionality - HUD Product Configuration

| GPIO | SIGNAL NAME | DESCRIPTION ⁽¹⁾ |
|---------|-------------------------|---|
| GPIO_00 | PMIC_CNTRL_OUT (input) | LED control feedback from the TPS99000S-Q1. An external pulldown resistor must be used (connects to TPS99000S-Q1 Drive Enable). |
| GPIO_01 | PMIC_SEQ_STRT (output) | Sequence start output from the DLPC23xS-Q1. This must be connected to the TPS99000S-Q1 to time LED related actions and shadow TPS99000S-Q1 configuration registers. An external pulldown resistor must be used. |
| GPIO_02 | PMIC_COMP_OUT (input) | LED optical comparison feedback. This is used to count light pulses during each frame. This signal is active-low. An external pulldown resistor must be used. |
| GPIO_03 | PMIC_LED_SEN (output) | LED Shunt Enable - shunts current from LEDs to allow faster LED turn-off. An external pulldown resistor must be used. |
| GPIO_04 | PMIC_LED_DEN (output) | LED FET Drive Enable - enables LED current switching and defines LED pulse length. An external pulldown resistor must be used. |
| GPIO_05 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_06 | Host Available | Available for general host use through host commands |
| GPIO_07 | Host Available | Available for general host use through host commands |
| GPIO_08 | Host Available | Available for general host use through host commands |
| GPIO_09 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_10 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_11 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_12 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_13 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_14 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_15 | PMIC_WD1 (output) | Periodic signal that the DLPC23xS-Q1 processor generates during normal operation. TPS99000S-Q1 monitors this signal and reports if this signal stops pulsing. An external pulldown resistor must be used. |
| GPIO_16 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_17 | Host Available | Available for general host use through host commands |
| GPIO_18 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_19 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_20 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_21 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_22 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_23 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_24 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_25 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_26 | Host Available | Available for general host use through host commands |
| GPIO_27 | Host Available | Available for general host use through host commands |
| GPIO_28 | Host Available | Available for general host use through host commands |
| GPIO_29 | Host Available | Available for general host use through host commands |
| GPIO_30 | Host Available | Available for general host use through host commands |
| GPIO_31 | Host Available | Available for general host use through host commands |

(1) TI recommends that all unused Host Available GPIO be configured as a logic '0' output and be left unconnected in the system. If this is not done, an external pulldown resistor ($\leq 10 \text{ k}\Omega$) must be used to avoid floating inputs.

Table 7-8. GPIO Supported Functionality - Headlight Product Configuration

| GPIO | SIGNAL NAME | DESCRIPTION ⁽¹⁾ |
|---------|-------------------------|---|
| GPIO_00 | HL_PWM0 (output) | PWM 0 Output - This can be used for general purposes such as controlling the level of an external light source. |
| GPIO_01 | PMIC_SEQ_STRT (output) | Sequence start output from the DLPC23xS-Q1. This must be connected to the TPS99000S-Q1 to time LED related actions and shadow TPS99000S-Q1 configuration registers. An external pulldown resistor must be used. |
| GPIO_02 | HL_PWM1(output) | PWM 1 Output - This can be used for general purposes such as controlling the level of an external light source. |
| GPIO_03 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_04 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_05 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_06 | Host Available | Available for general host use through host commands |
| GPIO_07 | Host Available | Available for general host use through host commands |
| GPIO_08 | Host Available | Available for general host use through host commands |
| GPIO_09 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_10 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_11 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_12 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_13 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_14 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_15 | PMIC_WD1 (output) | Periodic signal that the DLPC23xS-Q1 processor generates during normal operation. TPS99000S-Q1 monitors this signal and reports if this signal stops pulsing. An external pulldown resistor must be used. |
| GPIO_16 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_17 | HL_PWM2 (output) | PWM 2 Output - This can be used for general purposes such as controlling the level of an external light source. |
| GPIO_18 | EXT_SMPL | Connects to TPS99000S-Q1 EXT_SMPL input. This sequence-aligned signal can be configured to trigger TPS99000S-Q1 ADC sampling. |
| GPIO_19 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_20 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_21 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_22 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_23 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_24 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_25 | Reserved for Future Use | An external pulldown resistor must be used |
| GPIO_26 | Host Available | Available for general host use through host commands |
| GPIO_27 | Host Available | Available for general host use through host commands |
| GPIO_28 | Host Available | Available for general host use through host commands |
| GPIO_29 | Host Available | Available for general host use through host commands |
| GPIO_30 | Host Available | Available for general host use through host commands |
| GPIO_31 | Host Available | Available for general host use through host commands |

(1) TI recommends that all unused Host Available GPIO be configured as a logic '0' output and be left unconnected in the system. If this is not done, an external pulldown resistor ($\leq 10\text{ k}\Omega$) must be used to avoid floating inputs.

7.3.8 Built-In Self Test (BIST)

The DLPC23xS-Q1 provides a significant amount of BIST support to manage the operational integrity of the system. This BIST support is divided into two general BIST types, which are non-periodic and periodic.

Non-periodic BISTs are tests that are typically run one time, and are run outside of normal operation because their activity will disturb the operation of the system. These tests are specified to be run either by a Flash parameter or by a Host command. The Flash parameter specifies which tests are to be run during system power-up and initialization. The Host command is used to select and specify the running of these tests when the system is in Standby Mode (often just before the system is powered down). Some examples of non-periodic tests are: tests for all of the ASIC memories, tests for the main data processing path, and testing of the DMD memory.

Periodic BISTs are tests that are run on an almost continual basis during normal ASIC operation. These tests are managed (set up, enabled, results gathered and evaluated) automatically by the ASIC embedded software. Some examples of periodic tests are: tuning and verification of the DMD High-Speed Interface, input source monitoring (clock, active pixels, active lines), and external video checksum monitoring.

For more information on BISTs, refer to [DLPC230-Q1, DLPC230S-Q1 Programmer's Guide for Display Applications](#), or [DLPC230-Q1 Programmer's Guide for Light Control Applications](#).

7.3.9 EEPROMs

The DLPC23xS-Q1 can optionally use an external I²C EEPROM memory device for storage of calibration data as an alternative to storing calibration data in the SPI flash memory. The EEPROM must be connected to the designated DLPC23xS-Q1 controller I²C interface (MSTR_XXX).

The DLPC23xS-Q1 supports the EEPROM devices listed in [Table 7-9](#).

Table 7-9. DLPC23xS-Q1 Supported EEPROMs

| MANUFACTURER | PART NUMBER | DENSITY (Kb) | PACKAGE SIZE |
|--------------|-------------|--------------|--------------|
| STMicro | M24C64A125 | 64 | S08 |
| STMicro | M24C128A125 | 128 | S08 |
| Atmel | A24C64D | 64 | S08 |
| Atmel | A24C128C | 128 | S08 |

7.3.10 Temperature Sensor

The DLPC23xS-Q1 requires an external temperature sensor (TMP411) to measure the DMD temperature through a remote temperature sense diode residing within the DMD. The DLPC23xS-Q1 also reads the local temperature reported by the TMP411 device. The TMP411 must be connected to the designated DLPC23xS-Q1 controller I²C interface (MSTR_XXX).

The DLPC23xS-Q1 uses an averaged DMD temperature reading to manage the thermal environment and/or operation of the DMD. This management occurs over the full range of temperatures supported by the DMD. This temperature reading is used change sequence operation across the temperature range, and park the DMD when it is operated outside of its allowable temperature specification.

7.3.11 Debug Support

The DLPC23xS-Q1 contains a test point output port, TSTPT_(7:0), which provides the Host with the ability to specify a number of initial system configurations, as well as to provide for ASIC debug support. These test points are tristated while reset is applied, are sampled as inputs approximately 1.5µs after reset is released, and then switch to outputs after the input values have been sampled. The sampled and captured input state for each of these signals is used to configure initial system configurations as specified in the table Pin Functions—Parallel Port Input Data and Control in [Section 4](#).

There are three other signals (JTAGTDO(3:1)) that are sampled as inputs approximately 1.5µs after reset is released, and then switched to outputs. The sampled and captured state for each of these JTAGTDO signals is used to configure the initial test mode output state of the TSTPT_(7:0) signals. [Table 7-10](#) defines the test mode selection for a few programmable output states for TSTPT_(7:0) as defined by JTAGTDO(3:1). For normal use (that is, no debug required), the default state of x111 (using weak internal pullups) must be used to allow for the normal use of these JTAG TDO signals.

To allow TI to make use of this debug capability, a jumper to an external pulldown is recommended for JTAGTDO(3:1).

Table 7-10. Test Mode Selection Scenario Defined by JTAGTDO(3:1)

| TSTPT_(7:0) OUTPUT ⁽¹⁾ | JTAGTDO(3:1) CAPTURED VALUE | |
|-----------------------------------|---|----------------------------|
| | x111 (DEFAULT) (NO SWITCHING ACTIVITY) | x010 CLOCK DEBUG OUTPUT |
| TSTPT(0) | HI-Z | 60MHz |
| TSTPT(1) | HI-Z | 30MHz |
| TSTPT(2) | HI-Z | 7.5MHz |
| TSTPT(3) | HI-Z | LOW |
| TSTPT(4) | HI-Z | 15MHz |
| TSTPT(5) | HI-Z | 60MHz |
| TSTPT(6) | HI-Z | LOW |
| TSTPT(7) | HI-Z | LOW |

(1) These are only the default output selections. Software can reprogram the selection at any time.

7.4 Device Functional Modes

The DLPC23xS-Q1 has three operational modes—Standby, Display, and Calibration—that are enabled through software commands through the host control interface.

7.4.1 Standby Mode

The system will automatically enter Standby mode after power is applied. This is a reduced functional mode that allows Flash update operations and Non-Periodic test operations. The DMD will be parked while the system is operating in this mode and no source can be displayed.

7.4.2 Display Mode

This is the main operational mode of the system. In this mode, normal display activities occur. In this mode the system can display video data and execute periodic BISTs. After system initialization, a host command can be used to transition to this mode from Standby mode. Alternatively, a flash configuration setting can be set to allow the system to automatically transition from standby to display mode after system initialization.

7.4.3 Calibration Mode

This mode is used to calibrate the system's light sources for the desired display properties. For head-up display applications, this includes the ability to adjust individual color light sources to achieve the desired brightness and color point.

8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The DLPC23xS-Q1 is designed to support projection-based automotive applications such as head-up display (HUD) and high resolution headlight.

This DLP® Products chipset consists of three components—the Digital Micromirror Device (DMD), the DLPC23xS-Q1, and the TPS99000S-Q1. The DMD (DLP5530S-Q1 or DLP462xS-Q1) is a light modulator consisting of tiny mirrors that are used to form and project images. The DLPC23xS-Q1 is a controller for the DMD; it formats incoming video sources and controls the timing of the DMD illumination sources and the DMD to display the incoming video source. The TPS99000S-Q1 is a controller for the illumination sources (LEDs or lasers) and a management IC for the entire chipset. In conjunction, the DLPC23xS-Q1 and the TPS99000S-Q1 can also be used for system-level monitoring, diagnostics, and failure detection features.

8.2 Typical Application

8.2.1 Head-Up Display

The figure below shows the system block diagram for a DLP® technology HUD.

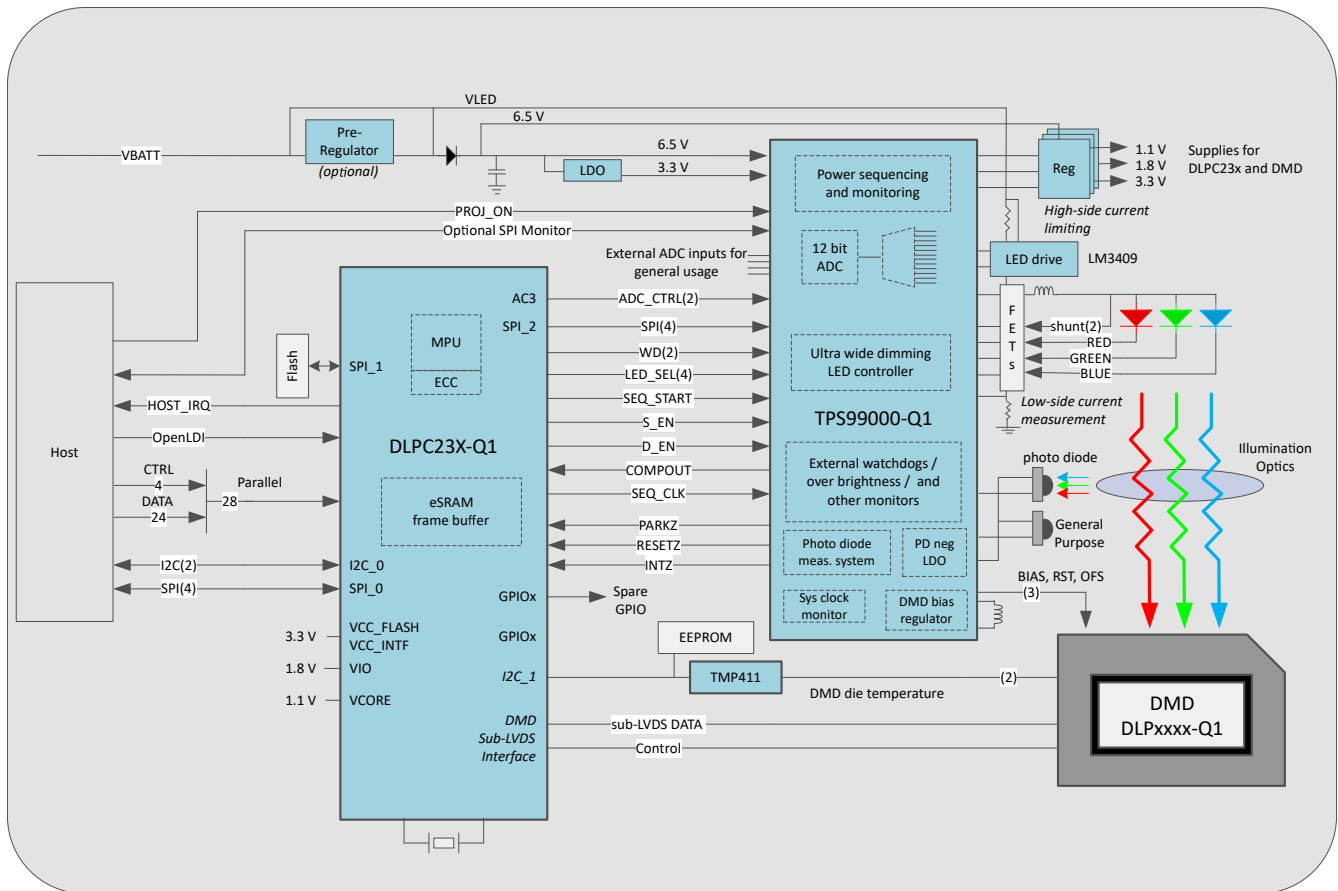


FIGURE 8-1. HUD System Block Diagram

8.2.1.1 Design Requirements

The DLPC23xS-Q1 is a controller for the DMD and the timing of the RGB LEDs in the HUD. It requests the proper timing and amplitude from the LEDs to achieve the requested color and brightness from the HUD across the entire operating range. It synchronizes the DMD with these LEDs to display full-color video content sent by the host.

The DLPC23xS-Q1 receives command and input video data from a host processor in the vehicle. Read and write (R/W) commands can be sent using either the I²C bus or SPI bus. The bus that is not being used for R/W commands can be used as a read-only bus for diagnostic purposes. Input video can be sent over an OpenLDI bus or a parallel 24-bit bus. The SPI flash memory provides the embedded software for the DLPC23xS-Q1's embedded processor, color calibration data, and default settings. The TPS99000S-Q1 provides diagnostic and monitoring information to the DLPC23xS-Q1 using a SPI bus and several other control signals such as PARKZ, INTZ, and RESETZ to manage power-up and power-down sequencing. The DLPC23xS-Q1 interfaces to a TMP411 through I²C for temperature information.

The outputs of the DLPC23xS-Q1 are LED drive information to the TPS99000S-Q1, control signals to the DMD, and monitoring and diagnostics information to the host processor. Based on a host requested brightness and the operating temperature, the DLPC23xS-Q1 determines the proper timing and amplitudes for the LEDs. It passes this information to the TPS99000S-Q1 using a SPI bus and several additional control signals such as D_EN, S_EN, and SEQ_STRT. It controls the DMD mirrors by sending data over a SubLVDS bus. It can alert the host about any critical errors using a HOST_IRQ signal.

The TPS99000S-Q1 is a highly-integrated mixed-signal IC that controls DMD power, the analog response of the LEDs, and provides monitoring and diagnostics information for the HUD system. The power sequencing and monitoring blocks of the TPS99000S-Q1 properly power up the DMD, provide accurate DMD voltage rails, as well as monitor the system's power rails during operation. The integration of these functions into one IC significantly reduces design time and complexity. The highly accurate photodiode (PD) measurement system and the dimming controller block precisely control the LED response. This enables a DLP technology HUD to achieve a very high dimming range (> 5000:1) with accurate brightness and color across the temperature range of the system. Finally, the TPS99000S-Q1 has several general-purpose ADCs that developers can use for system-level monitoring, such as over-brightness detection.

The TPS99000S-Q1 receives inputs from the DLPC23xS-Q1, power rail voltages for monitoring, a photodiode that is used to measure LED response, the host processor, and potentially several other ADC ports. The DLPC23xS-Q1 sends commands to the TPS99000S-Q1 over a SPI port and several other control signals. The TPS99000S-Q1 includes watchdogs to monitor the DLPC23xS-Q1 and verify it is operating as expected. The power rails are monitored by the TPS99000S-Q1 to detect power failures or glitches and request a proper power down of the DMD in case of an error. The photodiode's current is measured and amplified using a transimpedance amplifier (TIA) within the TPS99000S-Q1. The host processor can read diagnostics information from the TPS99000S-Q1 using a dedicated SPI bus, adding an independent monitoring path from the host processor. Additionally the host can request the system to be turned on or off using a PROJ_ON signal. The TPS99000S-Q1 has several general-purpose ADCs that can be used to implement other system features such as over-brightness and over-temperature detection.

The outputs of the TPS99000S-Q1 are LED drive signals, diagnostic information, and error alerts to the DLPC23xS-Q1. The TPS99000S-Q1 has signals connected to the LM3409 buck controller for high power LEDs and to discrete hardware that control the LEDs. The TPS99000S-Q1 can output diagnostic information to the host and the DLPC23xS-Q1 over two SPI buses. It also has signals such as RESETZ, PARKZ, and INTZ that can be used to trigger power down or reset sequences.

The DMD is a micro-electro-mechanical system (MEMS) device that receives electrical signals as an input (video data) and produces a mechanical output (mirror position). The electrical interface to the DMD is a SubLVDS interface driven with the DLPC23xS-Q1. The mechanical output is the state of more than 1.3 million mirrors in the DMD array that can be tilted $\pm 12^\circ$. In a projection system, the mirrors are used as pixels to display an image.

8.3 Power Supply Recommendations

8.3.1 Power Supply Management

The TPS99000S-Q1 manages power for the DLPC23xS-Q1 and DMD. See [Section 5.12](#) for all power sequencing and timing requirements.

8.3.2 Hot Plug Usage

The DLPC23xS-Q1 does not support Hot Plug use (for itself or for any DMD connected to the system). As such, the system must always be powered down prior to removal of the ASIC or DMD from any system.

8.3.3 Power Supply Filtering

The following filtering circuits are recommended for the various supply inputs. High frequency 0.1- μ F capacitors must be evenly distributed amongst the power balls and placed as close to the power balls as possible.

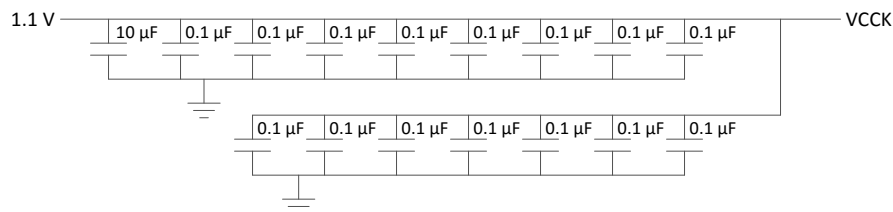


Figure 8-2. VCKK Recommended Filter

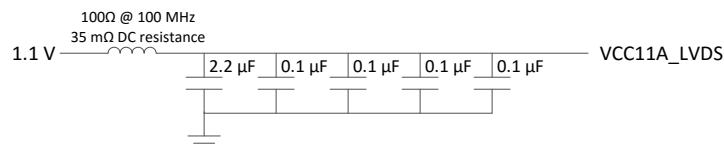


Figure 8-3. VCC11A_LVDS Recommended Filter

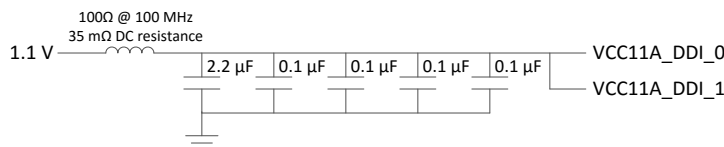


Figure 8-4. VCC11A_DDI Recommended Filter

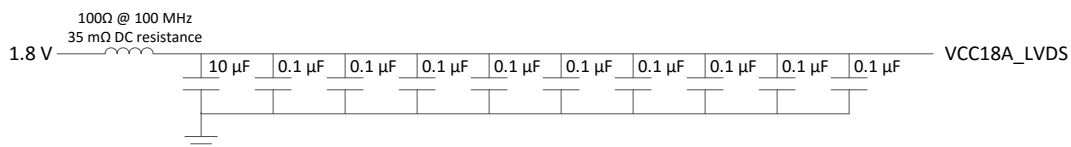


Figure 8-5. VCC18A_LVDS Recommended Filter

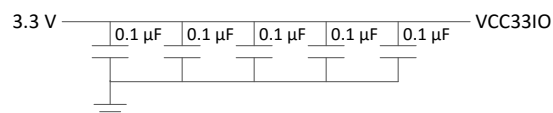


Figure 8-6. VCC33IO Recommended Filter

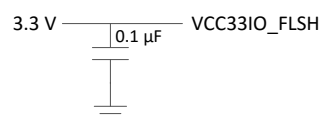


Figure 8-7. VCC33IO_FLSH Recommended Filter

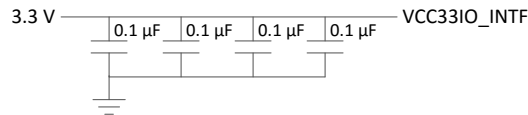


Figure 8-8. VCC33IO_INTF Recommended Filter

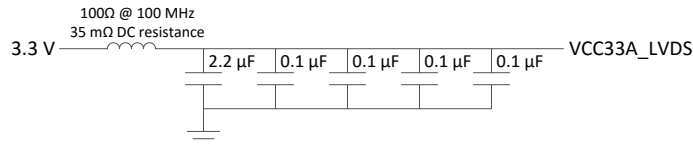


Figure 8-9. VCC33A_LVDS Recommended Filter

8.4 Layout

8.4.1 Layout Guidelines

8.4.1.1 PCB Layout Guidelines for Internal ASIC PLL Power

The following guidelines are recommended to achieve desired ASIC performance relative to the internal PLL. The DLPC23xS-Q1 contains two internal PLLs that have dedicated analog supplies (VCC11AD_PLLM, GND11AD_PLLM, VCC11AD_PLLD, GND11AD_PLLD). At a minimum, VCC11AD_PLLx power and GND11AD_PLLx ground pins must be isolated using a simple passive filter consisting of two series ferrites and two shunt capacitors (to widen the spectrum of noise absorption). Recommended values and layout are shown in [Table 8-1](#) and [Figure 8-10](#) respectively.

Table 8-1. Recommended PLL Filter Components

| COMPONENT | PARAMETER | RECOMMENDED VALUE | UNIT |
|-----------------|----------------------|-------------------|------|
| Shunt Capacitor | Capacitance | 0.1 | μF |
| Shunt Capacitor | Capacitance | 1.0 | μF |
| Series Ferrite | Impedance at 100 MHz | > 100 | Ω |
| | DC Resistance | < 0.40 | |

Because the PCB layout is critical to PLL performance, it is vital that the quiet ground and power are treated like analog signals. Additional design guidelines are as follows:

- All four components must be placed as close to the ASIC as possible.
- It is especially important to keep the leads of the high frequency capacitors as short as possible.
- A capacitor of each value must be connected across VCC11AD_PLLM / GND11AD_PLLM and VCC11AD_PLLD / GND11AD_PLLD respectively on the ASIC side of the ferrites.
- VCC11AD_PLLM and VCC11AD_PLLD must be a single trace from the DLPC23xS-Q1 to both capacitors and then through the series ferrites to the power source.
- The power and ground traces must be as short as possible, parallel to each other, and as close as possible to each other.

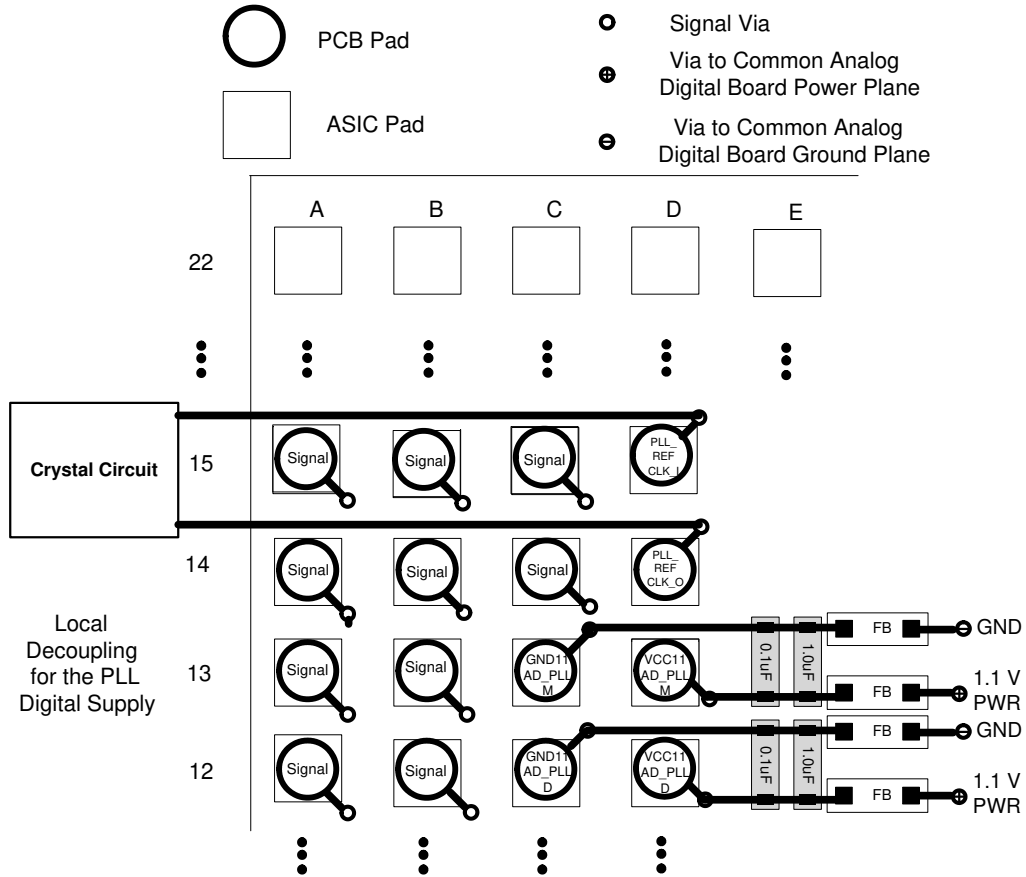


Figure 8-10. DLPC230S-Q1 PLL Filter Layout

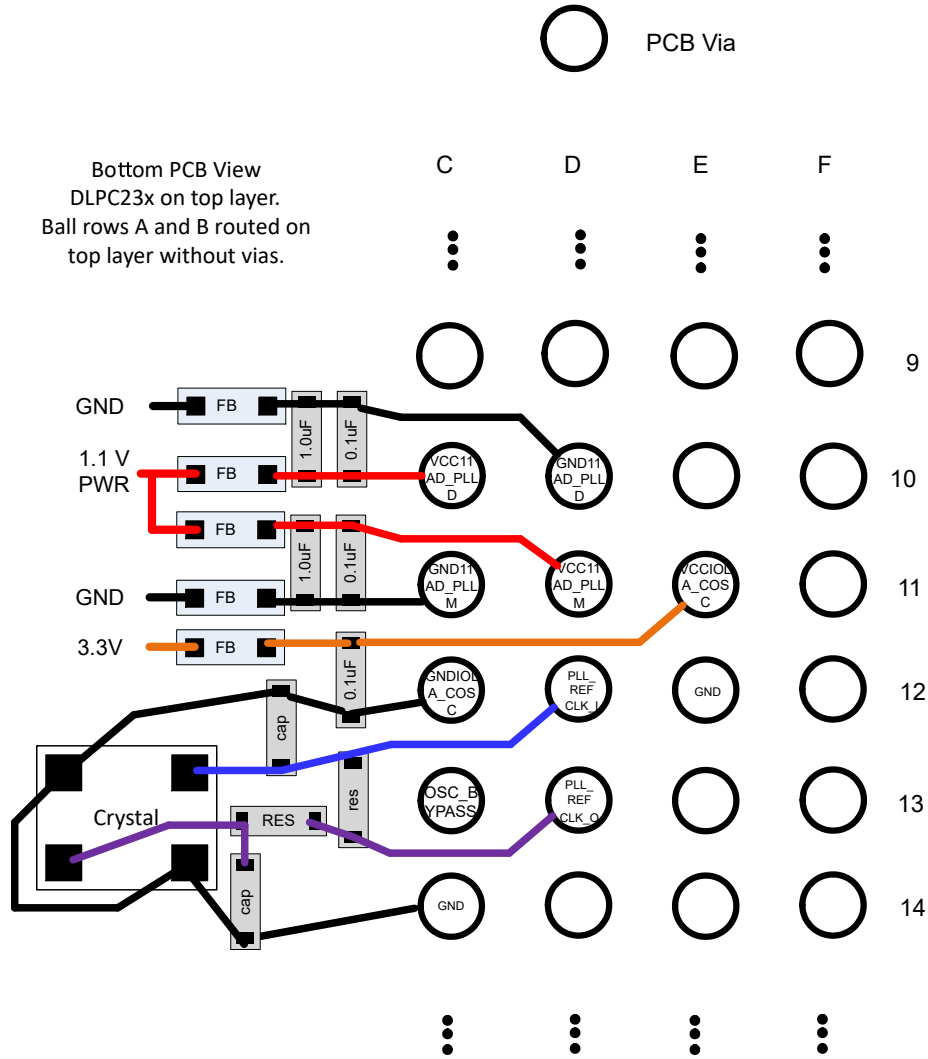
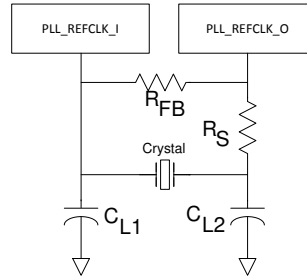


Figure 8-11. DLPC231S-Q1 PLL Filter & Crystal Layout

8.4.1.2 DLPC23xS-Q1 Reference Clock

The DLPC23xS-Q1 requires an external reference clock to feed its internal PLL. A crystal or oscillator can supply this reference. The recommended crystal configurations and reference clock frequencies are listed in [Table 8-2](#), with additional required discrete components shown in [Figure 8-12](#) and defined in [Table 8-2](#).



- A. C_L = Crystal load capacitance
- B. R_{FB} = Feedback Resistor

Figure 8-12. Discrete Components Required When Using Crystal

8.4.1.2.1 Recommended Crystal Oscillator Configuration

Table 8-2. Recommended Crystal Configuration

| PARAMETER | RECOMMENDED | UNIT |
|---|---|------|
| Crystal circuit configuration | Parallel resonant | |
| Crystal type | Fundamental (first harmonic) | |
| Crystal nominal frequency | 16 | MHz |
| Crystal frequency tolerance (including accuracy, temperature, aging and trim sensitivity) | ±200 | PPM |
| Maximum crystal equivalent series resistance (ESR) | 50 | Ω |
| Crystal load capacitance | 10 | pF |
| Temperature range | –40°C to +105°C | °C |
| Drive level (nominal) | 100 | μW |
| R_{FB} feedback resistor (nominal) | 1 | MΩ |
| C_{L1} external crystal load capacitor | See equation in ⁽¹⁾ | pF |
| C_{L2} external crystal load capacitor | See equation in ⁽²⁾ | pF |
| PCB layout | A ground isolation ring around the crystal is recommended | |

- (1) $CL1 = 2 \times (CL - Cstray_pll_refclk_i)$, where: $Cstray_pll_refclk_i$ = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_i .
- (2) $CL2 = 2 \times (CL - Cstray_pll_refclk_o)$, where: $Cstray_pll_refclk_o$ = Sum of package and PCB stray capacitance at the crystal pin associated with the ASIC pin pll_refclk_o .

The crystal circuit in the DLPC23xS-Q1 ASIC has dedicated power ($VCC3IO_COSC$) and ground ($GNDIOLA_COSC$) pins, with the recommended filtering shown in [Figure 8-13](#).

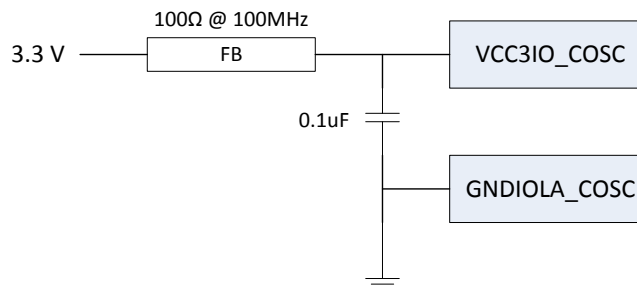


Figure 8-13. Crystal Power Supply Filtering

Table 8-3. DLPC23xS-Q1 Recommended Crystal Parts

| MANUFACTURER | PART NUMBER | SPEED | FREQUENCY TOLERANCE, FREQUENCY STABILITY, AGING/YEAR | ESR | LOAD CAPACITANCE | OPERATING TEMPERATURE |
|--------------|---------------------------|--------|--|----------|------------------|-----------------------|
| TXC | AM16070006 ⁽¹⁾ | 16 MHz | Freq Tolerance: ±10 ppm | 50-Ω max | 10 pF | -40°C to +125°C |
| | | | Freq Stability: ±50 ppm | | | |
| | | | Aging/Year: ±3 ppm | | | |

(1) This device requires a 3-kΩ series resistor to limit power.

If an external oscillator is used, the oscillator output must drive the PLL_REFCLK_O pin on the DLPC23xS-Q1 ASIC, the PLL_REFCLK_I pin must be left unconnected, and the OSC_BYPASS pin must = logic HIGH.

8.4.1.3 DMD Interface Layout Considerations

The DLPC23xS-Q1 ASIC subLVDS HS/LS differential interface waveform quality and timing is dependent on the total length of the interconnect system, the spacing between traces, the characteristic impedance, etch losses, and how well matched the lengths are across the interface. Thus, ensuring positive timing margin requires attention to many factors.

DLPC23xS-Q1 I/O timing parameters as well as DMD I/O timing parameters can be found in their corresponding data sheets. Similarly, PCB routing mismatch can be budgeted and met through controlled PCB routing. PCB design recommendations are provided in [Table 8-4](#) and [Figure 8-14](#) as a starting point for the customer.

Table 8-4. PCB Recommendations for DMD Interface

| PARAMETER ^{(1) (2)} | | MIN | MAX | UNIT |
|------------------------------|------------------------------|--|-----|------|
| T _W | Trace Width | 4 | | mils |
| T _S | Intra-lane Trace Spacing | 4 | | mils |
| T _{SPP} | Inter-lane Trace Spacing | 2 * (T _S + T _W) | | mils |
| R _{BGR} | Resistor - Bandgap Reference | 42.2 (1%) | | kΩ |

- (1) Recommendations to achieve the desired nominal differential impedance as specified by Tx_{load} in [Section 5.7](#) and [Section 5.8](#).
- (2) If using the minimum trace width and spacing to escape the ASIC ball field, widening these out after escape can be desirable if practical to achieve the target 100-Ω impedance (e.g. to reduce transmission line losses).

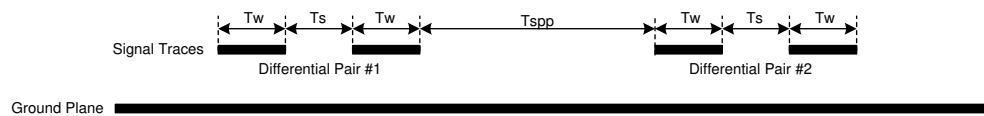


Figure 8-14. DMD Differential Layout Recommendations

8.4.1.4 General PCB Recommendations

TI recommends the following to achieve good thermal connectivity:

- A minimum of four power and ground planes
 - ZDQ package = 1oz copper power planes and 2oz copper ground planes
 - ZEK package = 1oz copper power planes and 1oz copper ground planes
- A copper plane beneath the thermal ball array containing a via farm with the following attributes
 - Copper plane area (top side of PCB, under package)
 - ZDQ package = 8.0mm × 8.0mm
 - ZEK package = 4.8mm × 4.8mm
 - Copper plane area (bottom side of PCB, opposite of package)
 - ZDQ package = 6.0mm × 6.0mm
 - ZEK package = 4.8mm × 4.8mm
 - Thermal via quantity
 - ZDQ package = 7 × 7 array of vias
 - ZEK package = 5 × 5 array of vias
 - Thermal via size
 - ZDQ package = 0.25mm (10 mils)
 - ZEK package = 0.203mm (8 mils)
 - Thermal via plating thickness
 - ZDQ package = 0.05mm (2 mils) wall thickness
 - ZEK package = 0.025mm (1 mils) wall thickness
- PCB copper coverage per layer
 - Power and ground layers: 90% minimum coverage
 - Top/bottom signal layers (ground fill to achieve coverage): 70% minimum coverage with 1.5oz copper

8.4.1.5 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, TI recommends that unused ASIC input pins be tied through a pullup resistor to its associated power supply or a pulldown to ground unless specifically noted otherwise in [Section 4](#) . For ASIC inputs with internal pullup or pulldown resistors, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Note that internal pullup and pulldown resistors are weak and must not be expected to drive the external line. When external pullup or pulldown resistors are needed for pins that have built-in weak pullups or pulldowns, use the value specified in [Table 4-11](#).

Unused output-only pins must never be tied directly to power or ground, but can be left open.

When possible, TI recommends that unused bidirectional I/O pins be configured to their output state such that the pin can be left open. If this control is not available and the pins can become an input, then they must be pulled up (or pulled down) using an appropriate, dedicated resistor.

8.4.1.6 Maximum Pin-to-Pin, PCB Interconnects Etch Lengths

Table 8-5. Max Pin-to-Pin PCB Interconnect Recommendations—DMD

| ASIC INTERFACE | SIGNAL INTERCONNECT TOPOLOGY ^{(1) (2)} | | UNIT |
|--------------------------------|---|-----------------------------------|------------|
| | SINGLE BOARD SIGNAL ROUTING LENGTH | MULTI-BOARD SIGNAL ROUTING LENGTH | |
| DMD_HS0_CLK_P DMD_HS0_CLK_N | 6.0 (152.4) | See ⁽³⁾ | in (mm) |

Table 8-5. Max Pin-to-Pin PCB Interconnect Recommendations—DMD (continued)

| ASIC INTERFACE | SIGNAL INTERCONNECT TOPOLOGY ^{(1) (2)} | | UNIT |
|--------------------------------------|---|-----------------------------------|------------|
| | SINGLE BOARD SIGNAL ROUTING LENGTH | MULTI-BOARD SIGNAL ROUTING LENGTH | |
| DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N | 6.0 (152.4) | See ⁽³⁾ | in (mm) |
| DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N | | | |
| DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N | | | |
| DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N | | | |
| DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N | | | |
| DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N | | | |
| DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N | | | |
| DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N | | | |
| DMD_HS1_CLK_P DMD_HS1_CLK_N | 6.0 (152.4) | See ⁽³⁾ | in (mm) |
| DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N | 6.0 (152.4) | See ⁽³⁾ | in (mm) |
| DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N | | | |
| DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N | | | |
| DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N | | | |
| DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N | | | |
| DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N | | | |
| DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N | | | |
| DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N | | | |
| DMD_LS0_CLK_P DMD_LS0_CLK_N | 6.5 (165.1) | See ⁽³⁾ | in (mm) |
| DMD_LS0_WDATA_P DMD_LS0_WDATA_N | 6.5 (165.1) | See ⁽³⁾ | in (mm) |
| DMD_LS0_RDATA | 6.5 (165.1) | See ⁽³⁾ | in (mm) |
| DMD_LS1_RDATA | 6.5 (165.1) | See ⁽³⁾ | in (mm) |
| DMD_DEN_ARSTZ | N/A | N/A | in (mm) |

(1) Max signal routing length includes escape routing.

(2) Multi-board DMD routing length is more restricted due to the impact of the connector.

(3) Due to board variations, these are impossible to define. Any board designs must SPICE simulate with the ASIC IBIS models to verify signal routing lengths do not exceed requirements.

Table 8-6. Max Pin-to-Pin PCB Interconnect Recommendations - TPS9900S-Q1

| ASIC INTERFACE | SIGNAL INTERCONNECT TOPOLOGY ^{(1) (2)} | | UNIT |
|----------------|---|-----------------------------------|------------|
| TPS9900S-Q1 | SINGLE BOARD SIGNAL ROUTING LENGTH | MULTI-BOARD SIGNAL ROUTING LENGTH | |
| PMIC_LEDSEL(3) | 6.0 (152.4) | See ⁽³⁾ | in (mm) |
| PMIC_LEDSEL(2) | | | |
| PMIC_LEDSEL(1) | | | |
| PMIC_LEDSEL(0) | | | |
| PMIC_ADC3_CLK | | | |
| PMIC_ADC3_MOSI | | | |
| PMIC_ADC3_MISO | | | |
| PMIC_SEQ_STRT | | | |

(1) Max signal routing length includes escape routing.

(2) Multiboard DMD routing length is more restricted due to the impact of the connector.

(3) Due to board variations, these are impossible to define. Any board designs must SPICE simulate with the ASIC IBIS models to verify signal routing lengths do not exceed requirements.

Table 8-7. High-Speed PCB Signal Routing Matching Requirements

| SIGNAL GROUP LENGTH MATCHING ^{(1) (2)} | | | | | |
|---|--------------------------------------|--------------------------------|---------------------|-----------------------------|------------|
| INTERFACE | SIGNAL GROUP | REFERENCE SIGNAL | MAX MISMATCH ZDQ324 | MAX MISMATCH ZEK324 | UNIT |
| DMD ⁽³⁾ | DMD_HS0_WDATA0_P DMD_HS0_WDATA0_N | DMD_HS0_CLK_P DMD_HS0_CLK_N | ±1.0 (±25.4) | ±1.0 (±25.4) | in (mm) |
| | DMD_HS0_WDATA1_P DMD_HS0_WDATA1_N | | | | |
| | DMD_HS0_WDATA2_P DMD_HS0_WDATA2_N | | | | |
| | DMD_HS0_WDATA3_P DMD_HS0_WDATA3_N | | | | |
| | DMD_HS0_WDATA4_P DMD_HS0_WDATA4_N | | | | |
| | DMD_HS0_WDATA5_P DMD_HS0_WDATA5_N | | | | |
| | DMD_HS0_WDATA6_P DMD_HS0_WDATA6_N | | | | |
| | DMD_HS0_WDATA7_P DMD_HS0_WDATA7_N | | | | |
| DMD ⁽⁴⁾ | DMD_HS0_x_P | DMD_HS0_x_N | ±0.025 (±0.635) | 0.0315±0.025 (0.8±0.635) | in (mm) |

Table 8-7. High-Speed PCB Signal Routing Matching Requirements (continued)

| SIGNAL GROUP LENGTH MATCHING ⁽¹⁾ ⁽²⁾ | | | | | |
|--|---|--------------------------------|---------------------|--|------------|
| INTERFACE | SIGNAL GROUP | REFERENCE SIGNAL | MAX MISMATCH ZDQ324 | MAX MISMATCH ZEK324 | UNIT |
| DMD ⁽³⁾ | DMD_HS1_WDATA0_P DMD_HS1_WDATA0_N | DMD_HS1_CLK_P DMD_HS1_CLK_N | ±1.0 (±25.4) | ±1.0 (±25.4) | in (mm) |
| | DMD_HS1_WDATA1_P DMD_HS1_WDATA1_N | | | | |
| | DMD_HS1_WDATA2_P DMD_HS1_WDATA2_N | | | | |
| | DMD_HS1_WDATA3_P DMD_HS1_WDATA3_N | | | | |
| | DMD_HS1_WDATA4_P DMD_HS1_WDATA4_N | | | | |
| | DMD_HS1_WDATA5_P DMD_HS1_WDATA5_N | | | | |
| | DMD_HS1_WDATA6_P DMD_HS1_WDATA6_N | | | | |
| | DMD_HS1_WDATA7_P DMD_HS1_WDATA7_N | | | | |
| DMD ⁽⁴⁾ | DMD_HS1_x_P | DMD_HS1_x_N | ±0.025 (±0.635) | 0.0315±0.025 (0.8±0.635) ⁽⁵⁾ | in (mm) |
| DMD ⁽³⁾ | DMD_LS0_WDATA_P DMD_LS0_WDATA_N | DMD_LS0_CLK_P DMD_LS0_CLK_N | ±1.0 (±25.4) | ±1.0 (±25.4) | in (mm) |
| DMD | DMD_LS0_WDATA DMD_LS0_RDATA DMD_LS1_RDATA | DMD_LS0_CLK | ±0.2 (±5.08) | ±0.2 (±5.08) | in (mm) |
| DMD ⁽⁴⁾ | DMD_LS0_x_P | DMD_LS0_x_N | ±0.025 (±0.635) | 0.0315±0.025 (0.8±0.635) ⁽⁵⁾ | in (mm) |
| DMD | DMD_DEN_ARSTZ | N/A | N/A | N/A | in (mm) |

Table 8-7. High-Speed PCB Signal Routing Matching Requirements (continued)

| SIGNAL GROUP LENGTH MATCHING ⁽¹⁾ ⁽²⁾ | | | | | |
|--|--------------------|------------------|-----------------------------|--|------------|
| INTERFACE | SIGNAL GROUP | REFERENCE SIGNAL | MAX MISMATCH ZDQ324 | MAX MISMATCH ZEK324 | UNIT |
| TPS99000S-Q1 | PMIC_LEDS EL(3) | PMIC_ADC3_CLK | ± 1.0 (± 25.4) | ± 1.0 (± 25.4) | in (mm) |
| | PMIC_LEDS EL(2) | | | | |
| | PMIC_LEDS EL(1) | | | | |
| | PMIC_LEDS EL(0) | | | | |
| | PMIC_SEQ_ STRT | | | | |
| | PMIC_ADC3 _MOSI | | | | |
| OpenLDI | Lx_DATAx_ N | Lx_DATAx_P | N/A | 0.0315 \pm 0.025 (0.8 \pm 0.635) ⁽⁶⁾ | in (mm) |
| OpenLDI | Lx_CLK_N | Lx_CLK_P | N/A | 0.0315 \pm 0.025 (0.8 \pm 0.635) ⁽⁶⁾ | in (mm) |

- (1) These routing requirements are specific to the PCB routing. Internal package routing mismatches in the DLPC23xS-Q1 and DMD have already been accounted for in these requirements.
- (2) Training is applied to DMD HS data lines, so defined matching requirements are slightly relaxed.
- (3) This is an inter-pair specification (that is, differential pair to differential pair within the group).
- (4) This is an intra-pair specification (that is, length mismatch between P and N for the same pair).
- (5) ZEK324 package trace length of the DMD interface differential N signals are 0.8mm longer than the P signals to simplify matching of the PCB signals.
- (6) ZEK324 package trace length of the OpenLDI interface differential P signals are 0.8mm longer than the N signals to simplify matching of the PCB signals.

8.4.1.7 Number of Layer Changes

- Single-ended signals: Minimize the number of layer changes.
- Differential signals: Individual differential pairs can be routed on different layers, but the signals of a given pair must not change layers.

8.4.1.8 Stubs

- Stubs must be avoided.

8.4.1.9 Terminations

- No external termination resistors are required on the DMD_HS or DMD_LS differential signals.
- The DMD_LS0_RDATA and DMD_LS1_RDATA single-ended signal paths must include a 10- Ω series termination resistor located as close as possible to the corresponding DMD pin.
- DMD_DEN_ARSTZ does not typically require a series resistor, however, for a long trace, one can be needed to reduce undershoot/overshoot.

8.4.1.10 Routing Vias

- The number of vias on each DMD_HS and DMD_LS signal must be minimized and must not exceed two. If two are required, one must be placed at each end of the line (one at the ASIC and one at the DMD).

8.4.2 Thermal Considerations

The underlying thermal limitation for the DLPC23xS-Q1 is that the maximum operating junction temperature (T_J) not be exceeded (this is defined in [Section 5.3](#)). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC23xS-Q1, and power dissipation of surrounding components. The DLPC23xS-Q1's package is designed primarily to extract heat through the power and ground planes of the PCB. Thus, copper content and airflow over the PCB are important factors.

TI highly recommends that after the host PCB is designed and built that the thermal performance be measured and validated.

To do this, measure the top center case temperature under the worse case product scenario (max power dissipation, max voltage, max ambient temperature) and validate that the maximum recommended case temperature (T_C) is not exceeded. This specification is based on the measured ϕ_{JT} for the DLPC23xS-Q1 package and provides a relatively accurate correlation to junction temperature. Take care when measuring this case temperature to prevent accidental cooling of the package surface. TI recommends a small (approximately 40 gauge) thermocouple. The bead and thermocouple wire must contact the top of the package and be covered with a minimal amount of thermally conductive epoxy. The wires must be routed closely along the package and the board surface to avoid cooling the bead through the wires.

9 Device and Documentation Support

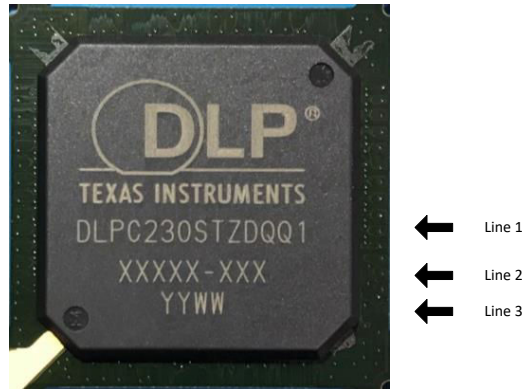
9.1 Device Support

9.1.1 Third-Party Products Disclaimer

TI'S PUBLICATION OF INFORMATION REGARDING THIRD-PARTY PRODUCTS OR SERVICES DOES NOT CONSTITUTE AN ENDORSEMENT REGARDING THE SUITABILITY OF SUCH PRODUCTS OR SERVICES OR A WARRANTY, REPRESENTATION OR ENDORSEMENT OF SUCH PRODUCTS OR SERVICES, EITHER ALONE OR IN COMBINATION WITH ANY TI PRODUCT OR SERVICE.

9.1.2 Device Nomenclature

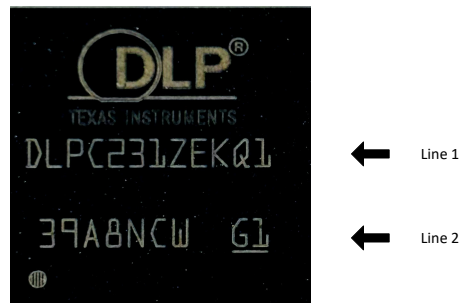
9.1.2.1 Device Markings DLPC230-Q1 or DLPC230S-Q1



Marking Definitions:

| | | |
|---------|--------------------------------|--|
| Line 1: | TI Part Number: Production | DLPC230 = Device ID blank or A, B, C ... = Part Revision Blank or S = Functional Safety T = Temperature –40°C to +105°C ambient operating temperature ZDQ = Package designator R = Tape & Reel, blank = tray Q1 = Automotive qualified |
| Line 2: | Vendor Lot and Fab Information | XXXXX = Fab lot number -XX = Fab Sublot X (last X) = Assembly Sublot The Fab is UMC12A. As such, the first character of the lot number is K |
| Line 3: | Vendor Year and Week code | YY = Year WW = Week Example, 1614 - parts built the 14 th week of 2016 |

9.1.2.2 Device Markings DLPC231-Q1 or DLPC231S-Q1



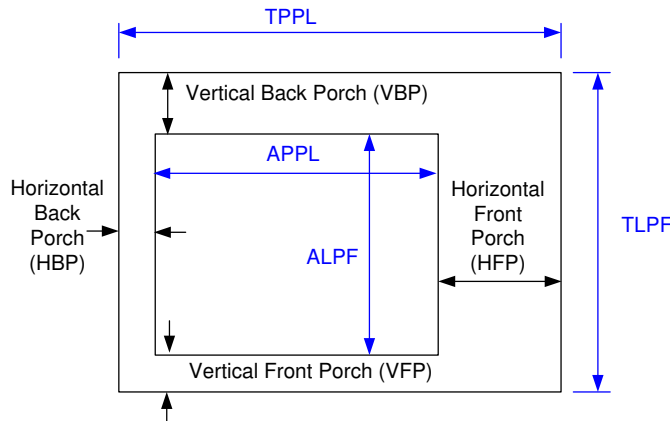
Marking Definitions:

Line 1: TI Part Number: Production DLPC231 = Device ID
 blank or A, B, C ... = Part Revision
 Blank or S = Functional Safety
 Blank or T = Temperature –40°C to +105°C ambient operating temperature
 ZEK = Package designator
 R = Tape & Reel, blank = tray
 Q1 = Automotive qualified

Line 2: Vendor Lot and Fab Information First 7 Characters = Lot Trace Code
 Last 2 Characters = Environmental Category

9.1.2.3 Video Timing Parameter Definitions

- Active Lines Per Frame (ALPF)** Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.
- Active Pixels Per Line (APPL)** Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.
- Horizontal Back Porch (HBP) Blanking** Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.
- Horizontal Front Porch (HFP) Blanking** Number of blank pixel clocks after the last active pixel but before Horizontal Sync.
- Horizontal Sync (HS)** Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.
- Total Lines Per Frame (TLPF)** Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).
- Total Pixel Per Line (TPPL)** Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).
- Vertical Sync (VS)** Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.
- Vertical Back Porch (VBP) Blanking** Number of blank lines after vertical sync but before the first active line.
- Vertical Front Porch (VFP) Blanking** Number of blank lines after the last active line but before vertical sync.



9.2 Trademarks

DLP® is a registered trademark of Texas Instruments.

All trademarks are the property of their respective owners.

9.3 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.4 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

10 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision C (September 2023) to Revision D (March 2024) | Page |
|---|-------------|
| • Updated section for inclusive terminology; Added note to Table 4-10 | 3 |
| • Changed <i>ESD Ratings</i> table to the automotive format; added <i>ESD Ratings</i> spec for ZEK package..... | 15 |
| • Removed "Advanced Information" comment; Updated footnote 2 example..... | 16 |
| • Updated Max current values for VCC1.1 and VCC1.8 total and each supply input..... | 17 |
| • Updated Package - Maximum Power..... | 21 |
| • Updated Section 5.20 for inclusive terminology..... | 31 |
| • Updated Section 5.21 for inclusive terminology..... | 32 |
| • Updated Section 7.3.9 for inclusive terminology..... | 48 |
| • Updated Section 7.3.10 for inclusive terminology..... | 48 |
| • Added DLPC231 Device Markings..... | 64 |
| • Updated ZDQ0324A package outline to show alternate mold dimension.; Added ZEK0324A package outline drawing to support DLPC231-Q1 and DLPC231S-Q1..... | 67 |

| Changes from Revision B (August 2023) to Revision C (September 2023) | Page |
|--|-------------|
| • Updated device name from DLP553x and DLP462x to DLP5530S and DLP4620S..... | 1 |
| • Changed the DMD Pins assignment: DMD_HS1_WDATA4_P—DMD_HS1_WDATA7_N for the DLPC231 device..... | 3 |

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|---------|
| DLPC230STZDQQ1 | ACTIVE | BGA | ZDQ | 324 | 1 | TBD | Call TI | Call TI | -40 to 105 | | Samples |
| DLPC231SZEKQ1 | ACTIVE | NFBGA | ZEK | 324 | 126 | TBD | Call TI | Call TI | -40 to 105 | DLPC231SZEKQ1 | Samples |
| DLPC231SZEKRQ1 | ACTIVE | NFBGA | ZEK | 324 | 1000 | TBD | Call TI | Call TI | -40 to 105 | DLPC231SZEKQ1 | Samples |
| DLPC23STZDQRQ1 | ACTIVE | BGA | ZDQ | 324 | 250 | TBD | Call TI | Call TI | -40 to 105 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

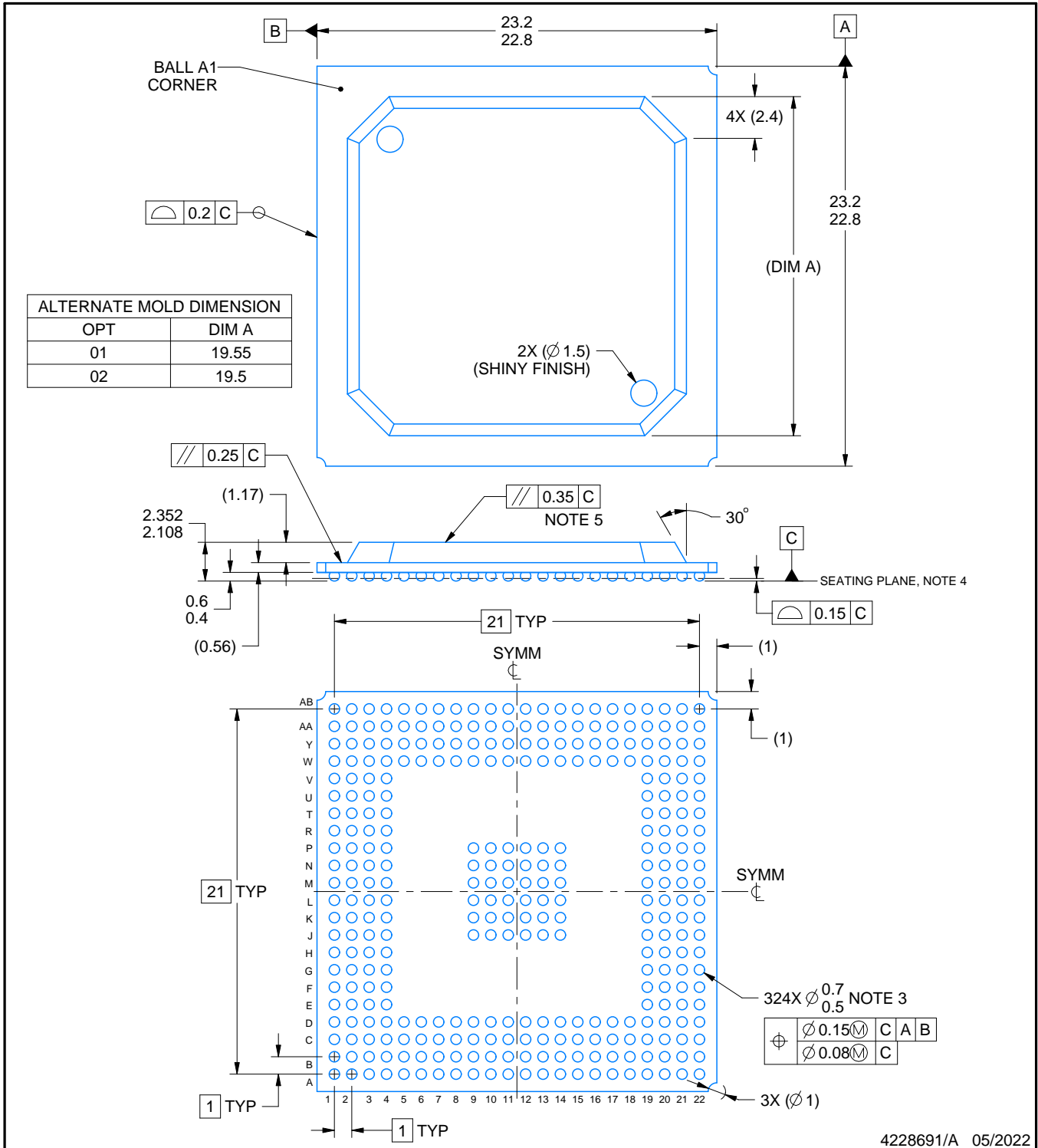
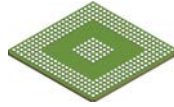
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



4228691/A 05/2022

NOTES:

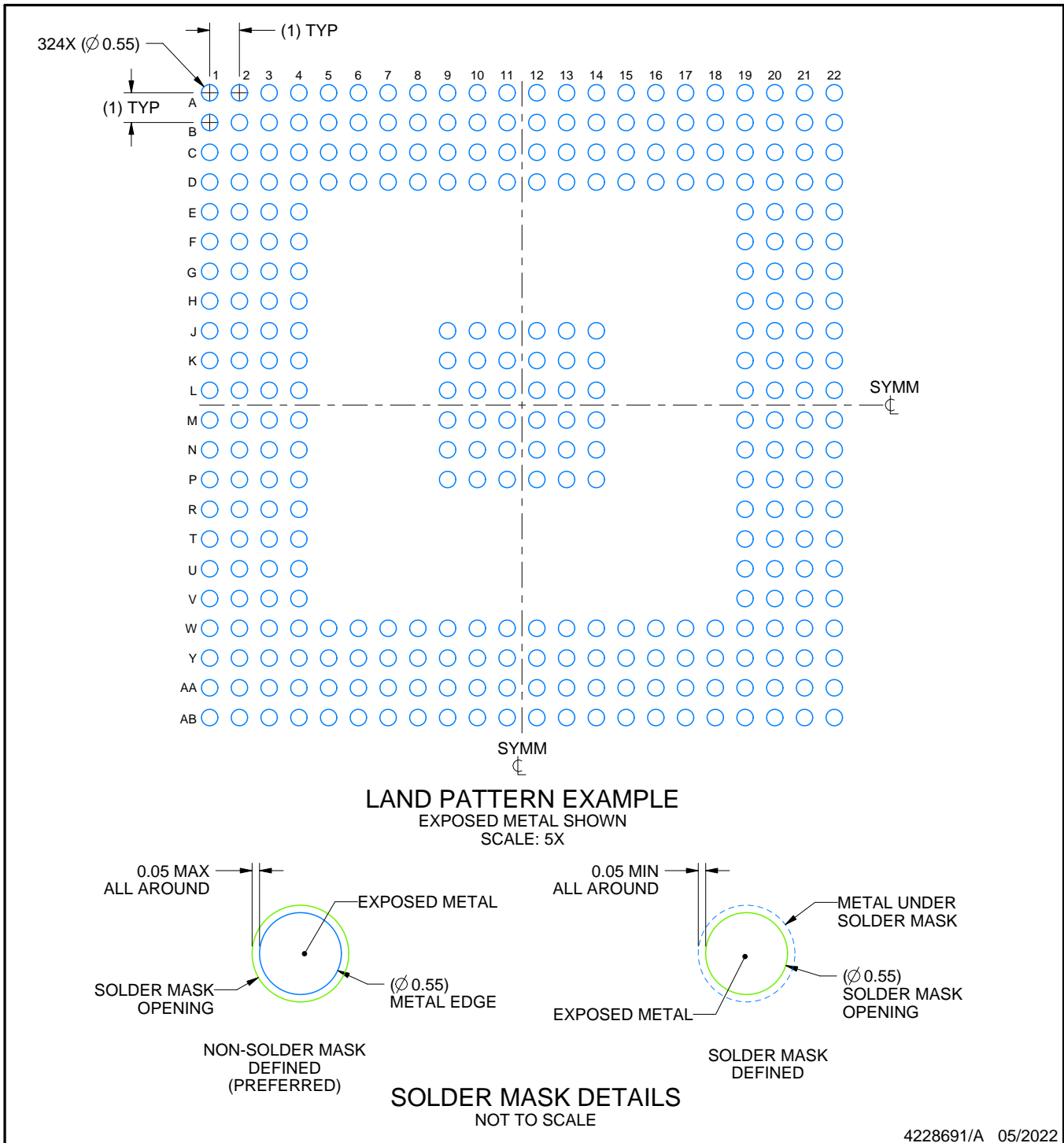
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension is measured at the maximum solder ball diameter parallel to datum plane C.
4. Datum C (Seating Plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on the top surface of package.

EXAMPLE BOARD LAYOUT

ZDQ0324A

BGA - 2.352 mm max height

BALL GRID ARRAY



4228691/A 05/2022

NOTES: (continued)

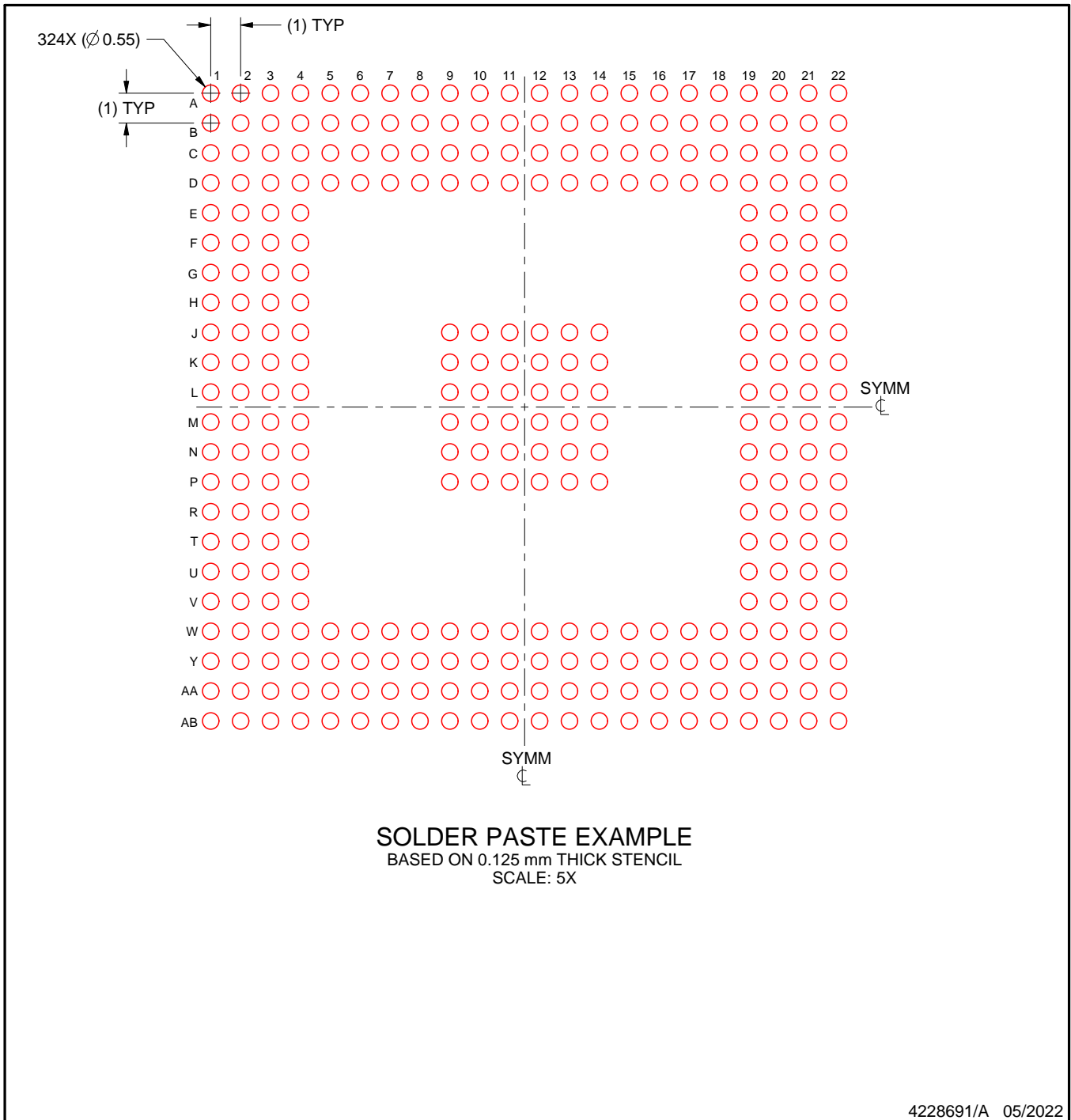
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. For information, see Texas Instruments literature number SPRAA99 (www.ti.com/lit/spraa99).

EXAMPLE STENCIL DESIGN

ZDQ0324A

BGA - 2.352 mm max height

BALL GRID ARRAY



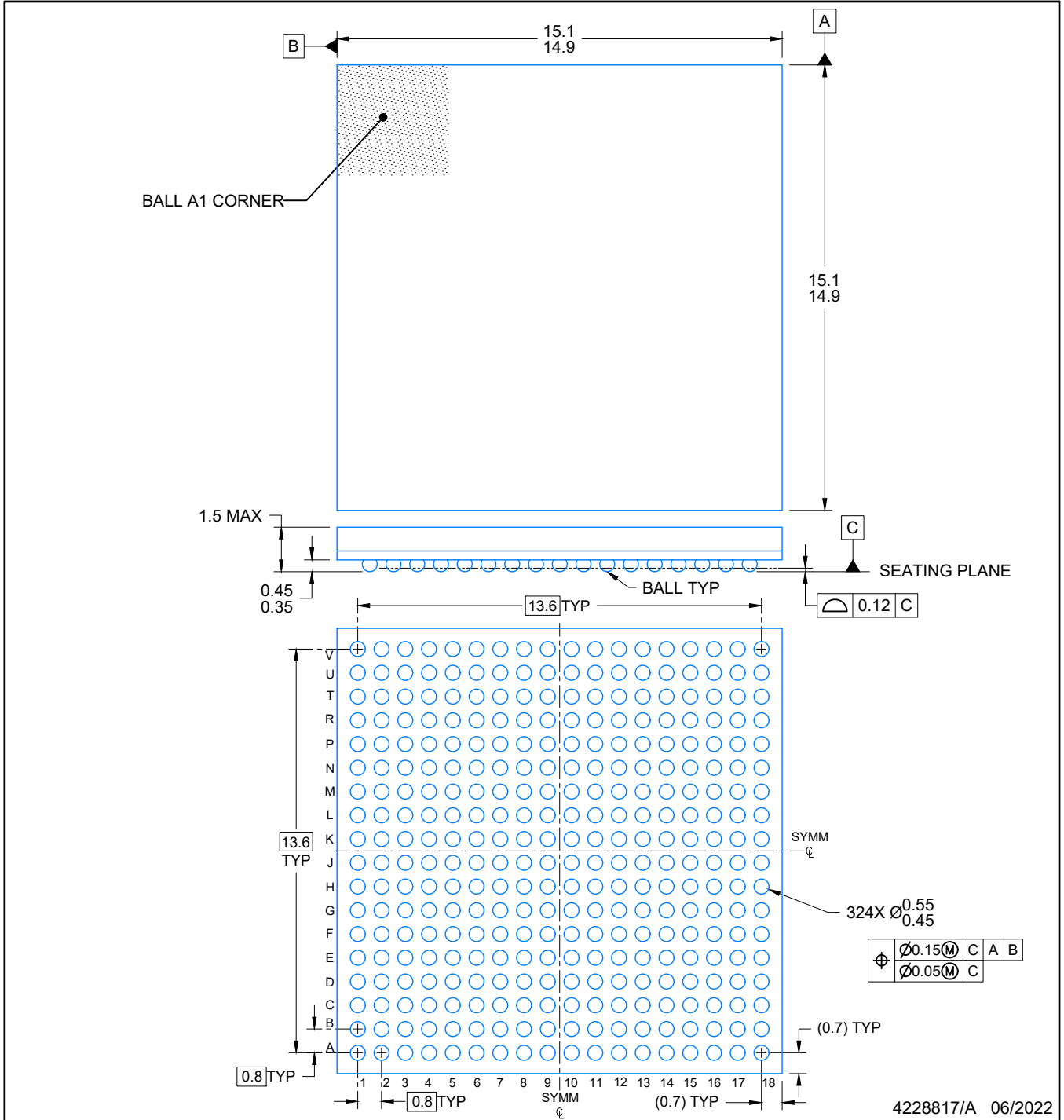
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

ZEK0324A

PACKAGE OUTLINE NFBGA - 1.5 mm max height

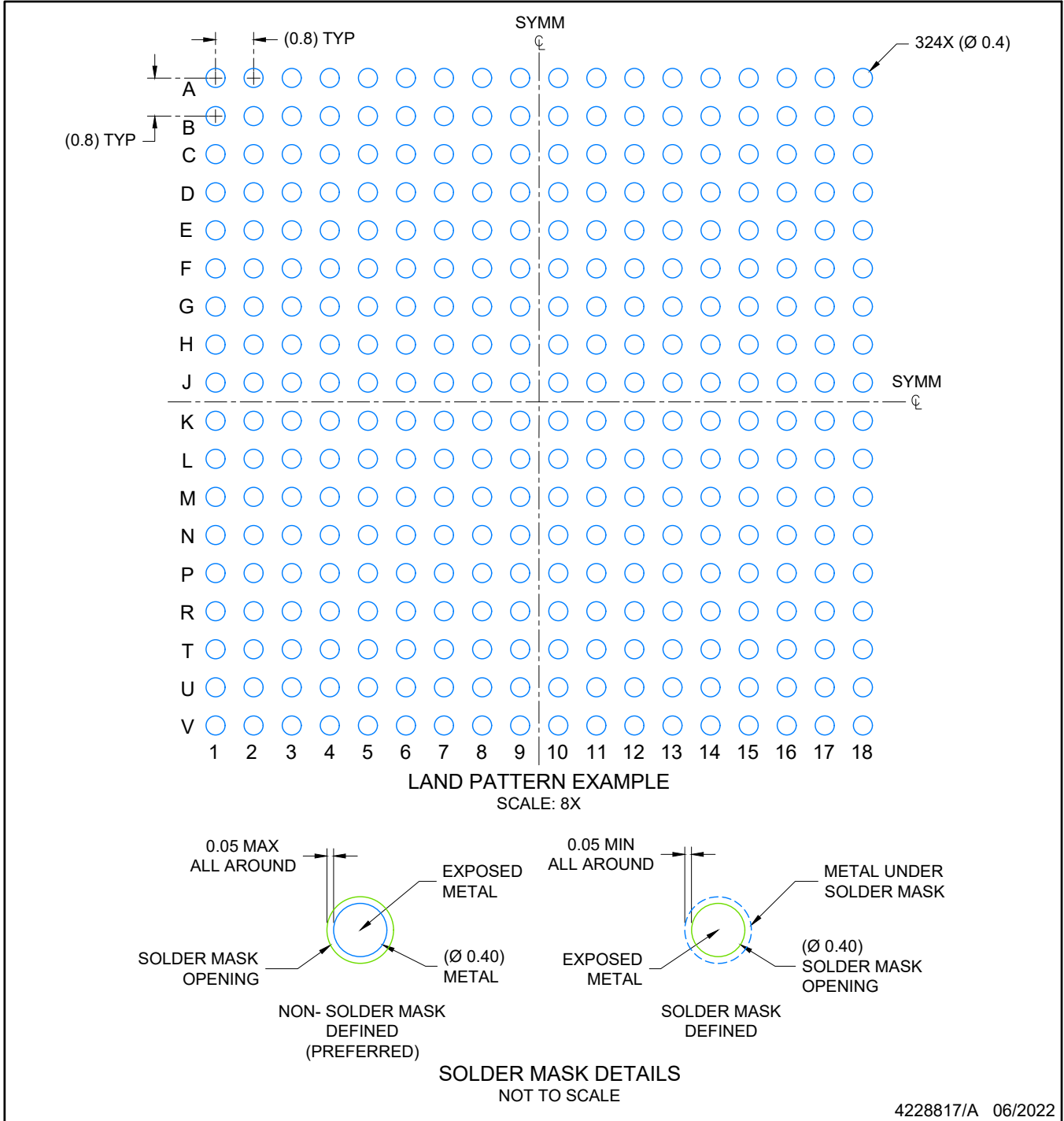
PLASTIC BALL GRID ARRAY



NOTES:

NanoFree is a trademark of Texas Instruments.

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



NOTES: (continued)

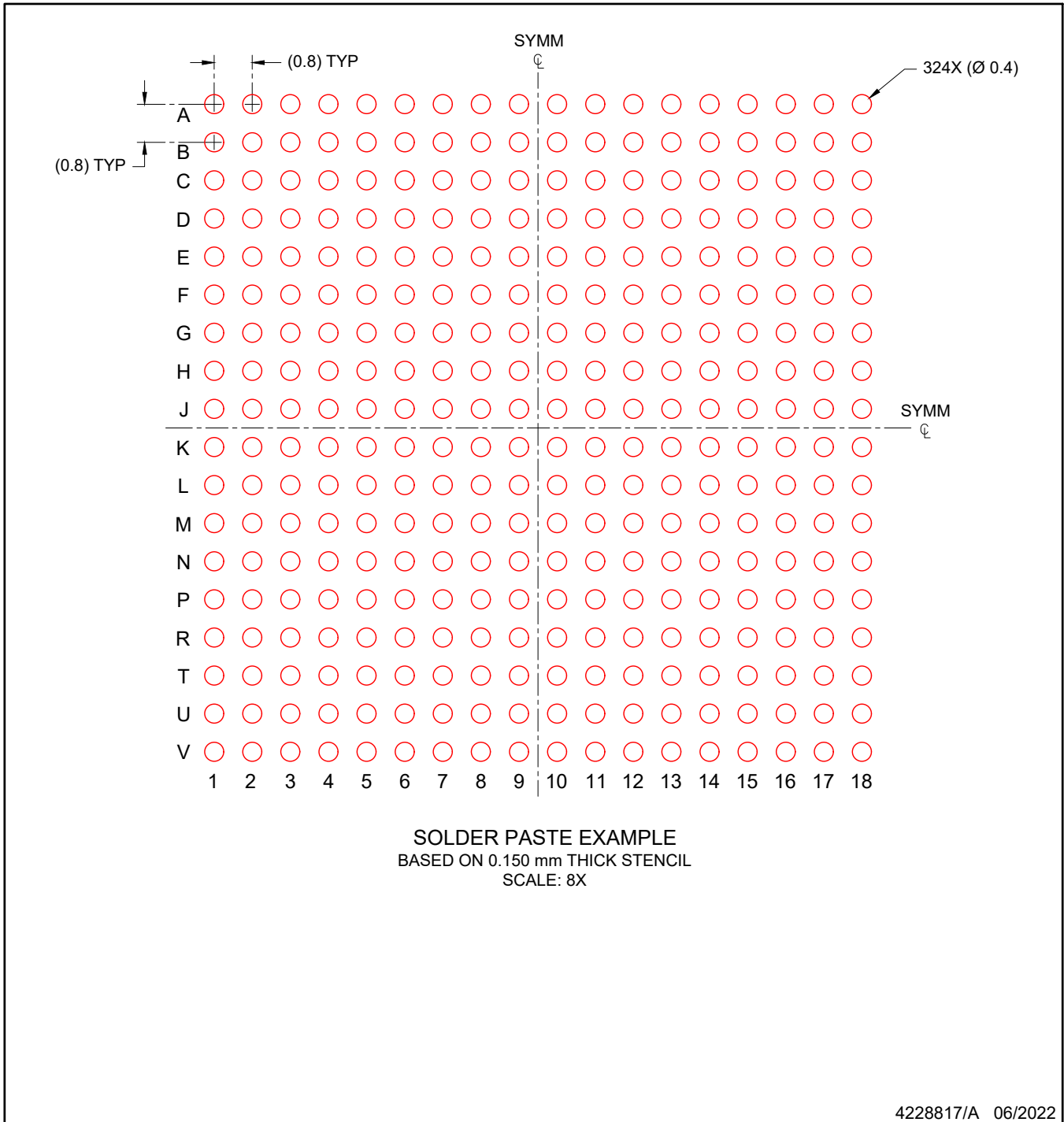
- Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature number SNVA009 (www.ti.com/lit/snva009).

EXAMPLE STENCIL DESIGN

ZEK0324A

NFBGA - 1.5 mm max height

PLASTIC BALL GRID ARRAY



NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

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