DRV3233-Q1 Automotive 24/12-V Battery 3-Phase Gate Driver Unit with accurate current sensing and enhanced diagnostics

ADVANCE INFORMATION

1 Features

- AEC-Q100 Test Guidance for automotive applications
  - Device ambient temperature: –40°C to +150°C
- Functional Safety-Compliant targeted
  - Developed for functional safety applications
  - Documentation to aid ISO 26262 system design will be available upon production release
  - Systematic capability up to ASIL D targeted
- Three phase half-bridge gate driver
  - Drives six N-channel MOSFETs (NMOS)
  - 4.5 to 60-V wide operating voltage range
  - Bootstrap architecture for high-side gate driver
  - Charge pump to support 100% PWM duty cycle and to generate overdrive supply
- Smart Gate Drive architecture
  - 45-level configurable peak gate drive current up to 1000 / 2000-mA (source / sink)
- Low-side Current Sense Amplifier
  - Sub-1 mV low input offset across temperature
  - 9-level adjustable gain
- SPI-based detailed configuration and diagnostics
- DRVOFF pin to disable driver independently
- High voltage wake up pin (nSLEEP)
- Multiple PWM interface options available
  - 6x, 3x, 1x PWM Modes
  - PWM over SPI
- Supports 3.3-V, and 5-V Logic Inputs
- Optional programmable OTP for reset settings
- Advanced and configurable protection features
  - Battery and power supply voltage monitors
  - Phase feedback comparator
  - MOSFET V_{DS} and R_{sense} over current monitors
  - MOSFET V_{GS} gate fault monitors
  - Internal regulator and clock monitors
  - Analog Built-In-Self-Test (ABIST)
  - Device thermal warning and shutdown
  - Fault condition indicator pin

2 Applications

- 12-V / 24-V Automotive Motor-Control Applications
  - Electrical Power Steering
  - Electrical Brake and Brake Assist
  - Transmissions and Pumps

3 Description

The DRV3233 is an integrated smart gate driver for 12-V and 24-V automotive three-phase BLDC applications. The device provides three half-bridge gate drivers, each capable of driving high-side and low-side N-channel power MOSFETs. The DRV3233 generates the correct gate drive voltages using an integrated bootstrap diode and a GVDD charge pump. The Smart Gate Drive architecture supports configurable peak gate drive current from 0.7-mA up to 1-A source and 2-A sink. The DRV3233 can operate from a single power supply with a wide input range of 4.5 to 60-V. A trickle charge pump allows for the gate drivers to support 100% PWM duty cycle control, and provides overdrive gate drive voltage of external switches.

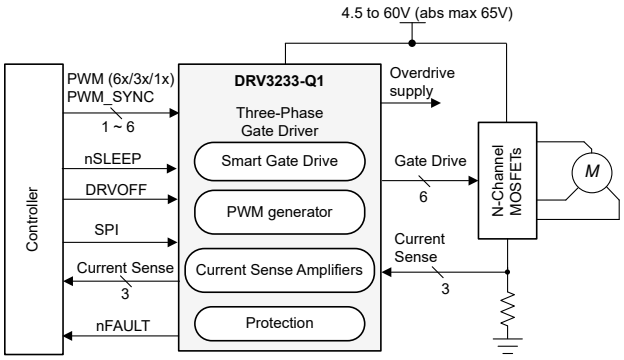
The DRV3233 provides low-side current sense amplifiers to support resistor based low-side current sensing. The low offset of the amplifiers enables the system to obtain precise motor current measurement.

A wide range of diagnostics and protection features integrated in the DRV3233 enable a robust motor drive system design and help eliminate the needs of external components. The highly configurable device response allows the device to be integrated seamlessly into a variety of system designs.

Package Information

PART NUMBER	PACKAGE(1)	PACKAGE SIZE(2)	BODY SIZE (NOM)
DRV3233-Q1	HTQFP (48)	9 mm x 9 mm	7 mm × 7 mm
	QFN (48)(3)	7 mm × 7 mm	7 mm × 7 mm
	QFN (40)(3)	7 mm × 5 mm	7 mm × 5 mm
	QFN (32)(3)	6 mm × 4 mm	6 mm × 4 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable.
(3) Product preview only. Contact TI for more information.



Simplified Schematic

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2023	*	Initial Release

ADVANCE INFORMATION

5 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

5.1 Package Option Addendum

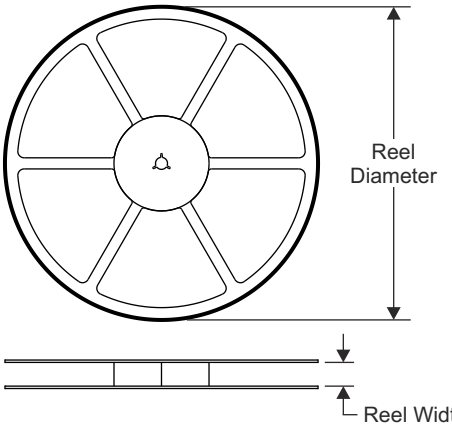
Packaging Information

Orderable Device	Status	Package Type	Package Drawing	Pins	Package Qty	Eco Plan	Lead/Ball Finish	MSL Peak Temp	Op Temp (°C)	Device Marking
PDRV3233EPHPRQ1	In Review	HTQFP	PHP	48	1000	RoHS & Green	NiPdAu	Level-3-260C-168 HR	-40 to 150	PDRV3233

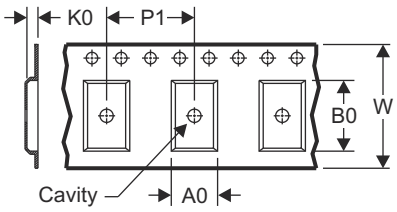
ADVANCE INFORMATION

5.2 Tape and Reel Information

REEL DIMENSIONS

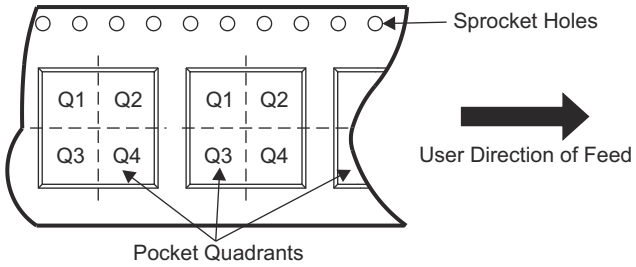


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

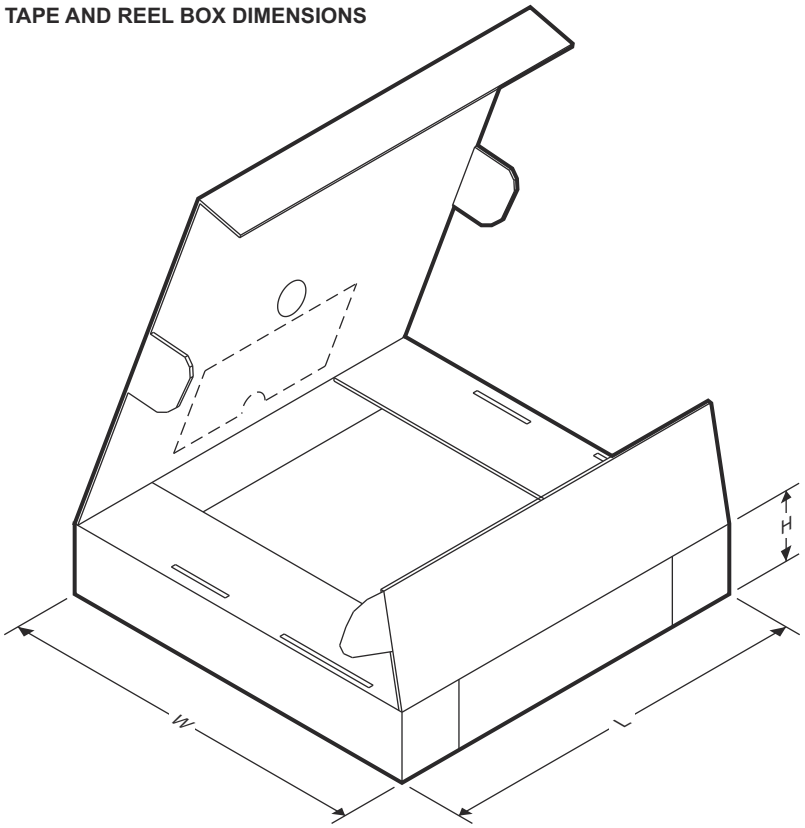


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PDRV3233EPHPRQ1	HTQFP	PHP	48	1000	330.0	16.4	9.6	9.6	1.5	12.0	16.0	2

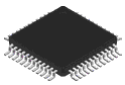
ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



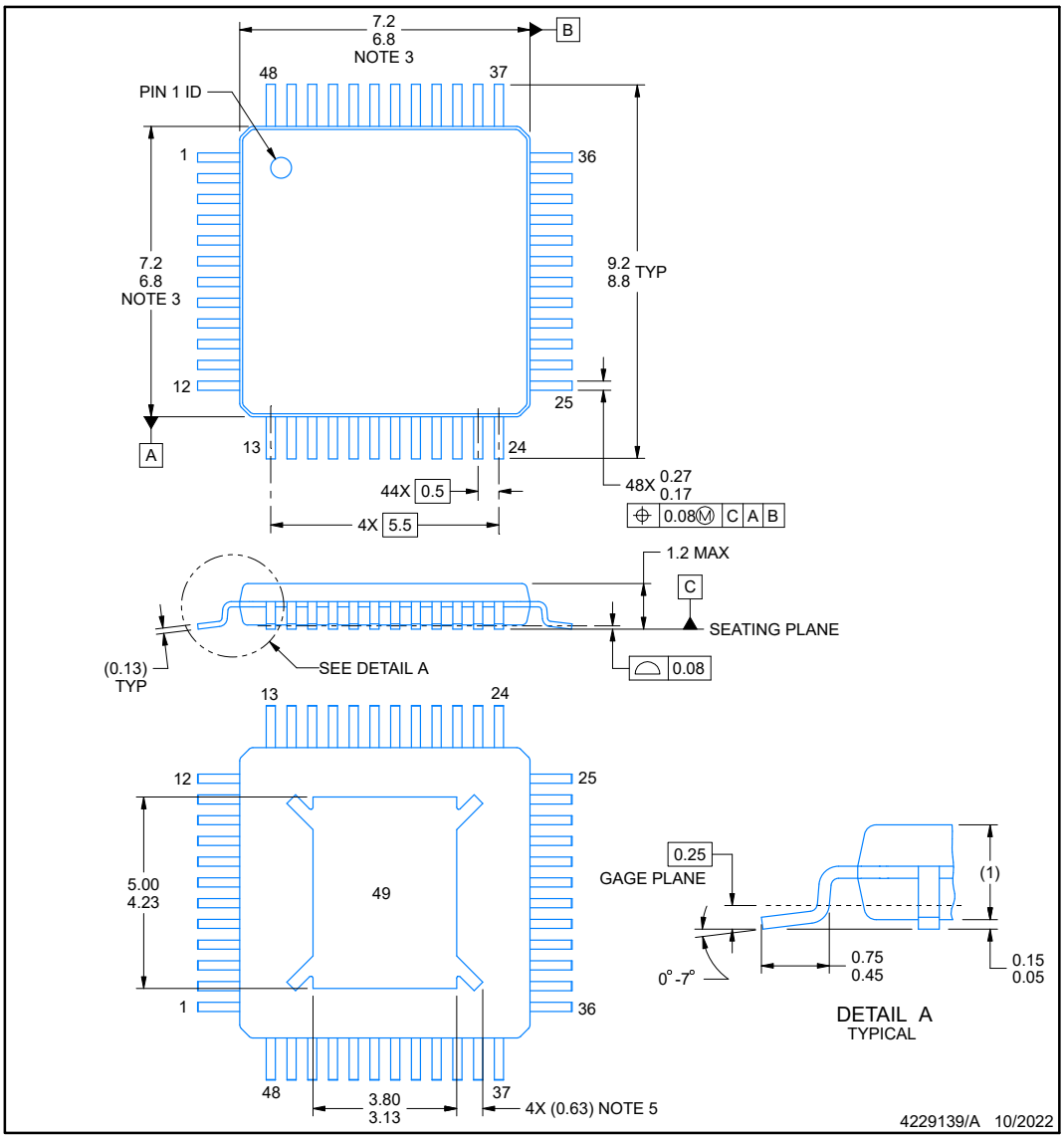
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PDRV3233EPHPRQ1	HTQFP	PHP	48	1000	336.6	336.6	31.8



PACKAGE OUTLINE

PHP0048P — **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.
5. Feature may not be present.

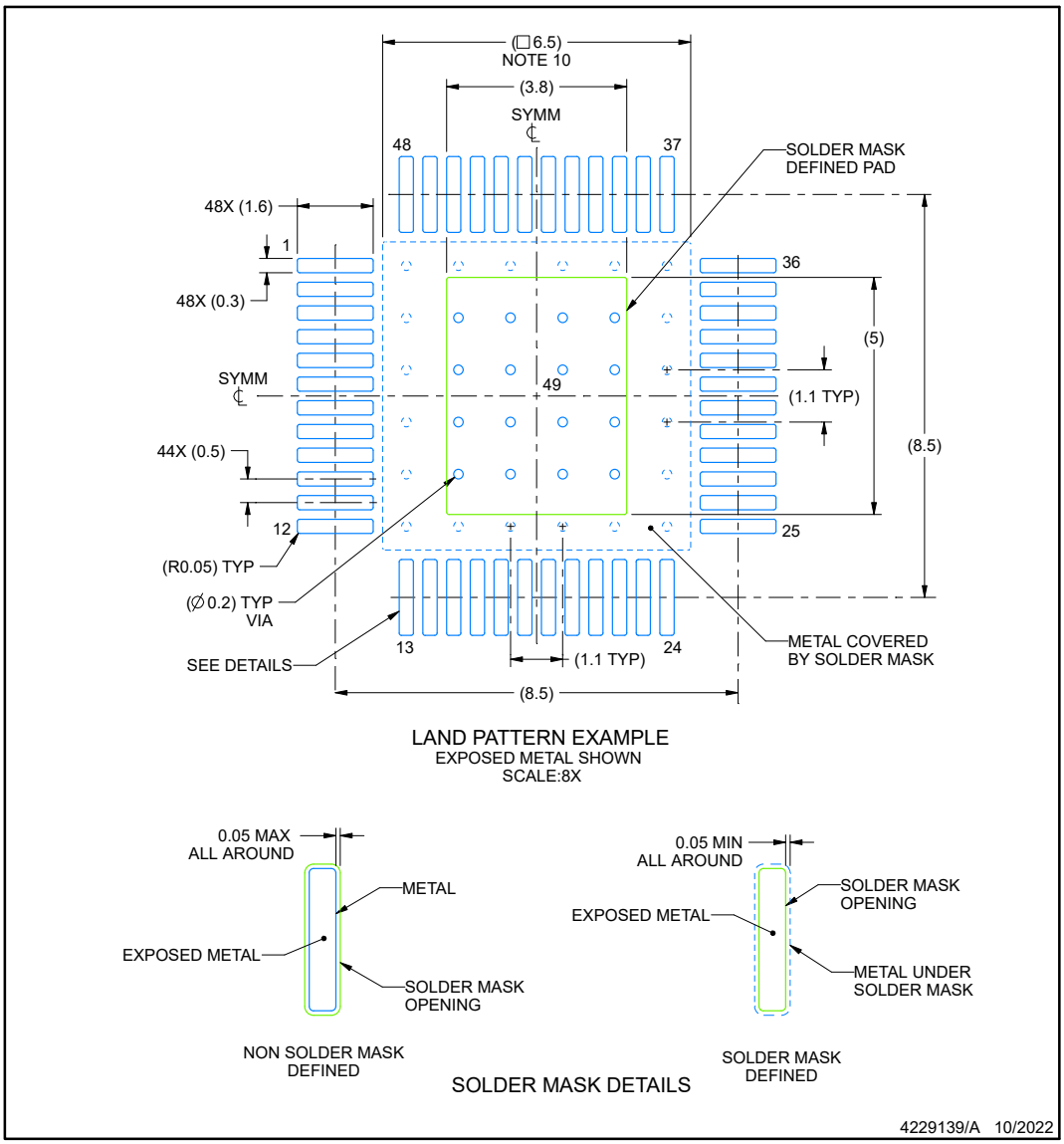
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

PHP0048P

PowerPAD™ HTQFP - 1.2 mm max height

PLASTIC QUAD FLATPACK



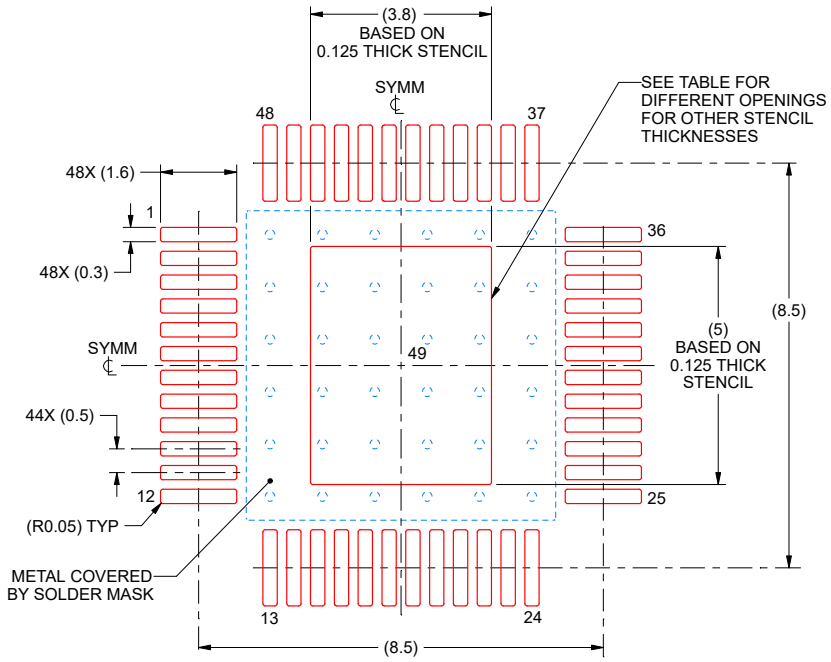
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. See technical brief, Powerpad thermally enhanced package, Texas Instruments Literature No. SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.
10. Size of metal pad may vary due to creepage requirement.

EXAMPLE STENCIL DESIGN

PHP0048P — **PowerPAD™ HTQFP - 1.2 mm max height**

PLASTIC QUAD FLATPACK



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	4.25 X 5.59
0.125	3.80 X 5.00 (SHOWN)
0.150	3.47 X 4.56
0.175	3.21 X 4.23

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PDRV3233EPHPRQ1	ACTIVE	HTQFP	PHP	48	1000	TBD	Call TI	Call TI	-40 to 150		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

GENERIC PACKAGE VIEW

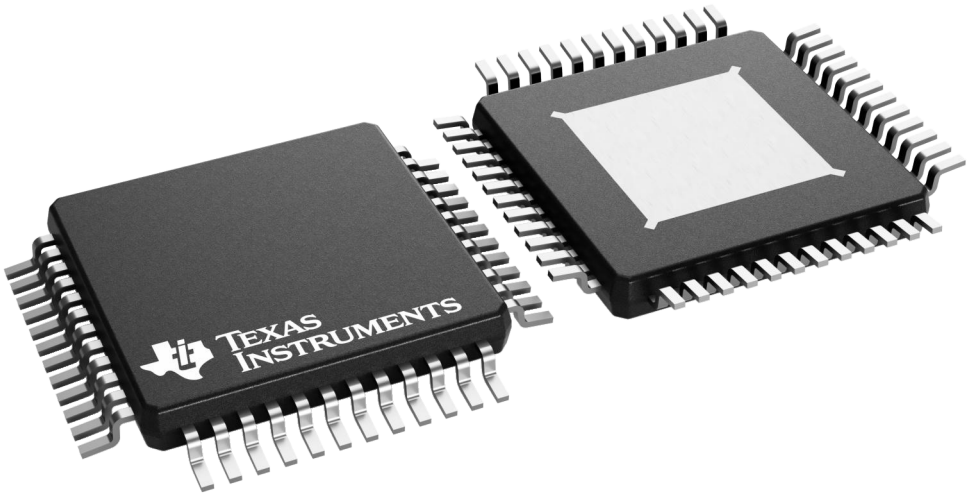
PHP 48

TQFP - 1.2 mm max height

7 x 7, 0.5 mm pitch

QUAD FLATPACK

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



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