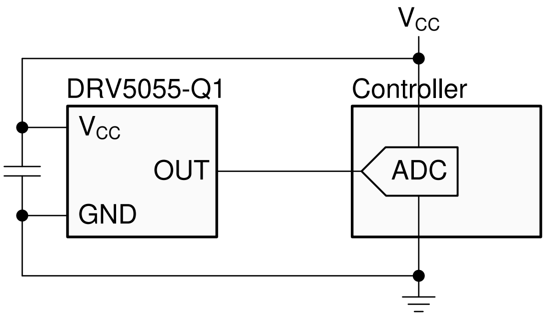
DRV5055-Q1 Automotive Ratiometric Linear Hall Effect Sensor

1 Features

- Ratiometric Linear Hall Effect Magnetic Sensor
- Operates From 3.3V and 5V Power Supplies
- Analog Output With V_{CC} / 2 Quiescent Offset
- Magnetic Sensitivity Options (At V_{CC} = 5V):
  - A1: 100mV/mT, ±21mT Range
  - A2/Z2: 50 mV/mT, ±42-mT Range
  - A3: 25mV/mT, ±85mT Range
  - A4: 12.5mV/mT, ±169mT Range
  - A5: –100mV/mT, ±21mT Range
- Fast 20kHz Sensing Bandwidth
- Low-Noise Output With ±1mA Drive
- Compensation for magnet temperature drift for A versions and none for Z versions
- AEC-Q100 Qualified for Automotive Applications:
  - Temperature Grade 0: –40°C to 150°C
- Standard Industry Packages:
  - Surface-Mount SOT-23
  - Through-Hole TO-92

2 Applications

- Automotive Position Sensing
- Brake, Acceleration, Clutch Pedals
- Torque Sensors
- Gear Shifters
- Throttle Position
- Height Leveling
- Powertrain and Transmission Components
- Absolute Angle Encoding
- Current Sensing



Typical Schematic

3 Description

The DRV5055-Q1 is a linear Hall effect sensor that responds proportionally to magnetic flux density. The device can be used for accurate position sensing in a wide range of applications.

The device operates from 3.3V or 5V power supplies. When no magnetic field is present, the analog output drives half of V_{CC}. The output changes linearly with the applied magnetic flux density, and various sensitivity options enable maximal output voltage swing based on the required sensing range. North and south magnetic poles produce unique voltages.

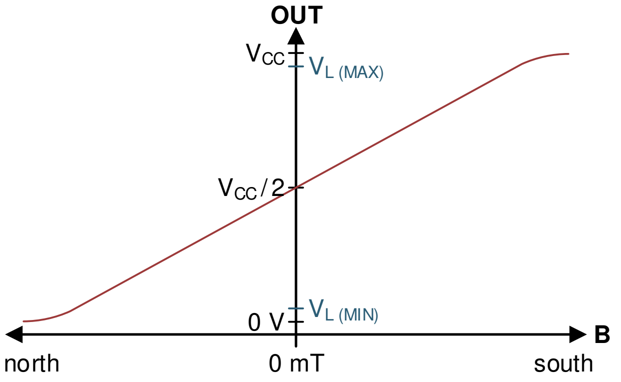
Magnetic flux perpendicular to the top of the package is sensed, and the two package options provide different sensing directions.

The device uses a ratiometric architecture that can eliminate error from V_{CC} tolerance when the external analog-to-digital converter (ADC) uses the same V_{CC} for its reference. Additionally, the device features magnet temperature compensation to counteract how magnets drift for linear performance across a wide –40°C to +150°C temperature range.

Package Information

PART NUMBER	PACKAGE[1]	PACKAGE SIZE[2]
DRV5055-Q1	DBZ (SOT-23, 3)	2.92mm × 2.37mm
	LPG (TO-92, 3)	4mm × 1.52mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.
(2) The package size (length × width) is a nominal value and includes pins, where applicable



Magnetic Response (A1, A2, A3, A4, Z2 Versions)

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4 Pin Configuration and Functions

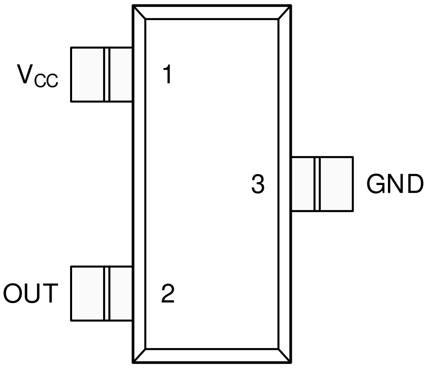


Figure 4-1. DBZ Package 3-Pin SOT-23 Top View

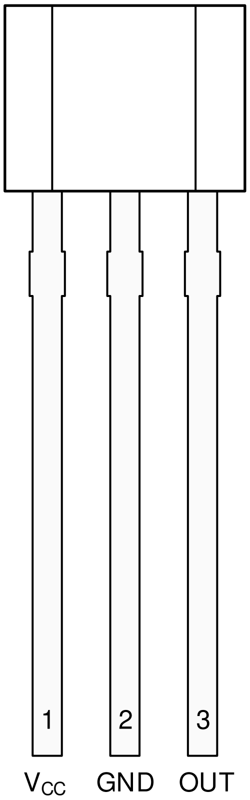


Figure 4-2. LPG Package 3-Pin TO-92 Top View

Table 4-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	SOT-23	TO-92		
V_{CC}	1	1	—	Power supply. TI recommends connecting this pin to a ceramic capacitor to ground with a value of at least 0.01 µF.
OUT	2	3	O	Analog output
GND	3	2	—	Ground reference

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply voltage	V_{CC}	–0.3	7	V
Output voltage	OUT	–0.3	V_{CC} + 0.3	V
Magnetic flux density, B_{MAX}		Unlimited		T
Operating junction temperature, T_J		–40	170	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	±2500	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Power supply voltage(1)	3	3.63	V
		4.5	5.5	
I_O	Output continuous current	–1	1	mA
T_A	Operating ambient temperature(2)	–40	150	°C

(1) There are two isolated operating V_{CC} ranges. For more information see the Operating V_{CC} Ranges section.
(2) Power dissipation and thermal limits must be observed.

5.4 Thermal Information

THERMAL METRIC(1)		DRV5055-Q1		UNIT
		SOT-23 (DBZ)	TO-92 (LPG)	
		3 PINS	3 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170	121	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	66	67	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49	97	°C/W
Y_{JT}	Junction-to-top characterization parameter	1.7	7.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	48	97	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application note.

5.5 Electrical Characteristics

for V_{CC} = 3V to 3.63V and 4.5V to 5.5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS[1]		MIN	TYP	MAX	UNIT
I_{CC}	Operating supply current				6	10	mA
t_{ON}	Power-on time (see Figure 6-4)				175	330	µs
f_{BW}	Sensing bandwidth				20		kHz
t_d	Propagation delay time	From change in B to change in OUT			10		µs
B_{ND}	Input-referred RMS noise density	V_{CC} = 5V			130		$nT/\sqrt{Hz}$
		V_{CC} = 3.3V			215		
B_N	Input-referred noise	$B_{ND} \times 6.6 \times \sqrt{20\ kHz}$	V_{CC} = 5V		0.12		mT_{PP}
			V_{CC} = 3.3V		0.2		
V_N	Output-referred noise[2]	$B_N \times S$	DRV5055A1, DRV5055A5		12		mV_{PP}
			DRV5055A2, DRV5055Z2		6		mV_{PP}
			DRV5055A3		3		mV_{PP}
			DRV5055A4		1.5		mV_{PP}

(1) B is the applied magnetic flux density.
(2) V_N describes voltage noise on the device output. If the full device bandwidth is not needed, noise can be reduced with an RC filter.

5.6 Magnetic Characteristics

for V_{CC} = 3V to 3.63V and 4.5V to 5.5V, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS(1)		MIN	TYP	MAX	UNIT
V_Q	Quiescent voltage	B = 0mT, T_A = 25°C	V_{CC} = 5V	2.43	2.5	2.57	V
			V_{CC} = 3.3V	1.59	1.65	1.71	
$V_{Q\Delta T}$	Quiescent voltage temperature drift	B = 0 mT, T_A = –40°C to 150°C versus 25°C			±1% × V_{CC}		V
V_{QRE}	Quiescent voltage ratiometry error(2)				±0.2		%
$V_{Q\Delta L}$	Quiescent voltage lifetime drift	High-temperature operating stress for 1000 hours			<0.5		%
S	Sensitivity	V_{CC} = 5V, T_A = 25°C	DRV5055A1	95	100	105	mV/mT
			DRV5055A2/Z2	47.5	50	52.5	
			DRV5055A3	23.8	25	26.2	
			DRV5055A4	11.9	12.5	13.2	
			DRV5055A5	–105	–100	–95	
		V_{CC} = 3.3V, T_A = 25°C	DRV5055A1	57	60	63	
			DRV5055A2/Z2	28.5	30	31.5	
			DRV5055A3	14.3	15	15.8	
			DRV5055A4	7.1	7.5	7.9	
			DRV5055A5	–63	–60	–57	
B_L	Linear magnetic sensing range(3) (4)	V_{CC} = 5V, T_A = 25°C	DRV5055A1, DRV5055A5	±21			mT
			DRV5055A2/Z2	±42			mT
			DRV5055A3	±85			mT
			DRV5055A4	±169			mT
		V_{CC} = 3.3V, T_A = 25°C	DRV5055A1, DRV5055A5	±22			mT
			DRV5055A2/Z2	±44			mT
			DRV5055A3	±88			mT
			DRV5055A4	±176			mT
V_L	Linear range of output voltage(4)			0.2		V_{CC} – 0.2	V
S_{TC}	Sensitivity temperature compensation for magnets(5)	DRV5055A1/A2/A3/A4			0.12		%/°C
		DRV5055Z2			0		%/°C
S_{LE}	Sensitivity linearity error(4)	V_{OUT} is within V_L			±1		%
S_{SE}	Sensitivity symmetry error(4)	V_{OUT} is within V_L			±1		%
S_{RE}	Sensitivity ratiometry error(2)	T_A = 25°C, with respect to V_{CC} = 3.3V or 5V		–2.5		2.5	%
$S_{\Delta L}$	Sensitivity lifetime drift	High-temperature operating stress for 1000 hours			<0.5		%

(1) B is the applied magnetic flux density.
(2) See the Ratiometric Architecture section.
(3) B_L describes the minimum linear sensing range at 25°C taking into account the maximum V_Q and Sensitivity tolerances.
(4) See the Sensitivity Linearity section.
(5) S_{TC} describes the rate the device increases Sensitivity with temperature. For more information, see the Sensitivity Temperature Compensation for Magnets section.

5.7 Typical Characteristics

for T_A = 25°C (unless otherwise noted)

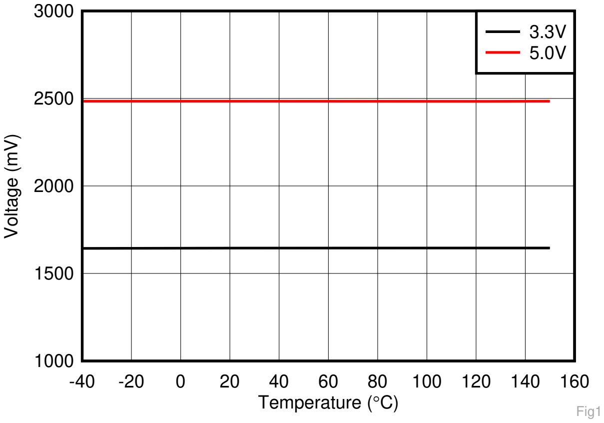


Figure 5-1. Quiescent Voltage vs Temperature

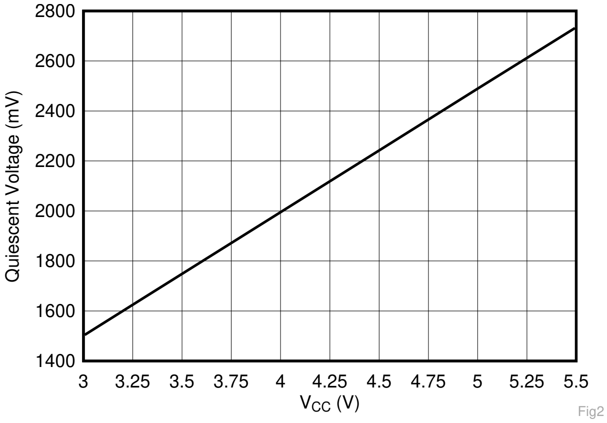
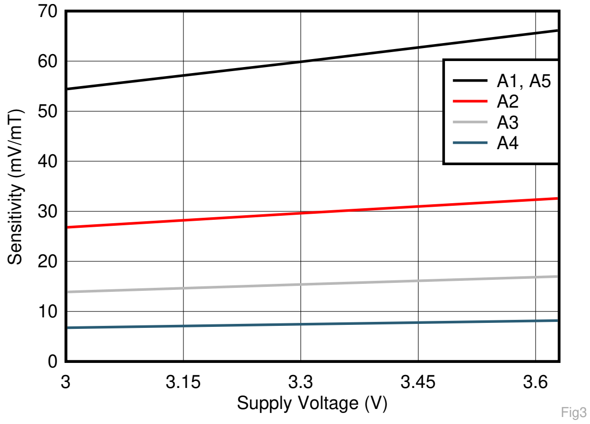
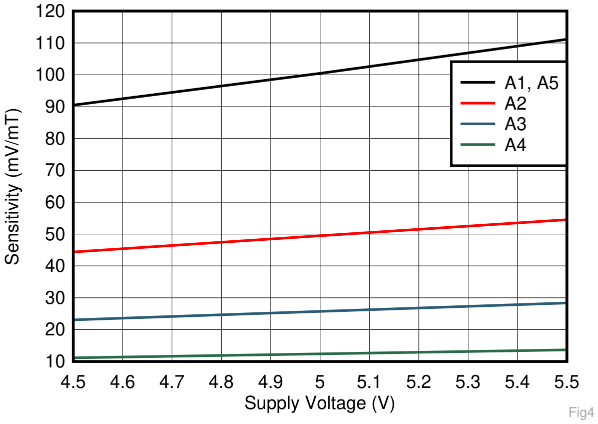


Figure 5-2. Quiescent Voltage vs Supply Voltage



V_{CC} = 3.3 V

Figure 5-3. Sensitivity vs Supply Voltage



V_{CC} = 5.0 V

Figure 5-4. Sensitivity vs Supply Voltage

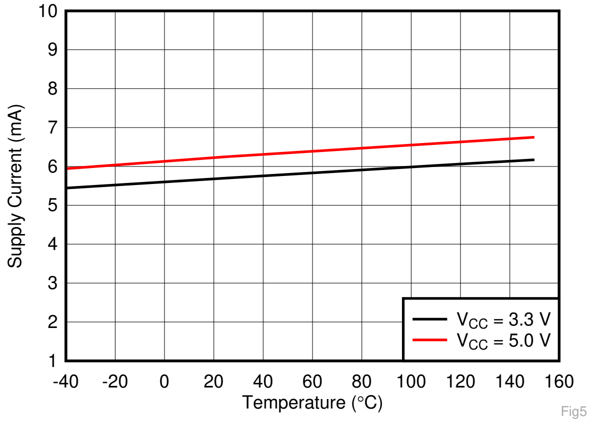
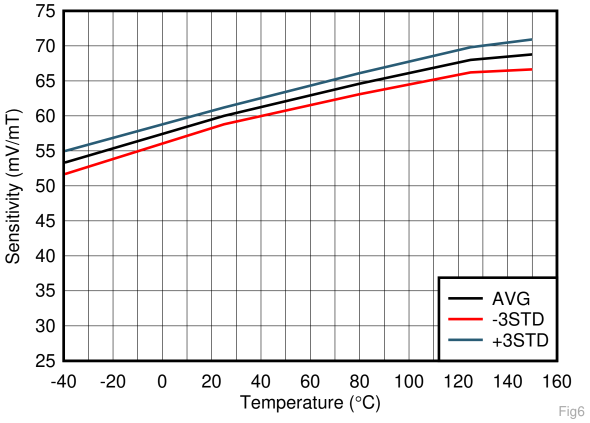


Figure 5-5. Supply Current vs. Temperature

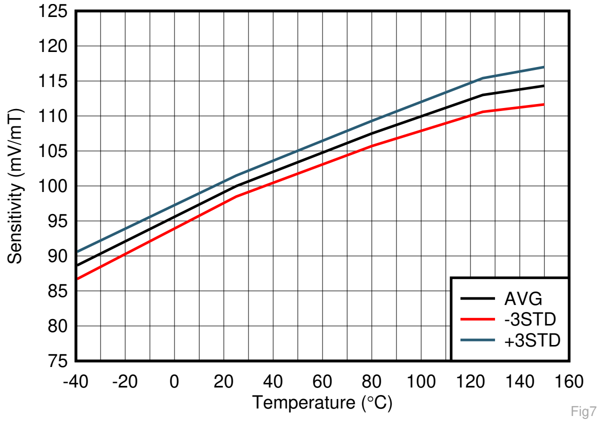


DRV5055A1, V_{CC} = 3.3 V

Figure 5-6. Sensitivity vs Temperature

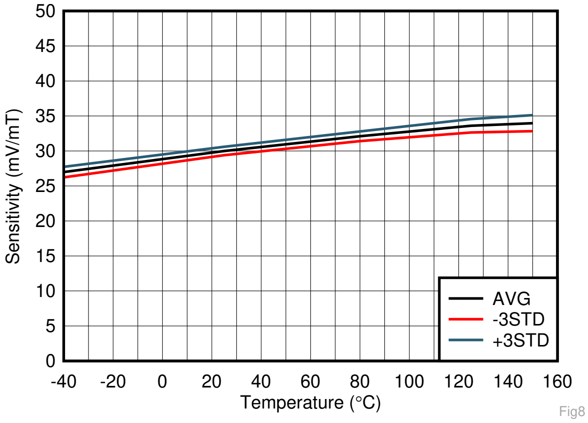
5.7 Typical Characteristics (continued)

for T_A = 25°C (unless otherwise noted)



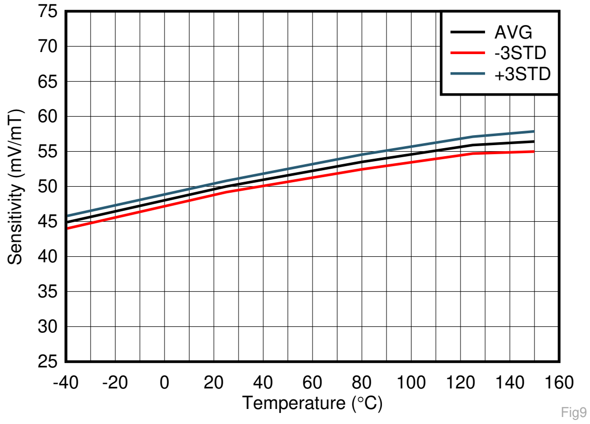
DRV5055A1, V_{CC} = 5.0 V

Figure 5-7. Sensitivity vs Temperature



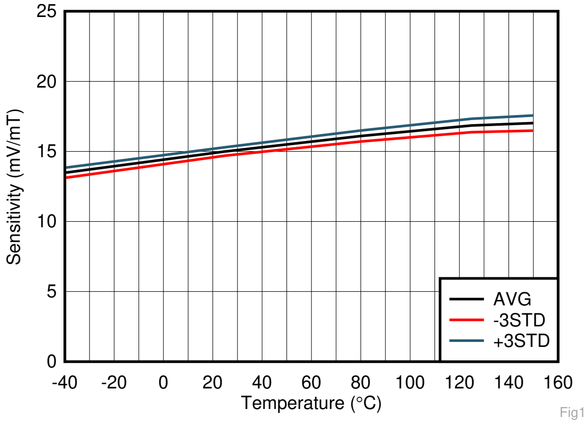
DRV5055A2, V_{CC} = 3.3 V

Figure 5-8. Sensitivity vs Temperature



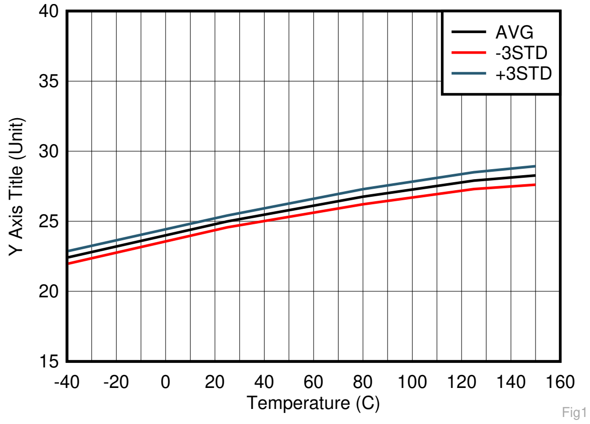
DRV5055A2, V_{CC} = 5.0 V

Figure 5-9. Sensitivity vs. Temperature



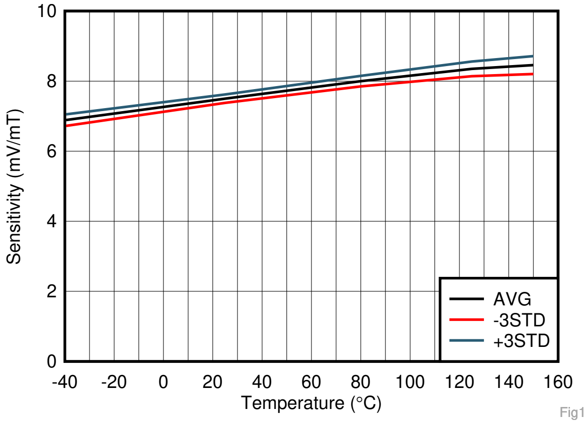
DRV5055A3, V_{CC} = 3.3 V

Figure 5-10. Sensitivity vs. Temperature



DRV5055A3, V_{CC} = 5.0 V

Figure 5-11. Sensitivity vs. Temperature

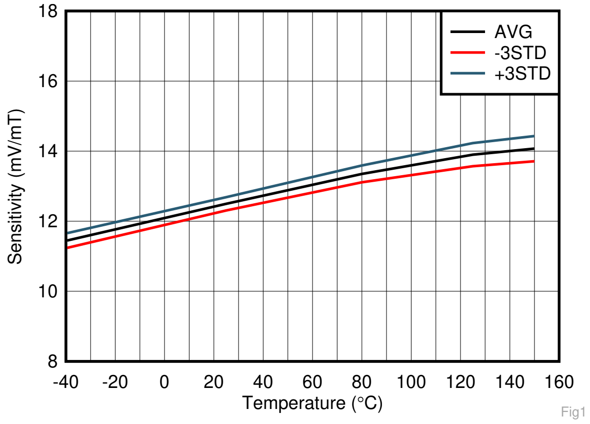


DRV5055A4, V_{CC} = 3.3 V

Figure 5-12. Sensitivity vs. Temperature

5.7 Typical Characteristics (continued)

for T_A = 25°C (unless otherwise noted)



DRV5055A4, V_{CC} = 5.0 V

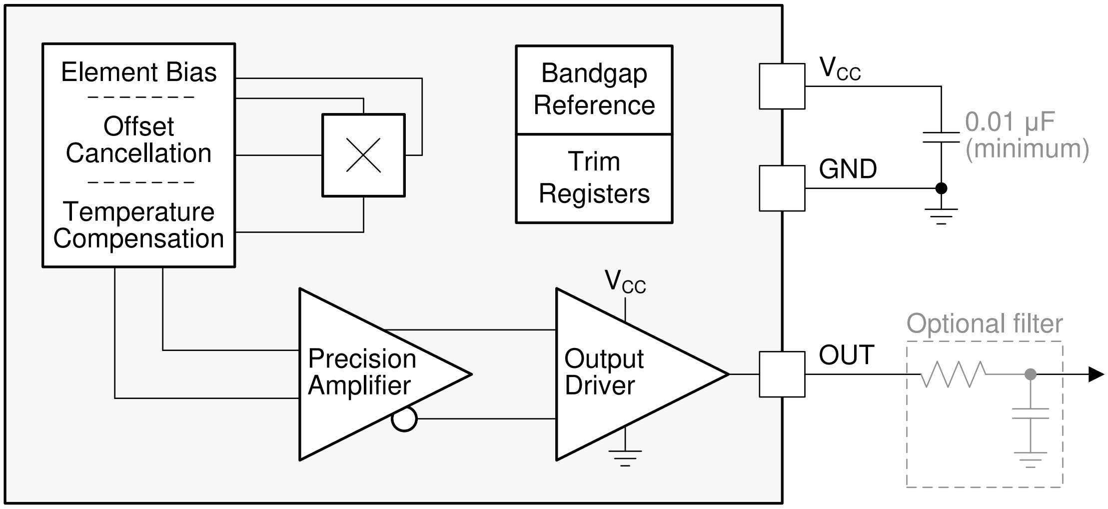
Figure 5-13. Sensitivity vs Temperature

6 Detailed Description

6.1 Overview

The DRV5055-Q1 is a 3-pin linear Hall effect sensor with fully integrated signal conditioning, temperature compensation circuits, mechanical stress cancellation, and amplifiers. The device operates from 3.3-V and 5-V (±10%) power supplies, measures magnetic flux density, and outputs a proportional analog voltage that is referenced to V_{CC}.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Magnetic Flux Direction

As shown in Figure 6-1, the DRV5055-Q1 is sensitive to the magnetic field component that is perpendicular to the top of the package.

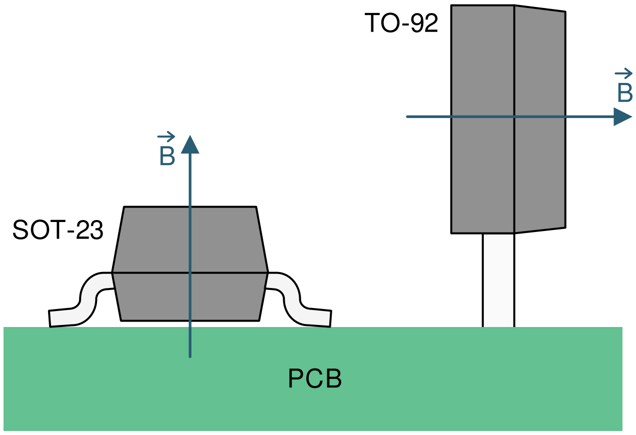


Figure 6-1. Direction of Sensitivity

Magnetic flux that travels from the bottom to the top of the package is considered positive in this document. This condition exists when a south magnetic pole is near the top (marked-side) of the package. Magnetic flux that travels from the top to the bottom of the package results in negative millitesla values.

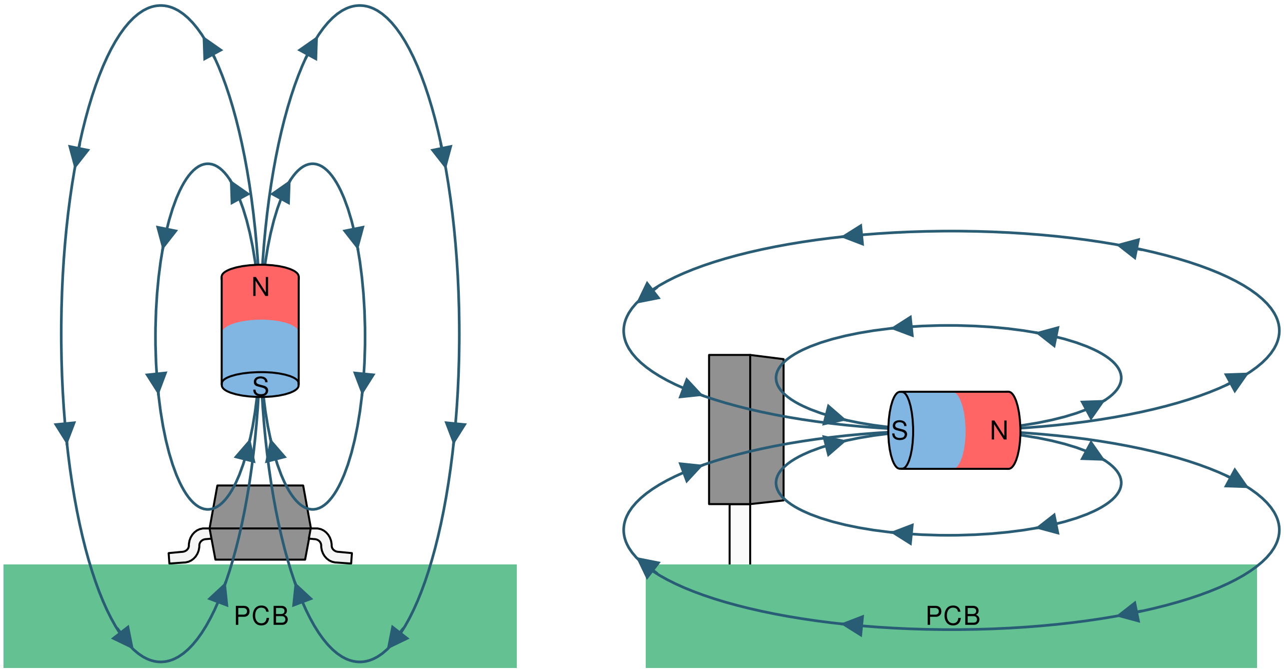


Figure 6-2. The Flux Direction for Positive B

6.3.2 Magnetic Response

When the DRV5055-Q1 is powered, the DRV5055-Q1 outputs an analog voltage according to Equation 1:

$$V_{OUT} = V_Q + B \times \left(\text{Sensitivity}_{(25°C)} \times \left(1 + S_{TC} \times \left(T_A - 25°C\right)\right)\right) \quad (1)$$

where

- V_Q is typically half of V_{CC}
- B is the applied magnetic flux density
- $\text{Sensitivity}_{(25°C)}$ depends on the device option and V_{CC}
- S_{TC} is typically 0.12%/°C for device options DRV5055A1 - DRV5055A4 and is 0%/°C for DRV5055Z2
- T_A is the ambient temperature
- V_{OUT} is within the V_L range

As an example, consider the DRV5055A3 with V_{CC} = 3.3 V, a temperature of 50°C, and 67 mT applied. Excluding tolerances, V_{OUT} = 1650 mV + 67 mT × (15 mV/mT × (1 + 0.0012/°C × (50°C – 25°C))) = 2685 mV.

6.3.3 Sensitivity Linearity

The device produces a linear response when the output voltage is within the specified V_L range. Outside this range, sensitivity is reduced and nonlinear. Figure 6-3 graphs the magnetic response.

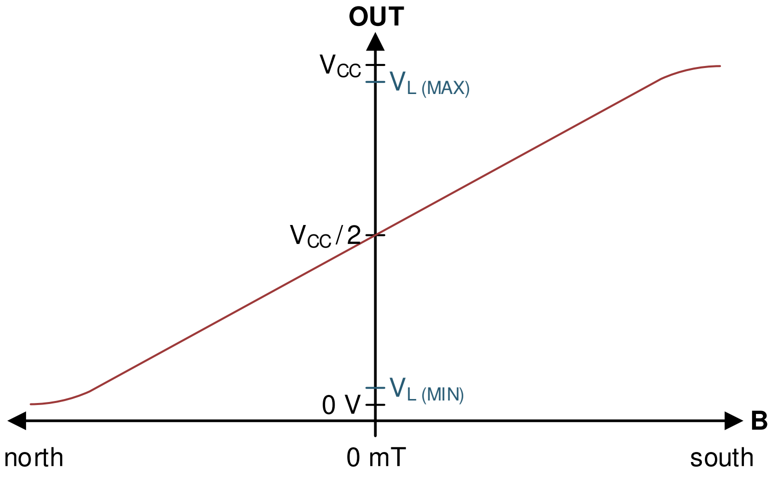


Figure 6-3. Magnetic Response

Equation 2 calculates parameter B_L, the minimum linear sensing range at 25°C taking into account the maximum quiescent voltage and sensitivity tolerances.

$$B_{L(MIN)} = \frac{V_{L(MAX)} - V_{Q(MAX)}}{S_{(MAX)}} \quad (2)$$

The parameter S_{LE} defines linearity error as the difference in sensitivity between any two positive B values, and any two negative B values, while the output is within the V_L range.

The parameter S_{SE} defines symmetry error as the difference in sensitivity between any positive B value and the negative B value of the same magnitude, while the output voltage is within the V_L range.

6.3.4 Ratiometric Architecture

The DRV5055-Q1 has a ratiometric analog architecture that scales the quiescent voltage and sensitivity linearly with the power-supply voltage. For example, the quiescent voltage and sensitivity are 5% higher when V_{CC} = 5.25 V compared to V_{CC} = 5 V. This behavior enables external ADCs to digitize a consistent value regardless of the power-supply voltage tolerance, when the ADC uses V_{CC} as its reference.

Equation 3 calculates the sensitivity ratiometry error:

$$S_{RE} = 1 - \frac{S_{(VCC)} / S_{(5V)}}{V_{CC} / 5V} \text{ for } V_{CC} = 4.5\text{ V to } 5.5\text{ V}, \qquad S_{RE} = 1 - \frac{S_{(VCC)} / S_{(3.3V)}}{V_{CC} / 3.3V} \text{ for } V_{CC} = 3\text{ V to } 3.63\text{ V} \quad (3)$$

where

- $S_{(VCC)}$ is the sensitivity at the current V_{CC} voltage
- $S_{(5V)}$ or $S_{(3.3V)}$ is the sensitivity when V_{CC} = 5 V or 3.3 V
- V_{CC} is the current V_{CC} voltage

Equation 4 calculates the quiescent voltage ratiometry error:

$$V_{QRE} = 1 - \frac{V_{Q(VCC)} / V_{Q(5V)}}{V_{CC} / 5V} \text{ for } V_{CC} = 4.5\text{ V to } 5.5\text{ V}, \qquad V_{QRE} = 1 - \frac{V_{Q(VCC)} / V_{Q(3.3V)}}{V_{CC} / 3.3V} \text{ for } V_{CC} = 3\text{ V to } 3.63\text{ V} \quad (4)$$

where

- $V_{Q(VCC)}$ is the quiescent voltage at the current V_{CC} voltage
- $V_{Q(5V)}$ or $V_{Q(3.3V)}$ is the quiescent voltage when V_{CC} = 5 V or 3.3 V
- V_{CC} is the current V_{CC} voltage

6.3.5 Operating V_{CC} Ranges

The DRV5055-Q1 has two recommended operating V_{CC} ranges: 3 V to 3.63 V and 4.5 V to 5.5 V. When V_{CC} is in the middle region between 3.63 V to 4.5 V, the device continues to function, but sensitivity is less known because there is a crossover threshold near 4 V that adjusts device characteristics.

6.3.6 Sensitivity Temperature Compensation for Magnets

Magnets generally produce weaker fields as temperature increases. The DRV5055-Q1 compensates by increasing sensitivity with temperature, as defined by the parameter S_{TC}. For device options DRV5055A1 - DRV5055A4, the sensitivity at T_A = 150°C is typically 12% higher than at T_A = 25°C. For device options DRV5055Z2, the sensitivity at T_A = 150°C is typically same as the value at T_A = 25°C.

6.3.7 Power-On Time

After the V_{CC} voltage is applied, the DRV5055-Q1 requires a short initialization time before the output is set. The parameter t_{ON} describes the time from when V_{CC} crosses 3 V until OUT is within 5% of V_Q, with 0 mT applied and no load attached to OUT. Figure 6-4 shows this timing diagram.

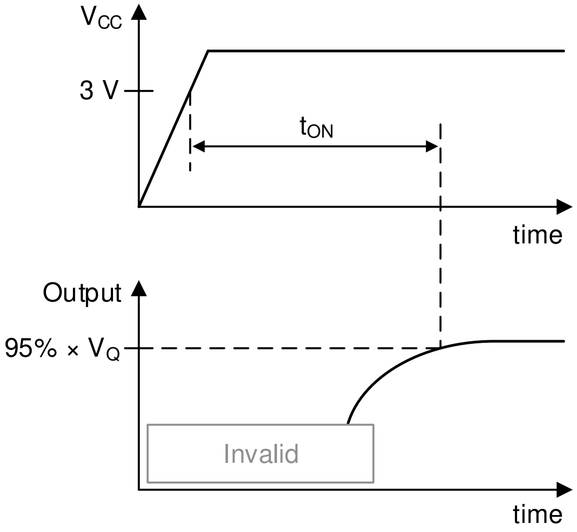


Figure 6-4. t_{ON} Definition

6.3.8 Hall Element Location

Figure 6-5 shows the location of the sensing element inside each package option.

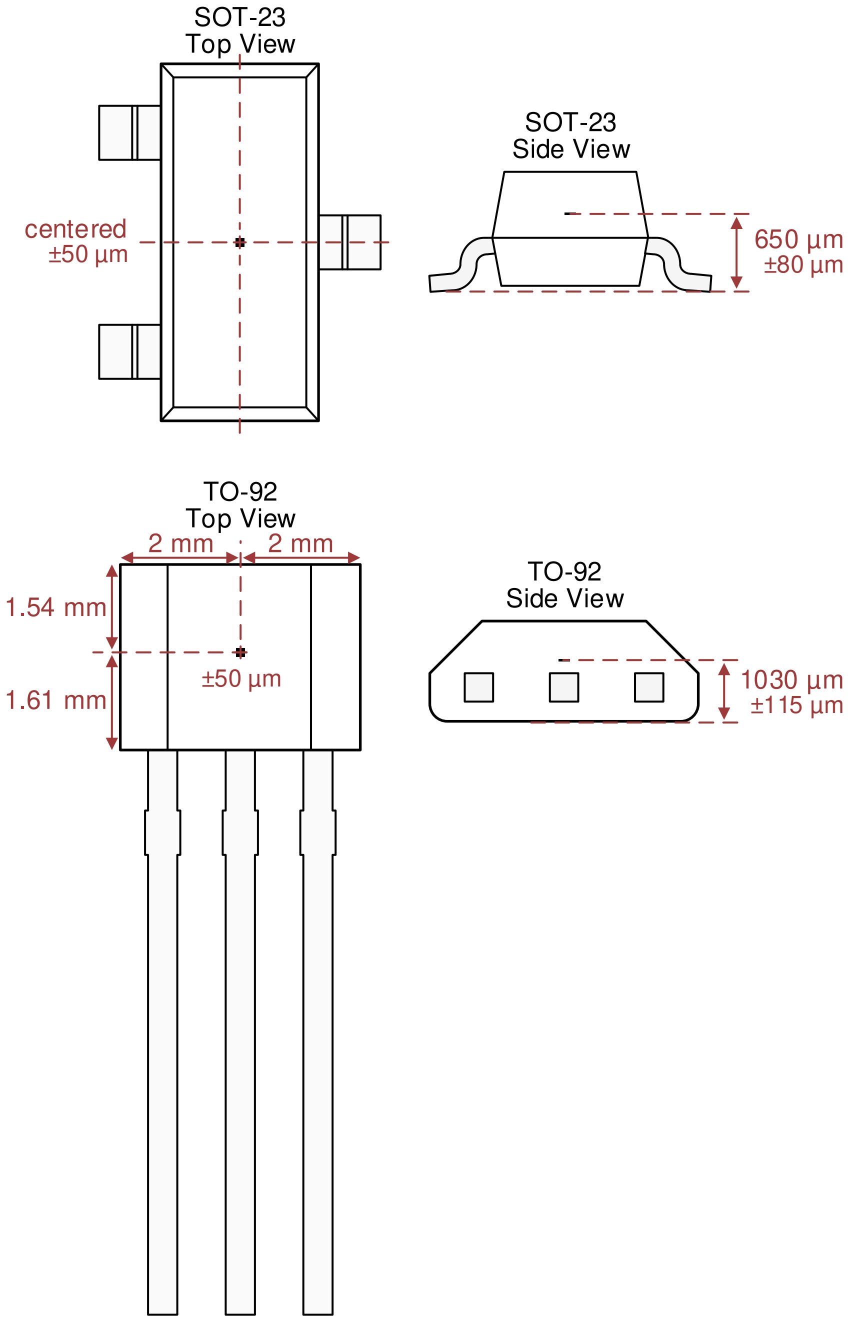


Figure 6-5. Hall Element Location

6.4 Device Functional Modes

The DRV5055-Q1 has one mode of operation that applies when the *Recommended Operating Conditions* are met.

7 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

7.1.1 Selecting the Sensitivity Option

Select the highest DRV5055-Q1 sensitivity option that can measure the required range of magnetic flux density, so that the output voltage swing is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations at https://www.ti.com/product/drv5013.

7.1.2 Temperature Compensation for Magnets

The DRV5055-Q1 temperature compensation is designed to directly compensate the average drift of neodymium (NdFeB) magnets and partially compensate ferrite magnets. The residual induction (B_r) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite. When the operating temperature of a system is reduced, temperature drift errors are also reduced.

7.1.3 Adding a Low-Pass Filter

As shown in *Functional Block Diagram*, an RC low-pass filter can be added to the device output for the purpose of minimizing voltage noise when the full 20-kHz bandwidth is not needed. This filter can improve the signal-to-noise ratio (SNR) and overall accuracy. Do not connect a capacitor directly to the device output without a resistor in between because doing so can make the output unstable.

7.1.4 Designing for Wire Break Detection

Some systems must detect if interconnect wires become open or shorted. The DRV5055-Q1 can support this function.

First, select a sensitivity option that causes the output voltage to stay within the V_L range during normal operation. Second, add a pullup resistor between OUT and V_{CC}. TI recommends a value between 20 kΩ to 100 kΩ, and the current through OUT must not exceed the I_O specification, including current going into an external ADC. Then, if the output voltage is ever measured to be within 150 mV of V_{CC} or GND, a fault condition exists. Figure 7-1 shows the circuit, and Table 7-1 describes fault scenarios.

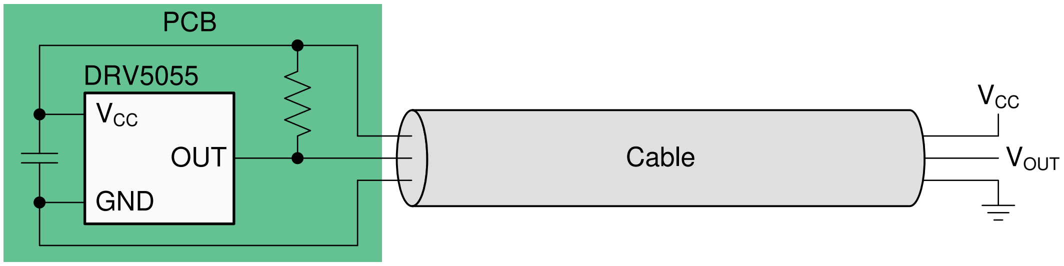


Figure 7-1. Wire Fault Detection Circuit

Table 7-1. Fault Scenarios and the Resulting V_{OUT}

FAULT SCENARIO	V_{OUT}
V_{CC} disconnects	Close to GND
GND disconnects	Close to V_{CC}
V_{CC} shorts to OUT	Close to V_{CC}
GND shorts to OUT	Close to GND

7.2 Typical Application

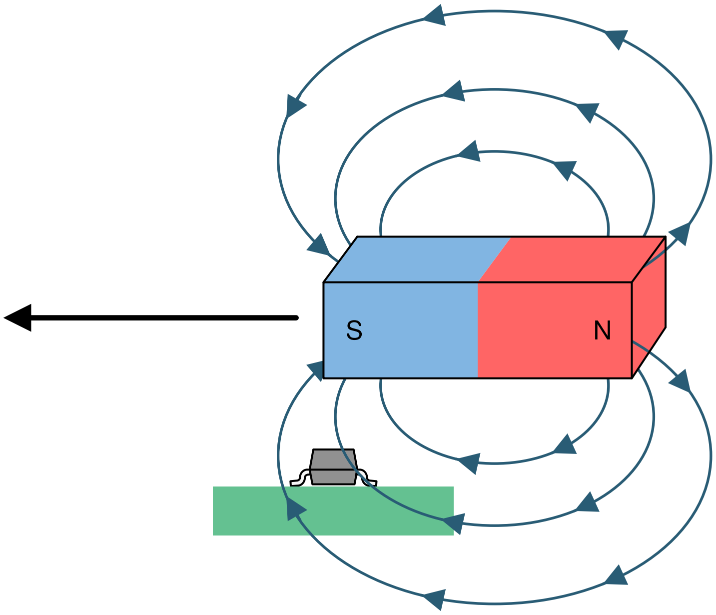


Figure 7-2. Common Magnet Orientation

7.2.1 Design Requirements

Use the parameters listed in Table 7-2 for this design example.

Table 7-2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
V_{CC}	5 V
Magnet	15 × 5 × 5 mm NdFeB
Travel distance	12 mm
Maximum B at the sensor at 25°C	±75 mT
Device option	DRV5055A3

7.2.2 Detailed Design Procedure

Linear Hall effect sensors provide flexibility in mechanical design, because many possible magnet orientations and movements produce a usable response from the sensor. Figure 7-2 shows one of the most common orientations, which uses the full north to south range of the sensor and causes a close-to-linear change in magnetic flux density as the magnet moves across.

When designing a linear magnetic sensing system, always consider these three variables: the magnet, sensing distance, and the range of the sensor. Select the DRV5055-Q1 with the highest sensitivity that has a B_L (linear magnetic sensing range) that is larger than the maximum magnetic flux density in the application. To determine the magnetic flux density the sensor receives, TI recommends using magnetic field simulation software, referring to magnet specifications, and testing.

7.2.3 Application Curve

Figure 7-3 shows the simulated magnetic flux from a NdFeB magnet.

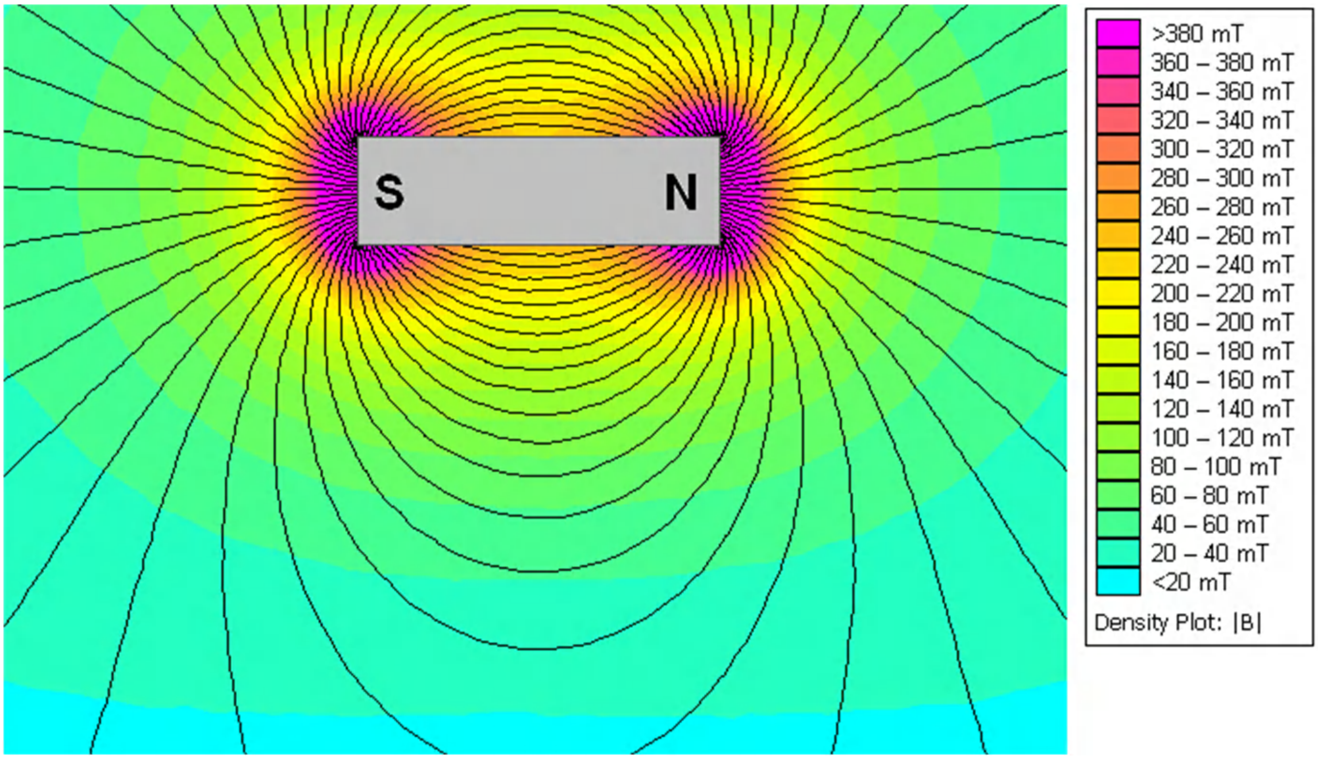


Figure 7-3. Simulated Magnetic Flux

7.3 Best Design Practices

The Hall element is sensitive to magnetic fields that are perpendicular to the top of the package, therefore a correct magnet approach must be used for the sensor to detect the field. Figure 7-4 shows correct and incorrect approaches.

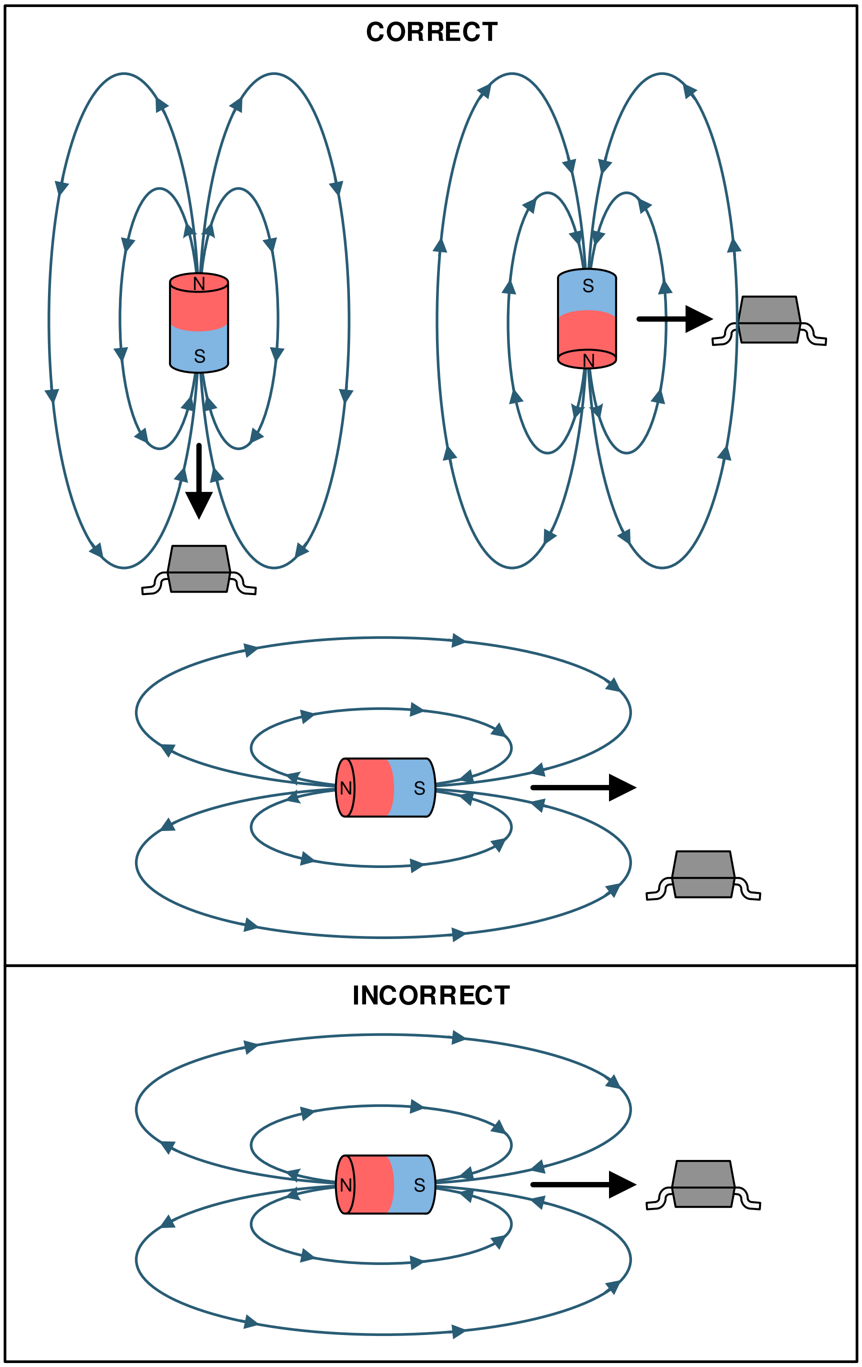


Figure 7-4. Correct and Incorrect Magnet Approaches

7.4 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01 µF.

7.5 Layout

7.5.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed circuit boards, which makes placing the magnet on the opposite side possible.

7.5.2 Layout Examples

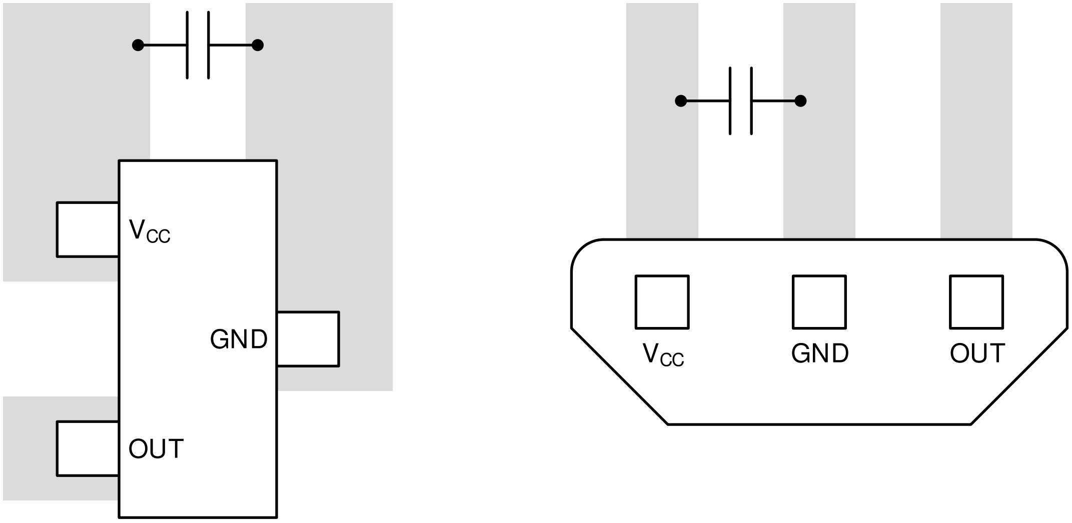


Figure 7-5. Layout Examples

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *Overview Using Linear Hall Effect Sensors to Measure Angle* application brief
- Texas Instruments, *Incremental Rotary Encoder Design Considerations* application brief

8.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

8.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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8.4 Trademarks

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8.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (July 2018) to Revision D (June 2024)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	1
• Changed *Device Information* table to *Package Information*	1
• Changed number of sensitivity options from five to various in *Description*	1
• Added the Z2 device variant to the data sheet	1
• Changed *Dos and Donts* table to *Best Design Practices*	18

Changes from Revision B (January 2018) to Revision C (July 2018)	Page
• Released to production	1

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV5055A1EDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	55A1Z	Samples
DRV5055A1ELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	55A1Z	Samples
DRV5055A1ELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	55A1Z	Samples
DRV5055A2EDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	55A2Z	Samples
DRV5055A2ELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	55A2Z	Samples
DRV5055A2ELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	55A2Z	Samples
DRV5055A3EDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	55A3Z	Samples
DRV5055A3ELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	55A3Z	Samples
DRV5055A3ELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	55A3Z	Samples
DRV5055A4EDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 150	55A4Z	Samples
DRV5055A4ELPGMQ1	ACTIVE	TO-92	LPG	3	3000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	55A4Z	Samples
DRV5055A4ELPGQ1	ACTIVE	TO-92	LPG	3	1000	RoHS & Green	SN	N / A for Pkg Type	-40 to 150	55A4Z	Samples
DRV5055Z2EDBZRQ1	ACTIVE	SOT-23	DBZ	3	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 150	55Z2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF DRV5055-Q1 :

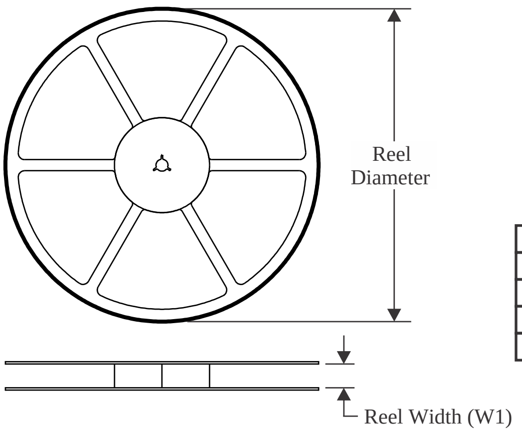
- Catalog : DRV5055

NOTE: Qualified Version Definitions:

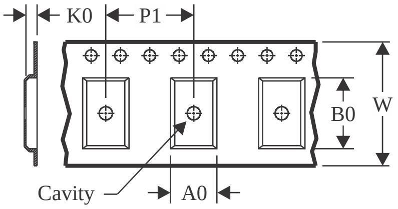
  - Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

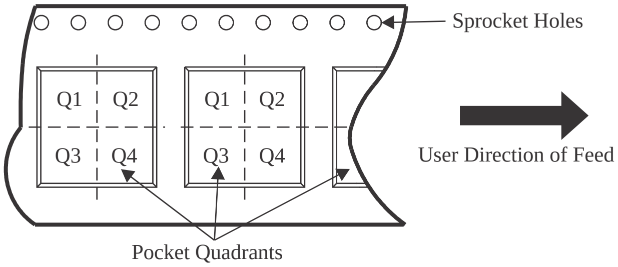


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

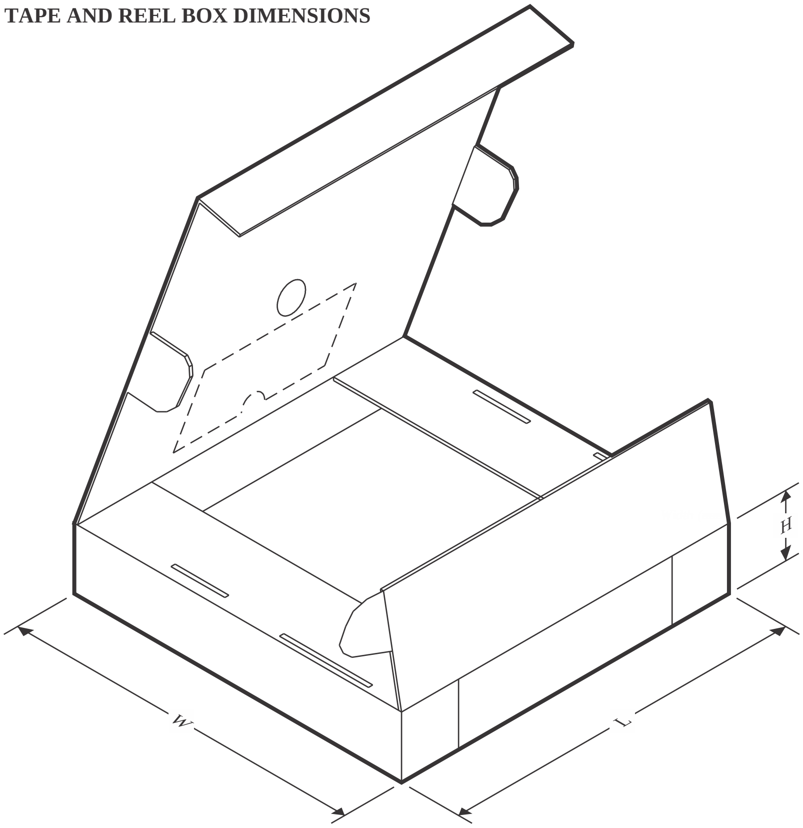
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

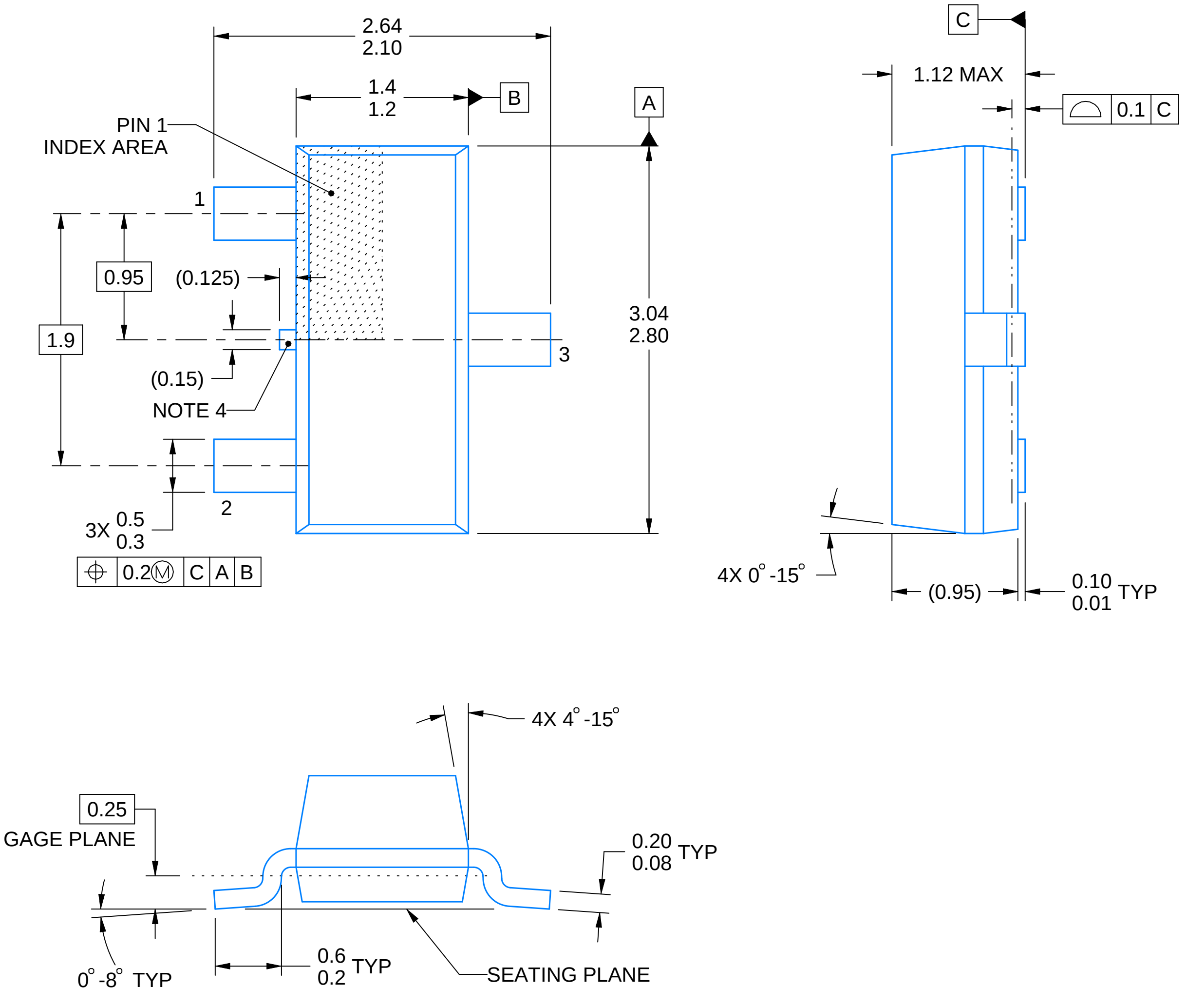
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV5055A1EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A2EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A3EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055A4EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.15	2.77	1.22	4.0	8.0	Q3
DRV5055Z2EDBZRQ1	SOT-23	DBZ	3	3000	180.0	8.4	3.2	2.85	1.3	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV5055A1EDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055A2EDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055A3EDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055A4EDBZRQ1	SOT-23	DBZ	3	3000	213.0	191.0	35.0
DRV5055Z2EDBZRQ1	SOT-23	DBZ	3	3000	210.0	185.0	35.0



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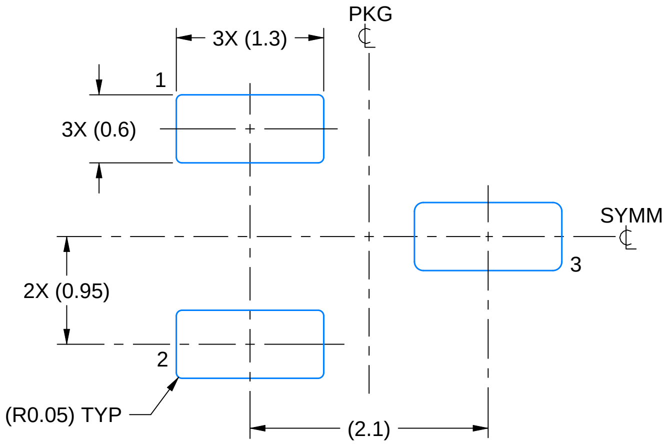
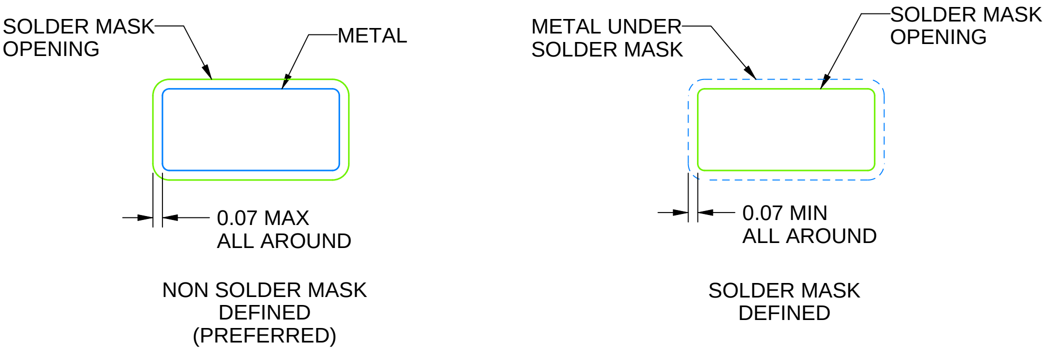
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration TO-236, except minimum foot length.
4. Support pin may differ or may not be present.
5. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side



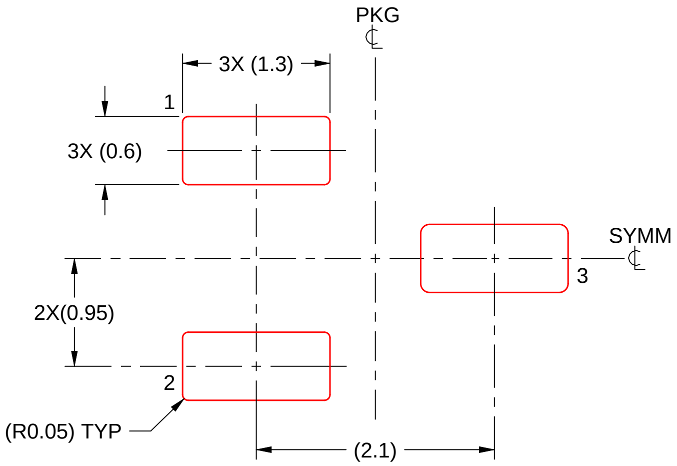
LAND PATTERN EXAMPLE
SCALE:15X



SOLDER MASK DETAILS

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

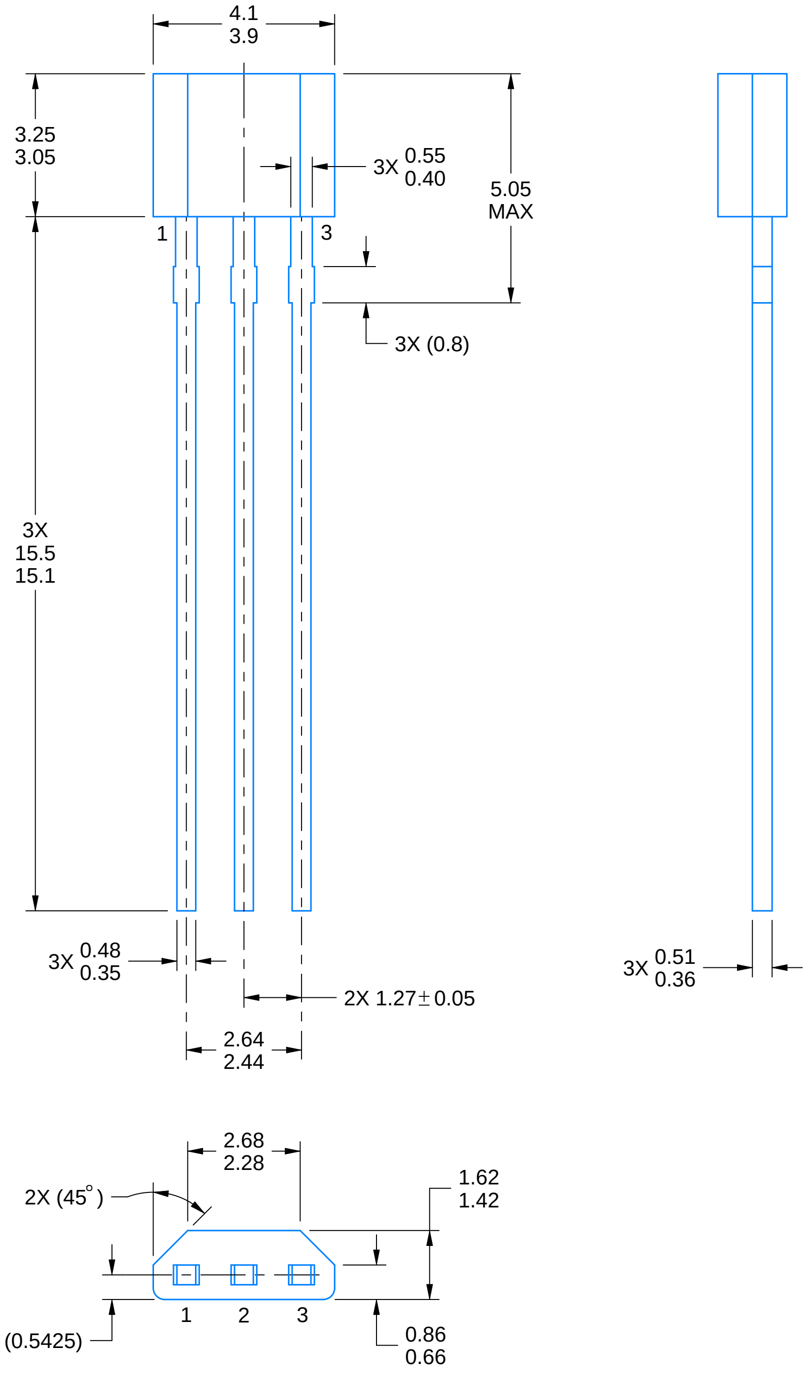
NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

TO-92 - 5.05 mm max height

TRANSISTOR OUTLINE



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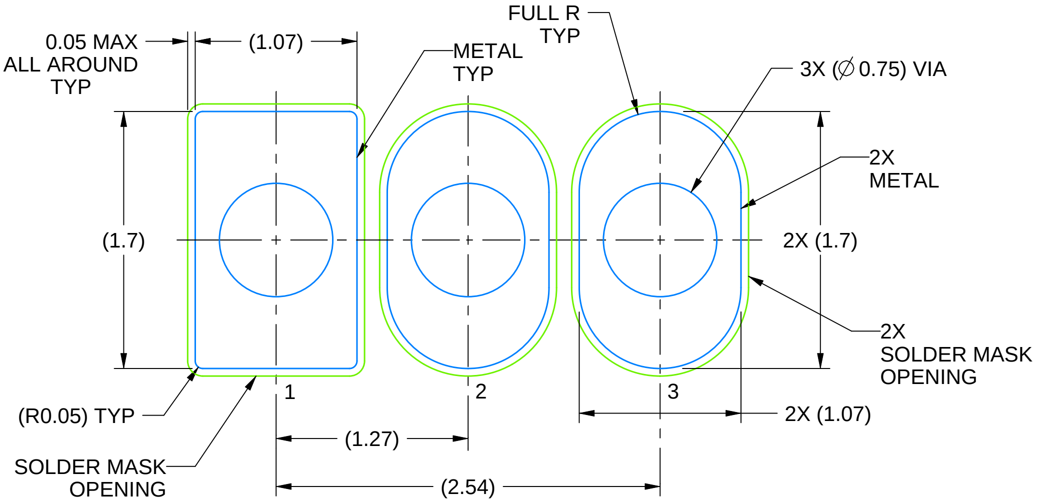
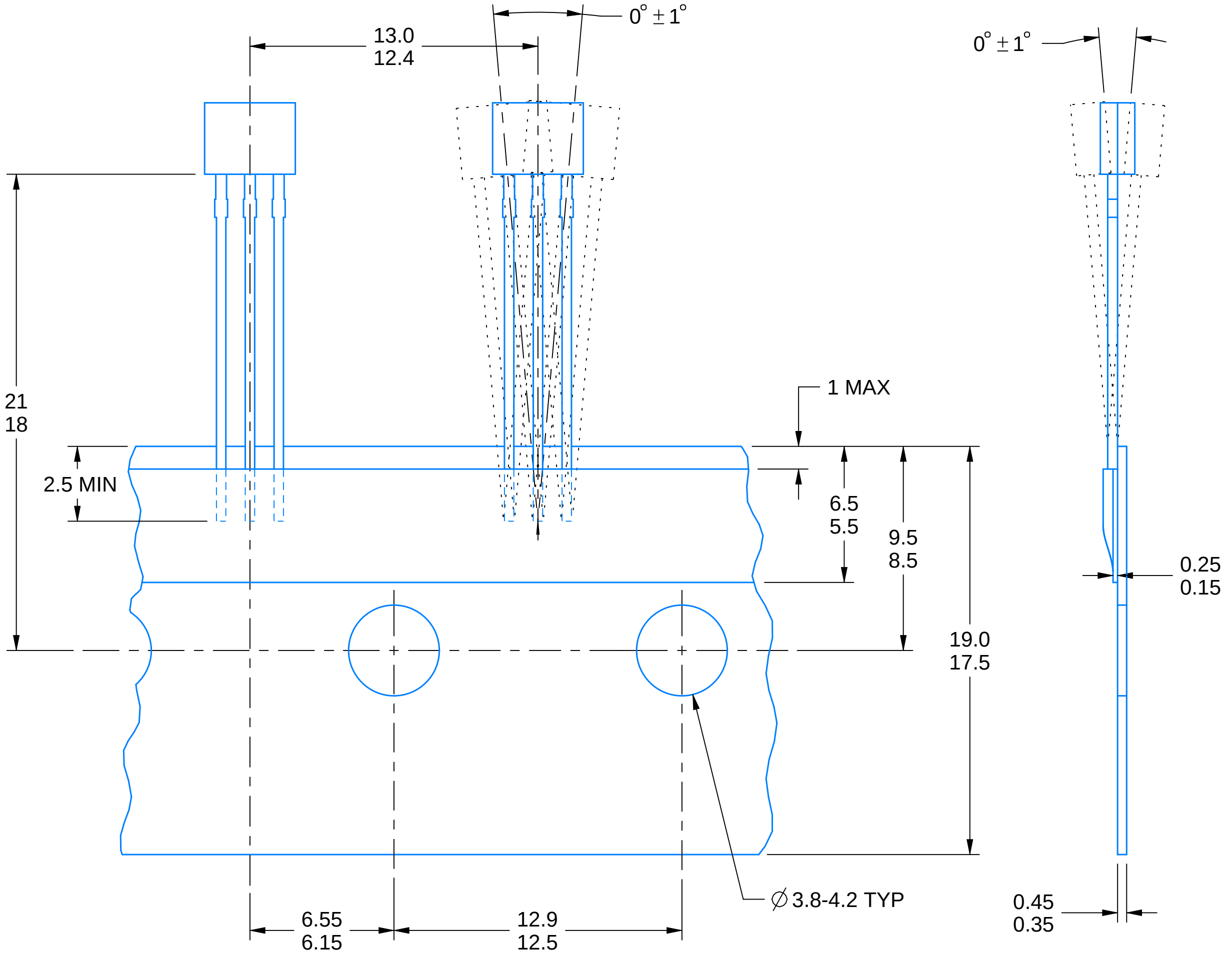
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE:20X



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