FEATURES

- ±3-A Maximum Output Current
- Low Supply Voltage Operation: 2.8 V to 5.5 V
- High Efficiency Generates Less Heat
- Over-Current and Thermal Protection
- Fault Indicators for Over-Current, Thermal and Under-Voltage Conditions
- Two Selectable Switching Frequencies
- Internal or External Clock Sync
- PWM Scheme Optimized for EMI
- 9x9 mm PowerPAD™ Quad Flatpack

APPLICATIONS

- Thermoelectric Cooler (TEC) Driver
- Laser Diode Biasing

DESCRIPTION

The DRV591 is a high-efficiency, high-current power amplifier ideal for driving a wide variety of thermoelectric cooler elements in systems powered from 2.8 V to 5.5 V. PWM operation and low output stage on-resistance significantly decrease power dissipation in the amplifier.

The DRV591 is internally protected against thermal and current overloads. Logic-level fault indicators signal when the junction temperature has reached approximately 130°C to allow for system-level shutdown before the amplifier’s internal thermal shutdown circuitry activates. The fault indicators also signal when an over-current event has occurred. If the over-current circuitry is tripped, the DRV591 automatically resets (see application information section for more details).

The PWM switching frequency may be set to 500 kHz or 100 kHz depending on system requirements. To eliminate external components, the gain is fixed at approximately 2.3 V/V.
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

**ABSOLUTE MAXIMUM RATINGS**

over operating free-air temperature range unless otherwise noted

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, AVDD, PVDD</td>
<td>–</td>
<td>–0.3 to 5.5</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Input voltage, VI</td>
<td>–</td>
<td>–0.3 to VDD + 0.3</td>
<td>–</td>
<td>V</td>
</tr>
<tr>
<td>Output current, IO (FAULT0, FAULT1)</td>
<td>–</td>
<td>1</td>
<td>–</td>
<td>mA</td>
</tr>
<tr>
<td>Continuous total power dissipation</td>
<td>–</td>
<td>See Dissipation Rating Table</td>
<td>–</td>
<td></td>
</tr>
<tr>
<td>Operating free-air temperature range, TA</td>
<td>–</td>
<td>–40 to 85</td>
<td>–</td>
<td>°C</td>
</tr>
<tr>
<td>Operating junction temperature range, TJ</td>
<td>–</td>
<td>–40 to 150</td>
<td>–</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature range, Tsyr</td>
<td>–</td>
<td>–65 to 165</td>
<td>–</td>
<td>°C</td>
</tr>
</tbody>
</table>

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**RECOMMENDED OPERATING CONDITIONS**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>Min</th>
<th>Max</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage, AVDD, PVDD</td>
<td>–</td>
<td>2.8</td>
<td>5.5</td>
<td>V</td>
</tr>
<tr>
<td>High-level input voltage, VIH</td>
<td>–</td>
<td>–</td>
<td>FREQ, INT/EXT, SHUTDOWN, COSC</td>
<td>2</td>
</tr>
<tr>
<td>Low-level input voltage, VIL</td>
<td>–</td>
<td>–</td>
<td>FREQ, INT/EXT, SHUTDOWN, COSC</td>
<td>0.8</td>
</tr>
<tr>
<td>Operating free-air temperature, TA</td>
<td>–</td>
<td>–40</td>
<td>85</td>
<td>°C</td>
</tr>
</tbody>
</table>

**PACKAGE DISSIPATION RATINGS**

<table>
<thead>
<tr>
<th>Package</th>
<th>θJA (1)</th>
<th>θJC</th>
<th>T_A = 25°C</th>
<th>Power Rating</th>
</tr>
</thead>
<tbody>
<tr>
<td>VFP</td>
<td>29.4</td>
<td>1.2</td>
<td>4.1 W</td>
<td></td>
</tr>
</tbody>
</table>

(1) This data was taken using 2 oz trace and copper pad that is soldered directly to a JEDEC standard 4-layer 3 in × 3 in PCB.
## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range unless otherwise noted

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>TEST CONDITIONS</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Output offset voltage (measured differentially)</td>
<td>V&lt;sub&gt;I&lt;/sub&gt; = V&lt;sub&gt;DD/2&lt;/sub&gt;, I&lt;sub&gt;Q&lt;/sub&gt; = 0 A</td>
<td>14</td>
<td>100</td>
<td>mV</td>
</tr>
<tr>
<td></td>
<td>High-level input current</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.5V, V&lt;sub&gt;I&lt;/sub&gt; = V&lt;sub&gt;DD&lt;/sub&gt;</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Low-level input current</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5.5V, V&lt;sub&gt;I&lt;/sub&gt; = 0 V</td>
<td>1</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Integrated output noise voltage</td>
<td>f = 1 kHz to 10 kHz</td>
<td>40</td>
<td></td>
<td>µV</td>
</tr>
<tr>
<td></td>
<td>Common-mode voltage range</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V</td>
<td>1.2</td>
<td>3.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.3 V</td>
<td>1.2</td>
<td>2.1</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Closed-loop voltage gain</td>
<td></td>
<td>2.1</td>
<td>2.34</td>
<td>2.6</td>
</tr>
<tr>
<td></td>
<td>Voltage output (measured differentially)</td>
<td>I&lt;sub&gt;Q&lt;/sub&gt; = ±1 A, r&lt;sub&gt;DS(on)&lt;/sub&gt; = 65 mΩ, V&lt;sub&gt;DD&lt;/sub&gt; = 5 V</td>
<td>4.87</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>I&lt;sub&gt;Q&lt;/sub&gt; = ±3 A, r&lt;sub&gt;DS(on)&lt;/sub&gt; = 65 mΩ, V&lt;sub&gt;DD&lt;/sub&gt; = 5 V</td>
<td>4.61</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Drain-source on-state resistance</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V, I&lt;sub&gt;Q&lt;/sub&gt; = 4 A, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>High side</td>
<td>25</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low side</td>
<td>25</td>
<td>65</td>
<td>95</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.3 V, I&lt;sub&gt;Q&lt;/sub&gt; = 4 A, T&lt;sub&gt;A&lt;/sub&gt; = 25°C</td>
<td>High side</td>
<td>25</td>
<td>80</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Low side</td>
<td>25</td>
<td>90</td>
<td>140</td>
</tr>
<tr>
<td></td>
<td>Maximum continuous current output</td>
<td></td>
<td>3</td>
<td></td>
<td>A</td>
</tr>
<tr>
<td></td>
<td>Status flag output pins (FAULT0, FAULT1)</td>
<td>Sinking 200 µA</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Fault active (open drain output)</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>External clock frequency range</td>
<td>For 500 kHz operation</td>
<td>225</td>
<td>250</td>
<td>275</td>
</tr>
<tr>
<td></td>
<td></td>
<td>For 100 kHz operation</td>
<td>45</td>
<td>50</td>
<td>55</td>
</tr>
<tr>
<td></td>
<td>Quiescent current</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V, No load or filter</td>
<td>2</td>
<td>6.2</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td></td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 3.3 V, No load or filter</td>
<td>2</td>
<td>4.6</td>
<td>8</td>
</tr>
<tr>
<td></td>
<td>Quiescent current in shutdown mode</td>
<td>V&lt;sub&gt;DD&lt;/sub&gt; = 5 V, SHUTDOWN = 0.8 V</td>
<td>0</td>
<td>0.1</td>
<td>50</td>
</tr>
<tr>
<td></td>
<td>Output resistance in shutdown</td>
<td>SHUTDOWN = 0.8 V</td>
<td>2</td>
<td></td>
<td>kΩ</td>
</tr>
<tr>
<td></td>
<td>Power-on threshold</td>
<td></td>
<td>1.7</td>
<td>2.8</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Power-off threshold</td>
<td></td>
<td>1.6</td>
<td>2.6</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td>Thermal trip point</td>
<td>FAULT0 active</td>
<td>130</td>
<td></td>
<td>°C</td>
</tr>
<tr>
<td></td>
<td>Input impedance (IN+, IN–)</td>
<td></td>
<td>100</td>
<td></td>
<td>kΩ</td>
</tr>
</tbody>
</table>

## PIN ASSIGNMENTS

![PIN ASSIGNMENTS Diagram]
### Terminal Functions

<table>
<thead>
<tr>
<th>TERMINAL NAME</th>
<th>NO.</th>
<th>I/O</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>AGND</td>
<td>2</td>
<td>I</td>
<td>Analog ground</td>
</tr>
<tr>
<td>AREF</td>
<td>5</td>
<td>O</td>
<td>Connect 1 µF capacitor to ground for AREF voltage filtering</td>
</tr>
<tr>
<td>AVDD</td>
<td>1</td>
<td>I</td>
<td>Analog power supply</td>
</tr>
<tr>
<td>COSC</td>
<td>4</td>
<td>I</td>
<td>Connect capacitor to ground to set oscillation frequency (220 pF for 500 kHz, 1 nF for 100 kHz) when the internal oscillator is selected; connect clock signal when an external oscillator is used</td>
</tr>
<tr>
<td>FAULT0</td>
<td>10</td>
<td>O</td>
<td>Fault flag 0, low when active open drain output (see application information)</td>
</tr>
<tr>
<td>FAULT1</td>
<td>9</td>
<td>O</td>
<td>Fault flag 1, high when active open drain output (see application information)</td>
</tr>
<tr>
<td>FREQ</td>
<td>32</td>
<td>I</td>
<td>Selects 500 kHz switching frequency when a TTL logic low is applied to this terminal; selects 100 kHz switching frequency when a TTL logic high is applied</td>
</tr>
<tr>
<td>IN–</td>
<td>7</td>
<td>I</td>
<td>Negative differential input</td>
</tr>
<tr>
<td>IN+</td>
<td>6</td>
<td>I</td>
<td>Positive differential input</td>
</tr>
<tr>
<td>INT/EXT</td>
<td>31</td>
<td>I</td>
<td>Selects the internal oscillator when a TTL logic high is applied to this terminal; selects the use of an external oscillator when a TTL logic low is applied to this terminal</td>
</tr>
<tr>
<td>OUT–</td>
<td>14, 15, 16, 17</td>
<td>O</td>
<td>Negative bridge-tied load (BTL) output (4 pins)</td>
</tr>
<tr>
<td>OUT+</td>
<td>24, 25, 26, 27</td>
<td>O</td>
<td>Positive bridge-tied load (BTL) output (4 pins)</td>
</tr>
<tr>
<td>PGND</td>
<td>18, 19, 20, 21, 22, 23</td>
<td>O</td>
<td>High-current ground (6 pins)</td>
</tr>
<tr>
<td>PVDD</td>
<td>11, 12, 13, 28, 29, 30</td>
<td>I</td>
<td>High-current power supply (6 pins)</td>
</tr>
<tr>
<td>ROSC</td>
<td>3</td>
<td>I</td>
<td>Connect 120-kΩ resistor to AGND to set oscillation frequency (either 500 kHz or 100 kHz). Not needed if an external clock is used.</td>
</tr>
<tr>
<td>SHUTDOWN</td>
<td>8</td>
<td>I</td>
<td>Places the amplifier in shutdown mode when a TTL logic low is applied to this terminal; places the amplifier in normal operation when a TTL logic high is applied</td>
</tr>
</tbody>
</table>
FUNCTIONAL BLOCK DIAGRAM

IN

IN+

AGND

2.34 × R

2.34 × R

R

R

AVDD

PVDD

OUT−

PGND

PVDD

OUT+

PGND

SHUTDOWN

INT/EXT

FREQ

COSC

ROSC

AREF

TTL Input Buffer

Biases and References

Ramp Generator

Gate Drive

Gate Drive

Start-Up Protection Logic

OC Detect

Thermal

VDDok

FAULT0

FAULT1
TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
<th>FIGURE</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>vs Load resistance</td>
<td>2, 3</td>
</tr>
<tr>
<td>rDS(on)</td>
<td>Drain-source on-state resistance</td>
<td></td>
</tr>
<tr>
<td></td>
<td>vs Supply voltage</td>
<td>4</td>
</tr>
<tr>
<td></td>
<td>vs Free-air temperature</td>
<td>5</td>
</tr>
<tr>
<td></td>
<td>vs Free-air temperature</td>
<td>6</td>
</tr>
<tr>
<td>IQ</td>
<td>Supply current</td>
<td>7</td>
</tr>
<tr>
<td>PSRR</td>
<td>Power supply rejection ratio</td>
<td>8, 9</td>
</tr>
<tr>
<td>Closed loop response</td>
<td></td>
<td></td>
</tr>
<tr>
<td>IO</td>
<td>Maximum output current</td>
<td>12</td>
</tr>
<tr>
<td></td>
<td>vs Output voltage</td>
<td></td>
</tr>
<tr>
<td></td>
<td>vs Ambient temperature</td>
<td>13</td>
</tr>
<tr>
<td>VIO</td>
<td>Input offset voltage</td>
<td>14, 15</td>
</tr>
<tr>
<td></td>
<td>Common-mode input voltage</td>
<td></td>
</tr>
</tbody>
</table>

TEST SET-UP FOR GRAPHS

The LC output filter used in Figures 2, 3, 8, and 9 is shown below.

![LC Output Filter Diagram](image)

L1, L2 = 10 µH (part number: CDRH104R, manufacturer: Sumida)
C1, C2 = 10 µF (part number: ECJ-4YB1C106K, manufacturer: Panasonic)

**Figure 1. LC Output Filter**
TYPICAL CHARACTERISTICS

**EFFICIENCY vs LOAD RESISTANCE**

- **Figure 2**
  - Efficiency vs Load Resistance
  - $V_{DD} = 5\, V$
  - $f_s = 500\, kHz$
  - $P_O = 0.5\, W$
  - $P_O = 1\, W$
  - $P_O = 2\, W$

- **Figure 3**
  - Efficiency vs Load Resistance
  - $V_{DD} = 3.3\, V$
  - $f_s = 500\, kHz$
  - $P_O = 0.25\, W$
  - $P_O = 0.5\, W$
  - $P_O = 1\, W$

**DRAIN-SOURCE ON-STATE RESISTANCE vs SUPPLY VOLTAGE**

- **Figure 4**
  - $I_O = 1\, A$
  - $T_A = 25\, ^\circ C$
  - $R_{DS(on)}$ vs $V_{DD}$
  - Total
  - Low Side
  - High Side

**DRAIN-SOURCE ON-STATE RESISTANCE vs FREE-AIR TEMPERATURE**

- **Figure 5**
  - $V_{DD} = 5\, V$
  - $I_O = 1\, A$
  - $VFP\, Package$
  - Free-Air Temperature
  - Total
  - Low Side
  - High Side
TYPICAL CHARACTERISTICS

DRAIN-SOURCE ON-STATE RESISTANCE vs FREE-AIR TEMPERATURE

![Figure 6](image6)

SUPPLY CURRENT vs SUPPLY VOLTAGE

![Figure 7](image7)

POWER SUPPLY REJECTION RATIO vs FREQUENCY

![Figure 8](image8)

POWER SUPPLY REJECTION RATIO vs FREQUENCY

![Figure 9](image9)
TYPICAL CHARACTERISTICS

CLOSED LOOP RESPONSE

Figure 10

CLOSED LOOP RESPONSE

Figure 11
TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT CURRENT vs OUTPUT VOLTAGE

Figure 12

MAXIMUM OUTPUT CURRENT vs AMBIENT TEMPERATURE

Figure 13

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

Figure 14

INPUT OFFSET VOLTAGE vs COMMON-MODE INPUT VOLTAGE

Figure 15
OUTPUT FILTER CONSIDERATIONS

TEC element manufacturers provide electrical specifications for maximum dc current and maximum output voltage for each particular element. The maximum ripple current, however, is typically only recommended to be less than 10% with no reference to the frequency components of the current. The maximum temperature differential across the element, which decreases as ripple current increases, may be calculated with the following equation:

\[ \Delta T = \frac{1}{1 + N^2} \times \Delta T_{\text{max}} \]  

(1)

Where:
- \( \Delta T \) = actual temperature differential
- \( \Delta T_{\text{max}} \) = maximum temperature differential
- \( N \) = ratio of ripple current to dc current

According to this relationship, a 10% ripple current reduces the maximum temperature differential by 1%. An LC network may be used to filter the current flowing to the TEC to reduce the amount of ripple and, more importantly, protect the rest of the system from any electromagnetic interference (EMI).

Any filter should always be placed as close as possible to the DRV591 to reduce EMI.

FILTER COMPONENT SELECTION

The LC filter, which may be designed from two different perspectives, both described below, helps estimate the overall performance of the system. The filter should be designed for the worst-case conditions during operation, which is typically when the differential output is at 50% duty cycle. The following section serves as a starting point for the design, and any calculations should be confirmed with a prototype circuit in the lab.

Any filter should always be placed as close as possible to the DRV591 to reduce EMI.
**LC FILTER IN THE FREQUENCY DOMAIN**

The transfer function for a 2nd order low-pass filter (Figures 17 and 18) is shown in equation (2):

\[
H_{LP}(j\omega) = \frac{1}{\left( \frac{\omega}{\omega_0} \right)^2 + \frac{1}{Q} \frac{j\omega}{\omega_0} + 1}
\]  

\( \omega_0 = \frac{1}{\sqrt{LC}} \)

\( Q = \text{quality factor} \)

\( \omega = \text{DRV591 switching frequency} \)

For the DRV591, the differential output switching frequency is typically selected to be 500 kHz. The resonant frequency for the filter is typically chosen to be at least one order of magnitude lower than the switching frequency. Equation (2) may then be simplified to give the following magnitude equation (3). These equations assume the use of the filter in Figure 17.

\[
\left| H_{LP} \right|_{dB} = -40 \log \left( \frac{f_s}{f_o} \right)
\]  

\( f_o = \frac{1}{2\pi\sqrt{LC}} \)

\( f_s = 500 \text{ kHz (DRV591 switching frequency)} \)

If \( L=10 \mu H \) and \( C=10 \mu F \), the cutoff frequency is 15.9 kHz, which corresponds to \(-60 \text{ dB of attenuation at the 500 kHz switching frequency. For VDD = 5 V, the amount of ripple voltage at the TEC element is approximately 5 mV.} \)

The average TEC element has a resistance of 1.5 \( \Omega \), so the ripple current through the TEC is approximately 3.4 mA. At the 3-A maximum output current of the DRV591, this 5.4 mA corresponds to 0.11% ripple current, causing less than 0.0001% reduction of the maximum temperature differential of the TEC element (see equation 1).

**LC FILTER IN THE TIME DOMAIN**

The ripple current of an inductor may be calculated using equation (4):

\[
\Delta I_L = \frac{(V_O - V_{TEC})DT_s}{L}
\]  

\( D = \text{duty cycle (0.5 worst case)} \)

\( T_s = 1/f_s = 1/500 \text{ kHz} \)

For \( V_O = 5 \text{ V} \), \( V_{TEC} = 2.5 \text{ V} \), and \( L = 10 \mu H \), the inductor ripple current is 250 mA. To calculate how much of that ripple current flows through the TEC element, however, the properties of the filter capacitor must be considered.

For relatively small capacitors (less than 22 \( \mu F \)) with very low equivalent series resistance (ESR, less than 10 m\( \Omega \)), such as ceramic capacitors, the following equation (5) may be used to estimate the ripple voltage on the capacitor due to the change in charge:

\[
\Delta V_C = \frac{\pi^2}{2} \left( 1 - D \right) \left( \frac{f_o}{f_s} \right)^2 V_{TEC}
\]

\( D = \text{duty cycle} \)

\( f_s = 500 \text{ kHz} \)

\( f_o = \frac{1}{2\pi\sqrt{LC}} \)

For \( L=10 \mu H \) and \( C=10 \mu F \), the cutoff frequency, \( f_o \), is 15.9 kHz. For worst case duty cycle of 0.5 and \( V_{TEC} = 2.5 \text{ V} \), the ripple voltage on the capacitors is 6.2 mV. The ripple current may be calculated by dividing the ripple voltage by the TEC resistance of 1.5 \( \Omega \), resulting in a ripple current through the TEC element of 4.1 mA. Note that this is similar to the value calculated using the frequency domain approach.

For larger capacitors (greater than 22 \( \mu F \)) with relatively high ESR (greater than 100 m\( \Omega \)), such as electrolytic capacitors, the ESR dominates over the charging-discharging of the capacitor. The following simple equation (6) may be used to estimate the ripple voltage:

\[
\Delta V_C = \Delta I_L \times R_{ESR}
\]

\( \Delta I_L = \text{inductor ripple current} \)

\( R_{ESR} = \text{filter capacitor ESR} \)

For a 100 \( \mu F \) electrolytic capacitor, an ESR of 0.1 \( \Omega \) is common. If the 10 \( \mu H \) inductor is used, delivering 250 mA of ripple current to the capacitor (as calculated above), then the ripple voltage is 25 mV. This is over ten times that of the 10 \( \mu F \) ceramic capacitor, as ceramic capacitors typically have negligible ESR.

**SWITCHING FREQUENCY CONFIGURATION: OSCILLATOR COMPONENTS R_{Osc} AND C_{Osc} AND FREQ OPERATION**

The onboard ramp generator requires an external resistor and capacitor to set the oscillation frequency. The frequency may be either 500 kHz or 100 kHz by selecting the proper capacitor value and by holding the FREQ pin either low (500 kHz) or high (100 kHz). Table 1 shows the values required and FREQ pin configuration for each switching frequency.

<table>
<thead>
<tr>
<th>SWITCHING FREQUENCY</th>
<th>R_{Osc}</th>
<th>C_{Osc}</th>
<th>FREQ</th>
</tr>
</thead>
<tbody>
<tr>
<td>500 kHz</td>
<td>120 k( \Omega )</td>
<td>220 pF</td>
<td>LOW (GND)</td>
</tr>
<tr>
<td>100 kHz</td>
<td>120 k( \Omega )</td>
<td>1 nF</td>
<td>HIGH (VDD)</td>
</tr>
</tbody>
</table>
For proper operation, the resistor $R_{\text{OSC}}$ should have 1% tolerance while capacitor $C_{\text{OSC}}$ should be a ceramic type with 10% tolerance. Both components should be grounded to AGND, which should be connected to PGND at a single point, typically where power and ground are physically connected to the printed-circuit board.

**EXTERNAL CLOCKING OPERATION**

To synchronize the switching to an external clock signal, pull the INT/EXT terminal low, and drive the clock signal into the COSC terminal. This clock signal must be from 10% to 90% duty cycle and meet the voltage requirements specified in the electrical specifications table. Since the DRV591 includes an internal frequency doubler, the external clock signal must be approximately 250 kHz. Deviations from the 250 kHz clock frequency are allowed and are specified in the electrical characteristic table. The resistor connected from ROSC to ground may be omitted from the circuit in this mode of operation—the source is disconnected internally.

**INPUT CONFIGURATION: DIFFERENTIAL AND SINGLE-ENDED**

If a differential input is used, it should be biased around the midrail of the DRV591 and must not exceed the common-mode input range of the input stage (see the operating characteristics at the beginning of the data sheet).

The most common configuration employs a single-ended input. The unused input should be tied to $V_{\text{DD}}/2$, which may be simply accomplished with a resistive voltage divider. For the best performance, the resistor values chosen should be at least 100 times lower than the input resistance of the DRV591. This prevents the bias voltage at the unused input from shifting when the signal input is applied. A small ceramic capacitor should also be placed from the input to ground to filter noise and keep the voltage stable. An op amp configured as a buffer may also be used to set the voltage at the unused input.

**FIXED INTERNAL GAIN**

The differential output voltage may be calculated using equation (7):

$$V_O = V_{\text{OUT}} + V_{\text{OUT}} = A_V (V_{\text{IN}} + V_{\text{IN}})$$

$A_V$ is the voltage gain, which is fixed internally at 2.34 V/V. The maximum and minimum ratings are provided in the electrical specification table at the beginning of the data sheet.

**POWER SUPPLY DECOUPLING**

To reduce the effects of high-frequency transients or spikes, a small ceramic capacitor, typically 0.1 μF to 1 μF, should be placed as close to each set of PVDD pins of the DRV591 as possible. For bulk decoupling, a 10 μF to 100 μF tantalum or aluminum electrolytic capacitor should be placed relatively close to the DRV591.

**AREF CAPACITOR**

The AREF terminal is the output of an internal mid-rail voltage regulator used for the onboard oscillator and ramp generator. The regulator may not be used to provide power to any additional circuitry. A 1 μF ceramic capacitor must be connected from AREF to AGND for stability (see oscillator components above for AGND connection information).

**SHUTDOWN OPERATION**

The DRV591 includes a shutdown mode that disables the outputs and places the device in a low supply current state. The SHUTDOWN pin may be controlled with a TTL logic signal. When SHUTDOWN is held high, the device operates normally. When SHUTDOWN is held low, the device is placed in shutdown. The SHUTDOWN pin must not be left floating. If the shutdown feature is unused, the pin may be connected to VDD.

**FAULT REPORTING**

The DRV591 includes circuitry to sense three faults:

- Overcurrent
- Undervoltage
- Overtemperature

These three fault conditions are decoded via the FAULT1 and FAULT0 terminals. Internally, these are open-drain outputs, so an external pull-up resistor of 5 kΩ or greater is required.

<table>
<thead>
<tr>
<th>FAULT1</th>
<th>FAULT0</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Overcurrent</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Undervoltage</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Overtemperature</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Normal operation</td>
</tr>
</tbody>
</table>

The over-current fault is reported when the output current exceeds four amps. As soon as the condition is sensed, the over-current fault is set and the outputs go into a high-impedance state for approximately 3 μs to 5 μs (500 kHz operation). After 3 μs to 5 μs, the outputs are re-enabled. If the over-current condition has ended, the fault is cleared and the device resumes normal operation. If the over-current condition still exists, the above sequence repeats.

The under-voltage fault is reported when the operating voltage is reduced below 2.8 V. This fault is not latched, so as soon as the power-supply recovers, the fault is cleared and normal operation resumes. During the under-voltage condition, the outputs go into a high-impedance state to prevent over-dissipation due to increased $r_{D(on)}$. 

---

The DRV591 as possible. For bulk decoupling, a 10 μF to 100 μF tantalum or aluminum electrolytic capacitor should be placed relatively close to the DRV591.
The over-temperature fault is reported when the junction temperature exceeds 130°C. The device continues operating normally until the junction temperature reaches 190°C, at which point the IC is disabled to prevent permanent damage from occurring. The system's controller must reduce the power demanded from the DRV591 once the over-temperature flag is set, or else the device switches off when it reaches 190°C. This fault is not latched; once the junction temperature drops below 130°C, the fault is cleared, and normal operation resumes.

POWER DISSIPATION AND MAXIMUM AMBIENT TEMPERATURE

Though the DRV591 is much more efficient than traditional linear solutions, the power drop across the on-resistance of the output transistors does generate some heat in the package, which may be calculated as shown in equation (8):

\[ P_{\text{DISS}} = (I_{\text{OUT}})^2 \times r_{DS(on), \text{total}} \]  

For example, at the maximum output current of 3 A through a total on-resistance of 130 mΩ (at \( T_J = 25°C \)), the power dissipated in the package is 1.17 W.

Calculate the maximum ambient temperature using equation (9):

\[ T_A = T_J - (\theta_{JA} \times P_{\text{DISS}}) \]  

PRINTED-CIRCUIT BOARD (PCB) LAYOUT CONSIDERATIONS

Since the DRV591 is a high-current switching device, a few guidelines for the layout of the printed-circuit board (PCB) must be considered:

1. **Grounding.** Analog ground (AGND) and power ground (PGND) must be kept separated, ideally back to where the power supply physically connects to the PCB, minimally back to the bulk decoupling capacitor (10 µF ceramic minimum). Furthermore, the PowerPAD ground connection should be made to AGND, not PGND. Ground planes are not recommended for AGND or PGND, traces should be used to route the currents. Wide traces (100 mils) should be used for PGND while narrow traces (15 mils) should be used for AGND.

2. **Power supply decoupling.** A small 0.1 µF to 1 µF ceramic capacitor should be placed as close to each set of PVDD pins as possible, connecting from PVDD to PGND. A 0.1 µF to 1 µF ceramic capacitor should also be placed close to the AVDD pin, connecting from AVDD to AGND. A bulk decoupling capacitor of at least 10 µF, preferably ceramic, should be placed close to the DRV591, from PVDD to PGND. If power supply lines are long, additional decoupling may be required.

3. **Power and output traces.** The power and output traces should be sized to handle the desired maximum output current. The output traces should be kept as short as possible to reduce EMI, i.e., the output filter should be placed as close to the DRV591 outputs as possible.

4. **PowerPAD.** The DRV591 in the Quad Flatpack package uses TI's PowerPAD technology to enhance the thermal performance. The PowerPAD is physically connected to the substrate of the DRV591 silicon, which is connected to AGND. The PowerPAD ground connection should therefore be kept separate from PGND as described above. The pad underneath the AGND pin may be connected underneath the device to the PowerPAD ground connection for ease of routing. For additional information on PowerPAD PCB layout, refer to the *PowerPAD Thermally Enhanced Package* application note, TI literature number SLMA002.

5. **Thermal performance.** For proper thermal performance, the PowerPAD must be soldered down to a thermal land, as described in the *PowerPAD Thermally Enhanced Package* application note, TI literature number SLMA002. In addition, at high current levels (greater than 2 A) or high ambient temperatures (greater than 25°C), an internal plane may be used for heat sinking. The vias under the PowerPAD should make a solid connection, and the plane should not be tied to ground except through the PowerPAD connection, as described above.
## PACKAGING INFORMATION

<table>
<thead>
<tr>
<th>Orderable Device</th>
<th>Status (1)</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>PIns</th>
<th>Package Qty</th>
<th>Eco Plan (2)</th>
<th>Lead/Ball Finish (6)</th>
<th>MSL Peak Temp (3)</th>
<th>Op Temp (°C)</th>
<th>Device Marking (4/5)</th>
<th>Samples</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV591VFP</td>
<td>ACTIVE</td>
<td>HLQFP</td>
<td>VFP</td>
<td>32</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>DRV591</td>
<td></td>
</tr>
<tr>
<td>DRV591VFPG4</td>
<td>ACTIVE</td>
<td>HLQFP</td>
<td>VFP</td>
<td>32</td>
<td>250</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>DRV591</td>
<td></td>
</tr>
<tr>
<td>DRV591VFPR</td>
<td>ACTIVE</td>
<td>HLQFP</td>
<td>VFP</td>
<td>32</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>DRV591</td>
<td></td>
</tr>
<tr>
<td>DRV591VFPRG4</td>
<td>ACTIVE</td>
<td>HLQFP</td>
<td>VFP</td>
<td>32</td>
<td>1000</td>
<td>Green (RoHS &amp; no Sb/Br)</td>
<td>NIPDAU</td>
<td>Level-3-260C-168 HR</td>
<td>-40 to 85</td>
<td>DRV591</td>
<td></td>
</tr>
</tbody>
</table>

(1) The marketing status values are defined as follows:
- **ACTIVE**: Product device recommended for new designs.
- **LIFEBUY**: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
- **NRND**: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
- **PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.
- **OBSOLETE**: TI has discontinued the production of the device.

(2) **RoHS**: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
- **RoHS Exempt**: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
- **Green**: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) **MSL, Peak Temp.**: The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) **Lead/Ball Finish**: Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**TAPE AND REEL INFORMATION**

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Reel Diameter</th>
<th>Reel Width</th>
<th>A0</th>
<th>B0</th>
<th>K0</th>
<th>P1</th>
<th>W</th>
<th>Pin1 Quadrant</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV591VFPR</td>
<td>HLQFP</td>
<td>VFP</td>
<td>32</td>
<td>1000</td>
<td>330.0</td>
<td>16.4</td>
<td>9.6</td>
<td>9.6</td>
<td>1.9</td>
<td>12.0</td>
<td>16.0</td>
<td>Q2</td>
</tr>
</tbody>
</table>

*All dimensions are nominal.*

**Notes:**
- A0 Dimension designed to accommodate the component width
- B0 Dimension designed to accommodate the component length
- K0 Dimension designed to accommodate the component thickness
- W Overall width of the carrier tape
- P1 Pitch between successive cavity centers

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*Image of TAPE AND REEL INFORMATION with diagrams and table.*
### TAPE AND REEL BOX DIMENSIONS

<table>
<thead>
<tr>
<th>Device</th>
<th>Package Type</th>
<th>Package Drawing</th>
<th>Pins</th>
<th>SPQ</th>
<th>Length (mm)</th>
<th>Width (mm)</th>
<th>Height (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>DRV591VFPR</td>
<td>HLQFP</td>
<td>VFP</td>
<td>32</td>
<td>1000</td>
<td>350.0</td>
<td>350.0</td>
<td>43.0</td>
</tr>
</tbody>
</table>

*All dimensions are nominal*
Images above are just a representation of the package family, actual package may vary. Refer to the product data sheet for package details.
THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

![Exposed Thermal Pad Dimensions](image)

**NOTE:** All linear dimensions are in millimeters.
VFP (S-PQFP-G32) PowerPAD™

Example Board Layout
Via pattern and copper pad size may vary depending on layout constraints

Example Stencil Design Based on a thickness of .127mm (.005\text{inch}). Reference table below for other solder stencil thicknesses

Example Solder Mask Opening (See Note F)

<table>
<thead>
<tr>
<th>CENTER POWER PAD SOLDER STENCIL OPENING</th>
</tr>
</thead>
<tbody>
<tr>
<td>STENCIL THICKNESS</td>
</tr>
<tr>
<td>-------------------</td>
</tr>
<tr>
<td>0.1mm</td>
</tr>
<tr>
<td>0.127mm</td>
</tr>
<tr>
<td>0.152mm</td>
</tr>
<tr>
<td>0.178mm</td>
</tr>
</tbody>
</table>

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50\% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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